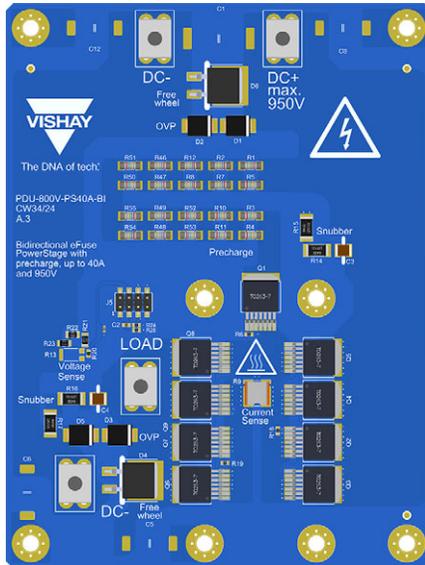


## Reference Design SiC MOSFET-Based 800 V, 40 A Bidirectional eFuse



### FEATURES

- Low TCR shunt for precise current measurement
- Low tracking error voltage divider
- Robust I/O port providing ESD protection and freewheel capabilities
- Fast switching speed

### KEY COMPONENTS

- [CMB0207](#) high pulse load carbon film MELF resistor
- [MXP120A045FE](#) SiC MOSFET
- [MXP120A250FE](#) SiC MOSFET

### LINKS TO ADDITIONAL RESOURCES

- [EFUSE-800V40ABI](#)

### DESCRIPTION

Electronic fuses (eFuses) are crucial in modern applications, especially in automotives. They are used to enhance overall vehicle safety by protecting against overcurrent, voltage spikes, and temperature rise. eFuses often comprise a control board and a power board. Here we focus on providing a complete power board design example that is based on Vishay’s SiC MOSFETs.

This power board is capable of handling voltages up to 950 V and 40 A current. The circuit can be easily scaled up for high current ratings. In addition to the eFuse functionality, the circuit benefits from a pre-charge circuit connected in parallel with the main eFuse switch, which avoids inrush currents into external uncharged capacitors.

The power circuit is fully equipped with all the required feedback signals, including the circuit current - which is measured by a Vishay low TCR shunt resistor - and the circuit voltage, which is measured by a low tracking error divider.

### OVERALL SYSTEM BLOCK DIAGRAM

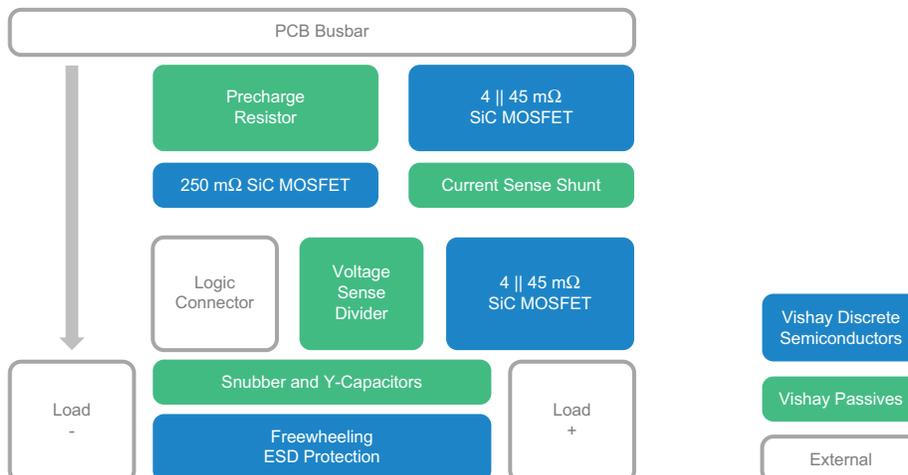


Fig. 1 - Overall System Block Diagram

## APPLICATION DESCRIPTION

The eFuse circuit should be able to supply and disconnect the current from the source side to the load side. It also provides a separate pre-charge path to avoid inrush currents when operating with capacitive loads.

### Pre-Charging

During the pre-charge, Q10 and (Q6 - Q9) should be turned on and (Q2 - Q5) should be turned off.

The DC-Link capacitor should be pre-charged first before the main switch is turned on. In this design the effective pre-charge resistance is 10 kΩ. This is achieved by using two series of ten 2 kΩ / 0.4 W resistors connected in parallel.

These resistors can be adjusted by the user to achieve the required pre-charge time according to the specific application.

Considering the existing setup, with a 10 kΩ pre-charge resistor and 800 V supply voltage, the initial peak current of the circuit will be about 80 mA ( $\frac{800}{10 \text{ k}\Omega}$ ).

$$P_R = I^2 \times R = (0.08 \text{ A})^2 \times 10 \text{ k}\Omega = 64 \text{ W (peak power)}$$

Each resistor should withstand ( $\frac{64}{20} \sim 3.2$ ) peak power for a duration equal to

$$5\tau = 5 \times R \times C = 5 \times 10 \text{ k}\Omega \times C$$

where C is the capacitance connected to the output of the eFuse.

### For the SiC Pre-Charge MOSFET

Assuming  $R_{DS(on)} = 250 \text{ m}\Omega$  at 80 °C and  $V_{GS} = 20 \text{ V}$ :

$$P = I^2 R = (0.08 \text{ A})^2 \times 250 \text{ m}\Omega = 1.6 \text{ mW.}$$

Considering the maximum junction to ambient thermal resistance  $R_{thJA} = 43 \text{ }^\circ\text{C/W}$ , the following simple thermal equation provides the temperature rise:

$$T_J = T_{amb} + dT \quad (1)$$

Where;

$T_J$  is the junction temperature

$T_{amb}$  is the ambient temperature

$dT$  is the temperature rise due to the energy dissipation. This can be calculated by applying  $P_{loss} \times R_{th}$ , or from the graphs provided in the datasheet

$P_{loss}$  is the power loss within the component

$R_{th}$  is the internal thermal resistance of the component.

$$T_J = T_{80 \text{ }^\circ\text{C}} + 1.6 \text{ mW} \times 43 \frac{^\circ\text{C}}{\text{W}} \sim 80.7 \text{ }^\circ\text{C}$$

(it indicates that no active cooling is required in this case)

### Normal Operation

During normal operation, (Q2 - Q9) should be turned on and Q10 should be turned off.

For the MOSFET, considering  $R_{DS(on)} = 45 \text{ m}\Omega$  at 80 °C and  $V_{GS} = 20 \text{ V}$  for 40 A divided by four MOSFETs in parallel, each MOSFET will have 10 A:

$$P = I^2 R = (10 \text{ A})^2 \times 45 \text{ m}\Omega = 4.5 \text{ W}$$

Considering the maximum junction to ambient thermal resistance  $R_{thJA} = 0.59 \text{ }^\circ\text{C/W}$ , the following simple thermal equation provides the temperature rise:

$$T_J = T_{80 \text{ }^\circ\text{C}} + 4.5 \text{ W} \times 0.59 \frac{^\circ\text{C}}{\text{W}} \sim 82.665 \text{ }^\circ\text{C} < T_{J \text{ max.}} (150 \text{ }^\circ\text{C})$$

It indicates that no active cooling is required in this case as well. The user should take care in calculating the actual temperature rise in the final application.

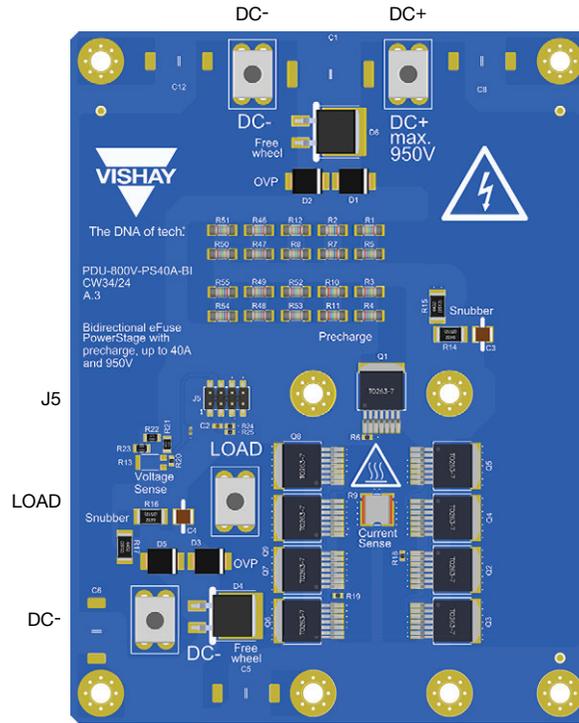
**PIN CONFIGURATION**


Fig. 2 - Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	SYMBOL	DESCRIPTION
DC+	DC+	Connect with HV DC voltage input; max. 950 V
DC-	DC-	Connect with reference point for DC input
LOAD	DC+	Connect with load; max. 950 V
DC-	DC-	Connect with reference point for LOAD
J5 / 1	+DC_SH+	Output load shunt positive
J5 / 3	+DC_SH-	Output load shunt negative
J5 / 5	GATE_SW_ON	Input gate switch fuse active high
J5 / 7	KS_SW_ON	Reference for GATE_SW_ON
J5 / 2	CD_LOAD_SNS_REF	Reference for DC_LOAD_SNS
J5 / 4	DC_LOAD_SNS	Output voltage divider for load voltage (950:1)
J5 / 6	GATE_PRECHARGE	Input for gate signal of pre-charge MOSFET- active high
J5 / 8	KS_PRECHARGE	Reference for gate signal of pre-charge MOSFET

RECOMMENDED OPERATING RANGE			
PARAMETER	MIN.	MAX.	UNIT
DCLINK+ to DCLINK-	25	950	V

**ABSOLUTE MAXIMUM RATINGS**

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)		
<b>ELECTRICAL PARAMETER</b>	<b>LIMITS</b>	<b>UNIT</b>
HV $U_{DC}$ to ref.	950	V
Ambient temperature	-40 to +125	$^{\circ}\text{C}$
Storage temperature	-40 to +150	$^{\circ}\text{C}$
Max. power consumption	1500	mW
Max. current consumption	300	mA
Isolation voltage	5	$\text{kV}_{RMS}$

**DIMENSIONS** in millimeters

EFUSE-800V40ABI

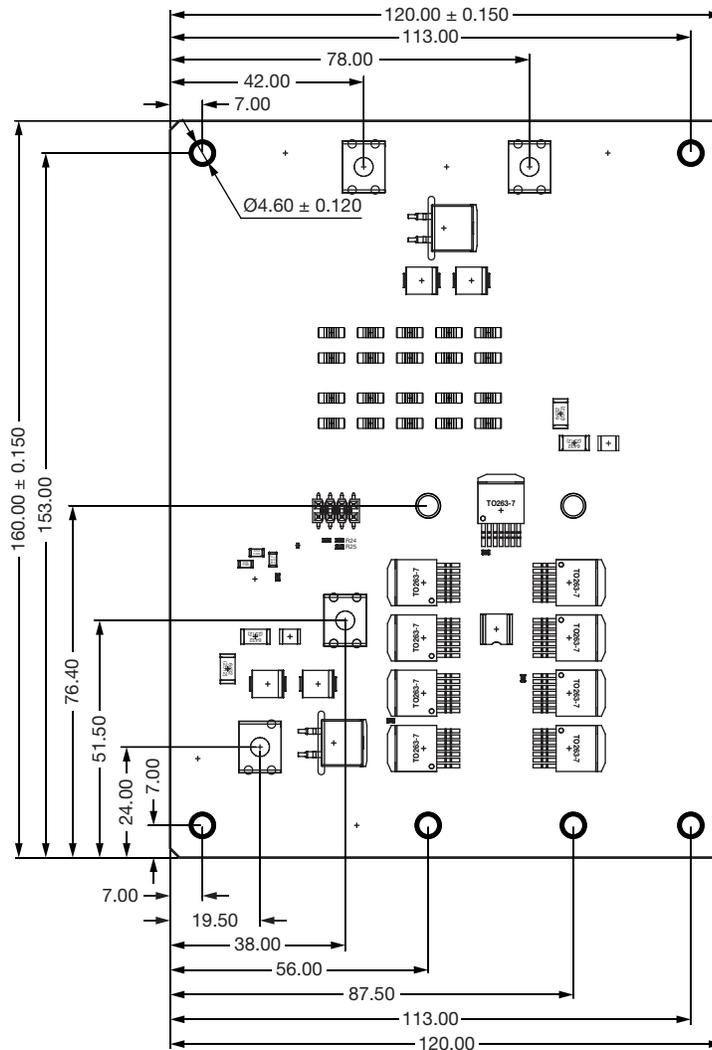

 Tolerances if not other defined:  $\pm 0.1$ 

Fig. 3



**PACKAGE LIST OF THE REFERENCE KIT**

- EFUSE-800V40ABI

**ADDITIONAL RESOURCES**

[1] [Thermal Management in Surface-Mounted Resistor Applications](#)



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