dsPIC33CK to dsPIC33AK Migration and Performance Enhancement Guide

Introduction

This document provides information for the dsPIC33CK to dsPIC33AK device migration and highlights the following:

- Key Features and Improvements
- Key Information to Migrate at the System Level
- Peripherals/Features that Received Significant Updates
- Peripherals/Features with Minor Changes and Performance Enhancements
- Software Migration

Please note that some features may not be available. Refer to the device-specific data sheet for more details. The device data sheet and errata are available for download from the Microchip website at: https://www.microchip.com.

Table of Contents

Introduction....1

1. Key Features....3

2. System Migration....4

3. Significant Migration Considerations....5
   - 3.1. CPU....5
   - 3.2. FPU....6
   - 3.3. Memory Organization....6
   - 3.4. Program Memory....6
   - 3.5. Data Memory....7
   - 3.6. Configuration Bits....7
   - 3.7. Interrupt Controller....7
   - 3.8. Clock Generator/Oscillator....7
   - 3.9. Security....8
   - 3.10. Peripheral Access Control....8
   - 3.11. ADC....9
   - 3.12. BiSS....9
   - 3.13. DMA....9
   - 3.14. Ports/IOIM....9
   - 3.15. PMU....10

4. Minor Migration Considerations and Performance Enhancements....11
   - 4.1. PWM....11
   - 4.2. CBG....11
   - 4.3. Op Amp....11
   - 4.4. Comparator and DAC....11
   - 4.5. I^2C....11
   - 4.6. UART....12
   - 4.7. MCCP/SCCP....12

5. Software Migration....13

Microchip Information....14
- The Microchip Website....14
- Product Change Notification Service....14
- Customer Support....14
- Microchip Devices Code Protection Feature....14
- Legal Notice....14
- Trademarks....15
- Quality Management System....16
- Worldwide Sales and Service....17

1. Key Features

The dsPIC33AK device family includes many new features and changes from the dsPIC33CK device family. The code developed for the dsPIC33CK family devices can be ported to the dsPIC33AK family devices after making the appropriate changes, as described in this document. The dsPIC33AK family devices feature many improvements and new capabilities, such as:

- Higher Speed (200 MIPs) CPU with Additional Instructions
- Single and Double Precision Hardware Floating Point Unit (FPU)
- Instructions Upgraded to 32-bit Wide
- Data bus upgraded to 32-bit wide
- Data, program and SFR space forms a Non-overlapping Unified Memory Map
- 2KB Instruction Cache
- Clock Generator Structures, Including Configurable Backup Oscillator Sources
- Additional Clock Monitors
- Interrupt Controller Including Collapsible and Movable IVTs
- Improved Security Module
- Higher Speed ADC (40 MSPS)
- Bidirectional Serial Synchronous (BiSS) Protocol Module
- IO Integrity Module (IOIM)
- Performance Monitor Unit (PMU)
- Additional Current Bias Generators (CBG)
- Functional Safety Enhancements

2. System Migration

This section describes general features and topics that are not dedicated to a specific module or peripheral and are considered system level to help users migrate between families. Key system migration considerations include the following:

- Pinouts have changed including additional Power/Ground pairs.
- Configuration bits have changed and are split between 2 sections, one dedicated to the device's operation and one dedicated to security.
  - Configuration bits are now located at absolute addresses.
  - Each configuration section also includes a backup configuration section.
  - Many configuration bits have been moved to the SFR space.
- SFR addresses have changed, including many 16-bit dsPIC33CK registers that have combined into one 32-bit dsPIC33AK register.
- Peripheral Pin Select (PPS) mappings have been rearranged.
- Interrupt vectors have been rearranged.

3. Significant Migration Considerations

Each section of this document describes one peripheral or major feature of the dsPIC33AK device family. For more information on new or modified modules, refer to a specific device's **"dsPIC33AK Family Data Sheet"** available on www.microchip.com. The topics covered include:

- CPU
- FPU
- Memory Organization
- Program Memory
- Data Memory
- Configuration Bits
- Interrupt Controller
- Clock Generator/Oscillator Module
  - Clock monitors
- Security
- ADC
- BiSS
- DMA
- Ports/GPIO
  - IO integrity monitor
- PMU

3.1 CPU

The dsPIC33AK family of devices have a CPU architecture featuring a 5-stage interlocked instruction pipeline, speculative execution and prefetch branch prediction to reduce conditional branch latency. In addition, a 2kB instruction cache is implemented for faster access times. Due to the architecture changes, the oscillator frequency is now equal to the instruction cycle frequency (MHz = MIPS). The dsPIC33AK devices have 16x32-bit W-Regs and 2x72-bit accumulators. They also include seven alternate contexts, one per IPL, for W0-W7 and seven alternate contexts for the 2x72-bit accumulators, RCOUNT and CORCON.

The core uses a mixed size, 16/32-bit instruction set for optional optimization, which has been significantly improved while maintaining backwards compatibility. Notable changes include the `REPEAT{W}` instruction supporting larger counts and the `DTB` instruction replacing the `DO` looping structure, allowing for unlimited nesting of loops. MIN and MAX are instructions that were present in dsPIC33CK, however they are now updated with additional data limits for operating on W-Regs.

DSP support has also improved. Because of the 32-bit architecture, the multiplier is 33x33 bits. The accumulators are also not memory mapped. They are directly addressed. The MAC instructions have also been improved. MAC instructions can now utilize any W-Reg and do not require a prefetch, which greatly helps the syntax.

Furthermore, the dsPIC33AK devices feature a dedicated hardware module called the Floating-Point Unit (FPU) for single and double precision floating-point operations. Additionally, the FPU operates on its own pipeline, providing faster and more efficient processing.

Table 3-1. dsPIC33CK and dsPIC33AK CPU Comparison

Feature	dsPIC33CK	dsPIC33AK
Speed	100 MHz	200 MHz

.....continued

Feature	dsPIC33CK	dsPIC33AK
Pipeline	1-stage	5-stage
Alternate Register Contexts	4	7
Paging Registers	Yes: TBLPAG, DSRPAG, DSWPAG, YPAG	No, direct addressing
Working Registers	16 x 16-bit	16 x 32-bit
Accumulators	2 x 40-bit	2 x 72-bit
Notable New Instructions	-	DTB, MIN, MAX, MOVIF, DISICTL(W)

3.2 FPU

The Floating-Point Unit (FPU) is a hardware module that follows a load-store architecture and is designed to provide a complete IEEE 754-2019 compliant FPU with support for single and double precision. With the addition of the FPU, the CPU now fetches instructions, decodes them and issues floating-point operations to the FPU. The FPU then executes the instruction using its own independent load-store instruction pipeline. This allows both the CPU and FPU to execute their respective instructions concurrently, provided there are no data hazards that stall the pipeline. Since the CPU and FPU are separate, FPU operands and results are local to the FPU. The CPU moves data to and from the FPU using dedicated move instructions and can conditionally branch based on the FPU status.

The FPU has 32x32-bit F-Regs (FPU Working Registers) for single-precision operations. If using double-precision operations, the FPU utilizes the existing F-Regs to allow for 16x64-bit F-Regs. It also has seven alternate contexts for F0-F7 in addition to alternate contexts for FCR and FSR.

3.3 Memory Organization

Two new features of the Bus Matrix (BMX) module are the ability to execute code from RAM and support multiple peripheral buses at different speeds.

Previously, in dsPIC33CK devices, all special function registers (SFRs) were bussed from the same clock speed. However, in dsPIC33AK devices, there are now three different peripheral buses operating at different speeds to optimize bus access needs. These buses are Fast (1:1 System Clock), Standard (1:2 System Clock) and Slow (1:4 System Clock).

3.4 Program Memory

The dsPIC33AK devices have undergone significant changes in their Flash memory architecture, mostly due to the increase to a 32-bit architecture. The instruction word has increased from 24-bits to 32-bits. dsPIC33AK devices also write four instruction words at a time, which can be thought of as a 128-bit quad word. Since ECC is also included on flash, the total bit width is 140 bits. This accounts for nine bits of ECC, three reserved bits and the 128-bit quad word. The dsPIC33AK Flash memory is now integrated into the unified memory map, enabling direct addressing without the need for a table page, table read and table write. These features, along with the ECC registers and forced fault injection functions, provide support for Functional Safety. The Flash memory also includes a CRC feature to verify Flash contents.

Table 3-2. dsPIC33CK and dsPIC33AK Program Memory Comparison

Feature	dsPIC33CK	dsPIC33AK
Instruction Word	24-bits	32-bits
Flash Row	128 IW (3,072-bits)	128 IW (4,096-bits)
Flash Page	1,024 IW (24,576-bits)	1,024 IW (32,768-bits)
Unified Memory Map	No, need a table page, table read, table write	Yes, direct addressing
Error Correcting Code (ECC)	Yes	Yes
ECC Fault Injection	Yes	Yes

.....continued

Feature	dsPIC33CK	dsPIC33AK
Flash Cycle Redundancy Check (CRC)	-	Yes
Instruction Cache	-	Yes

3.5 Data Memory

The dsPIC33AK's data memory is integrated into the unified memory map, allowing direct access to addresses without the need for Extended Data Space (EDS) as required by dsPIC33CK devices. Similar to dsPIC33CK devices, there are two SRAM blocks: X and Y. However, the ability to read and write to Y RAM is new to dsPIC33AK. An additional new feature for dsPIC33AK devices is the ability to execute from RAM to reduce instruction cycle latency for critical code. Previous features only available on Flash are now applied to RAM, such as ECC on RAM including Bus error on a DED event and interrupt on a SEC event. The RAM ECC also supports fault injection for Functional Safety. The RAM with ECC includes 32-bit data and 7-bits of ECC, while 16-bit and 8-bit writes are still supported.

3.6 Configuration Bits

The dsPIC33AK device's configuration bits are also included in the unified memory map. Whereas the dsPIC33CK device's configuration bits were always the last row of program memory. Now, the dsPIC33AK device's configuration bits are at an absolute address. The entire configuration region is divided into two distinct areas. The first region contains configuration bits related to the operation of the device. The second region is dedicated to the security options of the device. Clock configuration bits have been relocated to the SFR space, and some configuration bits do not exist anymore. A notable configuration bit that has been removed is the one that required the user to designate which program pair was to be used for debugging. Now, this is done automatically based on the previous successful programming session.

3.7 Interrupt Controller

The interrupt controller has undergone significant changes on dsPIC33AK devices. The Alternate Vector Table (AIVT) in dsPIC33CK devices has been replaced with a Relocatable Interrupt Vector Table (RIVT). Unlike AIVT, which was fixed in the boot segment, RIVT allows the vector table to be relocated anywhere in the memory map using the IVTBASE register. Additionally, a Collapsed Interrupt Vector Table (CIVT) has been introduced, which serves as a common vector for all interrupts that can be enabled with the IVTC register. The DISI function in dsPIC33CK devices has been replaced with DISICTL in dsPIC33AK devices, but it still serves the purpose of changing the Interrupt Priority Level (IPL) threshold. The Reset `GOTO` instruction has been replaced with a Reset vector, which indicates the location of the first instruction fetch after a device Reset. dsPIC33AK devices now feature a Vector Fail Address (VFA) to handle situations when a vector fetch fails. In addition, the INTCONx registers have been reorganized in dsPIC33AK devices.

Table 3-3. dsPIC33CK and dsPIC33AK Interrupt Controller Comparison

Feature	dsPIC33CK	dsPIC33AK
AIVT Replaced with RIVT	Alternate Interrupt Vector Table (AIVT)	Remappable Interrupt Vector Table (RIVT)
Collapsed Interrupt Vector	-	Yes
Disable Interrupt Control	DISI	DISICTL
Reset Vector	Reset GOTO	Reset Vector
Vector Fail Address (VFA)	-	Yes

3.8 Clock Generator/Oscillator

Similar to the dsPIC33CK devices, a variety of different clock sources may be used by the CPU and peripherals in dsPIC33AK devices. The dsPIC33AK devices have an improved centralized clock system using multiple clock generators and PLLs that can be independently configured. The clock generators are associated with a specific feature or peripheral. The CPU and peripheral buses also

use a clock generator that must be configured prior to user code execution. The device data sheet can be used to determine all the clock generator function correlations. Unlike the dsPIC33CK, the dsPIC33AK uses SFRs to control clock functions instead of configuration bits. The clock generators have also become more modular and use similar register sets for clock generators and PLLs; this includes additional output enable bits and clock/PLL ready bits that are intended to be polled until the clock or PLL is ready. The dsPIC33AK includes a new module, the Clock Monitor, which can be used to warn when the monitor detects clock deviations. In addition to this monitoring, there is a Fail-Safe Clock Monitor (FSCM) for each generator. Each generator also has a configurable backup source and includes a fault injection to verify clock failures. In the dsPIC33CK devices, there was a dedicated REFO, which is still true in dsPIC33AK devices, but now, REFO has its own Clock Generator.

Table 3-4. dsPIC33CK and dsPIC33AK Clock Generator/Oscillator Comparison

Feature	dsPIC33CK	dsPIC33AK
Clock Sources	Up to 5	Up to 6
PLL Generators	2	2
Clock Generators	-	Up to 16
Fractional Dividers	1 global	1 per generator
Backup Clock Sources	Fixed	Configurable
Fail Safe Clock Monitor	1 global	1 per generator
Fault Injection	-	1 per generator
Clock Monitors	-	Up to 4

3.9 Security

The dsPIC33CK devices possessed CodeGuard™ security features that are similar to those found in dsPIC33AK. However, the security features for dsPIC33AK have been completely redesigned and now include additional features that support security services such as Secure Boot, Immutable Root of Trust (IRT), Code Access Protect (Read/Write/Execute/CRC), ICSP™ Program/Erase Disable, Flash Write Protection, Flash OTP and Flash Code Partitioning. With dsPIC33AK devices, Flash memory can be divided into eight sections, and each region can be configured for a firmware configurable region, OTP region or IRT region. The type of region can be configured by setting the configuration bits, and there are different options available depending on the desired security level. For a detailed comparison between the security features of dsPIC33CK and dsPIC33AK devices, refer to Table 3-5.

Table 3-5. dsPIC33CK and dsPIC33AK Security Comparison

Feature	dsPIC33CK	dsPIC33AK
Read Access Control – ICSP	Yes	Yes
Read Access Control – Firmware	-	Yes
Write Access Control	-	Yes
Erase Access Control	-	Yes
Execution Access Control	-	Yes
CRC Access Control	-	Yes
IRT Support	-	Yes
OTP Support	-	Yes
Entire Flash OTP by ICSP Write Inhibit	Yes	Yes

3.10 Peripheral Access Control

Peripheral Access Controller (PAC) is a new module, and it safeguards against inadvertent activation or deactivation of critical peripherals. Previously, users of dsPIC33CK devices were required to enter a specific sequence of 0x55 and 0xAA to NVMKEY to unlock and lock peripherals. This process has now been replaced with the PAC module, which enables the locking and unlocking of specific peripheral Special Function Registers (SFRs) and SFR ranges through a write enable bit and lock bit.

3.11 ADC

The dsPIC33AK devices are equipped with an ADC that boasts a maximum conversion rate of 40 MSPS. This ADC now features a configurable channel-based configuration, allowing for any input signal pin (positive and negative) to be assigned to a specific channel. The channel-based and configurable nature of this ADC enable different sampling times, trigger sources and dedicated result comparators to be set for each channel. Additionally, the ADC supports several accumulation modes and features a second accumulator on the last three channels for implementing second-order filtering. For a comprehensive comparison of dsPIC33CK and dsPIC33AK features, refer to Table 3-6.

Table 3-6. dsPIC33CK and dsPIC33AK ADC Comparison

Feature	dsPIC33CK	dsPIC33AK
Number of Analog Conversion Cores	3-5 cores, 3.5 MSPS	2-5 cores, 40 MSPS
Maximum Signal Source Impedance (200 ns Sampling Time)	1 kOhm, CHold = ~ 16pF	22 kOhms, Chold = ~1 pF
Sampling Time Selection	Same for all core channels	Selectable for each input
Inputs Conversion Priority/Order	Fixed	Programmable
Conversion Result Comparators	Typically 4	Up to 20 (1 per channel)
Result Accumulators	Typically 4	Up to 20 (1 per channel)
Trigger Selection	Set for each input	Set for each channel

3.12 BiSS

The dsPIC33AK devices include a new peripheral known as the Bidirectional Serial Synchronous (BiSS) module. This open-source serial protocol facilitates high-speed communication between sensors and actuators. The module boasts three serial communication lines, support for eight data channels, 64-bit data lengths and speeds of up to 10 Mbps when used with an RS485/RS422 interface. Additionally, it features automatic sensor triggering, enabling immediate sampling after the previous communication is complete. The module also includes line delay compensation for long wire distances, as well as safety features such as CRC, error and warning flags. The BiSS module supports various modes, including BiSS-C, SSI, host and client communication, host and multiple client communication and host with bus communication. This versatile module is ideal for applications such as rotary encoders, torque sensors and motor drives.

3.13 DMA

There are four major improvements to the DMA module in dsPIC33A devices. This includes Ping Pong mode, pattern matching, channel chaining and bit manipulation capabilities. Ping Pong mode allows for one channel to process data while another is fetching data. Pattern matching allows the DMA to recognize data patterns in the internal buffer when transferring from the source to destination. Channel chaining can be used to trigger one channel off of another channel. Finally, you can now directly manipulate bits in the DMA write cycle such as invert, clear and set.

3.14 Ports/IOIM

In general, the GPIO and ports of dsPIC33AK devices function similarly to those of dsPIC33CK devices. However, dsPIC33AK devices come with an additional feature called the IO Integrity Monitor (IOIM), which is designed to monitor IO's for faults in Functional Safety applications. The IOIM includes configurable monitor inputs, a configurable blanking delay, selectable clock inputs as well as fault injection capability. The IO integrity monitor uses a change detector circuit that compares the reference signal with a selected feedback signal and accommodates the delay between signals using an edge detection-based blanking timer. After a programmable amount of time, the selected feedback state is compared to the reference input state, and an error event will occur if a mismatch is detected.

3.15 PMU

The Performance Monitor Unit (PMU) module offers the ability to monitor and control multiple counters, which can be used to quantify code execution time. The PMU provides a means to quantify non-deterministic behaviors, such as mispredicted CPU branches, data dependency stalls in the CPU pipeline, read/write of a slow SFR bus, bus arbitration conflicts, an instruction cache miss and more.

4. Minor Migration Considerations and Performance Enhancements

The following section briefly describes peripherals that gained minor modifications from the dsPIC33CK devices, as well as the peripherals that experienced performance improvements.

4.1 PWM

The PWM for dsPIC33AK devices has undergone performance improvements with minimal changes to functionality. Data registers have been expanded to 20 bits and applied values need to be scaled accordingly. The pins for the PWM now include the ability to use dedicated pins and/or PPS pins. The operation modes are largely the same from dsPIC33CK devices, however the second family of dsPIC33AK devices will include an LLC Resonant Converted mode. For a detailed comparison of the performance differences between dsPIC33CK and dsPIC33AK devices, refer to Table 4-1.

Table 4-1. dsPIC33CK and dsPIC33AK PWM Performance Differences

Feature	dsPIC33CK	1st Family of dsPIC33AK	2nd Family of dsPIC33AK
PWM Time Base	16-bits	20-bits	20-bits
Fine Edge Placement Resolution	250 ps	-	78 ps
Standard Resolution	500 MHz	400 MHz	800 MHz
Minimum LEB Resolution	8 LSBs	5 LSBs	5 LSBs

4.2 CBG

The dsPIC33AK CBG module has removed the current sinks that were present in the dsPIC33CK devices and now only supports current sources. Unlike the dsPIC33CK CBG module, which only had 10 uA and 50 uA current sources, the dsPIC33AK CBG module offers four 10 uA fixed sources and four selectable outputs that range from 30 uA to 200 uA. Please note that the fixed sources and selectable sources share device pins.

Table 4-2. dsPIC33CK and dsPIC33AK CBG Comparison

Features	dsPIC33CK	dsPIC33AK
Fixed 10 uA Current Sources	4	4
Current Sources/Sinks	4 Current Sources or Current Sinks	4 Current Sources
Current Source Range	Fixed 50 uA	Selectable from 30-200 uA
Pins for Each Source	Dedicated pin for IBIASx and dedicated pin for ISRCx	Shared pin for IBIASx/ISRCx

4.3 Op Amp

The Op Amp in dsPIC33AK devices now has a user configurable offset adjustment. This feature enables users to perform their own calibration and override the factory default values to accommodate any offset errors. Additionally, the performance of the Op Amp has been enhanced; it is a 100MHz bandwidth Op Amp with low-input offset and is unity-gain stable.

4.4 Comparator and DAC

The dsPIC33AK devices Comparator and DAC have undergone notable improvements. The comparator response time is significantly improved to 5 ns, and the device now features INL and DNL correction capability. For INL compensation, the user can copy calibration space that the factory has set. The user can then tune those values further by adjusting the drive strength for the rise and fail times. For DNL, the user can enable ripple reduction which should stretch the falling edge and use DNLADJ for further tuning.

4.5 I^2C

The I^2C module in dsPIC33AK devices has several additional features compared to dsPIC33CK devices. These include the ability to configure clients with unique addresses or a range of addresses,

a smart mode that requires minimal user interaction and simplifies application code, and an automatic clock release based on the [SSPND] status bit. The software does not have to enable host reception for each byte. Additionally, the module offers increased support for SMBus and PMBus, including packet error checking (PEC), clock low timeout, bus idle timeout, cumulative timeout and frame error detection. The module also now includes a receive trigger and transmit trigger for the DMA.

4.6 UART

The dsPIC33AK devices now include an added [WIP] bit that indicates when registers can be updated.

4.7 MCCP/SCCP

The MCCP functionality is not included in the first family of dsPIC33AK devices. However, the second family of dsPIC33AK devices will include MCCP. In general, the MCCP/SCCP functionality in dsPIC33AK devices remains largely unaltered compared to dsPIC33CK devices.

5. Software Migration

In addition to the hardware changes, there are some significant changes in the software. All the registers are now 32-bit, which means the software will reflect this change. Integers will all default to 32-bit instead of 16-bit. Int and long int are both 32-bit. The alignment of structure members, bit fields and related padding has changed as a result.

Due to the unified memory map, C-type qualifiers, attributes and memory spaces related to the former dsPIC33CK memory architecture are no longer required or accepted in addition to several related Assembly operators and section attributes. There are also no special conversions needed in Assembly for addresses in program memory. It can be represented simply as byte addresses.

For more details, please refer to the MPLAB® XC-DSC C Compiler User's Guide (DS50003589) and MPLAB XC-DSC Assembler, Linker and Utilities User's Guide (DS50003590).

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

ISBN: 978-1-6683-4839-0

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	**Australia - Sydney** Tel: 61-2-9868-6733	**India - Bangalore** Tel: 91-80-3090-4444	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393
Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455	**China - Beijing** Tel: 86-10-8569-7000	**India - New Delhi** Tel: 91-11-4160-8631	**Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829
Austin, TX Tel: 512-257-3370	**China - Chengdu** Tel: 86-28-8665-5511	**India - Pune** Tel: 91-20-4121-0141	**Finland - Espoo** Tel: 358-9-4520-820
Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088	**China - Chongqing** Tel: 86-23-8980-9588	**Japan - Osaka** Tel: 81-6-6152-7160	**France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79
Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075	**China - Dongguan** Tel: 86-769-8702-9880	**Japan - Tokyo** Tel: 81-3-6880- 3770	**Germany - Garching** Tel: 49-8931-9700
Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924	**China - Guangzhou** Tel: 86-20-8755-8029	**Korea - Daegu** Tel: 82-53-744-4301	**Germany - Haan** Tel: 49-2129-3766400
Detroit Novi, MI Tel: 248-848-4000	**China - Hangzhou** Tel: 86-571-8792-8115	**Korea - Seoul** Tel: 82-2-554-7200	**Germany - Heilbronn** Tel: 49-7131-72400
Houston, TX Tel: 281-894-5983	**China - Hong Kong SAR** Tel: 852-2943-5100	**Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906	**Germany - Karlsruhe** Tel: 49-721-625370
Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380	**China - Nanjing** Tel: 86-25-8473-2460	**Malaysia - Penang** Tel: 60-4-227-8870	**Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44
Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800	**China - Qingdao** Tel: 86-532-8502-7355	**Philippines - Manila** Tel: 63-2-634-9065	**Germany - Rosenheim** Tel: 49-8031-354-560
Raleigh, NC Tel: 919-844-7510	**China - Shanghai** Tel: 86-21-3326-8000	**Singapore** Tel: 65-6334-8870	**Israel - Hod Hasharon** Tel: 972-9-775-5100
New York, NY Tel: 631-435-6000	**China - Shenyang** Tel: 86-24-2334-2829	**Taiwan - Hsin Chu** Tel: 886-3-577-8366	**Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781
San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270	**China - Shenzhen** Tel: 86-755-8864-2200	**Taiwan - Kaohsiung** Tel: 886-7-213-7830	**Italy - Padova** Tel: 39-049-7625286
Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078	**China - Suzhou** Tel: 86-186-6233-1526	**Taiwan - Taipei** Tel: 886-2-2508-8600	**Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340
	China - Wuhan Tel: 86-27-5980-5300	**Thailand - Bangkok** Tel: 66-2-694-1351	**Norway - Trondheim** Tel: 47-72884388
	China - Xian Tel: 86-29-8833-7252	**Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Poland - Warsaw** Tel: 48-22-3325737
	China - Xiamen Tel: 86-592-2388138		**Romania - Bucharest** Tel: 40-21-407-87-50
	China - Zhuhai Tel: 86-756-3210040		**Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91
			Sweden - Gothenberg Tel: 46-31-704-60-40
			Sweden - Stockholm Tel: 46-8-5090-4654
			UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820