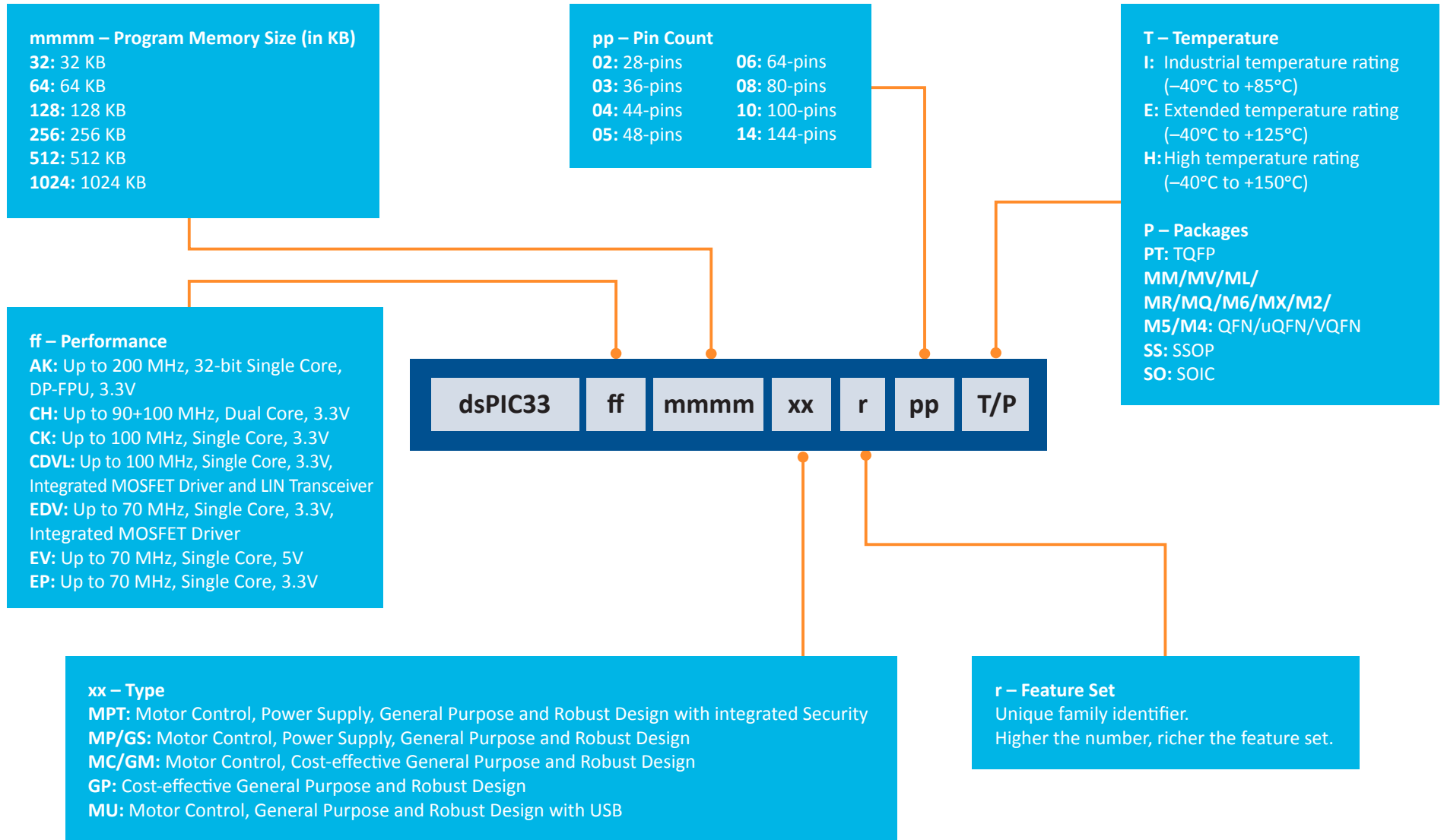


Quick Reference Guide

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|--|--|---|--|
| 1: dsPIC33 DSCs offer SAR ADC and high-speed ADC security, PWM lock* | 2: dsPIC33 DSCs offer general-purpose DAC and audio DAC | 3: Hardware Safety Features: | L1: Includes WDT, oscillator fail-safe, illegal opcode detect, TRAP, reset trace, register lock, frequency check, CodeGuard™ |
| L2: Includes features of L1 + CRC | L3: Includes features of L2 + Flash ECC and/or DMT | L4: Includes features of L3 + RAM MBIST | L5: Includes L4 + ECC RAM + IOIM |
| DSCs with 5V operating Voltage | Note: Similar family of devices with fewer variations are grouped with the same color coding | | *PWM lock available in devices with MC PWM/SMPs PWM peripheral (5V) dsPIC33 |

dsPIC33 DSC Part Number Decoder



| INTEGRATED ANALOG: Sensor Interfacing and Signal Conditioning | |
|--|---|
| ADC: Analog-to-Digital Converter | General-purpose ADC with up to 10-/12-bit resolution |
| HS ADC: High-Speed Analog-to-Digital Converter | High-speed SAR ADC with 12-bit resolution and sampling speed of 10 Msps |
| DAC: Digital-to-Analog Converter | General-purpose DAC with resolution up to 16-bit resolution |
| ΔΣ DAC: Delta-Sigma Digital-to-Analog Converter | Second-order digital bipolar, two output channel Delta-Sigma DAC with stereo operation support |
| HS Comp: High-Speed Comparator | General-purpose rail-to-rail comparator with <1 ns response time |
| OPA/PGA: Operational Amplifier and Programmable Gain Amplifiers | General-purpose op amp and PGAs for internal and external signal source conditioning |
| WAVEFORM CONTROL: PWM Drive and Waveform Generation | |
| SCCP: Single Capture/Compare/PWM | Multi-purpose 16-/32-bit input capture, output compare and PWM |
| MCCP: Multiple Capture/Compare/PWM | Multi-purpose 16-/32-bit input capture, output compare and PWM with up to six outputs and an extended range of output control features |
| PWM: Pulse Width Modulation | 16-bit PWM with up to nine independent time bases |
| MC PWM: Motor Control Pulse Width Modulation | Motor control 16-bit PWM with multiple synchronized pulse-width modulation, up to six outputs with four duty cycle generators and resolution up to 1 ns |
| SMPS PWM: Power Supply Pulse Width Modulation | Power supply 16-bit PWM with multiple synchronized pulse-width modulation, up to eight outputs with four independent time bases and resolution up to 1 ns |
| IC: Input Capture | Input capture with an independent timer base to capture an external event |
| OC: Output Compare | Output compare with an independent time base to compare value with compare registers and generate a single output pulse, or a train of output pulses on a compare match event |
| TIMERS AND INTERFACES | |
| Host BiSS Interface | Host bidirectional Serial Synchronous (BiSS) is a digital interface for actuators used in position control |
| 16-/32-bit Timer | General-purpose 16-/32-bit timer/counter with compare capability |
| QEI: Quadrature Encoder Interface | Quadrature encoder interface to increment encoders for obtaining mechanical position data |
| SAFETY AND MONITORING: Hardware Monitoring and Fault Detection | |
| Error Correction Code | ECC detects the presence of single and double bit errors, and corrects single bit error automatically |
| RAM MBIST: Memory Built-In Self-Test | RAM MBIST tests for functional correctness of all memory locations |
| WDT: Watch Dog Timer | System supervisory circuit that generates a reset when software timing anomalies are detected within a configurable critical window |
| DMT: Dead Man Timer | System supervisory circuit that generates a reset when instruction sequence anomalies are detected within a configurable critical window |
| CRC: Cyclical Redundancy Check with Memory Scan | Automatically calculates CRC checksum of Program/Data/EE memory for NVM integrity and a general-purpose 16-bit CRC for use with memory and communications data |
| IO Integrity Monitors (IOIM) | The module validates the IO functionality in safety-critical applications by checking an output signal against a reference |
| Hardware Safety Features | Hardware Safety features include Flash error correction, RAM MBIST, backup system oscillator, WDT, DMT, CRC scan, etc. |
| Functional Safety - ISO 26262/IEC 61508 | Functional Ready Devices are ideal for automotive and industrial safety applications requiring ISO 26262 (ASIL B/C) and IEC 61508 (SIL 2/3) safety compliance. |
| IEC 60730 Class B Safety | IEC 60730 Functional Safety Ready Devices offers Class B safety diagnostic libraries for designing household applications |

| COMMUNICATIONS: General, Industrial, Lighting and Automotive | |
|--|---|
| USB OTG: Universal Serial Bus | USB 2.0 full-speed (host and device), low-speed (host) and On-The-Go (OTG) support |
| CAN/CAN FD: Controller Area Network | Industrial- and automotive-centric communication bus |
| UART: Universal Asynchronous Receiver Transceiver | General-purpose full-duplex, 8-bit or 9-bit data serial communications with optional ISO 7816 Smart Card support |
| LIN: Local Interconnect Network | 1. Industrial- and automotive-centric communication bus 2. Support for LIN when using the EUSART |
| I²C: Inter-Integrated Circuit | General purpose 2-wire inter IC serial interface for communicating with other peripherals or microcontroller devices |
| SPI: Serial Peripheral Interface | General-purpose 4-wire synchronous serial interface for communicating with other peripherals or microcontroller devices |
| I²S: Data Converter Interface | 3-wire synchronous half duplex serial interface to handle the stereo data |
| SENT: Single-Edge Nibble Transmission | SENT is an unidirectional, single-wire serial communications protocol designed for point-to-point transmission of signal values |
| USER INTERFACE: CAPACITIVE TOUCH SENSING | |
| Capacitive Touch Sensing | Capacitive sensing for touch buttons, sliders and system measurement and deduction (e.g. water level, intrusion detection, etc) |
| EMBEDDED SECURITY | |
| Security Access Control | Helps in realizing secure boot, secure firmware update, secure debug access control, code protection and device locking |
| CodeGuard Security - Secure Boot | Allows devices to configure the boot segment as a read-only section of memory to protect the bootloader from modification via remote digital attacks. |
| Flash OTP by ICSP™ Write Inhibit | Flash OTP by ICSP™ Write Inhibit enables Flash to be configured as One-Time Programmable (OTP) memory with the ability to write and read protect the Flash memory |
| Integrated Secure Subsystem (HSM) | Supports implementing secure boot, Message Authentication, trusted firmware updates, mutual node authentication and multiple key management protocols |
| SYSTEM FLEXIBILITY: System Peripherals and Interconnects | |
| Dual Partition Flash | Dual partition Flash operation, allowing the support of robust bootloader systems and fail-safe storage of application code, with options designed to enhance code security |
| CLC: Configurable Logic Cell | Integrated combinational and sequential logic with custom interconnection and re-routing of digital peripherals |
| PPS: Peripheral Pin Select | I/O pin remapping of digital peripherals for greater design flexibility and improved EMI board layout |
| PTG: Peripheral Trigger Generator | User-programmable sequencer, capable of generating complex trigger signal sequences to coordinate the operation of other peripherals |
| DMA: Direct Memory Access | Direct memory access for transfer of data between the CPU and its peripherals without CPU assistance |
| DOZE, IDLE, SLEEP and PMD | Low-power saving modes |

Learn more about dsPIC33 DSCs at
www.microchip.com/dsPIC