RX260/RX261 Group, RX130 Group

Differences Between the RX260/RX261 Group and the RX130 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX261 Group and RX130 Group. It also explains key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX261 Group and the 100-pin package version of the RX130 Group as the maximum specifications. For details about the differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual of the products in question.

Target Devices

- RX260/RX261 Group, RX130 Group

Contents

1. Comparison of Built-In Functions of RX260/RX261 Group and RX130 Group

The following is a comparison of the built-in functions of the RX260/RX261 Group and the RX130 Group. For details about the functions, see section 1. Comparison of Built-In Functions of RX260/RX261 Group and RX130 Group and section 5. Reference Documents.

Table 1.1 shows a Comparison of Built-In Functions of RX130 Group and RX260/RX261 Group.

Table 1.1 Comparison of Built-In Functions of RX130 Group and RX260/RX261 Group

Function	RX130	RX260/ RX261
CPU	●	
Operating modes	○	
Address space	▲	
Resets	●	
Option-setting memory (OFSM)	●/▲	
Voltage detection circuit (LVDAb)	●/▲	
Clock generation circuit	●/▲	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●/▲/■	
Register write protection function	▲	
Exception handling	●	
Interrupt controller (ICUb)	●/▲	
Buses	▲	
Memory protection unit (MPU)	×	○
DMA controller (DMACA)	×	○
Data transfer controller (DTCa): RX130, (DTCb): RX260/RX261	●	
Event link controller (ELC)	●/▲/■	
I/O ports	▲	
Multi-function pin controller (MPC)	●/▲/■	
Multi-function timer pulse unit 2 (MTU2a)	○	×
General-purpose PWM timer (GPTWa)	×	○
Port output enable 2 (POE2a)	○	×
Port output enable for GPTW (POEGc)	×	○
8-bit timer (TMR): RX130, (TMRa): RX260/RX261	▲	
Compare match timer (CMT)	○	
Realtime clock (RTCc): RX130, (RTCBa): RX260/RX261	●	
Low power timer (LPT): RX130, (LPTa): RX260/RX261	●	
Watchdog timer (WDTA)	×	○
Independent watchdog timer (IWDTa)	●/▲	
USB 2.0 FS host/function module (USBe)*1	×	○
Serial communications interface (SCIg, SCIh): RX130, (SCIk, SCIh): RX260/RX261	●/▲/■	
Serial communications interface (RSCI)	×	○

Function	RX130	RX260/ RX261
I²C bus interface (RIICa)	○	
CAN FD module (CANFD) *1	×	○
Serial peripheral interface (RSPIa): RX130, (RSPIc): RX260/RX261	●/▲/■	
CRC calculator (CRC)	○	
Remote control signal receiver (REMC): RX130, (REMCa): RX260/RX261	●/▲/■	
Renesas Secure IP (RSIP-E11A)*1	×	○
Capacitive touch sensing unit (CTSUa): RX130, (CTSU2SLa): RX260/RX261	●/▲/■	
12-bit A/D converter (S12ADE)	●/▲	
D/A converter (DAa)	○	
Temperature sensor (TEMPSA)	▲	
Comparator B (CMPBa)	●	
Data operation circuit (DOC)	○	
RAM	●/▲	
Flash memory (FLASH)	●/▲	
Packages	■	

Note: 1. Not implemented in RX260 Group products.

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications and a comparison of registers.

In the comparative overview, **red text** indicates specifications which are included only in one of the MCU groups, and specifications that differ between the two groups.

In the register comparison, **red text** indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specifications that do not differ are not listed.

2.1 CPU

Table 2.1 shows a Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX130	RX261
CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 64 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard built-in instructions: 111 Basic instructions: 77 Single-precision floating-point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions that conform to the IEEE 754 standard

2.2 Address Space

Figure 2.1 shows a Comparative Memory Map of Single-Chip Mode.

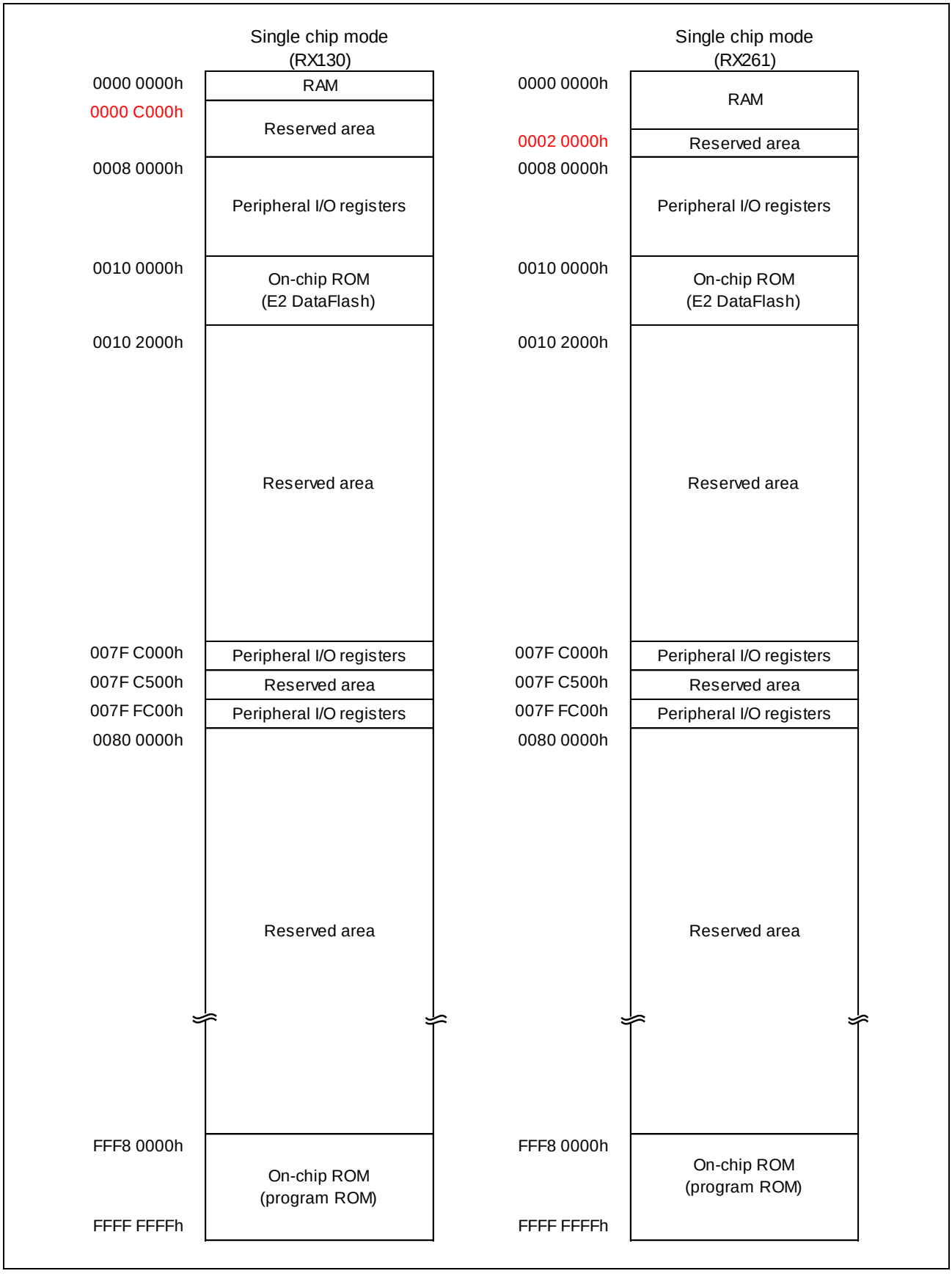

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Resets

Table 2.2 shows a Comparative Overview of Reset Sources and Table 2.3 shows a Comparison of Reset-Related Registers.

Table 2.2 Comparative Overview of Reset Sources

Item	RX130	RX261
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Independent watchdog timer reset	The independent watchdog timer underflows or a refresh error occurs.	The independent watchdog timer underflows or a refresh error occurs.
Watchdog timer reset	—	The watchdog timer underflows or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.3 Comparison of Reset-Related Registers

Register	Bit	RX130	RX261
RSTSR2	WDTRF	—	Watchdog timer reset detect flag

2.4 Option-Setting Memory

Table 2.4 shows a Comparison of Option-Setting Memory Registers.

Table 2.4 Comparison of Option-Setting Memory Registers

Register	Bit	RX130 (OFSM)	RX261 (OFSM)
OFS0	WDTSTRT	—	WDT start mode select bit
	WDTTOPS[1:0]	—	WDT timeout period select bits
	WDTCKS[3:0]	—	WDT clock division ratio select bits
	WDTRPES[1:0]	—	WDT window end position select bits
	WDTRPSS[1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0:0: 3.84 V is selected. 0:1: 2.82 V is selected. 1:0: 2.51 V is selected. 1:1: 1.90 V is selected.	Voltage detection 0 level select bits b1 b0 0:0: 3.85 V is selected. 0:1: 2.85 V is selected. 1:0: 2.53 V is selected. 1:1: 1.90 V is selected.
	VDSEL2	—	Voltage detection 0 level select bit 2
	HOCOFRQ[1:0]	—	HOCO frequency select bits

2.5 Voltage Detection Circuit

Table 2.5 shows a Comparative Overview of Voltage Detection Circuits and Table 2.6 shows a Comparison of Voltage Detection Circuit Registers.

Table 2.5 Comparative Overview of Voltage Detection Circuits

Item		RX130 (LVDAb)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
				Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR. EXVCCINP2 bit.			Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR. EXVCCINP2 bit.
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from fourteen levels using LVDLVLR. LVD1LVL [3:0] bits	Selectable from four levels using LVDLVLR. LVD2LVL [1:0] bits	Selectable from five levels using the OFS1 register	Selectable from sixteen levels using LVDLVLR. LVD1LVL [3:0] bits	Selectable from four levels using LVDLVLR. LVD2LVL [1:0] bits
	Monitoring flags	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection

Item		RX130 (LVDAb)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Resets	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin
	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, VCC or CMPA2 pin > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, VCC or CMPA2 pin > Vdet2, or both
Event link function		—	Available: Event output at Vdet1 passage detection	—	—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection

Table 2.6 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX130 (LVDAb)	RX261 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during voltage drop) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the preceding are prohibited.	Voltage detection 1 level select bits (Standard voltage during voltage drop) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V 1 1 1 0: 1.75 V 1 1 1 1: 1.65 V Settings other than the preceding are prohibited.
		The initial value after a reset differs.	
	LVD2LVL[1:0]	Voltage detection 2 level select bits (Standard voltage during voltage drop) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during voltage drop) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V

2.6 Clock Generation Circuit

Table 2.7 shows a Comparative Overview of Clock Generation Circuits and Table 2.8 shows a Comparison of Clock Generation Circuit Registers.

Table 2.7 Comparative Overview of Clock Generation Circuits

Item	RX130	RX261
Uses	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the CANFD (message buffer RAM) and GPTW.
	• Generates the peripheral module clocks (PCLKB and PCLKD) supplied to peripheral modules. PCLKD is the operating clock for the S12AD module, and PCLKB is the operating clock for modules other than S12AD.	• Generates the peripheral module clock (PCLKB) supplied to peripheral modules. • Generates the peripheral module (for analog conversion) clock (PCLKD) supplied to the S12AD.
	• Generates the FlashIF clock (FCLK) supplied to the FlashIF.	• Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the USB clock (UCLK) supplied to the USB.
	• Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the dedicated RTC sub-clock (RTCSCLK) supplied to the RTC. • Generates the dedicated IWDT clock (IWDTCLK) supplied to the IWDT.	• Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC clock (RTCSCLK) supplied to the RTC. • Generates the dedicated IWDT clock (IWDTCLK) supplied to the IWDT. • Generates the CANFD clock (CANFDCLK) supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) supplied to the CANFD.
	• Generates the LPT clock (LPTCLK) supplied to the LPT. • Generates the REMC clock (REMCLK) supplied to the REMC.	• Generates the LPT clock (LPTCLK) supplied to the LPT. • Generates the REMC clock (REMCLK) supplied to the REMC.

Item	RX130	RX261
Operating frequencies	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (when programming and erasing ROM and E2 DataFlash) — 32 MHz (max.) (when reading from E2 DataFlash) • LPTCLK: The same frequency as that of the selected oscillator. • REMCLK: The same frequency as that of the selected oscillator. • CACCLK: Same frequency as each oscillator. • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz	• ICLK: 64 MHz (max.) • PCLKA: 64 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 64 MHz (max.) • FCLK: — 1 MHz to 64 MHz (when programming and erasing ROM and E2 DataFlash) — 64 MHz (max.) (when reading from E2 DataFlash) • UCLK: 48 MHz • CANFDCLK: 32 MHz (max.) • CANFDMCLK: 20 MHz (max.) • LPTCLK: — 32.768 kHz (when sub-clock is selected) — 15 kHz (when the dedicated IWDT clock (IWDTCLK) is selected) — 1 MHz (when the LOCO clock (divided by 4) is selected) • REMCLK: The same frequency as that of the selected oscillator. • CACCLK: The same frequency as that of the selected oscillator. • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz
Main clock oscillator	• Resonator frequency: — 1 MHz to 20 MHz (VCC ≥ 2.4 V) — 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcibly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and the GPTW pin can be forcibly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • External clock input frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN, XCOUT • Sub-clock external input pin: EXCIN • Drive capacity switching function

Item	RX130	RX261
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (in increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (in increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz
PLL2 circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (in increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 24 MHz, 32 MHz, 48 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.8 Comparison of Clock Generation Circuit Registers

Register	Bit	RX130	RX261
SCKCR	PCKA	—	Peripheral module clock A (PCLKA) select bit
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Settings other than the preceding are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 Settings other than the preceding are prohibited.
PLL2CR	—	—	PLL2 control register
PLL2CR2	—	—	PLL2 control register 2
SOSCCR	SOSTP	Sub-clock oscillator control register	Sub-clock oscillator control register
		The initial value after a reset differs.	
HOFCR	—	High-speed on-chip oscillator forced oscillation control register	—
OSCOVFSR	PL2OVF	—	PLL2 clock oscillation stabilization flag

Register	Bit	RX130	RX261
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs) 0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) Settings other than the preceding are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)	Main clock oscillator wait time b4 b0 0 0 0 0 0: Wait time = 0 cycles (0 µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs) 0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131072 cycles (32.768 ms) Settings other than the preceding are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)
CKOCR	CKOSEL [3:0]	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Sub-clock Settings other than the preceding are prohibited.	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO select 0 0 0 1: HOCO select 0 0 1 0: Main clock oscillator select 0 0 1 1: Sub-clock oscillator select 0 1 0 0: PLL circuit select 1 0 0 0: CTSU monitor clock select Settings other than the preceding are prohibited.
	CKODIV [2:0]	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: Divided by 2 0 1 0: Divided by 4 0 1 1: Divided by 8 1 0 0: Divided by 16 Settings other than the preceding are prohibited.	CLKOUT output division ratio select bits b14 b12 0 0 0: Divided by 1 0 0 1: Divided by 2 0 1 0: Divided by 4 0 1 1: Divided by 8 1 0 0: Divided by 16 1 0 1: Divided by 32 1 1 0: Divided by 64 1 1 1: Divided by 128

Register	Bit	RX130	RX261
MOFCR	MODRV21	Main clock oscillator drive capability switch bit VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited	Main clock oscillator drive capability switch bit 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
LOCOTRR	—	Low-speed on-chip oscillator trimming register	—
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
CANFDCKDIVCR	—	—	CANFD clock division control register
USBCKCR	—	—	USB clock control register
CANFDCKCR	—	—	CANFD clock control register
SOMCR	—	—	Sub-clock oscillator mode control register

2.7 Low Power Consumption

Table 2.9 shows a Comparative Overview of Low Power Consumption Functions, Table 2.10 shows a Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 shows a Comparative of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX130	RX261
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	The CPU, peripheral modules, or oscillators can be stopped to enter a low power consumption state.	The CPU, peripheral modules, or oscillators can be stopped to enter a low power consumption state.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.10 Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX261
Sleep mode	Enter method	Control register + instruction	Control register + instruction
	Exit method other than reset	Interrupt	Interrupt
	State after exit	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating possible	Operating possible
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Operating possible	Operating possible
	Low-speed on-chip oscillator	Operating possible	Operating possible
	IWDT dedicated on-chip oscillator	Operating possible	Operating possible
	PLL	Operating possible	Operating possible
	PLL2	—	Operating possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh): RX130 (0000 0000h to 0001 FFFFh): RX261	Operating possible (retained)	Operating possible (retained)
	DMAC	—	Operating possible
	DTC	Operating possible	Operating possible
	Flash memory	Operating	Operating
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Remote control signal receiver (REMC)	Operating possible	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	Low power timer (LPT)	Operating possible	Operating possible
	Voltage detection circuit (LVD)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operating possible	Operating possible
	I/O ports	Operating	Operating
	RTCOUT output	Operating possible	Operating possible
	CLKOUT output	Operating possible	Operating possible
	Comparator B	Operating possible	Operating possible
Deep sleep mode	Enter method	Control register + instruction	Control register + instruction
	Exit method other than reset	Interrupt	Interrupt
	State after exit	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating possible	Operating possible
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Operating possible	Operating possible
	Low-speed on-chip oscillator	Operating possible	Operating possible
	IWDT dedicated on-chip oscillator	Operating possible	Operating possible
	PLL	Operating possible	Operating possible
	PLL2	—	Operating possible
	CPU	Stopped (retained)	Stopped (retained)

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX261
Deep sleep mode	RAM0 (0000 0000h to 0000 BFFFh): RX130 (0000 0000h to 0001 FFFFh): RX261	Stopped (retained)	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Remote control signal receiver (REMC)	Operating possible	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	Low power timer (LPT)	Operating possible	Operating possible
	Voltage detection circuit (LVD)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operating possible	Operating possible
	I/O ports	Operating	Operating
	RTCOUT output	Operating possible	Operating possible
	CLKOUT output	Operating possible	Operating possible
	Comparator B	Operating possible	Operating possible
Software standby mode	Enter method	Control register + instruction	Control register + instruction
	Exit method other than reset	Interrupt	Interrupt
	State after exit	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Operating possible	Stopped
	Low-speed on-chip oscillator	Stopped	Operating possible
	IWDT dedicated on-chip oscillator	Operating possible	Operating possible
	PLL	Stopped	Stopped
	PLL2	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh): RX130 (0000 0000h to 0001 FFFFh): RX261	Stopped (retained)	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Remote control signal receiver (REMC)	Operating possible	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	Low power timer (LPT)	Operating possible	Operating possible
	Voltage detection circuit (LVD)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX261
Software standby mode	RTCOUT output	Operating possible	Operating possible
	CLKOUT output	Operating possible	Operating possible
	Comparator B	Operating possible	Operating possible
Snooze mode	Enter method	—	The condition that enters snooze mode is met while in software standby mode
	Exit method other than reset	—	Interrupt or condition that exits snooze mode is met
	State after exit	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operating possible
	Sub-clock oscillator	—	Operating possible
	High-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	—	Operating possible
	IWDT dedicated on-chip oscillator	—	Operating possible
	PLL	—	Operating possible
	PLL2	—	Operating possible
	CPU	—	Stopped (retained)
	RAM	—	Operating possible (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Operating possible
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operating possible
	Realtime clock (RTC)	—	Operating possible
	Low power timer (LPT)	—	Operating possible
	Remote control signal receiver (REMC)	—	Operating possible
	Voltage detection circuit (LVD)	—	Operating possible
	Power-on reset circuit	—	Operating
	Peripheral modules	—	Operating possible
	I/O ports	—	Operating
	RTCOUT output	—	Operating possible
	CLKOUT output	—	Operating possible
	Comparator B	—	Operating possible

Note: “Operating possible” indicates that the control register setting determines whether the state is operating or stopped.
“Stopped (retained)” indicates that internal operations are suspended with internal register values retained.

Table 2.11 Comparative of Low Power Consumption Registers

Register	Bit	RX130	RX261
MSTPCRA	MSTPA7	—	General-purpose PWM timer module stop bit
	MSTPA9	Multi-function timer pulse unit module stop bit	—
	MSTPA14	—	Compare match timer (unit 1) module stop bit
	MSTPA28	Data transfer controller module stop bit Target module: DTC	DMA controller/data transfer controller module stop bit Target module: DMAC/DTC
MSTPCRB	MSTPB19	—	USB 2.0 FS host/function module stop bit
MSTPCRC	MSTPC0	RAM module stop bit Target module: RAM (0000 0000h to 0000 FFFFh)	RAM module stop bit Target module: RAM (0000 0000h to 0001 FFFFh)
	MSTPC28	Remote control signal receiver 1 module stop bit	—
MSTPCRD	MSTPD9	—	CANFD0 module stop bit
	MSTPD31	—	RSIP module stop bit
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than the preceding are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the preceding are prohibited.
SOPCCR	SOPCM	Sub operating power control mode select bit 0: High-speed operating mode or middle-speed operating mode 1: Low-speed operating mode	Sub operating power control mode select bit 0: High-speed operating mode, middle-speed operating mode, or middle-speed operating mode 2 1: Low-speed operating mode
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2
RPSCR	—	—	RAM power-saving control register

2.8 Register Write Protection Functions

Table 2.12 shows a Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX130	RX261
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, PLL2CR, PLL2CR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR, CANFDCKCR, CANFDCKDIVCR, USBCKCR
PRC1 bit	• Register related to operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, RPSCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	• Registers related to low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	• Registers related to low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Exception Handling

Table 2.13 shows a Comparative Overview of Exception Handling, Table 2.14 shows a Comparison of Vectors, and Table 2.15 shows a Comparison of Instructions for Returning from Exception Handling Routines.

Table 2.13 Comparative Overview of Exception Handling

Item	RX130	RX261
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.14 Comparison of Vectors

Item		RX130	RX261
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupts	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.15 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX130	RX261
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		—	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupts	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controllers

Table 2.16 shows a Comparative Overview of Interrupt Controllers and Table 2.17 shows a Comparison of Interrupt Controller Registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX130 (ICUb)	RX261 (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each source of connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or rising and falling edges can be set at the source level. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or rising and falling edges can be set at the source level. • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	An ELSR8l or ELSR18l interrupt can be generated by an ELC event.	An ELSR8l, ELSR18l, or ELSR19l interrupt can be generated by an ELC event.
	Interrupt priority	Priority is set by register.	Priority is set by register.
	Fast interrupt function	Faster CPU interrupt handling can be enabled. This can be enabled for a single interrupt source only.	Faster CPU interrupt handling can be enabled. This can be enabled for a single interrupt source only.
	DTC and DMAC control	The DTC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupts from NMI pins • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported	• Interrupts from NMI pins • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	An interrupt is generated when an oscillation stop is detected.	An interrupt is generated when an oscillation stop is detected.
	WDT underflow/ refresh error interrupt	—	An interrupt is generated by underflow of the down counter or a refresh error.
	IWDT underflow/ refresh error interrupt	An interrupt is generated by underflow of the down counter or a refresh error.	An interrupt is generated by underflow of the down counter or a refresh error.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage monitoring circuit 1 (LVD1)

Item		RX130 (ICUb)	RX261 (ICUb)
Non-maskable interrupts	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Interrupt from voltage monitoring circuit 2 (LVD2)
	RAM error interrupt	—	An interrupt is generated when a RAM parity check error is detected.
Return from low power consumption modes	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by any non-maskable interrupt and any other interrupt.
	Deep sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by any non-maskable interrupt and any other interrupt.
	Software standby mode	Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, or an RTC alarm or periodic interrupt.	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm or periodic interrupt, REMC, USB0 resume), or ELSR8 interrupt (LPT-dedicated interrupt).
	Snooze mode	—	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm or periodic interrupt, REMC, USB0 resume), or SNZI interrupt (snooze exit interrupt).

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX130 (ICUb)	RX261 (ICUb)
DMRSRm	—	—	DMAC trigger select register m
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit

2.11 Buses

Table 2.18 shows a Comparative Overview of Buses.

Table 2.18 Comparative Overview of Buses

Item		RX130	RX261
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to ROM
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules • Operates in synchronization with the peripheral module clocks (PCLKB and PCLKD)	• Connected to peripheral modules (peripheral modules other than internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (Touch) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB0, CANFD, CTSU, REMC, and RSCI) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	—	• Connected to peripheral modules (GPTW) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	—	• Connected to peripheral modules (CANFD (message buffer RAM)) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.19 Comparison of Bus-Related Registers

Register	Bit	RX130	RX261
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPHB[1:0]	—	Internal peripheral bus 4, 5 priority control bits

2.12 Data Transfer Controller

Table 2.20 shows a Comparative Overview of Data Transfer Controllers and Table 2.21 shows a Comparison of Data Transfer Controller Registers.

Table 2.20 Comparative Overview of Data Transfer Controllers

Item	RX130 (DTCa)	RX261 (DTCb)
Number of transfer channels	Equal to the total number of interrupt sources that can start a DTC transfer.	Equal to the total number of interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits, or 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits, or 1,024 bytes.
Chain transfer function	• Multiple data transfers can be executed consecutively in response to a single transfer request (chain transfer). • For chain transfers, you can select “performed only when the transfer counter becomes 0” or “every time”.	• Multiple data transfers can be executed consecutively in response to a single transfer request (chain transfer). • For chain transfers, you can select “performed only when the transfer counter becomes 0” or “every time”.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected and executed based on the transfer data. • Only one sequence transfer trigger source can be selected at a time. • A maximum of 256 sequences can be specified for a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • An entire sequence can be executed for a single request, or the sequence can be suspended and resumed on the next transfer request (this is called sequence division).

Item	RX130 (DTCa)	RX261 (DTCb)
Transfer space	• Short address mode: 16 MB (non-reserved areas within the ranges from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh) • Full address mode: 4 GB (non-reserved areas within the range from 0000 0000h to FFFF FFFFh)	• Short address mode: 16 MB (non-reserved areas within the ranges from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh) • Full address mode: 4 GB (non-reserved areas within the range from 0000 0000h to FFFF FFFFh)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of a specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of a specified number of data units.
Event link function	An event link request is generated after a single data transfer (or after one block for block transfers).	An event link request is generated after a single data transfer (or after one block for block transfers).
Read skip	A setting can be specified that skips the reading of transfer information when the same transfer is repeated.	A setting can be specified that skips the reading of transfer information when the same transfer is repeated.
Write-back skip	Write-back can be skipped for transferred data that is not updated if the address of the transfer source or destination is fixed.	Write-back can be skipped for transferred data that is not updated if the address of the transfer source or destination is fixed.
Write-back disable	—	Write-back of transfer information can be disabled.
Displacement addition	—	Displacement can be added to the source address (selectable at the transfer information level).
Low power consumption function	Can transition to module stop state.	Can transition to module stop state.

Table 2.21 Comparison of Data Transfer Controller Registers

Register	Bit	RX130 (DTCa)	RX261 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.13 Event Link Controller

Table 2.22 shows a Comparative Overview of Event Link Controllers, Table 2.23 shows a Comparison of Event Link Controller Registers, Table 2.24 shows a Correspondence Between ELSRn Registers and Peripheral Modules, and Table 2.25 shows a Correspondence Between Event Signal Names Set in ELSRn.ELS[7:0] and Signal Numbers.

Table 2.22 Comparative Overview of Event Link Controllers

Item	RX130 (ELC)	RX261 (ELC)
Event link function	• 47 types of event signal can be directly linked to peripheral modules. • The operation of timer-related peripheral modules at event input can be selected. • Event link operation is supported for port B — Single port: Event linkage can be set for a specified single port. — Port group: Event linkage can be set for a group of specified ports (selected from a maximum of eight ports).	• 116 types of event signal can be directly linked to peripheral modules. • The operation of timer-related peripheral modules at event input can be selected. • Event link operation is supported for port B and port E — Single port: Event linkage can be set for a specified single port. — Port group: Event linkage can be set for a group of specified ports (selected from a maximum of eight ports).
Low power consumption function	Can transition to module stop state.	Can transition to module stop state.

Table 2.23 Comparison of Event Link Controller Registers

Register	Bit	RX130 (ELC)	RX261 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 14 to 16, 18, 20, 22, 24, 25)	Event link setting register n (n = 7, 8, 10, 12, 14 to 16, 18 to 28, 48 to 56)
	ELS[7:0]	Event link select bits 00h: Disables event output to the applicable peripheral module. 08h to 6Ah: Specify the number of the event signal to be linked. Settings other than the preceding are prohibited.	Event link select bits 00h: Disables event signal output to the applicable peripheral module. 1Fh to C6h: Specify the number of the event signal to be linked. Settings other than the preceding are prohibited.
ELOPA	—	Event link option setting register A	—
ELOPB	—	Event link option setting register B	—
PGR2	—	—	Port group setting register 2
PGC2	—	—	Port group control register 2
PDBF2	—	—	Port buffer register 2
PEL2	—	—	Event link port setting register 2
PEL3	—	—	Event link port setting register 3

Table 2.24 Correspondence Between ELSRn Registers and Peripheral Modules

Register	RX130 (ELC)	RX261 (ELC)
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	—
ELSR4	MTU4	—
ELSR7	CMT1	CMT1
ELSR8	ICU (LPT-dedicated interrupt)	ICU (LPT-dedicated interrupt)
ELSR10	TMR0	TMR0
ELSR12	TMR2	TMR2
ELSR14	CTSU	CTSU
ELSR15	S12AD	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	—	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	—	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	—	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	—	Single port 2
ELSR27	—	Single port 3
ELSR28	—	Clock source switches to LOCO
ELSR48	—	GPTW event source A (all channels)
ELSR49	—	GPTW event source B (all channels)
ELSR50	—	GPTW event source C (all channels)
ELSR51	—	GPTW event source D (all channels)
ELSR52	—	GPTW event source E (all channels)
ELSR53	—	GPTW event source F (all channels)
ELSR54	—	GPTW event source G (all channels)
ELSR55	—	GPTW event source H (all channels)
ELSR56	—	S12AD (ELCTRG01N)

Table 2.25 Correspondence Between Event Signal Names Set in ELSRn.ELS[7:0] and Signal Numbers

Value of ELS[7:0] Bits	RX130 (ELC)	RX261 (ELC)
08h	MTU1 compare match 1A	—
09h	MTU1 compare match 1B	—
0Ah	MTU1 overflow	—
0Bh	MTU1 underflow	—
0Ch	MTU2 compare match 2A	—
0Dh	MTU2 compare match 2B	—
0Eh	MTU2 overflow	—
0Fh	MTU2 underflow	—
10h	MTU3 compare match 3A	—
11h	MTU3 compare match 3B	—
12h	MTU3 compare match 3C	—
13h	MTU3 compare match 3D	—
14h	MTU3 overflow	—
15h	MTU4 compare match 4A	—
16h	MTU4 compare match 4B	—
17h	MTU4 compare match 4C	—
18h	MTU4 compare match 4D	—
19h	MTU4 overflow	—
1Ah	MTU4 underflow	—
1Fh	CMT1 compare match 1	CMT1 compare match 1
22h	TMR0 compare match A0	TMR0 compare match A0
23h	TMR0 compare match B0	TMR0 compare match B0
24h	TMR0 overflow	TMR0 overflow
28h	TMR2 compare match A2	TMR2 compare match A2
29h	TMR2 compare match B2	TMR2 compare match B2
2Ah	TMR2 overflow	TMR2 overflow
2Eh	—	RTC periodic event (Select 1/256 seconds, 1/128 seconds, 1/64 seconds, 1/32 seconds, 1/16 seconds, 1/8 seconds, 1/4 seconds, 1/2 seconds, 1 second, or 2 seconds.)
31h	—	IWDT underflow/refresh error
32h	LPT compare match 0	LPT compare match 0
33h	—	LPT compare match 1
34h	S12AD comparison conditions are met	S12AD comparison conditions are met
35h	S12AD comparison conditions are not met	S12AD comparison conditions are not met
3Ah	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh	SCI5 receive data full	SCI5 receive data full
3Ch	SCI5 transmit data empty	SCI5 transmit data empty
3Dh	SCI5 transmit end	SCI5 transmit end
4Eh	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh	RIIC0 receive data full	RIIC0 receive data full
50h	RIIC0 transmit data empty	RIIC0 transmit data empty
51h	RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	RX130 (ELC)	RX261 (ELC)
52h	—	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h	—	RSPI0 idle
54h	—	RSPI0 receive data full
55h	—	RSPI0 transmit data empty
56h	—	RSPI0 transmit end
58h	S12AD A/D conversion end	S12AD A/D conversion end
59h	Comparison result change of comparator B0	Comparison result change of comparator B0
5Ah	Comparison result change of comparator B0/B1	Comparison result change of comparator B0/B1
5Bh	LVD1 voltage detection	LVD1 voltage detection
5Ch	—	LVD2 voltage detection
5Dh	—	DMAC0 transfer end
5Eh	—	DMAC1 transfer end
5Fh	—	DMAC2 transfer end
60h	—	DMAC3 transfer end
61h	DTC transfer end	DTC transfer end
62h	—	Clock generation circuit oscillation stop detection
63h	Input edge detection of input port group 1	Input edge detection of input port group 1
64h	—	Input edge detection of input port group 2
65h	Input edge detection of single input port 0	Input edge detection of single input port 0
66h	Input edge detection of single input port 1	Input edge detection of single input port 1
67h	—	Input edge detection of single input port 2
68h	—	Input edge detection of single input port 3
69h	Software event	Software event
6Ah	DOC data operation condition met	DOC data operation condition met
80h	—	GPTW0 compare match A
81h	—	GPTW0 compare match B
82h	—	GPTW0 compare match C
83h	—	GPTW0 compare match D
84h	—	GPTW0 compare match E
85h	—	GPTW0 compare match F
86h	—	GPTW0 overflow
87h	—	GPTW0 underflow
88h	—	GPTW0 A/D conversion start request A
89h	—	GPTW0 A/D conversion start request B
8Ah	—	GPTW1 compare match A
8Bh	—	GPTW1 compare match B
8Ch	—	GPTW1 compare match C
8Dh	—	GPTW1 compare match D
8Eh	—	GPTW1 compare match E
8Fh	—	GPTW1 compare match F
90h	—	GPTW1 overflow
91h	—	GPTW1 underflow
92h	—	GPTW1 A/D conversion start request A
93h	—	GPTW1 A/D conversion start request B
94h	—	GPTW2 compare match A

Value of ELS[7:0] Bits	RX130 (ELC)	RX261 (ELC)
95h	—	GPTW2 compare match B
96h	—	GPTW2 compare match C
97h	—	GPTW2 compare match D
98h	—	GPTW2 compare match E
99h	—	GPTW2 compare match F
9Ah	—	GPTW2 overflow
9Bh	—	GPTW2 underflow
9Ch	—	GPTW2 A/D conversion start request A
9Dh	—	GPTW2 A/D conversion start request B
9Eh	—	GPTW3 compare match A
9Fh	—	GPTW3 compare match B
A0h	—	GPTW3 compare match C
A1h	—	GPTW3 compare match D
A2h	—	GPTW3 compare match E
A3h	—	GPTW3 compare match F
A4h	—	GPTW3 overflow
A5h	—	GPTW3 underflow
A6h	—	GPTW4 compare match A
A7h	—	GPTW4 compare match B
A8h	—	GPTW4 compare match C
A9h	—	GPTW4 compare match D
AAh	—	GPTW4 compare match E
ABh	—	GPTW4 compare match F
ACh	—	GPTW4 overflow
ADh	—	GPTW4 underflow
AEh	—	GPTW5 compare match A
AFh	—	GPTW5 compare match B
B0h	—	GPTW5 compare match C
B1h	—	GPTW5 compare match D
B2h	—	GPTW5 compare match E
B3h	—	GPTW5 compare match F
B4h	—	GPTW5 overflow
B5h	—	GPTW5 underflow
B6h	—	GPTW6 compare match A
B7h	—	GPTW6 compare match B
B8h	—	GPTW6 compare match C
B9h	—	GPTW6 compare match D
BAh	—	GPTW6 compare match E
BBh	—	GPTW6 compare match F
BCh	—	GPTW6 overflow
BDh	—	GPTW6 underflow
BEh	—	GPTW7 compare match A
BFh	—	GPTW7 compare match B
C0h	—	GPTW7 compare match C
C1h	—	GPTW7 compare match D
C2h	—	GPTW7 compare match E
C3h	—	GPTW7 compare match F

Value of ELS[7:0] Bits	RX130 (ELC)	RX261 (ELC)
C4h	—	GPTW7 overflow
C5h	—	GPTW7 underflow
C6h	—	GPTW (OPS) U-/V-/W-phase input edge detected

2.14 I/O Ports

Table 2.26 to Table 2.29 show a comparative overview of I/O ports, Table 2.30 shows a Comparison of I/O Port Functions, and Table 2.31 shows a Comparison of I/O Port Registers.

Table 2.26 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX130 (100-Pin)	RX261 (100-Pin)
PORT0	P03 to P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0,PH3, PH6, PH7
PORTJ	PJ1, PJ3, PJ6, PJ7	PJ1, PJ3, PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.27 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX130 (80-Pin)	RX261 (80-Pin)
PORT0	P03 to P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3, PH6, PH7
PORTJ	PJ1, PJ6, PJ7	PJ1, PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.28 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX130 (64-Pin)	RX261 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6

Port Symbol	RX130 (64-Pin)	RX261 (64-Pin)
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3, PH6, PH7
PORTJ	PJ6, PJ7	PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.29 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX130 (48-Pin)	RX261 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P45 to P47	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC0 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3
PORTJ	PJ6, PJ7	PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.30 Comparison of I/O Port Functions

Item	Port Symbol	RX130	RX261
Input pull-up function	PORT0	P03 to P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	P50 to P55
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTG	—	PG7
	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	PJ1, PJ3, PJ6, PJ7	PJ1, PJ3, PJ6, PJ7
Open drain output function	PORT1	P12 to P17	P12 to P17
	PORT2	P20, P21 to P23, P26, P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT5	—	P50 to P52, P54
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD2	PD0 to PD2
	PORTE	PE0 to PE3	PE0 to PE7
	PORTG	—	PG7
	PORTJ	PJ3	—
5 V tolerance	PORT1	P16, P17	P12, P13, P16, P17
Drive capacity switching	PORT0	P03 to P07	—
	PORT1	P12 to P17	—
	PORT2	P20 to P27	—
	PORT3	P30 to P34, P36, P37	—
	PORT4	P40 to P47	—
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	—
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD7	—
	PORTE	PE0 to PE7	—
	PORTH	PH0 to PH3	—
	PORTJ	PJ1, PJ3, PJ6, PJ7	—

Table 2.31 Comparison of I/O Port Registers

Register	Bit	RX130	RX261
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B6	Pm0 to Pm6 pin mode control bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm6 pin mode control bits (m = 0 to 5, A to E, G, H, J)
	B7	Pm7 pin mode control bit (m = 0 to 5, A to E, H, J) b7 0: Use pin as general I/O port (initial value). 1: Use pin as I/O port for peripheral functions.	Pm7 pin mode control bit (m = 0 to 5, A to E, G, H, J) PG7 b7 0: Use pin as general I/O port. 1: Use pin as the MD function (initial value). Others b7 0: Use pin as general I/O port (initial value). 1: Use pin as I/O port for peripheral functions.
ODR0	B2, B3	Pm1 output type select bits (m =1 to 3, A to E, J) • P21, P31, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N channel open drain b3 This bit is read as 0. The write value must be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N channel open drain 1 0: P channel open drain 1 1: Hi-Z	Pm1 output type select bits (m = 1 to 3, 5, A to E, J) • P21, P31, P51, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N channel open drain b3 This bit is read as 0. The write value must be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N channel open drain 1 0: P channel open drain 1 1: Prohibited
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, A to C)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 5, A to C, E, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
DSCR	—	Drive capacity control register (m =1 to 3, 5, A to E, H, J)	—
PRWCNTR	—	—	Port reading wait control register

2.15 Multi-Function Pin Controller

Table 2.32 shows a Comparison of Multiplexed Pin Assignments, and Table 2.33 to Table 2.43 show comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **orange text** indicates pins that are present in the RX130 Group only, and **blue text** indicates pins that are present in the RX261 Group only. A circle (○) indicates that a function is assigned to the pin, a cross (×) indicates that the pin is not present or that no function is assigned, and grayed out items indicate functions that are not implemented.

Table 2.32 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupts	NMI (input)	P35	○	○	○	○	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○	○	○	○	○
		PD0	○	○	×	×	○	○	×	×
		PH1*7	○	○	○	○	○	○	○	○
	IRQ1 (input)	P31	○	○	○	○	○	○	○	○
		PD1	○	○	×	×	○	○	×	×
		PH2*7	○	○	○	○	○	○	○	○
	IRQ2 (input)	P32	○	○	○	×	○	○	○	×
		P12	○	○	×	×	○	○	×	×
		PD2	○	○	×	×	○	○	×	×
		P36	×	×	×	×	○	○	○	○
	IRQ3 (input)	P13	○	○	×	×	○	○	×	×
		P33	○	×	×	×	○	×	×	×
		PD3	○	×	×	×	○	×	×	×
	IRQ4 (input)	PB1	○	○	○	○	○	○	○	○
		P14	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		PD4	○	×	×	×	○	×	×	×
		P37	×	×	×	×	○	○	○	○
	IRQ5 (input)	PA4	○	○	○	○	○	○	○	○
		P15	○	○	○	○	○	○	○	○
		PD5	○	×	×	×	○	×	×	×
		PE5	○	○	○	×	○	○	○	×
	IRQ6 (input)	PA3	○	○	○	○	○	○	○	○
		P16	○	○	○	○	○	○	○	○
		PD6	○	×	×	×	○	×	×	×
		PE6	○	×	×	×	○	×	×	×
	IRQ7 (input)	PE2	○	○	○	○	○	○	○	○
		P17	○	○	○	○	○	○	○	○
		PD7	○	×	×	×	○	×	×	×
		PE7	○	×	×	×	○	×	×	×
Clock generation circuit	CLKOUT (output)	PE3	○	○	○	○	○	○	○	○
		PE4	○	○	○	○	○	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	○	×	×				
		PB3	○	○	○	○				
	MTIOC0B (input/output)	P13	○	○	×	×				
		P15	○	○	○	○				
		PA1	○	○	○	○				

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC0C (input/output)	P32	○	○	○	×				
		PB1	○	○	○	○				
	MTIOC0D (input/output)	P33	○	×	×	×				
		PA3	○	○	○	○				
	MTIOC1A (input/output)	P20	○	○	×	×				
		PE4	○	○	○	○				
	MTIOC1B (input/output)	P21	○	○	×	×				
		PB5	○	○	○	○				
	MTIOC2A (input/output)	P26	○	○	○	○				
		PB5	○	○	○	○				
	MTIOC2B (input/output)	P27	○	○	○	○				
		PE5	○	○	○	×				
	MTIOC3A (input/output)	P14	○	○	○	○				
		P17	○	○	○	○				
		PC1	○	×	×	×				
		PC7	○	○	○	○				
		PJ1	○	○	×	×				
	MTIOC3B (input/output)	P17	○	○	○	○				
		P22	○	×	×	×				
		PB7	○	○	○	×				
		PC5	○	○	○	○				
	MTIOC3C (input/output)	P16	○	○	○	○				
		PC0	○	×	×	×				
		PC6	○	○	○	○				
		PJ3	○	×	×	×				
	MTIOC3D (input/output)	P16	○	○	○	○				
		P23	○	×	×	×				
		PB6	○	○	○	×				
		PC4	○	○	○	○				
	MTIOC4A (input/output)	P24	○	×	×	×				
		PA0	○	○	○	×				
		PB3	○	○	○	○				
		PE2	○	○	○	○				
	MTIOC4B (input/output)	P30	○	○	○	○				
		P54	○	○	○	×				
		PC2	○	○	○	×				
		PD1	○	○	×	×				
		PE3	○	○	○	○				
	MTIOC4C (input/output)	P25	○	×	×	×				
		PB1	○	○	○	○				
		PE1	○	○	○	○				
		PE5	○	○	○	×				
	MTIOC4D (input/output)	P31	○	○	○	○				
		P55	○	○	○	×				
		PC3	○	○	○	×				
		PD2	○	○	×	×				
		PE4	○	○	○	○				
	MTIC5U (input)	PA4	○	○	○	○				
		PD7	○	×	×	×				

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIC5V (input)	PA6	○	○	○	○				
		PD6	○	×	×	×				
	MTIC5W (input)	PB0	○	○	○	○				
		PD5	○	×	×	×				
	MTCLKA (input)	P14	○	○	○	○				
		P24	○	×	×	×				
		PA4	○	○	○	○				
		PC6	○	○	○	○				
	MTCLKB (input)	P15	○	○	○	○				
		P25	○	×	×	×				
		PA6	○	○	○	○				
		PC7	○	○	○	○				
	MTCLKC (input)	P22	○	×	×	×				
		PA1	○	○	○	○				
		PC4	○	○	○	○				
	MTCLKD (input)	P23	○	×	×	×				
		PA3	○	○	○	○				
		PC5	○	○	○	○				
Port output enable 2	POE0# (input)	PC4	○	○	○	○				
		PD7	○	×	×	×				
	POE1# (input)	PB5	○	○	○	○				
		PD6	○	×	×	×				
	POE2# (input)	P34	○	○	×	×				
		PA6	○	○	○	○				
		PD5	○	×	×	×				
	POE3# (input)	P33	○	×	×	×				
		PB3	○	○	○	○				
		PD4	○	×	×	×				
	POE8# (input)	P17	○	○	○	○				
		P30	○	○	○	○				
		PD3	○	×	×	×				
		PE3	○	○	○	○				
8-bit timer	TMO0 (output)	P22	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
		PH1*7	○	○	○	○	○	○	○	○
	TMCI0 (input)	P21	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
		PH3	○	○	○	○	○	○	○	○
	TMRI0 (input)	P20	○	○	×	×	○	○	×	×
		PA4	○	○	○	○	○	○	○	○
		PH2*7	○	○	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	TMCI1 (input)	P12	○	○	×	×	○	○	×	×
		P54	○	○	○	×	○	○	○	×
		PC4	○	○	○	○	○	○	○	○
	TMRI1 (input)	P24	○	×	×	×	○	×	×	×
		PB5	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMO2 (output)	P16	○	○	○	○	○	○	○	○
		PC7	○	○	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	×	×	○	○	×	×
		P32	○	○	○	×	○	○	○	×
		P55	○	○	○	×	○	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		PA6	○	○	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○	○	○
		P33	○	×	×	×	○	×	×	×
Serial communications interface	RXD0 (input) / SMISO0 (input/output) / SSCL0 (input/output)	P21	○	×	×	×				
	TXD0 (output) / SMOSI0 (input/output) / SSDA0 (input/output)	P20	○	×	×	×				
	SCK0 (input/output)	P22	○	×	×	×				
	CTS0# (input) / RTS0# (output) / SS0# (input)	P23	○	×	×	×				
	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○	○	○
		P27	○	○	○	○	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	○	○
		PC2	○	○	○	×	○	○	○	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC3	○	○	○	×	○	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
		PC4	○	○	○	○	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○	○	○	○	○
		PC0	○	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	P33	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PD1	○	○	×	×	○	○	×	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	PB1	○	○	○	○	○	○	○	○
		PD0	○	○	×	×	○	○	×	×
		P32	○	○	○	×	○	○	○	×
	SCK6 (input/output)	P34	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	○	○
		PD2	○	○	×	×	○	○	×	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	○	×	×	○	○	×	×
		PJ3	○	×	×	×	○	×	×	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○	×	×	×				
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○	×	×	×				
	SCK8 (input/output) /	PC5	○	×	×	×				
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○	×	×	×				
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○	×	×	×				
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○	×	×	×				
	SCK9 (input/output)	PB5	○	×	×	×				
	CTS9# (input) / RTS9# (output) / SS9# (input) (RX130)/	PB4	○	×	×	×				
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○	○*3	○	○	○	○*3
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○	○*4	○	○	○	○*4
	SCK12 (input/output)	PE0	○	○	○	×	○	○	○	×
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○	○*5	○	○	○	○*5
	RXD000 (input) / SMISO000 (input/output) / SSCL000 (input/output)	P21					○	×	×	○
	TXD000 (output) / TXDA000 (output) / SMOSI000 (input/output) / SSDA000 (input/output)	P20					○	○*6	×	×

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK000 (input/output)	P22					○	×	×	×
	CTS000# (input) / RTS000# (output) / SS000# (input)	P23					○	×	×	×
	RXD008 (input) / SMISO008 (input/output) / SSCL008 (input/output)	PC6					○	○	○	○
	TXD008 (output) / TXDA008 (output) / SMOSI008 (input/output) / SSDA008 (input/output)	PC7					○	○	○	○
	SCK008 (input/output)	PC5					○	○	○	○
	CTS008# (input) / RTS008# (output) / SS008# (input)	PC4					○	○	○	○
	RXD009 (input) / SMISO009 (input/output) / SSCL009 (input/output)						○	○	○	×
	TXD009 (output) / TXDA009 (output) / SMOSI009 (input/output) / SSDA009 (input/output)	PB6					○	○	○	×
	SCK009 (input/output)	PB7					○	○	○	×
	CTS009# (input) / RTS009# (output) / SS009# (input)	PB5					○	○	×	×
	TXDB000 (output)	P22					○	×	×	×
	DE000 (output)	P23					○	×	×	×
	TXDB008 (output)	PC5					○	○	○	○
	DE008 (output)	PC4					○	○	○	○
	TXDB009 (output)	PB5					○	○	○	×
	DE009 (output)	PB4					○	○	×	×
I^2C bus interface	SCL (input/output) (RX130)/ SCL0 (input/output) (RX261)	P16	○	○	○	○	○	○	○	○
		P12	○	○	×	×	○	○	×	×
	SDA (input/output) (RX130)/ SCL0 (input/output) (RX261)	P17	○	○	○	○	○	○	○	○
		P13	○	○	×	×	○	○	×	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○	○	○
		PA6	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○	○	○
		PA7	○	×	×	×	○	×	×	×
		PC7	○	○	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	×	○	○	○	×
		PC0	○	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	SSLA2 (output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
	SSLA3 (output)	PA2	○	○	×	×	○	○	×	×
		PC2	○	○	○	×	○	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	○	×	○	○	○	×
		P32	○	○	○	×	○	○	○	×
	RTCIC0 (input)*1	P30					○	○	○	×
	RTCIC1 (input)*1	P31					○	○	○	×
	RTCIC2 (input)*1	P32					○	○	○	×
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	×	○	○	○	×
	AN004 (input)*1	P44	○	○	○	×	○	○	○	×
	AN005 (input)*1	P45	○	○	○	○	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	○	○	○	○	○	○
	AN016 (input)*1	PE0	○	○	○	×	○	○	○	×
	AN017 (input)*1	PE1	○	○	○	○	○	○	○	○
	AN018 (input)*1	PE2	○	○	○	○	○	○	○	○
	AN019 (input)*1	PE3	○	○	○	○	○	○	○	○
	AN020 (input)*1	PE4	○	○	○	○	○	○	○	○
	AN021 (input)*1	PE5	○	○	○	×	○	○	○	×
	AN022 (input)*1	PE6	○	×	×	×	○	×	×	×
	AN023 (input)*1	PE7	○	×	×	×	○	×	×	×
	AN024 (input)*1	PD0	○	○	×	×	○	○	×	×
	AN025 (input)*1	PD1	○	○	×	×	○	○	×	×
	AN026 (input)*1	PD2	○	○	×	×	○	○	×	×
	AN027 (input)*1	PD3	○	×	×	×	○	×	×	×
	AN028 (input)*1	PD4	○	×	×	×	○	×	×	×
	AN029 (input)*1	PD5	○	×	×	×	○	×	×	×
	AN030 (input)*1	PD6	○	×	×	×	○	×	×	×
	AN031 (input)*1	PD7	○	×	×	×	○	×	×	×
	ADTRG0# (input)	P07	○	○	×	×	○	○	×	×
		P16	○	○	○	○	○	○	○	○
		P25	○	×	×	×	○	×	×	×
D/A converter	DA0 (output)*1	P03	○	○	○	×	○	○	○	×
	DA1 (output)*1	P05	○	○	○	×	○	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	×	○	○	○	×
		PC7	○	○	○	○	○	○	○	○
		PH0	○	○	○	○	○	○	○	○
LVD voltage detection input	CMPA2 (input)*1	PE4	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Comparator B	CMPB0 (input)*1	PE1	○	○	○	○	○	○	○	○
	CVREFB0 (input)*1	PE2	○	○	○	○	○	○	○	○
	CMPOB0 (output)	PE5	○	○	○	×	○	○	○	×
	CMPB1 (input)*1	PA3	○	○	○	○	○	○	○	○
	CVREFB1 (input)*1	PA4	○	○	○	○	○	○	○	○
	CMPOB1 (output)	PB1	○	○	○	○	○	○	○	○
Capacitive touch sensing unit (CTSU)	TSCAP (—)	PC4	○	○	○	○	○	○	○	○
	TS0 (input/output)	P32	○	○	○	×	○	○	○	×
	TS1 (input/output)	P31	○	○	○	○	○	○	○	○
	TS2 (output) (input/output)*8	P30	○	○	○	○	○	○	○	○
	TS3 (output) (input/output)*8	P27	○	○	○	○	○	○	○	○
	TS4 (output) (input/output)*8	P26	○	○	○	○	○	○	○	○
	TS5 (output) (input/output)*8	P15	○	○	○	○	○	○	○	○
	TS6 (output) (input/output)*8	P14	○	○	○	○	○	○	○	○
	TS7 (output) (input/output)*8	PH3	○	○	○	○	○	○	○	○
	TS8 (output) (input/output)*8	PH2*7	○	○	○	○	○	○	○	○
	TS9 (output) (input/output)*8	PH1*7	○	○	○	○	○	○	○	○
	TS10 (output) (input/output)*8	PH0	○	○	○	○	○	○	○	○
	TS11 (output) (input/output)*8	P55	○	○	○	×	○	○	○	×
	TS12 (output) (input/output)*8	P54	○	○	○	×	○	○	○	×
	TS13 (output) (input/output)*8	PC7	○	○	○	○	○	○	○	○
	TS14 (output) (input/output)*8	PC6	○	○	○	○	○	○	○	○
	TS15 (output) (input/output)*8	PC5	○	○	○	○	○	○	○	○
	TS16 (output) (input/output)*8	PC3	○	○	○	×	○	○	○	×
	TS17 (output) (input/output)*8	PC2	○	○	○	×	○	○	○	×
	TS18 (output) (input/output)*8	PB7	○	○	○	×	○	○	○	×
	TS19 (output) (input/output)*8	PB6	○	○	○	×	○	○	○	×
	TS20 (output) (input/output)*8	PB5	○	○	○	○	○	○	○	○
	TS21 (output) (input/output)*8	PB4	○	○	×	×	○	○	×	×
	TS22 (output) (input/output)*8	PB3	○	○	○	○	○	○	○	○
	TS23 (output) (input/output)*8	PB2	○	○	×	×	○	○	×	×
	TS24 (output) (input/output)*8	PB1	○	○	○	○	○	○	○	○
	TS25 (output) (input/output)*8	PB0	○	○	○	○	○	○	○	○
	TS26 (output) (input/output)*8	PA6	○	○	○	○	○	○	○	○
	TS27 (output) (input/output)*8	PA5	○	○	×	×	○	○	×	×
	TS28 (output) (input/output)*8	PA4	○	○	○	○	○	○	○	○
	TS29 (output) (input/output)*8	PA3	○	○	○	○	○	○	○	○
	TS30 (output) (input/output)*8	PA2	○	○	×	×	○	○	×	×
	TS31 (output) (input/output)*8	PA1	○	○	○	○	○	○	○	○
	TS32 (output) (input/output)*8	PA0	○	○	○	×	○	○	○	×
	TS33 (output) (input/output)*8	PE4	○	○	○	○	○	○	○	○
	TS34 (output) (input/output)*8	PE3	○	○	○	○	○	○	○	○
	TS35 (output) (input/output)*8	PE2	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Remote control signal receiver	PMC0	P51	○	×	×	×	○	×	×	×
		P53					○	×	×	×
		PB3					○	○	○	○
		PC3					○	○	○	×
		PC4					○	○	○	○
		PC5					○	○	○	○
	PMC1	P52	○	×	×	×				
General-purpose PWM timer	GTIOC0A (input/output) / GTIOC0A# (input/output)	P17					○	○	○	○
		P22					○	×	×	×
		PA0					○	○	○	×
		PA1					○	○	○	○
		PB7					○	○	○	×
		PC5					○	○	○	○
		PH0					○	○	○	○
	GTIOC0B (input/output) / GTIOC0B# (input/output)	P16					○	○	○	○
		P17					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PA6					○	○	○	○
		PB0					○	○	○	○
		PB6					○	○	○	×
		PC4					○	○	○	○
		PH1*7					○	○	○	○
	GTIOC1A (input/output) / GTIOC1A# (input/output)	P24					○	×	×	×
		P32					○	○	○	×
		P55					○	○	○	×
		PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTIOC1B (input/output) / GTIOC1B# (input/output)	P25					○	×	×	×
		P33					○	×	×	×
		PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
		PE5					○	○	○	×
		PH2*7					○	○	○	○
	GTIOC2A (input/output) / GTIOC2A# (input/output)	P21					○	○	×	×
		P30					○	○	○	○
		P54					○	○	○	×
		PB0					○	○	○	○
		PC2					○	○	○	×
		PD1					○	○	×	×
		PE3					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC2B (input/output) / GTIOC2B# (input/output)	P20					○	○	×	×
		P31					○	○	○	○
		P55					○	○	○	×
		PA3					○	○	○	○
		PB1					○	○	○	○
		PC3					○	○	○	×
		PD2					○	○	×	×
		PE4					○	○	○	○
		PH3					○	○	○	○
	GTIOC3A (input/output) / GTIOC3A# (input/output)	P22					○	×	×	×
		P34					○	○	×	×
	GTIOC3A (input/output) / GTIOC3A# (input/output)	PB2					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIOC3B (input/output) / GTIOC3B# (input/output)	P13					○	○	×	×
		P15					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PB3					○	○	○	○
	GTIOC4A (input/output) / GTIOC4A# (input/output)	P20					○	○	×	×
		PA4					○	○	○	○
		PE4					○	○	○	○
	GTIOC4B (input/output) / GTIOC4B# (input/output)	P16					○	○	○	○
		P21					○	○	×	×
		PA5					○	○	×	×
		PB5					○	○	○	○
		PE3					○	○	○	○
	GTIOC5A (input/output) / GTIOC5A# (input/output)	P26					○	○	○	○
		PA6					○	○	○	○
		PB5					○	○	○	○
	GTIOC5B (input/output) / GTIOC5B# (input/output)	P15					○	○	○	○
		P27					○	○	○	○
		PA7					○	×	×	×
		PE5					○	○	○	×
	GTIOC6A (input/output) / GTIOC6A# (input/output)	P14					○	○	○	○
		P17					○	○	○	○
		P25					○	×	×	×
		PB4					○	○	×	×
		PC1					○	×	×	×
		PC7					○	○	○	○
	GTIOC6A (input/output) / GTIOC6A# (input/output)	PJ1					○	○	×	×
	GTIOC6B (input/output) / GTIOC6B# (input/output)	P16					○	○	○	○
		P24					○	×	×	×
		PB5					○	○	○	○
		PC0					○	×	×	×
		PC6					○	○	○	○
		PJ3					○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC7A (input/output) / GTIOC7A# (input/output)	P13					○	○	×	×
		P32					○	○	○	×
		PB1					○	○	○	○
		PB6					○	○	○	×
		PC5					○	○	○	○
	GTIOC7B (input/output) / GTIOC7B# (input/output)	P14					○	○	○	○
		P33					○	×	×	×
		PA3					○	○	○	○
		PB7					○	○	○	×
	GTETRGA (input)	P14					○	○	○	○
		P24					○	×	×	×
		PA4					○	○	○	○
		PC2					○	○	○	×
		PC6					○	○	○	○
	GTETRGB (input)	P15					○	○	○	○
		P25					○	×	×	×
		PA3					○	○	○	○
		PA6					○	○	○	○
		PC3					○	○	○	×
	GTETRGB (input)	PC7					○	○	○	○
	GTETRGC (input)	P16					○	○	○	○
		P22					○	×	×	×
		PA1					○	○	○	○
		PB2					○	○	×	×
		PC0					○	×	×	×
		PC4					○	○	○	○
	GTETRGD (input)	P17					○	○	○	○
		P23					○	×	×	×
		PA3					○	○	○	○
		PB3					○	○	○	○
		PC1					○	×	×	×
		PC5					○	○	○	○
	GTCPPO0 (output)	P14					○	○	○	○
		P17					○	○	○	○
		PC1					○	×	×	×
		PC7					○	○	○	○
		PJ1					○	○	×	×
	GTIU (input)	P34					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIV (input)	P13					○	○	×	×
		P15					○	○	○	○
		PA1					○	○	○	○
	GTIW (input)	P32					○	○	○	×
		PB1					○	○	○	○
		PC5					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTOULO (output)	P16					○	○	○	○
		PA6					○	○	○	○
		PC4					○	○	○	○
		PH1*7					○	○	○	○
	GTOUUP (output)	P17					○	○	○	○
		PA1					○	○	○	○
		PC5					○	○	○	○
		PH0					○	○	○	○
	GTOVLO (output)	PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
	GTOVUP (output)	PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTOWLO (output)	P31					○	○	○	○
		PA3					○	○	○	○
		PB1					○	○	○	○
		PE4					○	○	○	○
	GTOWUP (output)	P30					○	○	○	○
		PB0					○	○	○	○
		PC2					○	○	○	×
	GTOWUP (output)	PE3					○	○	○	○
Low-power timer	LPTO (output)	P26					○	○	○	○
		PB3					○	○	○	○
		PC7					○	○	○	○
CANFD module	CTX0 (output)	P14					○	○	○	○
		P32					○	○	○	×
		P54					○	○	○	×
		PD1					○	○	×	×
	CRX0 (input)	P15					○	○	○	○
		P33					○	×	×	×
		P55					○	○	○	×
		PD2					○	○	×	×
USB 2.0 FS host/function module	USB0_DP (input/output)	PH1*2,*7					○	○	○	○
	USB0_DM (input/output)	PH2*2,*7					○	○	○	○
	USB0_VBUS (input)	P16					○	○	○	○
		PB5					○	○	○	○
	USB0_EXICEN (output)	P21					○	○	×	×
		PC6					○	○	○	○
	USB0_VBUSEN (output)	P16					○	○	○	○
		P24					○	×	×	×
		P26					○	○	○	○
		P32					○	○	○	×
	USB0_OVRCURA (input)	P14					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC)				RX261 (MPC)			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
USB 2.0 FS host/function module	USB0_OVRCURB (input)	P16					○	○	○	○
		P22					○	×	×	×
	USB0_ID (input)	P20					○	○	×	×
		PC5					○	○	○	○

Notes: 1. To use this pin function, select general input by setting the PORT.PDR.Bm bit and PORT.PMR.Bm bit for the applicable pin to 0.
2. Pins PH1 and PH2 for RX260 Group products. Pins USB0_DP and USB0_DM for RX261 Group products.
3. SMISO12 function is not available.
4. SMOSI12 function is not available.
5. SS12# function is not available.
6. TXDA000 function is not available.
7. RX261 Group products are not equipped with ports PH1 and PH2.
8. Output pin for RX130 Group products and input/output pin for RX261 Group products.

Table 2.33 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX130 (n = 2 to 7)	RX261 (n = 2 to 7)
P12PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 01111b: SCL	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 01111b: SCL0
P13PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00101b: TMO3 01111b: SDA	Pin function select bits 00000b: Hi-Z 00011b: GTIV 00101b: TMO3 01111b: SDA0 10100b: GTIOC3B 10101b: GTIOC7A 10110b: GTIOC3B# 10111b: GTIOC7A#
P14PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: TMRI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS6	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTX0 10001b: USB0_OVRCURA 10100b: GTIOC6A 10101b: GTIOC7B 10110b: GTIOC6A# 10111b: GTIOC7B# 11000b: GTETRGA 11001b: TS6
P15PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 11001b: TS5	Pin function select bits 00000b: Hi-Z 00011b: GTIV 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRX0 10100b: GTIOC3B 10101b: GTIOC5B 10110b: GTIOC3B# 10111b: GTIOC5B# 11000b: GTETRGB 11001b: TS5

Register	Bit	RX130 (n = 2 to 7)	RX261 (n = 2 to 7)
P16PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6B# 00010b: GTETRGC 00011b: GTOULO 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL0 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB 10100b: GTIOC0B 10101b: GTIOC4B 10110b: GTIOC0B# 10111b: GTIOC4B# 11000b: GTIOC6B
P17PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6A# 00010b: GTETRGD 00011b: GTCPPO0 00100b: GTOUUP 00101b: TMO1 01010b: SCK1 01101b: MISOA 01111b: SDA0 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC6A

Table 2.34 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
P20PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00101b: TMRI0 01010b: TXD0/SMOSI0/SSDA0	Pin function select bits 00000b: Hi-Z 00001b: TMRI0 01010b: TXD000/TXDA000/ SMOSI000/SSDA000 10001b: USB0_ID 10100b: GTIOC2B 10101b: GTIOC4A 10110b: GTIOC2B# 10111b: GTIOC4A#
P21PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00101b: TMCI0 01010b: RXD0/SMISO0/SSCL0	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 01010b: RXD000/SMISO000/ SSCL000 10001b: USB0_EXICEN 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B#
P22PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00101b: TMO0 01010b: SCK0	Pin function select bits 00000b: Hi-Z 00101b: TMO0 01010b: SCK000 01100b: TXDB000 10001b: USB0_OVRCURB 10100b: GTIOC0A 10101b: GTIOC3A 10110b: GTIOC0A# 10111b: GTIOC3A# 11000b: GTETRGC
P23PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKD 01011b: CTS0#/RTS0#/SS0#	Pin function select bits 00000b: Hi-Z 01011b: CTS000#/RTS000#/ SS000# 01100b: DE000 10100b: GTIOC0B 10101b: GTIOC3B 10110b: GTIOC0B# 10111b: GTIOC3B# 11000b: GTETRGD

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
P24PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00010b: MTCLKA 00101b: TMRI1	Pin function select bits 00000b: Hi-Z 00101b: TMRI1 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC6B 10110b: GTIOC1A# 10111b: GTIOC6B# 11000b: GTETRGA
P25PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTCLKB 01001b: ADTRG0#	Pin function select bits 00000b: Hi-Z 01001b: ADTRG0# 10100b: GTIOC1B 10101b: GTIOC6A 10110b: GTIOC1B# 10111b: GTIOC6A# 11000b: GTETRGB
P26PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 11001b: TS4	Pin function select bits 00000b: Hi-Z 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10001b: USB0_VBUSEN 10100b: GTIOC5A 10110b: GTIOC5A# 11001b: TS4 11011b: LPTO
P27PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 01010b: SCK1 11001b: TS3	Pin function select bits 00000b: Hi-Z 00101b: TMCI3 01010b: SCK1 10100b: GTIOC5B 10110b: GTIOC5B# 11001b: TS3

Table 2.35 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX130 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P30PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 11001b: TS2	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 00101b: TMRI3 01010b: RXD1/SMISO1/SSCL1 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS2
P31PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS1	Pin function select bits 00000b: Hi-Z 00011b: GTOWLO 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS1
P32PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 11001b: TS0	Pin function select bits 00000b: Hi-Z 00011b: GTIW 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 10000b: CTX0 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC7A 10110b: GTIOC1A# 10111b: GTIOC7A# 11001b: TS0
P33PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00101b: TMRI3 00111b: POE3# 01011b: RXD6/SMISO6/SSCL6	Pin function select bits 00000b: Hi-Z 00101b: TMRI3 01011b: RXD6/SMISO6/SSCL6 10000b: CRX0 10100b: GTIOC1B 10101b: GTIOC7B 10110b: GTIOC1B# 10111b: GTIOC7B#

Register	Bit	RX130 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P34PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI3 00111b: POE2# 01011b: SCK6	Pin function select bits 00000b: Hi-Z 00001b: GTIU 00101b: TMCI3 01011b: SCK6 10100b: GTIOC3A 10110b: GTIOC3A#
P36PFS	PSEL[4:0]	—	Pin function select bits
P37PFS	PSEL[4:0]	—	Pin function select bits
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/64-pin) P31: IRQ1 (100/64-pin) P32: IRQ2 (100/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/80/64/48-pin) P31: IRQ1 (100/80/64/48-pin) P32: IRQ2 (100/80/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin) P36: IRQ2 (80/64/48-pin) P37: IRQ4 (80/64/48-pin)

Table 2.36 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX130 (n = 1, 2, 4, 5)	RX261 (n = 1, 3 to 5)
P52PFS	PSEL[4:0]	Pin function select bits	—
P53PFS	PSEL[4:0]	—	Pin function select bits
P54PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 11001b: TS12	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS12
P55PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 11001b: TS11	Pin function select bits 00000b: Hi-Z 00101b: TMO3 10000b: CRX0 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11001b: TS11

Table 2.37 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PA0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00111b: CACREF 01101b: SSLA1 11001b: TS32	Pin function select bits 00000b: Hi-Z 00010b: GTOVUP 00111b: CACREF 01101b: SSLA1 10100b: GTIOC0A 10101b: GTIOC1A 10110b: GTIOC0A# 10111b: GTIOC1A# 11001b: TS32
PA1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 01010b: SCK5 01101b: SSLA2 11001b: TS31	Pin function select bits 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGC 00011b: GTIV 00100b: GTOUUP 01010b: SCK5 01101b: SSLA2 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC3B 11001b: TS31
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 01010b: RXD5/SMISO5/SSCL5 11001b: TS29	Pin function select bits 00000b: Hi-Z 00001b: GTIOC7B# 00010b: GTETRGB 00011b: GTETRGD 00100b: GTOVLO 01000b: GTOWLO 01010b: RXD5/SMISO5/SSCL5 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7B 11001b: TS29

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PA4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28	Pin function select bits 00000b: Hi-Z 00010b: GTOVLO 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10100b: GTIOC1B 10101b: GTIOC4A 10110b: GTIOC1B# 10111b: GTIOC4A# 11000b: GTETRGA 11001b: TS28
PA5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01101b: RSPCKA 11001b: TS27	Pin function select bits 00000b: Hi-Z 01101b: RSPCKA 10100b: GTIOC4B 10110b: GTIOC4B# 11001b: TS27
PA6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26	Pin function select bits 00000b: Hi-Z 00011b: GTOULO 00101b: TMCI3 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10100b: GTIOC0B 10101b: GTIOC5A 10110b: GTIOC0B# 10111b: GTIOC5A# 11000b: GTETRGB 11001b: TS26
PA7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01101b: MISOA 	Pin function select bits 00000b: Hi-Z 01101b: MISOA 10100b: GTIOC5B 10110b: GTIOC5B#

Table 2.38 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 10100b: GTIOC0B 10101b: GTIOC2A 10110b: GTIOC0B# 10111b: GTIOC2A# 11001b: TS25
PB1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11001b: TS24	Pin function select bits 00000b: Hi-Z 00001b: GTIOC7A# 00010b: GTOVLO 00011b: GTIW 00100b: GTOWLO 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B 11000b: GTIOC7A 11001b: TS24
PB2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 11001b: TS23	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC7A 10110b: GTIOC7A# 11000b: GTETRGC 11001b: TS23

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22	Pin function select bits 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGD 00011b: GTIU 00100b: GTOVUP 00101b: TMO0 01011b: SCK6 10100b: GTIOC1A 10101b: GTIOC3A 10110b: GTIOC1A# 10111b: GTIOC3A# 11000b: GTIOC3B 11001b: TS22 11011b: LPTO 11100b: PMC0
PB4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01011b: CTS9#/RTS9#/SS9# 11001b: TS21	Pin function select bits 00000b: Hi-Z 01011b: CTS009#/RTS009#/ SS009# 01100b: DE009 10100b: GTIOC6A 11100b: GTIOC6A# 11001b: TS21
PB5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01010b: SCK9 11001b: TS20	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6B# 00101b: TMRI1 01010b: SCK009 01100b: TXDB009 10001b: USB0_VBUS 10100b: GTIOC4B 10101b: GTIOC5A 10110b: GTIOC4B# 10111b: GTIOC5A# 11000b: GTIOC6B 11001b: TS20
PB6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 01010b: RXD9/SMISO9/SSCL9 11001b: TS19	Pin function select bits 00000b: Hi-Z 01010b: RXD009/SMISO009/ SSCL009 10100b: GTIOC0B 10101b: GTIOC7A 10110b: GTIOC0B# 10111b: GTIOC7A# 11001b: TS19

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PB7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 11100b: TS18	Pin function select bits 00000b: Hi-Z 01010b: TXD009/TXDA009/ SMOSI009/SSDA009 10100b: GTIOC0A 10101b: GTIOC7B 10110b: GTIOC0A# 10111b: GTIOC7B# 11100b: TS18

Table 2.39 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PC0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1	Pin function select bits 00000b: Hi-Z 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGC
PC1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 01010b: SCK5 01101b: SSLA2	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 01010b: SCK5 01101b: SSLA2 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGD
PC2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS17	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10100b: GTIOC2A 10110b: GTIOC2A# 11000b: GTETRGA 11001b: TS17
PC3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01010b: TXD5/SMOSI5/SSDA5 11001b: TS16	Pin function select bits 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5 10100b: GTIOC2B 10110b: GTIOC2B# 11000b: GTETRGB 11001b: TS16 11100b: PMC0

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PC4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP	Pin function select bits 00000b: Hi-Z 00001b: GTIU 00100b: GTOULO 00101b: TMCI1 01010b: SCK5 01011b: CTS008#/RTS008#/ SS008# 01100b: DE008 01101b: SSLA0 10100b: GTIOC0B 10101b: GTIOC3A 10110b: GTIOC0B# 10111b: GTIOC3A# 11000b: GTETRGC 11001b: TSCAP 11100b: PMC0
PC5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15	Pin function select bits 00000b: Hi-Z 00010b: GTOUUP 00011b: GTIW 00101b: TMRI2 01010b: SCK008 01100b: TXDB008 01101b: RSPCKA 10001b: USB0_ID 10100b: GTIOC0A 10101b: GTIOC7A 10110b: GTIOC0A# 10111b: GTIOC7A# 11000b: GTETRGD 11001b: TS15 11100b: PMC0
PC6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI12 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS14	Pin function select bits 00000b: Hi-Z 00101b: TMCI2 01010b: RXD008/SMISO008/ SSCL008 01101b: MOSIA 10001b: USB0_EXICEN 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGA 11001b: TS14

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PC7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMO2 00111b: CACREF 01010b: TXD008/TXDA008/ SMOSI008/SSDA008 01101b: MISOA 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGB 11001b: TS13 11011b: LPTO

Table 2.40 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PD1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01011b: RXD6/SMISO6/SSCL6	Pin function select bits 00000b: Hi-Z 01011b: RXD6/SMISO6/SSCL6 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A#
PD2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01011b: SCK6	Pin function select bits 00000b: Hi-Z 01011b: SCK6 10000b: CRX0 10100b: GTIOC2B 10110b: GTIOC2B#
PD3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE8#	Pin function select bits 00000b: Hi-Z
PD4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE3#	Pin function select bits 00000b: Hi-Z
PD5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00111b: POE2#	Pin function select bits 00000b: Hi-Z
PD6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: POE1#	Pin function select bits 00000b: Hi-Z

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PD7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00111b: POE0#	Pin function select bits 00000b: Hi-Z

Table 2.41 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PE1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 01100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12	Pin function select bits 00000b: Hi-Z 00010b: GTOVLO 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 10100b: GTIOC1B 10110b: GTIOC1B#
PE2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 01100b: RXD12/RXDX12/ SMISO12/SSCL12 11001b: TS35	Pin function select bits 00000b: Hi-Z 00010b: GTOVUP 01100b: RXD12/RXDX12/ SMISO12/SSCL12 10100b: GTIOC1A 10110b: GTIOC1A# 11001b: TS35
PE3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B# 11001b: TS34
PE4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 01001b: CLKOUT 11001b: TS33	Pin function select bits 00000b: Hi-Z 00001b: GTIOC4A# 00010b: GTOVUP 00011b: GTOWLO 01001b: CLKOUT 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11000b: GTIOC4A 11001b: TS33

Register	Bit	RX130 (n = 0 to 7)	RX261 (n = 0 to 7)
PE5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 10000b: CMPOB0	Pin function select bits 00000b: Hi-Z 10000b: CMPOB0 10100b: GTIOC1B 10101b: GTIOC5B 10110b: GTIOC1B# 10111b: GTIOC5B#

Table 2.42 Comparison of PHn Pin Function Control Registers (PHnPFS)

Register	Bit	RX130 (n = 0 to 3)	RX261 (n = 0 to 3)
PH0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: CACREF 11001b: TS10	Pin function select bits 00000b: Hi-Z 00010b: GTOUUP 00111b: CACREF 10100b: GTIOC0A 10110b: GTIOC0A# 11001b: TS10
PH1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMO0 11001b: TS9	Pin function select bits 00000b: Hi-Z 00011b: GTOULO 00101b: TMO0 10100b: GTIOC0B 10110b: GTIOC0B# 11001b: TS9
PH2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMRI0 11001b: TS8	Pin function select bits 00000b: Hi-Z 00101b: TMRI0 10100b: GTIOC1B 10110b: GTIOC1B# 11001b: TS8
PH3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 11001b: TS7	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS7

Table 2.43 Comparison of PJn Pin Function Control Registers (PJnPFS)

Register	Bit	RX130 (n = 1, 3, 6, 7)	RX261 (n = 1, 3, 6, 7)
PJ1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 10100b: GTIOC6A 10110b: GTIOC6A#
PJ3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 01011b: CTS6#/RTS6#/SS6#	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC6B 10110b: GTIOC6B#

2.16 8-Bit Timer

Table 2.44 shows a Comparative Overview of 8-Bit Timer.

Table 2.44 Comparative Overview of 8-Bit Timer

Item	RX130 (TMR)	RX261 (TMRa)
Count clock	• Frequency dividing clocks: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock	• Internal clocks: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable from compare match A, compare match B, or external counter reset signal.	Selectable from compare match A, compare match B, or external counter reset signal.
Timer output	Output pulses with an arbitrary duty cycle or PWM output	Output pulses with an arbitrary duty cycle or PWM output
Two channel cascading connection	• 16-Bit counter mode 16-bit timer using TMR0 as the upper 8 bits and TMR1 for the lower 8 bits (or TMR2 as the upper 8 bits and TMR3 as the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (and TMR3 can be used to count TMR2 compare matches).	• 16-Bit counter mode 16-bit timer using TMR0 as the upper 8 bits and TMR1 for the lower 8 bits (or TMR2 as the upper 8 bits and TMR3 as the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (and TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	Event reception can trigger one of the following three operations: (1) Count start operation (TMR0, TMR2) (2) Event counter operation (TMR0, TMR2) (3) Count restart operation (TMR0, TMR2)	Event reception can trigger one of the following three operations: (1) Count start operation (TMR0, TMR2) (2) Event counter operation (TMR0, TMR2) (3) Count restart operation (TMR0, TMR2)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
SCI baud rate clock generation (RX130) SCI base clock generation (RX261)	Generates the SCI baud rate clock	Generates the SCI base clock
REMC receive clock generation	Generates the operating clock for REMC (remote control signal receiver)	Generates the operating clock for REMC (remote control signal receiver)
Low power consumption function	Can transition to module stop state at the unit level	Can transition to module stop state at the unit level

2.17 Compare Match Timer

Table 2.45 shows a Comparison of Compare Match Timer Registers.

Table 2.45 Comparison of Compare Match Timer Registers

Item	RX130 (CMT)	RX261 (CMT)
CMSTR1	—	Compare match timer start register 1

2.18 Realtime Clock

Table 2.46 shows a Comparative Overview of Realtime Clock and Table 2.47 shows a Comparison of Realtime Clock Registers.

Table 2.46 Comparative Overview of Realtime Clock

Item	RX130 (RTCc)	RX261 (RTCBa)
Count mode	Calendar count mode/ binary count mode	Calendar count mode/ binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (crystal or external clock) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, day, day-of-week, hour, minute, and second are counted and represented in BCD — 12 hour/24 hour mode switching function — 30-second adjustment function (times less than 30 seconds are rounded down to 00 seconds, and times of 30 seconds or higher are rounded up to one minute) — Automatic adjustment for leap years • Binary count mode Seconds are counted in 32 bits and represented in binary • Common to both modes — Start/stop function — Sub-second digits are represented in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1Hz/64Hz) output	• Calendar count mode — Year, month, day, day-of-week, hour, minute, and second are counted and represented in BCD — 12 hour/24 hour mode switching function — 30-second adjustment function (times less than 30 seconds are rounded down to 00 seconds, and times of 30 seconds or higher are rounded up to one minute) — Automatic adjustment for leap years • Binary count mode Seconds are counted in 32 bits and represented in binary • Common to both modes — Start/stop function — Sub-second digits are represented in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1Hz/64Hz) output
Interrupts	• Alarm interrupt (ALM) Either of the following is selectable as the alarm interrupt condition: — Calendar count mode: Year, month, day, day-of-week, hour, minute, and second — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) Select an interrupt period of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second.	• Alarm interrupt (ALM) Either of the following is selectable as the alarm interrupt condition: — Calendar count mode: Year, month, day, day-of-week, hour, minute, and second — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) Select an interrupt period of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second.

Item	RX130 (RTCc)	RX261 (RTCBa)
Interrupts	• Carry interrupt (CUP) An interrupt is generated at either of the following timing: — When a carry is generated from the 64-Hz counter to the second counter — When a change in the 64-Hz counter coincides with reading from the R64CNT register Recovery from software standby mode can be triggered by an alarm interrupt or periodic interrupt	• Carry interrupt (CUP) An interrupt is generated at either of the following timing: — When a carry is generated from the 64-Hz counter to the second counter — When a change in the 64-Hz counter coincides with reading from the R64CNT register Recovery from software standby mode can be triggered by an alarm interrupt or periodic interrupt
Time capture function	—	• Time capture is implemented by edge detection of the time capture event input pin. At each input event, the system captures the month, day, hour, minute, and second, or a 32-bit binary counter value.
Event link function	—	Periodic event output

Table 2.47 Comparison of Realtime Clock Registers

Register	Bit	RX130 (RTCc)	RX261 (RTCBa)
RCR3	—	RTC control register 3	—
RTCCRn	—	—	Time capture control register n (n = 0 to 2)
RSECCPn BCNT0CPn	—	—	Second capture register n BCNT0 capture register n (n = 0 to 2)
RMINCPn BCNT1CPn	—	—	Minute capture register n BCNT1 capture register n (n = 0 to 2)
RHRCPn BCNT2CPn	—	—	Hour capture register n BCNT2 capture register n (n = 0 to 2)
RDAYCPn BCNT3CPn	—	—	Date capture register n BCNT3 capture register n (n = 0 to 2)
RMONCPn	—	—	Month capture register n (n = 0 to 2)

2.19 Low Power Timer

Table 2.48 shows a Comparative Overview of Low Power Timer and Table 2.49 shows a Comparison of Low Power Timer Registers.

Table 2.48 Comparative Overview of Low Power Timer

Item	RX130 (LPT)	RX261 (LPTa)
Clock source	Sub-clock oscillator IWDT dedicated on-chip oscillator	Sub-clock LOCO clock (divided by 4) Dedicated IWDT clock
Clock division ratios	Divided by 2, 4, 8, 16, or 32	Not divided or divided by 2, 4, 8, 16, or 32
Count operation	• Count up using 16-bit up-counter • Count operation can be continued even in software standby mode	• Count up using 16-bit up-counter • Count operation can be continued even in software standby mode.
Compare match	• Compare match 0 (compare match signals are only generated in software standby mode)	• Compare match 0 (compare match signals are only generated in software standby mode) • Compare match 1
PWM waveform generation	—	PWM waveforms can be output from the LPTO pin
Interrupts	—	Compare match 1
Event link function (output)	• Event signal output by compare match 0 (compare match signals are only generated in software standby mode)	• Compare match 0 (compare match signals are only generated in software standby mode) • Compare match 1

Table 2.49 Comparison of Low Power Timer Registers

Register	Bit	RX130 (LPT)	RX261 (LPTa)
LPTCR1	LPCNTPSSEL [2:0]	Low power timer clock division ratio select bits b2 b0 0 0 1: Clock source divided by 2 0 1 0: Clock source divided by 4 0 1 1: Clock source divided by 8 1 0 0: Clock source divided by 16 1 0 1: Clock source divided by 32 Settings other than the preceding are prohibited.	Clock division ratio select bits b2 b0 0 0 0: No division 0 0 1: Divided by 2 0 1 0: Divided by 4 0 1 1: Divided by 8 1 0 0: Divided by 16 1 0 1: Divided by 32 Settings other than the preceding are prohibited.

Register	Bit	RX130 (LPT)	RX261 (LPTa)
LPTCR1	LPCNTCKSEL (RX130) LPCNTCKSEL, LPCNTCKSEL2 (RX261)	Low power timer clock source select bit 0: Sub-clock oscillator select 1: Dedicated IWDT clock (IWDTCLK)	Low power timer clock source select bit Low power timer clock source select bit 2 LPCNTCKSEL LPCNTCKSEL2 0 0: Sub-clock 0 1: LOCO clock divided by 4 1 0: Dedicated IWDT clock (IWDTCLK) 1 1: LOCO clock divided by 4
	LPCMRE1	—	Compare match 1 enable bit
LPTCR2	OPOL	—	Output polarity select bit
	OLVL	—	Output level select bit
	PWME	—	PWM mode enable bit
LPCMR1	—	—	Low power timer compare register 1

2.20 Independent Watchdog Timer (IWDT)

Table 2.50 shows a Comparative Overview of Independent Watchdog Timer.

Table 2.50 Comparative Overview of Independent Watchdog Timer

Item	RX130 (IWDTa)	RX261 (IWDTa)
Count source	Dedicated IWDT clock (IWDTCLK)	Dedicated IWDT clock (IWDTCLK)
Clock division ratios	Divided by 1, 16, 32, 64, 128, or 256	Divided by 1, 16, 32, 64, 128, or 256
Count operation	Count down using 14-bit down-counter	Count down using 14-bit down-counter
Count start conditions	• Auto start mode: Counting starts automatically after a reset is released • Register start mode: Counting starts when triggered by a refresh operation (writing 00h and then FFh to the IWDTRR register)	• Auto start mode: Counting starts automatically after a reset is released • Register start mode: Counting starts when triggered by a refresh operation (writing 00h and then FFh to the IWDTRR register)
Count stop conditions	• Reset (down-counter and other registers return to their initial values) • Entering low power consumption mode (depends on register setting) • Counting restarts when an underflow or refresh error occurs. (Auto-start mode: Counting automatically restarts after a reset or non-maskable interrupt request is output. Register start mode: Counting is restarted after a refresh.)	• Reset (down-counter and other registers return to their initial values) • Entering low power consumption mode (depends on register setting) • An underflow or refresh error occurs (in register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified. (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflow • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflow • A refresh occurs outside a refresh-permitted period (refresh error)
Non-maskable interrupt/ interrupt sources	• Down-counter underflow • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflow • A refresh occurs outside a refresh-permitted period (refresh error)
Reading counter value	• The value of the down-counter can be read by reading the IWDTSR register.	• The value of the down-counter can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX130 (IWDTa)	RX261 (IWDTa)
Auto start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function when transitioning to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function when transitioning to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (IWDT register control)	• Selecting the clock division ratio after a refresh operation (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function when transitioning to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock division ratio after a refresh operation (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function when transitioning to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

2.21 Serial Communications Interface

Table 2.51 shows a Comparative Overview of Serial Communication Interfaces, Table 2.52 shows a Comparison of SCI Channel Specifications, and Table 2.53 shows a Comparison of Serial Communication Interface Registers.

Table 2.51 Comparative Overview of Serial Communication Interfaces

Item		RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Number of channels		• SCIh: 1 channel • SCIg: 6 channels	• SCIk: 3 channels • SCIh: 1 channel
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator	Bit rate specifiable by on-chip baud rate generator
Full-duplex communication		• Transmitter: Continuous transmission is enabled by a double-buffer configuration • Receiver: Continuous reception is enabled by a double-buffer configuration	• Transmitter: Continuous transmission is enabled by a double-buffer configuration • Receiver: Continuous reception is enabled by a double-buffer configuration
Data transfer		Selectable from LSB first or MSB first	Selectable from LSB first or MSB first
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1, SCI5, and SCI6 only)
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completed generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, and receive error, or data match (SCI1, SCI5, and SCI6 only) • Completed generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can transition to module stop state.	Individual channels can transition to module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, and framing error	Parity error, overrun error, and framing error
	Hardware flow control	CTSn# and RTSn# pins can be used to control transmission and reception.	CTSn# and RTSn# pins can be used to control transmission and reception.

Item		RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	Data match detection	—	Compares receive data with the contents of a comparison data register, and generates an interrupt request when they match. (SCI1, SCI5, and SCI6 only)
	Start-bit detection	Selection of low level or falling edge	Selection of low level or falling edge
	Adjustment of receive data sampling timing	—	The sampling point of the receive data can be shifted forward or backward relative to the center of the data.
	Transmit signal transition timing adjustment	—	The falling or rising edge of the transmit data can be delayed.
	Break detection	When a framing error occurs, breaks can be detected by reading the RXDn pin level directly.	When a framing error occurs, breaks can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.
	Clock source	• An internal clock or external clock can be selected. • The transfer rate clock can be input from TMR. (SCI5 and SCI6)	• An internal or external clock can be selected. • The transfer rate clock can be input from TMR. (SCI5, SCI6, and SCI12)
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Function for serial communication among multiple processors	Function for serial communication among multiple processors
	Noise cancellation	Digital noise filters are built into the signal paths from input on the RXDn pins	Digital noise filters are built into the signal paths from input on the RXDn pins
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used to control transmission and reception.	CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically re-sent when an error signal is received during transmission.	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically re-sent when an error signal is received during transmission.
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Support for fast mode	Support for fast mode

Item		RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Simple I²C mode	Noise cancellation	• Digital noise filters are built into the SSCLn and SSDAn input signal paths • Adjustable noise cancellation width	• Digital noise filters are built into the SSCLn and SSDAn input signal paths • Adjustable noise cancellation width
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state
	Clock settings	There are four options for clock phase and clock polarity settings	There are four options for clock phase and clock polarity settings
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Support for break field low width output and generation of interrupt on output completion • Support for detection of bus collision and generation of interrupt on detection	• Support for break field low width output and generation of interrupt on output completion • Support for detection of bus collision and generation of interrupt on detection
	Start frame reception	• Support for break field low width detection and generation of interrupt on detect completion • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rate	• Support for break field low width detection and generation of interrupt on detect completion • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rate
	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signals • Half-duplex communication employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing for the sampling of data received through the RXDX12 pin • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signals • Half-duplex communication employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing for the sampling of data received through the RXDX12 pin
	Timer function	Usable as a reload timer	Usable as a reload timer

Item	RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Bit rate modulation function	Errors can be reduced by correcting the output of the on-chip baud rate generator.	Errors can be reduced by correcting the output of the on-chip baud rate generator.
Event link function (supported by SCI5 only)	• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.52 Comparison of SCI Channel Specifications

Item	RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Data match detection	—	SCI1, SCI5, SCI6
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.53 Comparison of Serial Communication Interface Registers

Register	Bit	RX130 (SCIg, SCIh)	RX261 (SCIk, SCIh)
SEMR	ITE	—	Instant transmission enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

2.22 Serial Peripheral Interface

Table 2.54 shows a Comparative Overview of Serial Peripheral Interfaces and Table 2.55 shows a Comparison of Serial Peripheral Interface Registers.

Table 2.54 Comparative Overview of Serial Peripheral Interfaces

Item	RX130 (RSPIa)	RX261 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is possible. • Communication mode: Full-duplex or transmit-only can be selected • The RSPCK polarity can be changed • The RSPCK phase can be changed	• Use of MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected • The RSPCK polarity can be changed • The RSPCK phase can be changed
Data format	• Selectable between MSB first and LSB first • Transfer bit length is selectable from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transfer/receive buffers • A maximum of four frames can be transferred in one instance of transmission/reception (with each frame consisting of a maximum of 32 bits).	• Selectable between MSB first and LSB first • Transfer bit length is selectable from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transfer/receive buffers • A maximum of four frames can be transferred in one instance of transmission/reception (with each frame consisting of a maximum of 32 bits). • Transmit and receive data can be swapped in byte units
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). — Width at high level: Four PCLK cycles — Width at low level: Four PCLK cycles	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 4). — Width at high level: Two PCLK cycles — Width at low level: Two PCLK cycles
Buffer configuration	• Double buffer configuration for transmit and receive buffers • 128-bit transmit and receive buffers	• Double buffer configuration for transmit and receive buffers • 128-bit transmit and receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX130 (RSPIa)	RX261 (RSPIc)
SSL control function	Four SSL pins per channel (SSLA0 to SSLA3) • In single-master mode, SSLA0 to SSLA3 are output pins. • In multi-master mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are either output pins or unused. • In slave mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are unused. • Configurable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Configurable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Configurable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Function for changing SSL polarity	• Four SSL pins per channel (SSLA0 to SSLA3) • In single-master mode, SSLA0 to SSLA3 are output pins. • In multi-master mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are either output pins or unused. • In slave mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are unused. • Configurable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Configurable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Configurable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK — Setting unit: 1 RSPCK • Function for changing SSL polarity
Control in master transfer mode	• Transfers of a maximum of eight commands can be executed sequentially in a loop • The following can be set for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer • MOSI signal value are configurable on SSL negation • RSPCK auto-stop function	• Transfers of a maximum of eight commands can be executed sequentially in a loop. • The following can be set for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value are configurable on SSL negation • RSPCK auto-stop function
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt

Item	RX130 (RSPI)	RX261 (RSPIc)
Event link function (output)	—	• The following events can be output to the event link controller (RSPI0): — Receive buffer full event — Transmit buffer empty event — Error event (mode fault, overrun, underrun, or parity error) — Idle event — Communication complete event
Others	• Function for switching between CMOS output and open-drain output • RSPI initialization function • Loopback mode	• RSPI initialization function • Loopback mode
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

Table 2.55 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX130 (RSPIa)	RX261 (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error 1: Mode fault error	Mode fault error flag 0: No mode fault error, no underrun error 1: Mode fault error or underrun error
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Accessible size • Longword (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Accessible size • Longword (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data and no parity check of receive data is performed. 1: A parity bit is added to transmit data and a parity check of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data but no parity check of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data and no parity check of receive data is performed. 1: A parity bit is not added to transmit data and a parity check of receive data is performed.
SPDCR2	—	—	RSPI data control register 2

2.23 Remote Control Signal Receiver

Table 2.56 shows a Comparative Overview of Remote Control Signal Receivers and Table 2.57 shows a Comparison of Remote Control Signal Receiver Registers.

Table 2.56 Comparative Overview of Remote Control Signal Receivers

Item	RX130 (REMC)		RX261 (REMCa)
External pulse input	**REMC0**	**REMC1**	**REMC0**
Operating clock sources	• IWDTCLK • Sub-clock • HOCO clock • TMR compare match output (TMO0) • PCLKB	• IWDTCLK • Sub-clock • HOCO clock • TMR compare match output (TMO2) • PCLKB	• IWDTCLK • Sub-clock • TMR compare match output (TMO0) • PCLKB
Detection patterns	• Header pattern • Data ‘0’ pattern • Data ‘1’ pattern • Special data pattern		• Header pattern • Data ‘0’ pattern • Data ‘1’ pattern • Special data pattern
Receive buffer	8 bytes (64 bits)		8 bytes (64 bits)
Interrupt request signal	REMCI0	REMCI1	REMCI0
Interrupt sources	• Compare match • Receive error • Data reception complete • Receive buffer full • Header pattern match • Data ‘0’ pattern or data ‘1’ pattern match • Special data pattern match		• Compare match (Compare bit count: 1 to 16 bits) • Receive error • Data reception complete • Receive buffer full • Header pattern match • Data ‘0’ pattern or data ‘1’ pattern match • Special data pattern match
Interrupt mode	—		Either of the following two interrupt modes can be selected for the four interrupt sources of compare match, data reception complete, header pattern match, and special data pattern match. • Normal interrupt mode — An interrupt request is generated when any of the interrupt request generation condition is met. • Sequential interrupt mode — An interrupt request is generated when the interrupt request generation conditions are met for all the enabled interrupt sources.

Item	RX130 (REMC)		RX261 (REMCa)
External pulse input	**REMC0**	**REMC1**	**REMC0**
Selectable functions	• Input signal inversion • Digital filter function (matching two or three times) • Pattern end setting		• Input signal inversion • Digital filter function (matching two or three times) • Pattern end setting
Low power consumption function	• Individual channels can transition to module stop state. • Signal reception during low power consumption state and recovery from low power consumption state in response to the REMC interrupt request are available.		• Can transition to module stop state • Signal reception during low power consumption state and recovery from low power consumption state in response to the REMC interrupt request are available.

Table 2.57 Comparison of Remote Control Signal Receiver Registers

Register	Bit	RX130 (REMC)	RX261 (REMCa)
REMCON1	CSRC[3:0]	Operating clock select bits b6 b3 x 0 0 0: Hi-Z x 0 1 0: TMR compare match output x 1 0 0: Sub-clock x 1 0 1: HOCO clock/512 0 1 1 0: PCLKB/64 1 1 1 0: PCLKB/512	Operating clock select bits b6 b3 x 0 0 0: Hi-Z x 0 1 0: TMR compare match output x 1 0 0: Sub-clock 0 1 1 0: PCLKB/64 1 1 1 0: PCLKB/512 Settings other than the preceding are prohibited.
	INTMD	—	Interrupt mode select bit
REMCPC	CPN[2:0] (RX130) CPN[3:0] (RX261)	Compare bit count specification bits When the setting value of the CPN[2:0] bits is n, bits n to 0 are compared. (n = 0 to 7)	Compare bit count specification bits When the setting value of the CPN[3:0] bits is n, bits n to 0 are compared. (n = 0 to 15)
REMCPD	CPD	Compare value setting bits [7:0]	Compare value setting bits [15:0]
HOSCR	—	HOCO clock supply control register	—

2.24 Capacitive Touch Sensing Unit

Table 2.58 shows a Comparative Overview of Capacitive Touch Sensing Units and Table 2.59 shows a Comparison of Capacitive Touch Sensing Unit Registers.

Table 2.58 Comparative Overview of Capacitive Touch Sensing Units

Item		RX130 (CTSUa)	RX261 (CTSU2SLa)
Operating clock		PCLK, PCLK/2, or PCLK/4	Selectable from PCLKB (1 MHz and higher), PCLKB/2, PCLKB/4, and PCLKB/8
I/O pins	Electrostatic capacitance measurement pins	TS0 to TS35 (36 channels)	TS0 to TS35 (36 channels)
	TSCAP pin	Pin for LPF (Low-pass filter) connection	Capacitor connection pin for measurement power supply (0.01 µF)
Measurement methods	Self-capacitance method	Measured from the charging and discharging current relative to the electrostatic capacitance of an electrode	Measured from the charging and discharging current relative to the electrostatic capacitance of an electrode
	Mutual capacitance method	Measured from the charging and discharging current relative to the electrostatic capacitance between the transmission electrode and reception electrode	Measured from the charging and discharging current relative to the electrostatic capacitance between the transmission electrode and reception electrode
	Current measurement mode	—	Direct reading of current flowing on pin
Scan modes	Single scan mode	Electrostatic capacitance is measured on an arbitrary channel — Self-capacitance single scan mode	Electrostatic capacitance is measured on one channel
	Multi-scan mode	Electrostatic capacitance is measured successively on multiple arbitrary channels — Self-capacitance multi-scan mode — Mutual capacitance multi-scan mode	Electrostatic capacitance is measured successively on multiple channels
	Full scan mode	Electrostatic capacitance is measured successively on multiple arbitrary channels by mutual capacitance — Mutual capacitance full scan mode	—
Noise prevention		Synchronous noise prevention, high-pass noise prevention	• Sensor drive pulse spectrum diffusion function • Sensor drive pulse random phase shift function • Noise hopping function using multiple-frequency sensor drive pulses

Item	RX130 (CTSUa)	RX261 (CTSU2SLa)
Individual pin adjustment	—	• Offset current adjustment function • Specification of sensor drive pulse frequency • Specification of measurement duration
Measurement start conditions	• Software trigger • External trigger (event input from event link controller (ELC))	• Software trigger • External trigger (event input from event link controller (ELC))
Automatic operations	—	• Automatic correction function • Automatic judgment function
Low power operation	—	Support for measurement in snooze mode • Measurement is initiated by external trigger input via ELC • Snooze mode can be ended by non-touch judgment using the automatic judgment function • Snooze mode can be canceled by measurement end interrupt
Interrupt sources	—	• Register setting request interrupt (CTSUWR) • Measurement result read request interrupt (CTSURD) • Measurement end interrupt (CTSUFN)
Event link function	—	Measurement start trigger input
Low power consumption function	—	Can transition to module stop state

Table 2.59 Comparison of Capacitive Touch Sensing Unit Registers

Register	Bit	RX130 (CTSUa)	RX261 (CTSU2SLa)
CTSUCRA	—	—	CTSU control register A
CTSUCRB	—	—	CTSU control register B
CTSUMCH	—	—	CTSU measurement channel register
CTSUCHACA	—	—	CTSU channel enable control register A
CTSUCHACB	—	—	CTSU channel enable control register B
CTSUCHTRCA	—	—	CTSU channel transmit/receive control register A
CTSUCHTRCB	—	—	CTSU channel transmit/receive control register B
CTSUSR	—	—	CTSU status register
CTSUSO	—	—	CTSU sensor offset register
CTSUSCNT	—	—	CTSU sensor counter
CTSUCALIB	—	—	CTSU calibration register
CTSUSUCLKA	—	—	CTSU sensor unit clock control register A
CTSUSUCLKB	—	—	CTSU sensor unit clock control register B

Register	Bit	RX130 (CTSUa)	RX261 (CTSU2SLa)
CTSUTRIMA	—	—	CTSU trimming register A
CTSUTRIMB	—	—	CTSU trimming register B
CTSUOPT	—	—	CTSU option setting register
CTSUSCNTACT	—	—	CTSU sensor counter automatic correction table access register
CTSUMCACTn	—	—	CTSU multi-clock automatic correction table n (n = 1 to 3)
CTSUAJCR	—	—	CTSU automatic judgment control register
CTSUAJTHR	—	—	CTSU threshold register
CTSUAJMMAR	—	—	CTSU moving average result register
CTSUAJBLACT	—	—	CTSU baseline average intermediate result register
CTSUAJBLAR	—	—	CTSU baseline average result register
CTSUAJRR	—	—	CTSU automatic judgment result register
CTSUADCC	—	—	CTSU A/D converter connection control register
CTSUCR0	—	CTSU control register 0	—
CTSUCR1	—	CTSU control register 1	—
CTSUSDPRS	—	CTSU synchronous noise reduction setting register	—
CTSUSST	—	CTSU sensor stabilization wait control register	—
CTSUMCH0	—	CTSU measurement channel register 0	—
CTSUMCH1	—	CTSU measurement channel register 1	—
CTSUCHACn (n = 0 to 3)	—	CTSU channel enable control register n	—
CTSUCHAC4	—	CTSU channel enable control register 4	—
CTSUCHTRCn (n = 0 to 3)	—	CTSU channel transmit/receive control register n	—
CTSUCHTRC4	—	CTSU channel transmit/receive control register 4	—
CTSUDCLKC	—	CTSU high-pass noise reduction control register	—
CTSUST	—	CTSU status register	—
CTSUSSC	—	CTSU high-pass noise reduction spectrum diffusion control register	—
CTSUSO0	—	CTSU sensor offset register 0	—
CTSUSO1	—	CTSU sensor offset register 1	—
CTSUSC	—	CTSU sensor counter	—
CTSURC	—	CTSU reference counter	—
CTSUERRS	—	CTSU error status register	—
CTSUTRMR	—	CTSU reference current calibration register	—

2.25 12-Bit A/D Converter

Table 2.60 shows a Comparative Overview of 12-Bit A/D Converters and Table 2.61 shows a Comparison of 12-Bit A/D Converter Registers.

Table 2.60 Comparative Overview of 12-Bit A/D Converters

Item	RX130 (S12ADE)	RX261 (S12ADE)
Number of units	1 unit	1 unit
Input channels	24 channels	25 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	Per channel: 1.4 µs (when A/D conversion clock ADCLK = 32 MHz)	Per channel: 0.7 µs (ADCCR.CCS bit = 0), 0.5 µs (ADCCR.CCS bit = 1) (when A/D conversion clock ADCLK = 64 MHz)
A/D conversion clock	The peripheral module clock PCLK and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	The peripheral module clock PCLKB and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 24 registers for analog input, and one register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • Support for A/D conversion results to be output with 12-bit accuracy • In addition mode, A/D conversion results are added and stored in A/D data registers as data whose number of bits is the number of bits for conversion accuracy + 2 bits/4 bits. • Double trigger mode (available in single scan mode or group scan mode) — The first instance of A/D conversion data for analog input of a selected channel is stored in the data register for the channel, and the second instance is stored in the duplication register.	• 25 registers for analog input, and one register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • Support for A/D conversion results to be output with 12-bit accuracy • In addition mode, A/D conversion results are added and stored in A/D data registers as data whose number of bits is the number of bits for conversion accuracy + 2 bits/4 bits. • Double trigger mode (available in single scan mode or group scan mode) — The first instance of A/D conversion data for analog input of a selected channel is stored in the data register for the channel, and the second instance is stored in the duplication register.

Item	RX130 (S12ADE)	RX261 (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of a maximum of 24 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output — A/D conversion is performed only once on the internal reference voltage • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of a maximum of 24 arbitrarily selected channels. • Group scan mode: — The analog inputs of a maximum of 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected at the group level is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode: (when group A priority control is selected) — If a trigger for group A is input during A/D conversion of group B, A/D conversion of group B is stopped and A/D conversion is performed for group A. — A/D conversion can be configured to restart (rescan) for group B after A/D conversion of group A has completed.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of a maximum of 25 arbitrarily selected channels — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of a maximum of 25 arbitrarily selected channels • Group scan mode: — The analog inputs of a maximum of 25 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected at the group level is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode: (when group A priority control is selected) — If a trigger for group A is input during A/D conversion of group B, A/D conversion of group B is stopped and A/D conversion is performed for group A. — A/D conversion can be configured to restart (rescan) for group B after A/D conversion of group A has completed.
A/D conversion start conditions	• Software trigger • Synchronous trigger Trigger from the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be initiated by the ADTRG0# pin	• Software trigger • Synchronous trigger Trigger from the general-purpose PWM timer (GPTW) or event link controller (ELC) • Asynchronous trigger A/D conversion can be initiated by the external trigger ADTRG0# pin

Item	RX130 (S12ADE)	RX261 (S12ADE)
Functions	• Variable sampling state count function • Self-diagnosis function of 12-bit A/D converter • Option to select between A/D-converted value addition mode and average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (A/D-converted data duplication function) • A/D data register automatic clear function • Compare function (window A and window B) • 16 ring buffers when using the compare function	• Variable sampling state count function • Self-diagnosis function of 12-bit A/D converter • Option to select between A/D-converted value addition mode and average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (A/D-converted data duplication function) • A/D data register automatic clear function • Compare function (window A and window B) • 16 ring buffers when using the compare function
Interrupt sources	• Except in double trigger mode and group scan mode, scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, the scan end interrupt request (S12ADI0) is generated on completion of a double scan. • In group scan mode, the scan end interrupt request (S12ADI0) is generated when scanning of group A has completed. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • When double trigger mode is selected in group scan mode, the scan end interrupt request (S12ADI0) is generated at the completion of a double scan for group A. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • The S12ADI0 and GBADI interrupts can activate the data transfer controller (DTC).	• Except in double trigger mode and group scan mode, scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, the scan end interrupt request (S12ADI0) is generated on completion of a double scan. • In group scan mode, the scan end interrupt request (S12ADI0) is generated when scanning of group A has completed. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • When double trigger mode is selected in group scan mode, the scan end interrupt request (S12ADI0) is generated at the completion of a double scan for group A. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).
Event link function	• An ELC event is generated on scan completion except when the completed scan is of group B in group scan mode. • An ELC event is generated on completion of a scan of group B when in group scan mode. • An ELC event is generated on completion of all scans. • Scanning can be initiated by a trigger from the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode	• An ELC event is generated on scan completion except when the completed scan is of group B in group scan mode. • An ELC event is generated on completion of a scan of group B when in group scan mode. • An ELC event is generated on completion of all scans. • Scanning can be initiated by a trigger from the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

Table 2.61 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX130 (S12ADE)	RX261 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 7, 16 to 31)	A/D data register y (y = 0 to 8,16 to 31)
ADANSA0	ANSA008	—	A/D conversion channel select bit
ADANSB0	ANSB008	—	A/D conversion channel select bit
ADADS0	ADS008	—	A/D-converted value addition/average channel select bit
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)
ADCMPANSR0	CMPCHA008	—	Compare window A channel select bit
ADCMPLR0	CMPLCHA008	—	Compare window A comparison condition select bit
ADCMPSR0	CMPSTCHA008	—	Compare window A flag
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : : 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the preceding are prohibited.	Compare window B channel select bits b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 0 1 0 0 0: AN008 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : : 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the preceding are prohibited.
ADCCR	—	—	A/D convert cycle control register

2.26 Temperature Sensor

Table 2.62 shows a Comparison of Temperature Sensor Registers.

Table 2.62 Comparison of Temperature Sensor Registers

Register	Bit	RX130 (TEMPSA)	RX261 (TEMPSA)
TSCDRH,TSCDRL (RX130) TSCDR (RX261)	—	Temperature sensor calibration data register	Temperature sensor calibration data register

2.27 Comparator B

Table 2.63 shows a Comparative Overview of Comparator B.

Table 2.63 Comparative Overview of Comparator B

Item	RX130 (CMPBa)	RX261 (CMPBa)
Analog input voltage	Input voltage to CMPBn pin (n = 0, 1)	Input voltage to CMPBn pin
Reference input voltage	Input voltage to CVREFBn pin (n = 0, 1) or internal reference voltage	Input voltage to CVREFBn pin or internal reference voltage
Comparison result	The comparison result read from the CPBFLG.CPBnOUT flag (n = 0, 1) can be output to the CMPOBn pin.	The comparison result read from the CPBFLG.CPBnOUT flag can be output to the CMPOBn pin.
Interrupt requests	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes
Timing of event generation to ELC	• When the comparison result of comparator B0 changes • When the comparison result of comparator B0 or B1 changes	• When the comparison result of comparator B0 changes • When the comparison result of comparator B0 or B1 changes
POE source output timing	—	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes
Selectable functions	• Digital filter function Select whether to enable the digital filter, and the sampling frequency • Window function Select whether the window function (low-side reference voltage (VRFL) < CMPBn (n = 0, 1) < high-side reference voltage (VRFH)) is enabled or disabled. • Reference input voltage Select between CVREFBn pin input or internal reference voltage (generated internally) (n = 0, 1). • Comparator B response speed Select high-speed mode or low-speed mode	• Digital filter function Select whether to enable the digital filter, and the sampling frequency • Window function Select whether the window function (VRFL < CMPBn < VRFH) is enabled or disabled • Reference input voltage Select between CVREFBn pin input or internal reference voltage (generated internally). • Comparator B response speed Select high-speed mode or low-speed mode
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

2.28 RAM

Table 2.64 shows a Comparative Overview of RAM.

Table 2.64 Comparative Overview of RAM

Item	RX130	RX261
RAM size	Maximum of 48 KB	128 KB
RAM addresses	• For 48 KB RAM RAM0: 0000 0000h to 0000 BFFFh • For 32 KB RAM RAM0: 0000 0000h to 0000 7FFFh • For 16 KB RAM RAM0: 0000 0000h to 0000 3FFFh • For 10 KB RAM RAM0: 0000 0000h to 0000 27FFh	• RAM: 0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Read and write access are both performed in a single cycle. • RAM can be enabled or disabled.	• Read and write access are both performed in a single cycle. *1 • RAM can be enabled or disabled.
Low power consumption function	Can transition to module stop state	Ability to enable module stop state
Error check function	—	• Parity error detection • A non-maskable or maskable interrupt is generated when an error occurs

Note: 1. The number of cycles doubles when access crosses the 8-byte boundary.

Table 2.65 Comparison of RAM Registers

Register	Bit	RX130	RX261
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.29 Flash Memory

Table 2.66 shows a Comparative Overview of Flash Memory and Table 2.67 shows a Comparison of Flash Memory Registers.

Table 2.66 Comparative Overview of Flash Memory

Item	RX130	RX261
Memory size	• User area: Maximum of 512 KB • Data area: 8 KB • Extra area: Stores start-up area information, access window information, and unique IDs	• User area: Maximum of 512 KB • User boot area: 8 KB • Extra area: Stores start-up area information, access window information, and unique IDs
Addresses	• 512 KB — FFF8 0000h to FFFF FFFFh • Products with memory size of 384 KB — FFFA 0000h to FFFF FFFFh • Products with memory size of 256 KB — FFFC 0000h to FFFF FFFFh • Products with memory size of 128 KB — FFFE 0000h to FFFF FFFFh • Data area — 0010 0000h to 0010 1FFFh	• 512 KB — FFF8 0000h to FFFF FFFFh • Products with memory size of 384 KB — FFFA 0000h to FFFF FFFFh • Products with memory size of 256 KB — FFFC 0000h to FFFF FFFFh • Data area — 0010 0000h to 0010 1FFFh
Operating clock	• FCLK: 1 to 32 MHz (in ROM P/E mode and E2 DataFlash P/E mode) Maximum of 32 MHz (in E2 DataFlash read mode)	• FCLK: 1 to 64 MHz (in ROM P/E mode and E2 DataFlash P/E mode) Maximum of 64 MHz (in E2 DataFlash read mode) • HOCO clock: 24 MHz, 32 MHz, 48 MHz, or 64 MHz (in ROM P/E mode and E2 DataFlash P/E mode)
Software commands	• The following software commands are implemented: — Program, blank check, block erase, and unique ID read • The following commands are implemented for extra area programming: — Start-up area information program and access window information program	• The following software commands are implemented: — Program, blank check, block erase, and all-block erase • The following commands are implemented for extra area programming: — Start-up area information program, access window protect, and access window information program
Values after erase	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupts	An interrupt (FRDYI) is generated at completion of software command processing or forced stop processing	An interrupt (FRDYI) is generated at completion of software command processing or forced stop processing

Item	RX130	RX261
On-board programming	• Boot mode (SCI interface) — Uses channel 1 of the serial communications interface (SCI1) in asynchronous communication mode — The user area and data area can be programmed • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program	• Boot mode (SCI interface) — Uses channel 1 of the serial communications interface (SCI1) in asynchronous communication mode — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Boot mode (USB interface) — Uses channel 0 (USB0) of the USB 2.0 function module — The user area and data area can be programmed. — Flash memory can be rewritten in self-powered or bus-powered mode — The product can connect to a personal computer using only a USB cable • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming	The user area and data area can be programmed by using a flash programmer compatible with the MCU.	—
ID code protection	• Connections to serial programmers can be permitted or denied based on ID code in boot mode • Connections to an on-chip debugging emulator can be controlled using ID codes	• Connections to serial programmers can be permitted or denied based on ID code in boot mode. • Connections to an on-chip debugging emulator can be controlled using ID codes
Start-up program protection function	A function used to safely program blocks 0 to 15	A function used to safely program blocks 0 to 7
Area protection	During self-programming, this function enables programming only of specified blocks in the user area, while preventing programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area, while preventing programming of the other blocks.
Background operation (BGO) function	Programs on the ROM can run while the E2 DataFlash is being rewritten.	Programs on the ROM can run while the E2 DataFlash is being rewritten.

Table 2.67 Comparison of Flash Memory Registers

Register	Bit	RX130	RX261
MEMWAITR	—	—	Memory wait cycle setting register
FPMCR	FMS0, FMS1, FMS2 (RX130) FMS0, FMS1 (RX261)	Flash operating mode select bits FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the preceding are prohibited.	Flash operating mode select bits FMS1 FMS0 0 0: ROM/E2 DataFlash read mode 0 1: ROM P/E mode 1 0: E2 DataFlash P/E mode 1 1: Setting prohibited
	LVPE	Low-voltage P/E mode enable bit	—
	FMS2	Flash operating mode select bit 2	—
FISR	PCKA[4:0] (RX130) PCKA[5:0] (RX261)	Peripheral clock notification bits Bits used to set the frequency of the FlashIF clock (FCLK)	Peripheral clock notification bits Bits used to set the frequency of the FlashIF clock (FCLK)
FCR	CMD[3:0]	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Unique ID read Settings other than the preceding are prohibited.	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than the preceding are prohibited.
	DRC	Data read completion bit	—
FEXCR	CMD[2:0]	Software command setting bits b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than the preceding are prohibited.	Software command setting bits b2 b0 0 0 1: Start-up area information program/access window protect 0 1 0: Access window information program Settings other than the preceding are prohibited.
FSARH	—	Flash processing start address register H (b8 to b0)	Flash processing start address register H (b15 to b0)
FRBH	—	Flash read buffer register H	—
FRBL	—	Flash read buffer register L	—
FWBH/FWL (RX130) FWBn (RX261)	—	Flash write buffer register H/L	Flash write buffer register n (n = 0 to 3)
FSTATR1	DRRDY	Data read ready flag	—

Register	Bit	RX130	RX261
FEAMH	—	Flash error address monitor register H (b8 to b0)	Flash error address monitor register H (b15 to b0)
FSCMR	AWPR	—	Access window protect flag
UIDRn	—	Unique ID register n (n = 0 to 31)(b7 to b0)	Unique ID register n (n = 0 to 3)(b31 to b0)

2.30 Packages

As shown in Table 2.68, there are differences in the package drawing codes and availability of some package types. Please bear this in mind at the board design stage.

Table 2.68 Packages

Package Type	RENESAS Code	
	RX130	**RX261**
64-Pin LQFP	○	×
48-pin HWQFN	PWQN0048KB-A PWQN0048KE-A	PWQN0048KC-A

○: Package available (RENESAS code omitted), ×: Package not available

3. Comparison of Pin Functions

The following presents a comparison of pin functions, and compares the pins used for the power supply, clocks, and system control. **Blue text** indicates pin functions that are included in only one of the MCU groups, and **red text** indicates pin functions that are present in both groups but differ in some respect. Pin functions whose specifications do not differ between the groups are shown in **black text**.

3.1 100-Pin Package

Table 3.1 shows a Comparison of 100-Pin Package Pin Functions.

Table 3.1 Comparison of 100-Pin Package Pin Functions

100-Pin	RX130 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
1	P06*3	P06*3
2	P03*3/DA0	P03*3/DA0
3	P04*3	P04*3
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/GTIOC6B/GTIOC6B#/CTS6#/RTS6#/SS6#
5	VCL	VCL
6	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
7	MD/FINED	MD/FINED/PG7
8	XCIN	XCIN/PH7
9	XCOUT	XCOUT/EXCIN/PH6
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ2
14	VCC	VCC
15	P35/NMI	UPSEL/P35/NMI
16	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/IRQ4
17	P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3	P33/GTIOC1B/GTIOC7B/GTIOC1B#/GTIOC7B#/TMRI3/RXD6/SMISO6/SSCL6/CRX0*2/IRQ3
18	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
19	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	P30/MTIOC4B/POE8#/TMRI3/RXD1/SMISO1/SSCL1/TS2/IRQ0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
22	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
23	P25/MTIOC4C/MTCLKB/ADTRG0#	P25/GTIOC1B/GTIOC6A/GTIOC1B#/GTIOC6A#/GTETRGB/ADTRG0#
24	P24/MTIOC4A/MTCLKA/TMRI1	P24/GTIOC1A/GTIOC6B/GTIOC1A#/GTIOC6B#/GTETRGA/TMRI1/USB0_VBUSEN*2
25	P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#	P23/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTETRGD/CTS000#/RTS000#/SS000#/DE000
26	P22/MTIOC3B/MTCLKC/TMO0/SCK0	P22/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTETRGC/TMO0/SCK000/TXDB000/USB0_OVRCURB*2

100-Pin	RX130 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
27	P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/ TMCI0/RXD000/SMISO000/SSCL000/ USB0_EXICEN*2
28	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/ TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/ USB0_ID*2
29	P17/MTIOC3A/MTIOC3B/TMO1/ POE8#/SCK1/MISOA/SDA0/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
30	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL0/IRQ6/RTCOUT/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/TS5/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
32	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/TS6/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
33	P13/MTIOC0B/TMO3/SDA0/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/ GTIV/TMO3/SDA0/IRQ3
34	P12/TMCI1/SCL0/IRQ2	P12/TMCI1/SCL0/IRQ2
35	PH3/TMCI0/TS7	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
36	PH2/TMRI0/TS8/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/ TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1/
37	PH1/TMO0/TS9/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP2 TS9*1/IRQ0*1/
38	PH0/TS10/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
39	P55/MTIOC4D/TMO3/TS11	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11
40	P54/MTIOC4B/TMCI1/TS12	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
41	P53	P53/PMC0
42	P52/PMC1	P52
43	P51/PMC0	P51/PMC0
44	P50	P50
45	PC7/MTIOC3A/MTCLKB/TMO2/TXD8/SMOSI8/ SSDA8/MISOA/TS13/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
46	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/ SSCL8/MOSIA/TS14	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
47	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/ TS15	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
48	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/SSLA0/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP

100-Pin	RX130 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
49	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
50	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/MTIOC3A/SCK5/SSLA2	PC1/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/SCK5/SSLA2
52	PC0/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1	PC0/GTIOC6B/GTIOC6B#/GTETRGC/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/TS18	PB7/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
54	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/TS19	PB6/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
55	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9/TS20	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*2/TS20
56	PB4/CTS9#/RTS9#/SS9#/TS21	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
57	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
58	PB2/CTS6#/RTS6#/SS6#/TS23	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
59	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
62	VSS	VSS
63	PA7/MISOA	PA7/GTIOC5B/GTIOC5B#/MISOA
64	PA6/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/RSPCKA/TS27	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
66	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
68	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
70	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
71	PE7/IRQ7/AN023	PE7/IRQ7/AN023
72	PE6/IRQ6/AN022	PE6/IRQ6/AN022

100-Pin	RX130 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
73	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/ IRQ5/AN021/CMPOB0
74	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/ CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
75	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/ TS34/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/ TS34/AN019
76	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/ CVREFB0
77	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/AN017/ CMPB0
78	PE0/SCK12/AN016	PE0/SCK12/AN016
79	PD7/MTIC5U/POE0#/IRQ7/AN031	PD7/IRQ7/AN031
80	PD6/MTIC5V/POE1#/IRQ6/AN030	PD6/IRQ6/AN030
81	PD5/MTIC5W/POE2#/IRQ5/AN029	PD5/IRQ5/AN029
82	PD4/POE3#/IRQ4/AN028	PD4/IRQ4/AN028
83	PD3/POE8#/IRQ3/AN027	PD3/IRQ3/AN027
84	PD2/MTIOC4D/SCK6/IRQ2/AN026	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*2/ IRQ2/AN026
85	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/ SSCL6/CTX0*2/IRQ1/AN025
86	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P47*3/AN007	P47*3/AN007
88	P46*3/AN006	P46*3/AN006
89	P45*3/AN005	P45*3AN005
90	P44*3/AN004	P44*3/AN004
91	P43*3/AN003	P43*3/AN003
92	P42*3/AN002	P42*3/AN002
93	P41*3/AN001	P41*3/AN001
94	VREFL0/PJ7*3	VREFL0/PJ7*3
95	P40*3/AN000	P40*3/AN000
96	VREFH0/PJ6*3	VREFH0/PJ6*3
97	AVCC0	AVCC0
98	P07*3/ADTRG0#	P07*3/ADTRG0#
99	AVSS0	AVSS0
100	P05*3/DA1	P05*3DA1

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.

3.2 80-Pin Package

Table 3.2 shows a Comparison of 80-Pin Package Pin Functions.

Table 3.2 Comparison of 80-Pin Package Pin Functions

80-Pin	RX130 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
1	P06*3	P06*3
2	P03*3/DA0	P03*3/DA0
3	P04*3	P04*3
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
6	MD/FINED	MD/FINED/PG7
7	XCIN	XCIN/PH7
8	XCOUT	XCOUT/EXCIN/PH6
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ2
13	VCC	VCC
14	P35/NMI	UPSEL/P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/ IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ TS0/IRQ2/RTCOUT	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/ IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/ SSCL1/TS2/IRQ0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
19	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
21	P21/MTIOC1B/TMCI0	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/ TMCI0/RXD000/SMISO000/SSCL000/ USB0_EXICEN*2
22	P20/MTIOC1A/TMRI0	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/ TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/ USB0_ID*2
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/ MISOA/SDA0/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL0/IRQ6/RTCOUT/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/TS5/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/TS6/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4

80-Pin	RX130 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
27	P13/MTIOC0B/TMO3/SDA0/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/GTIV/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL0/IRQ2	P12/TMCI1/SCL0/IRQ2
29	PH3/TMCI0/TS7	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
30	PH2/TMRI0/TS8/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
31	PH1/TMO0/TS9/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/IRQ0*1
32	PH0/TS10/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/TS10
33	P55/MTIOC4D/TMO3/TS11	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/TMO3/CRX0*2/TS11
34	P54/MTIOC4B/TMCI1/TS12	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
35	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/GTCPPO0/TMO2/LPTO/CACREF/TXD008/TXDA008/SMOSI008/SSDA008/MISOA/TS13
36	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/RXD008/SMISO008/SSCL008/MOSIA/USB0_EXICEN*2/TS14
37	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/SSLA0/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1/SCK5/CTS008#/RTS008#/SS008#/DE008/SSLA0/PMC0/TSCAP
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
41	PB7/PC1*4/MTIOC3B/TS18	PB7/PC1*4/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
42	PB6/PC0*4/MTIOC3D/TS19	PB6/PC0*4/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*2/TS20
44	PB4/TS21	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
46	PB2/CTS6#/RTS6#/SS6#/TS23	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
48	VCC	VCC
49	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25

80-Pin	RX130 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA/TS26	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
52	PA5/RSPCKA/TS27	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
53	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
54	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/ TS29/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
55	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
56	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
57	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF/SSLA1/TS32
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/ IRQ5/AN021/CMPOB0
59	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/ CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
60	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/ TS34/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/ TS34/AN019
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/ CVREFB0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/AN017/ CMPB0
63	PE0/SCK12/AN016	PE0/SCK12/AN016
64	PD2/MTIOC4D/SCK6/IRQ2/AN026	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*2/ IRQ2/AN026
65	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/ AN025	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/ SSCL6/CTX0*2/IRQ1/AN025
66	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
67	P47*3AN007	P47*3/AN007
68	P46*3/AN006	P46*3/AN006
69	P45*3/AN005	P45*3/AN005
70	P44*3/AN004	P44*3/AN004
71	P43*3/AN003	P43*3/AN003
72	P42*3/AN002	P42*3/AN002
73	P41*3/AN001	P41*3/AN001
74	VREFL0/PJ7*3	VREFL0/PJ7*3
75	P40*3/AN000	P40*3/AN000
76	VREFH0/PJ6*3	VREFH0/PJ6*3
77	AVCC0	AVCC0
78	P07*3/ADTRG0#	P07*3/ADTRG0#
79	AVSS0	AVSS0
80	P05*3/DA1	P05*3/DA1

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 and PC1 are available only when the port switching function is selected.

3.3 64-Pin Package

Table 3.3 shows a Comparison of 64-Pin Package Pin Functions.

Table 3.3 Comparison of 64-Pin Package Pin Functions

64-Pin	RX130 (64-Pin LFQFP/LQFP)	RX261 (64-Pin LFQFP)
1	P03*3/DA0	P03*3/DA0
2	VCL	VCL
3	MD/FINED	MD/FINED/PG7
4	XCIN	XCIN/PH7
5	XCOUT	XCOUT/EXCIN/PH6
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ2
10	VCC	VCC
11	P35/NMI	UPSEL/P35/NMI
12	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ TS0/IRQ2/RTCOUT	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/ IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/ SSCL1/TS2/IRQ0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/ MISOA/SDA0/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL0/IRQ6/RTCOUT/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/TS5/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/TS6/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
21	PH3/TMCI0/TS7	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
22	PH2/TMRI0/TS8/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/ USB0_DM*2/TS8*1/IRQ1*1
23	PH1/TMO0/TS9/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
24	PH0/TS10/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
25	P55/MTIOC4D/TMO3/TS11	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11
26	P54/MTIOC4B/TMCI1/TS12	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12

64-Pin	RX130 (64-Pin LFQFP/LQFP)	RX261 (64-Pin LFQFP)
27	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/ CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
28	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ SSLA0/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/ SMOSI5/SSDA5/PMC0/TS16
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/ TS17	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/ RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/PC1*4/MTIOC3B/TS18	PB7/PC1*4/GTIOC0A/GTIOC7B/GTIOC0A#/ GTIOC7B#/TXD009/TXDA009/SMOSI009/ SSDA009/TS18
34	PB6/PC0*4/MTIOC3D/TS19	PB6/PC0*4/GTIOC0B/GTIOC7A/GTIOC0B#/ GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/ USB0_VBUS*2/TS20
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/ TS22	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/ TMO0/LPTO/SCK6/PMC0/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/ SSDA6/TS24/IRQ4/CMPOB1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/ TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/ CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/ TS25	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/ GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA/TS26	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/ TS29/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
45	PA0/MTIOC4A/SSLA1/TS32/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF/SSLA1/TS32

64-Pin	RX130 (64-Pin LFQFP/LQFP)	RX261 (64-Pin LFQFP)
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/ IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/ CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/ TS34/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/ TS34/AN019
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/ CVREFB0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/AN017/ CMPB0
51	PE0/SCK12/AN016	PE0/SCK12/AN016
52	P47*3/AN007	P47*3/AN007
53	P46*3/AN006	P46*3/AN006
54	P45*3/AN005	P45*3/AN005
55	P44*3/AN004	P44*3/AN004
56	P43*3/AN003	P43*3/AN003
57	P42*3/AN002	P42*3/AN002
58	P41*3/AN001	P41*3/AN001
59	VREFL0/PJ7*3	VREFL0/PJ7*3
60	P40*3/AN000	P40*3/AN000
61	VREFH0/PJ6*3	VREFH0/PJ6*3
62	AVCC0	AVCC0
63	P05*3/DA1	P05*3/DA1
64	AVSS0	AVSS0

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 and PC1 are available only when the port switching function is selected.

3.4 48-Pin Package

Table 3.4 shows a Comparison of 48-Pin Package Pin Functions.

Table 3.4 Comparison of 48-Pin Package Pin Functions

48-Pin	RX130 (48-Pin LFQFP/HWQFN)	RX261 (48-Pin LFQFP/HWQFN)
1	VCL	VCL
2	MD/FINED	MD/FINED/PG7
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ2
7	VCC	VCC
8	P35/NMI	UPSEL/P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RXD1/SMISO1/SSCL1/TS2/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1/TS3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA0/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0_VBUS*2/USB0_VBUSEN*2/USB0_OVRCURB*2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/CRX0*2/TS5/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
17	PH3/TMCI0/TS7	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
18	PH2/TMRI0/TS8/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
19	PH1/TMO0/TS9/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/IRQ0*1
20	PH0/TS10/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/TS10
21	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/GTCPPO0/TMO2/LPTO/CACREF/TXD008/TXDA008/SMOSI008/SSDA008/MISOA/TS13
22	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/RXD008/SMISO008/SSCL008/MOSIA/USB0_EXICEN*2/TS14
23	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15

48-Pin	RX130 (48-Pin LFQFP/HWQFN)	RX261 (48-Pin LFQFP/HWQFN)
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ SSLA0/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
25	PB5/PC3*4/MTIOC2A/MTIOC1B/TMRI1/POE1#/ TS20	PB5/PC3*4/GTIOC4B/GTIOC5A/GTIOC4B#/ GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/ USB0_VBUS*2/TS20
26	PB3/PC2*4/MTIOC0A/MTIOC4A/TMO0/POE3#/ SCK6/TS22	PB3/PC2*4/GTIOC1A/GTIOC3A/GTIOC1A#/ GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/ GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
27	PB1/PC1*4/MTIOC0C/MTIOC4C/TMCI0/TXD6/ SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	PB1/ PC1*4/GTIOC1B/GTIOC2B/GTIOC1B#/ GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/ GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/ TS24/IRQ4/CMPOB1
28	VCC	VCC
29	PB0/PC0*4/MTIC5W/RXD6/SMISO6/SSCL6/ RSPCKA/TS25	PB0/ PC0*4/GTIOC0B/GTIOC2A/GTIOC0B#/ GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/ RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA/TS26	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/ TS29/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/ CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/TS34/ AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/TS34/ AN019
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/TS35/ IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/ AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SSDA12/TXDX12/SIOX12/AN017/CMPB0
39	P47/AN007	P47*3/AN007
40	P46*3/AN006	P46*3/AN006
41	P45*3/AN005	P45*3/AN005
42	P42*3/AN002	P42*3/AN002
43	P41*3/AN001	P41*3/AN001
44	VREFL0/PJ7*3	VREFL0/PJ7*3
45	P40*3/AN000	P40*3/AN000
46	VREFH0/PJ6	VREFH0/PJ6*3
47	AVCC0	AVCC0

48-Pin	RX130 (48-Pin LFQFP/HWQFN)	RX261 (48-Pin LFQFP/HWQFN)
48	AVSS0	AVSS0

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 to PC3 are available only when the port switching function is selected.

4. Important Information when Migrating Between MCUs

There are some considerations about the differences between the RX261 Group and RX130 Group.

4.1 Considerations for Functional Design

Some of the software that runs on the RX130 Group is compatible with the RX261 Group. However, due to differences in aspects such as operation timing and electrical characteristics, you must evaluate your circumstances thoroughly.

The following explains software-related matters to consider in relation to function settings that differ between the RX261 Group and RX130 Group.

Section 1. Comparison of Built-In Functions of RX260/RX261 Group and RX130 Group explains the differences between modules and functions.

For details, refer to the User's Manual: Hardware document listed in section 5. Reference Documents.

4.1.1 Clock Frequency Settings

The RX261 Group and RX130 Group have different restrictions in relation to clock frequency settings. For details, see Table 4.1.

Table 4.1 Comparison of Restrictions on Clock Frequency Settings

Item	RX130	RX261
Restrictions on clock frequency settings	—	PCLKA ≥ PCLKB PCLKB ≥ CANFDCLK (when CANFD is used) PCLKB ≥ CANFDMCLK (when CANFD is used)
Restrictions on clock frequency ratio	ICLK:FCLK = N:1 ICLK:PCLKB = N:1 ICLK:PCLKD = N:1	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKB = 2:1 (when CANFD is used)

4.1.2 PLL Circuit

The multiplication factor of the PLL circuit is within a range from 4 to 8× (in increments of 0.5) in the RX130 Group, and within a range from 4 to 15.5× (in increments of 0.5) in the RX261 Group. When using the PLL circuit, change the setting value of the PLLCR.STC bit to an appropriate value.

4.1.3 Initialization of the Voltage Detection Level Select Register (LVDLVLR)

LVDLVLR register initialization differs between products.

4.1.4 Initialization of the Sub-Clock Oscillator Control Register (SOSCCR)

SOSCCR register initialization differs between products.

4.1.5 Notes on High-Speed Operating Mode

The maximum operating frequency of the FLASH read time in high-speed operating mode differs between the RX130 Group and the RX261 Group. For details, see Table 4.2 Comparison of Maximum Operating Frequency of FLASH Read Time in High-Speed Operating Mode.

Table 4.2 Comparison of Maximum Operating Frequency of FLASH Read Time in High-Speed Operating Mode

Item	RX130	RX261
ICLK	32 MHz	64 MHz
FCLK	32 MHz	64 MHz
PCLKD	32 MHz	64 MHz
PCLKB	32 MHz	32 MHz
PCLKA	—	64 MHz

5. Reference Documents

User's Manual: Hardware

RX130 Group User's Manual: Hardware Rev.3.00 (R01UH0560EJ0300)
(The latest version is available from the Renesas Electronics website.)

RX260/RX261 Group User's Manual: Hardware Rev.1.00 (R01UH1045EJ0100)
(The latest version is available from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information is available from the Renesas Electronics website.)

Related Technical Updates

This application note contains information from the following technical updates:

- TN-RX*-A0147B/E
- TN-RX*-A0217A/E
- TN-RX*-A0227A/E
- TN-RX*-A0224B/E
- TN-RX*-A0238B/E
- TN-RX*-A0262A/E
- TN-RX*-A0263A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 26, 2024	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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