Toradex
Swiss. Embedded. Computing.

Colibri iMX6

Datasheet

Revision History

Date	Doc. Rev.	Colibri iMX6 Version	Changes
02-Jun-2014	Rev. 0.9	V1.0	Initial Release: Preliminary version
02-Jul-2014	Rev. 0.91	V1.0	Minor changes
03-Sep-2014	Rev. 0.92	V1.0	Update module picture on front page Corrections in description of recovery mode
14-Oct-2014	Rev. 0.93	V1.0	Quad and Dual words referring to iMX6 processor variants have been deleted from datasheet. Updated figure 2, Colibri iMX6 Block Diagram.
18-Nov-2014	Rev. 0.94	V1.0	Section 8.5 renamed and updated Additional information to RTC added (section 0 and 8.2) Add information to PMIC shutdown issue (section 7)
13-Jan-2015	Rev. 0.95	V1.0	Remove LVDS interface in Figure 1
06-May-2015	Rev. 0.96	V1.0	Additional information to recovery mode (section 6) Numbering of sections corrected (several section number appeared multiple)
25-Sep-2015	Rev. 1.0	V1.0	Remove assembly versions in revision history
18-Jan-2016	Rev. 1.1	V1.0	Section 5.10, I2C: Correction in table 5-18, DDC I2C signals available on the HDMI FFC Connector (X2) Section 0, Real-Time Clock (RTC): minor correction Section 6, Recovery Mode: minor correction, updated figure 8
31-Mar-2016	Rev. 1.2	V1.0	Section 7: add information to nRESET_OUT issue Section 4.3: add additional information to pin reset state Section 5.12: add information to SPI signal directions Minor changes
15-Jun-2016	Rev. 1.3	V1.0	Section 5.12: correction of maximum SPI clock speed Section 7: Move known issues to a separate errata document
14-Feb-2017	Rev. 1.4	V1.0	Section 1.5: Updated web-links Section 1.5.6: Updated heading Section 8.3.1: Updated web-links
24-Apr-2017	Rev. 1.5	V1.1	Update document for module version V1.1: Section 3.2.1, 4.1, 5.1.3, 5.11, 5.28, and 6 Add remark to eMMC flash endurance in section 1.3.2 Minor changes
09-May-2017	Rev. 1.6	V1.1	Remove recovery function from SODIMM pin 35: Section 3.2.1, 4.1, 5.11, and 6
29-May-2018	Rev. 1.7	V1.1	Added Power measurements (section 8.2)
15-Oct-2018	Rev. 1.8	V1.1	Section 3.1: Update information regarding FFC connector Section 5.17.1: Correct I2S Slave pins Section 5.17.2. Correct AC'97 pins Section 0: Add mechanical position of FFC Minor Changes
09-May-2019	Rev. 1.9	V1.1	Section 5.15 Added information for UHS-I 1.8V mode Section 8.2 Added missing power consumption values

Contents

1. Introduction

1.1 Hardware

The Colibri iMX6 is a computer module based on the Freescale© i.MX 6 embedded System-on-Chip (SoC). The SoC features a scalable multicore ARM Cortex™ A9 processor with one to four cores, depending on the version. The module delivers high CPU and graphical performance with minimum power consumption.

The Colibri iMX6 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature to achieve the best performance with the lowest power consumption. The module is also available in an industrial temperature range (-40°C to 85°C) variant.

The module targets a wide range of applications, including: Digital Signage, Medical Devices, Navigation, Industrial Automation, HMIs, Avionics, Entertainment system, POS, Data Acquisition, Thin Clients, Robotics, Gaming and much more.

It offers a wide range of interfaces from simple GPIOs, industry standard I2C, SPI, CAN, and UART buses through to high speed USB 2.0 interfaces and a 16/32bit external memory bus (parallel bus). The HDMI interface makes it very easy to connect large, full HD resolution displays.

The Colibri iMX6 module encapsulates the complexity associated with modern day electronic design, such as high speed impedance controlled layouts with high component density utilising blind and buried via technology. This allows the customer to create a carrier board which implements the application specific electronics generally being much less complicated. The module is compatible with the wide range of other computer modules within the Colibri family. This allows the customer to scale their product without the need to build different carrier boards for each project.

1.2 Software

The Colibri iMX6 comes with a core runtime licence for Windows Embedded Compact 2013. Windows Embedded Compact 7 and Embedded Linux images are also available. Toradex works with partners to support additional Operating Systems.

1.3 Main Features

1.3.1 CPU

	Colibri iMX6DL 512MB	Colibri iMX6DL 512MB IT	Colibri iMX6S 256MB	Colibri iMX6S 256MB IT
Freescale SoC	MCIMX6U5DVM10AC	MCIMX6U7CVM08AC	MCIMX6S5DVM10AC	MCIMX6S7CVM08AC
SoC Family	i.MX 6 DualLite	i.MX 6 DualLite	i.MX 6 Solo	i.MX 6 Solo
CPU Cores	2	2	1	1
L1 Instruction Cache (each core)	32KByte	32KByte	32KByte	32KByte
L1 Data Cache (each core)	32KByte	32KByte	32KByte	32KByte
L2 Cache (shared by cores)	512KB	512KB	512KB	512KB
NEON MPE	✓	✓	✓	✓
Maximum CPU frequency	996MHz	792MHz	996MHz	792MHz
ARM TrustZone	✓	✓	✓	✓
Advanced High Assurance Boot	✓	✓	✓	✓
Cryptographic Acceleration and Assurance Module	✓	✓	✓	✓
Secure Real-Time Clock	✓	✓	✓	✓
Secure JTAG Controller	✓	✓	✓	✓

1.3.2 Memory

	Colibri iMX6DL 512MB	Colibri iMX6DL 512MB IT	Colibri iMX6S 256MB	Colibri iMX6S 256MB IT
DDR3 RAM Size	512MByte	512MByte	256MByte	256MByte
DDR3 RAM Speed	800MT/s	800MT/s	800MT/s	800MT/s
DDR3 RAM Memory Width	64bit	64bit	32bit	32bit
eMMC NAND Flash* (8bit)	4GByte	4GByte	4GByte	4GByte

* eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear levelling in the eMMC controller makes sure the cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.3.3 Interfaces

	Colibri iMX6DL 512MB	Colibri iMX6DL 512MB IT	Colibri iMX6S 256MB	Colibri iMX6S 256MB IT
LCD RGB (24bit, 225 Mpixel/s)	1+1*	1+1*	1+1*	1+1*
HDMI 1.4a (266Mpixel/s)	1	1	1	1
VGA Analogue Video	-	-	-	-
Resistive Touch Screen	4 Wire	4 Wire	4 Wire	4 Wire
Analogue Audio Headphone out	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Line in	1 (Stereo)	1 (Stereo)	1 (Stereo)	1 (Stereo)
Analogue Audio Mic in	1 (Mono)	1 (Mono)	1 (Mono)	1 (Mono)
SSI (AC97/I²S)	4*	4*	4*	4*
ESAI	1*	1*	1*	1*

	Colibri iMX6DL 512MB	Colibri iMX6DL 512MB IT	Colibri iMX6S 256MB	Colibri iMX6S 256MB IT
S/PDIF	1* in / 1 out	1* in / 1 out	1* in / 1 out	1* in / 1 out
Parallel Camera Interface	1+1*	1+1*	1+1*	1+1*
I2C	1+2*	1+2*	1+2*	1+2*
SPI	1+3*	1+3*	1+3*	1+3*
UART	3+2*	3+2*	3+2*	3+2*
SD/SDIO/MMC	1+2*	1+2*	1+2*	1+2*
GPIO	Up to 154	Up to 154	Up to 154	Up to 154
USB 2.0 OTG (host/device)	1	1	1	1
USB 2.0 host	1	1	1	1
10/100 MBit/s Ethernet	1 (IEEE 1588)	1 (IEEE 1588)	1 (IEEE 1588)	1 (IEEE 1588)
PWM	4	4	4	4
Analogue Inputs	4	4	4	4
CAN	2*	2*	2*	2*
MLB	1*	-	1*	-
8bit NAND Interface	1*	1*	1*	1*
External Memory Bus	16bit / 32bit*	16bit / 32bit*	16bit / 32bit*	16bit / 32bit*

*These interfaces are available on pins that are not defined as standard interfaces in the Colibri architecture. They are alternate functions for pins which provide primary interfaces. There are restrictions on using different interfaces simultaneously, please check the available alternate functions to understand any constraints. For more information, please check also the list in section 1.4 and the description of the associated interface in section 5.

1.3.4 Graphics Processing Unit

	Colibri iMX6DL 512MB	Colibri iMX6DL 512MB IT	Colibri iMX6S 256MB	Colibri iMX6S 256MB IT
Independent Image Processing Units	1	1	1	1
OpenGL® ES 2.0 (532 M pixel/s)	✓	✓	✓	✓
Number of OpenGL® Shaders	1	1	1	1
Dedicated OpenVG 1.1 accelerator				
OpenVG 1.1	✓	✓	✓	✓
Windows Direct3D	✓	✓	✓	✓
OpenCL EP				
16x Line Anti-aliasing	✓	✓	✓	✓
8K x 8K texture and 8K x 8K rendering target	✓	✓	✓	✓
Ultra-threaded, unified vertex and fragment shaders	✓	✓	✓	✓

1.3.5 HD Video Decode

- ✓ MPEG-2 (Main, High Profile) – 1080p30, 720p60, (50Mbps)
- ✓ MPEG4/XviD (Simple, Advanced Simple Profile) – 1080p30 (40Mbps)
- ✓ H.263 (P0/P3) – 16CIF(1408x1152) 30fps (20Mbps)
- ✓ H.264 (Constrained Baseline, Baseline, Main, High Profile) – 1080p30, 720p60, (50Mbps)
- ✓ H.264-MVC (Baseline, Main, High Profile) – 720p60
- ✓ VC1 (Simple, Main, Advanced Profile) – 1080p30 (45Mbps)
- ✓ RV (8/9/10) – 1080p30 (40Mbps)
- ✓ DivX (3/4/5/6) – 1080p30 (40Mbps)
- ✓ On2 VP6/VP8 – 720p30 (20Mbps)
- ✓ AVS Jizhun – 1080p30 (40Mbps)
- ✓ MJPEG (Baseline) – 8192x8192 (120MPixel/s)

1.3.6 HD Video Encode

- ✓ MPEG4 (Simple Profile) – 720p30 (12Mbps)
- ✓ H.263 (P0/P3) – 4CIF(704x576) 30fps (8Mbps)
- ✓ H.264 (Constrained Baseline, Baseline Profile) – 1080p30, (14Mbps)
- ✓ MJPEG (Baseline) – 8192x8192 (160MPixel/s)

1.3.7 Supported Operating Systems

- ✓ Windows Embedded Compact 7
- ✓ Windows Embedded Compact 2013
- ✓ Embedded Linux
- ✓ Contact Toradex for Android
- ✓ Other operating systems are available through Toradex partners

1.4 Interface Overview

The table in Figure 1 shows the interfaces that are supported on the Colibri iMX6 module, and whether an interface is provided as a standard (primary) function or as an alternate function. The UART interface is an example of an interface that makes use of standard and alternate functions – three UART interfaces are provided as standard functions which are compatible with other Colibri modules while an additional two interfaces are available as alternate functions. Using alternate function UART interfaces limits the compatibility with other Colibri modules. The alternate function of a pin can only be used if the standard function is not used. Check section 4.4 for a list of all alternate functions of the SODIMM pins.

Feature	Total	Standard	Alternate Function
4 Wire Resistive Touch	1	1	
Analogue Inputs	4	4	
Analogue Audio (Line in/out, Mic in)	1	1	
CAN	2		2
CSI (Quad Lane)			
DSI (Dual Lane)			
Dual Channel LVDS Display (2x Single or 1x Dual)			
Fast Ethernet	1	1	
GPIO	154		154
AC97/I2S/SSI	4		4
ESAI	1		1
HDMI (TDMS)	1	1	
I2C	3	1	2*
Parallel Camera	2	1	1
Parallel LCD	2	1	1
PCI-Express			
PWM	4	4	
SATA			
SD/SDIO/MMC	3	1	2
S/PDIF In	1		1
S/PDIF Out	1	1	
SPI	4	1	3
UART	5	3	2
USB 2.0 OTG (host/device)	1	1	
USB 2.0 host	1	1	
VGA			
MLB	1*		1*
8bit NAND interface	1		1
External Memory Bus 16 bit non-multiplexed	1	1	
External Memory Bus 32 bit multiplexed	1		1

Figure 1: Colibri iMX6 Module Interfaces

*These interfaces are not available on all versions of the Colibri iMX6 module. Please see section 0 for more information

1.5 Reference Documents

1.5.1 Freescale i.MX 6

You will find the details about i.MX 6 SoC in the Datasheet and Reference Manual provided by NXP/Freescale.
http://www.nxp.com/

1.5.2 Ethernet Transceiver

Colibri iMX6 uses the Microchip/Micrel KSZ8041NL Ethernet PHY:
http://www.microchip.com/KSZ8041

1.5.3 Audio Codec

Colibri iMX6 uses the NXP/Freescale SGTL5000 Audio Codec"
http://www.nxp.com/products/media-and-audio-processing/data-converters/audio-converters/audio-codec/ultra-low-power-audio-codec:SGTL5000

1.5.4 Touch Screen Controller / ADC

Colibri iMX6 uses the STMicroelectronics STMPE811 Touchscreen Controller.
http://www.st.com

1.5.5 Toradex Developer Centre

You can find a lot of additional information in the Toradex Developer Centre, which is updated with the latest product support information on a regular basis.
Please note that the Developer Centre is common for all Toradex products. You should always check to ensure if information is valid or relevant for the Colibri iMX6.
http://developer.toradex.com

1.5.6 Colibri Carrier Board Schematics

We provide the complete schematics and the Altium project file which includes library symbols and IPC-7351 compliant footprints for the Colibri Evaluation Board and other Carrier Boards free of charge. This is a great help when designing your own Carrier Board.
http://developer.toradex.com/carrier-board-design

1.5.7 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin muxing of the Apalis and Colibri Modules. The tool allows comparing the interfaces of different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

2. Architecture Overview

2.1 Block Diagram

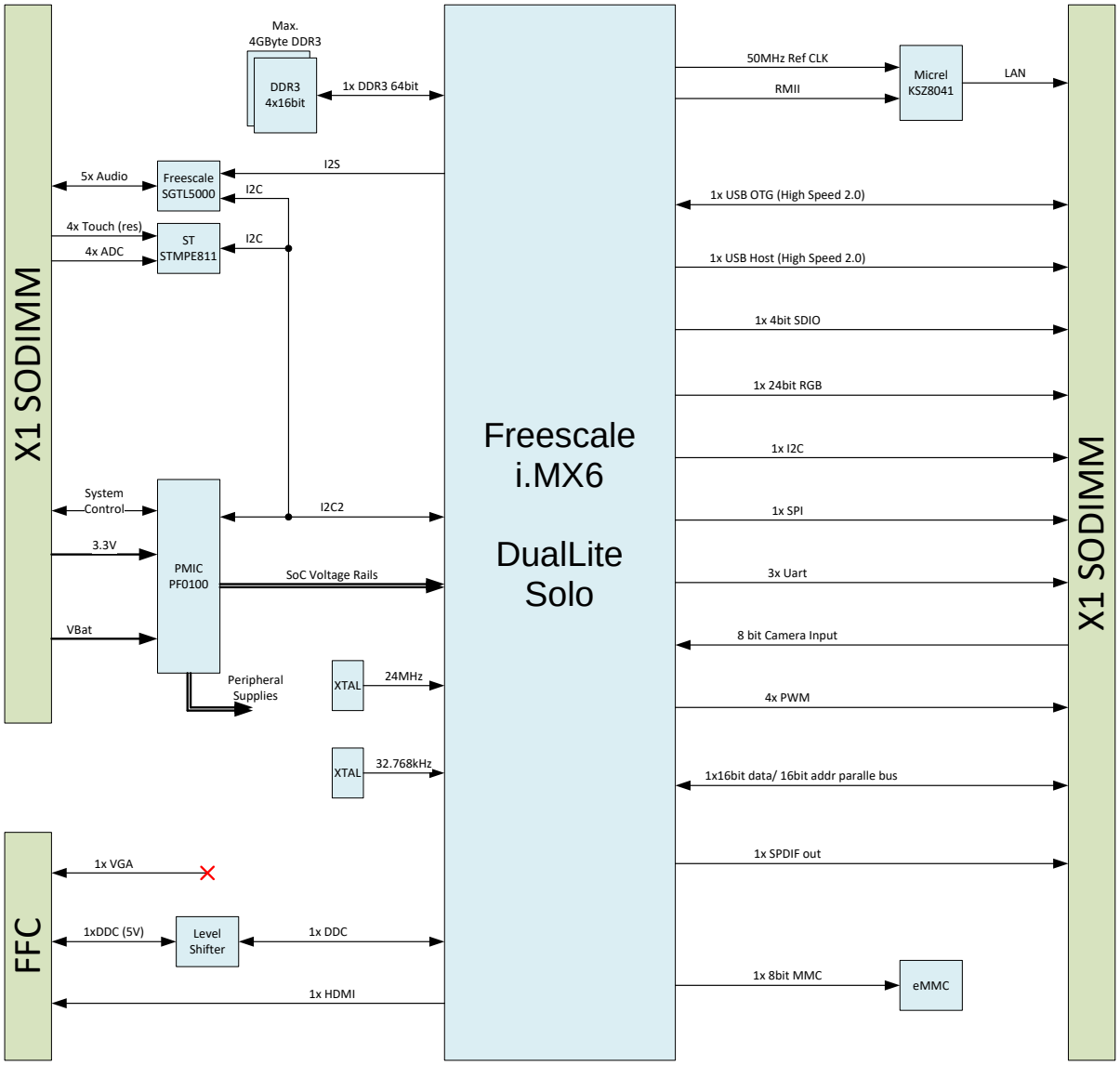

Figure 2 Colibri iMX6 Block Diagram

3. Colibri iMX6 Connectors

3.1 Physical Locations

The Colibri iMX6 is equipped with a 200 Pin SODIMM edge connector (X1) and an FCC connector (X2). The FFC connector is a Molex 52437-2471 with a 0.5mm pitch with 24 bottom contacts. The position of the connectors is shown in the figure below.

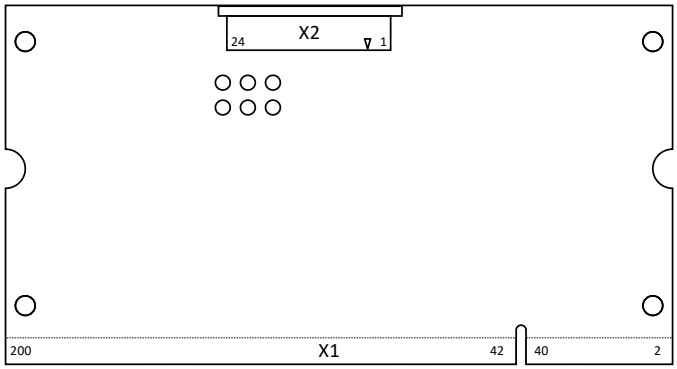

Figure 3: Location of the Colibri iMX6 connector (bottom view)

3.2 Assignment

3.2.1 SODIMM 200

The table below details the SODIMM 200-way connector pin functionality.

It should be noted that some of the pins are multiplexed; that is, there is more than one i.MX 6 SoC pin connected to one SODIMM pin. For example, GPIO01 and EIM_ADDR21 are both connected to SODIMM pin 67. Care should be taken to ensure that multiplexed pins are tri-stated when they are not being used (e.g. if i.MX 6 pin A and pin B are tied to SODIMM pin 1, then if i.MX 6 pin A is being driven, pin B should be tri-stated). Additional information can be found in chapter 4.1: Function Multiplexing.

- X1 Pin: Pin number on the SODIMM connector (X1).
- Compatible function: The default function which is compatible with all Colibri modules. IMPORTANT: There are some limitations. You can find more information about pin compatibility in the "**Colibri Migration Guide**".
- i.MX 6 CPU Ball: The name of the ball (a.k.a. pin) of the i.MX 6 SoC.
- Non i.MX 6 CPU Ball: Peripheral functions which are not directly provided by the i.MX 6 SoC.
- Note: Additional information. Some pins are noted as "no standard function". These pins can provide only the GPIO functionality and the listed alternate function, but not the Colibri compatible function. Some of the Colibri compatible functions might be emulated by programmatically manipulating the GPIO.

Table 3-1 X1 Connector

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
1	Audio Analogue Microphone Input		MIC_IN	SGTL5000 Pin 10
3	Audio Analogue Microphone GND		MIC_GND	GND switched, controlled with GPIO6_IO21

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
5	Audio Analogue Line-In Left		LINEIN_L	SGTL5000 Pin 9
7	Audio Analogue Line-In Right		LINEIN_R	SGTL5000 Pin 8
9	Audio_Analogue GND		VSS_AUDIO	GND
11	Audio_Analogue GND		VSS_AUDIO	
13	Audio Analogue Headphone GND		HEADPHONE_GND	Virtual GND, do not connect to normal GND
15	Audio Analogue Headphone Left		HEADPHONE_L	SGTL5000 Pin 4
17	Audio Analogue Headphone Right		HEADPHONE_R	SGTL5000 Pin 1
19	UART_C RXD	SD4_CMD		UART used in DTE mode
21	UART_C TXD	SD4_CLK		UART used in DTE mode
23	UART_A DTR	EIM_DATA24		
25	UART_A CTS, Keypad_In<0>	EIM_DATA19		
27	UART_A RTS	EIM_DATA20		
29	UART_A DSR	EIM_DATA25		
31	UART_A DCD	EIM_DATA23		
33	UART_A RXD	CSI0_DATA10		UART used in DTE mode
35	UART_A TXD	CSI0_DATA11		UART used in DTE mode
37	UART_A RI, Keypad_In<4>	NAND_DATA07		no standard function
39	GND		GND	
41	GND		GND	
43	WAKEUP Source<0>, SDCard CardDetect	NAND_DATA05		no standard function
45	WAKEUP Source<1>	EIM_ADDR16		no standard function
47	SDCard CLK	SD1_CLK		
49	SDCard DAT<1>	SD1_DATA1		
51	SDCard DAT<2>	SD1_DATA2		
53	SDCard DAT<3>	SD1_DATA3		
55	PS2 SDA1	GPIO07		no standard function
57	LCD RGB Data<16>	DISP0_DATA16		
59	PWM<A>, Camera Input Data<7>	SD4_DATA1/ EIM_ADDR22		Multiplexed (Two i.MX 6 Pins)
61	LCD RGB Data<17>	DISP0_DATA17		
63	PS2 SCL1	GPIO08		no standard function
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	EIM_ADDR24		Only camera input supported
67	PWM<D>, Camera Input Data<6>	GPIO01/ EIM_ADDR21		Multiplexed (Two i.MX 6 Pins)
69	PS2 SCL2	SD2_CMD		no standard function
71	Camera Input Data<0>, LCD Back-Light GPIO	EIM_DATA26		no standard function
73		EIM_DATA27		
75	Camera Input MCLK	NAND_CS2_B		
77		EIM_DATA18		

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
79	Camera Input Data<4>	EIM_ADDR19		
81	Camera Input VSYNC	EIM_DATA29		
83	GND		GND	
85	Camera Input Data<8>, Keypad_Out<4>	EIM_ADDR23		Only camera input supported
87	nReset Out		PMIC Reset Out	
89	nWE	EIM_RW		
91	nOE	EIM_OE		
93	RDnWR	SD2_CLK		Gated EIM_RW signal
95	RDY	EIM_WAIT		
97	Camera Input Data<5>	EIM_ADDR20		
99	nPWE	SD2_DATA3		Gated EIM_RW signal
101	Camera Input Data<2>	EIM_ADDR17		
103	Camera Input Data<3>	EIM_ADDR18		
105	nCS0	EIM_CS0		
107	nCS1	EIM_CS1		
109	GND		GND	
111	ADDRESS0	EIM_AD00		
113	ADDRESS1	EIM_AD01		
115	ADDRESS2	EIM_AD02		
117	ADDRESS3	EIM_AD03		
119	ADDRESS4	EIM_AD04		
121	ADDRESS5	EIM_AD05		
123	ADDRESS6	EIM_AD06		
125	ADDRESS7	EIM_AD07		
127		NAND_DATA06		no standard function
129	USB Host Power Enable	EIM_DATA31		
131	Usb Host Over-Current Detect	EIM_DATA30		
133		NAND_DATA03		no standard function
135	SPDIF_IN	NAND_DATA02		no standard function
137	USB Client Cable Detect, SPDIF_OUT	GPIO17/ USB_OTG_VBUS		Level shift circuit with more than one i.MX 6 pin
139	USB Host DP	USB_H1_DP		
141	USB Host DM	USB_H1_DN		
143	USB Client DP	USB_OTG_DP		
145	USB Client DM	USB_OTG_DN		
147	GND		GND	
149	DATA0	CSI0_DATA_EN		
151	DATA1	CSI0_VSYNC		
153	DATA2	CSI0_DATA04		
155	DATA3	CSI0_DATA05		
157	DATA4	CSI0_DATA06		
159	DATA5	CSI0_DATA07		

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
161	DATA6	CSI0_DATA08		
163	DATA7	CSI0_DATA09		
165	DATA8	CSI0_DATA12		
167	DATA9	CSI0_DATA13		
169	DATA10	CSI0_DATA14		
171	DATA11	CSI0_DATA15		
173	DATA12	CSI0_DATA16		
175	DATA13	CSI0_DATA17		
177	DATA14	CSI0_DATA18		
179	DATA15	CSI0_DATA19		
181	GND		GND	
183	Ethernet Link/Activity Status		LINK_AKT	KSZ8041 LED0
185	Ethernet Speed Status		SPEED100	KSZ8041 LED1
187	Ethernet TXO-		TXO-	
189	Ethernet TXO+		TXO+	
191	Ethernet GND		AGND_LAN	
193	Ethernet RXI-		RXI-	
195	Ethernet RXI+		RXI+	
197	GND		GND	
199	GND		GND	
2	Analogue Input <3>		AD3	STMPE811 Pin 12
4	Analogue Input <2>		AD2	STMPE811 Pin 11
6	Analogue Input <1>		AD1	STMPE811 Pin 9
8	Analogue Input <0>		AD0	STMPE811 Pin 8
10	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply
12	Audio_Analogue VDD		AVDD_AUDIO	3.3V Supply
14	Resistive Touch PX		TSPX	STMPE811 Pin 13
16	Resistive Touch MX		TSMX	STMPE811 Pin 16
18	Resistive Touch PY		TSPY	STMPE811 Pin 15
20	Resistive Touch MY		TSMY	STMPE811 Pin 1
22	VDD Fault Detect	ENET_REF_CLK		no standard function
24	Battery Fault Detect	DI0_PIN04		no standard function
26	nReset In		Reset input	
28	PWM<B>	GPIO09		
30	PWM<C>	SD4_DATA2		
32	UART_B CTS	SD4_DATA6		
34	UART_B RTS	SD4_DATA5		
36	UART_B RXD	SD4_DATA7		UART used in DTE mode
38	UART_B TXD	SD4_DATA4		UART used in DTE mode
40	VCC_BATT		VCC_BATT	RTC supply
42	3V3		3V3	
44	LCD RGB DE	DI0_PIN15		
46	LCD RGB Data<7>	DISP0_DATA07		

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
48	LCD RGB Data<9>	DISP0_DATA09		
50	LCD RGB Data<11>	DISP0_DATA11		
52	LCD RGB Data<12>	DISP0_DATA12		
54	LCD RGB Data<13>	DISP0_DATA13		
56	LCD RGB PCLK	DI0_DISP_CLK		
58	LCD RGB Data<3>	DISP0_DATA03		
60	LCD RGB Data<2>	DISP0_DATA02		
62	LCD RGB Data<8>	DISP0_DATA08		
64	LCD RGB Data<15>	DISP0_DATA15		
66	LCD RGB Data<14>	DISP0_DATA14		
68	LCD RGB HSYNC	DI0_PIN02		
70	LCD RGB Data<1>	DISP0_DATA01		
72	LCD RGB Data<5>	DISP0_DATA05		
74	LCD RGB Data<10>	DISP0_DATA10		
76	LCD RGB Data<0>	DISP0_DATA00		
78	LCD RGB Data<4>	DISP0_DATA04		
80	LCD RGB Data<6>	DISP0_DATA06		
82	LCD RGB VSYNC	DI0_PIN03		
84	3V3		3V3	
86	SPI CS	EIM_ADDR25		
88	SPI CLK	EIM_DATA21		
90	SPI RXD	EIM_DATA22		
92	SPI TXD	EIM_DATA28		
94	Camera Input HSYNC	EIM_EB3		
96	Camera Input PCLK	EIM_DATA17		
98	Camera Input Data<1>	SD2_DATA0		no standard function
100	Keypad_Out<1>	SD4_DATA3		no standard function
102		NAND_DATA04		no standard function
104		SD4_DATA0		no standard function
106	nCS2	SD2_DATA1		
108	3V3		3V3	
110	ADDRESS8	EIM_AD08		
112	ADDRESS9	EIM_AD09		
114	ADDRESS10	EIM_AD10		
116	ADDRESS11	EIM_AD11		
118	ADDRESS12	EIM_AD12		
120	ADDRESS13	EIM_AD13		
122	ADDRESS14	EIM_AD14		
124	ADDRESS15	EIM_AD15		
126	DQM0	EIM_EB0		
128	DQM1	EIM_EB1		
130	DQM2	SD2_DATA2		
132	DQM3	NAND_DATA00		no standard function

X1 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
134	ADDRESS25	NAND_DATA01		no standard function
136	ADDRESS24	DISP0_DATA18		no standard function
138	ADDRESS23	DISP0_DATA19		no standard function
140	ADDRESS22	DISP0_DATA20		no standard function
142	ADDRESS21	DISP0_DATA21		no standard function
144	ADDRESS20	DISP0_DATA22		no standard function
146	ADDRESS19	DISP0_DATA23		no standard function
148	3V3		3V3	
150	DATA16	EIM_LBA		no standard function
152	DATA17	EIM_BCLK		no standard function
154	DATA18	NAND_CS3_B		no standard function
156	DATA19	NAND_CS1_B		no standard function
158	DATA20	NAND_READY		no standard function
160	DATA21	NAND_ALE		no standard function
162	DATA22	NAND_WP_B		no standard function
164	DATA23	NAND_CS0_B		no standard function
166	DATA24	NAND_CLE		no standard function
168	DATA25	GPIO19		no standard function
170	DATA26	CSI0_HSYNC		no standard function
172	DATA27	CSI0_PIXCLK		no standard function
174	DATA28	GPIO04		no standard function
176	DATA29	GPIO05		no standard function
178	DATA30	KEY_COL4		no standard function
180	DATA31	GPIO02/ JTAG_MOD		no standard function/ JTAG mode strapping
182	3V3		3V3	
184	ADDRESS18	KEY_COL2		no standard function
186	ADDRESS17	KEY_ROW2		no standard function
188	ADDRESS16	KEY_ROW4		no standard function
190	SDCard CMD	SD1_CMD		
192	SDCard DAT<0>	SD1_DATA0		
194	I2C SDA	GPIO06		
196	I2C SCL	GPIO03		
198	3V3		3V3	
200	3V3		3V3	

3.2.2 HDMI FFC

This connector is compatible with the Colibri T20 and T30 but not backward compatible with the Colibri PXAxxx family or the Colibri VFxx. Its purpose is to provide the signals for the HDMI/DVI display interface.

Table 3-2 X2 Connector

X2 Pin	Compatible Function	i.MX 6 Ball	Non i.MX 6 Ball	Note
1	GND (Shield)		GND	
2	TMDS_CLK_P	HDMI_TX_CLK_P		
3	TMDS_CLK_N	HDMI_TX_CLK_N		
4	GND		GND	
5	TMDS_DATA0_P	HDMI_TX_DATA0_P		
	TMDS_DATA0_N	HDMI_TX_DATA0_N		
7	GND		GND	
8	TMDS_DATA1_P	HDMI_TX_DATA1_P		
9	TMDS_DATA1_N	HDMI_TX_DATA1_N		
10	GND		GND	
11	TMDS_DATA2_P	HDMI_TX_DATA2_P		
12	TMDS_DATA2_N	HDMI_TX_DATA2_N		
13	3V3_DDC_OUT		3V3 Switched	
14	HOTPLUG_DETECT	HDMI_TX_HPD		Level shifter on module, 5V tolerant
15	DDC_SCL	KEY_COL3		Level shifter on module, 5V tolerant
16	DDC_SDA	KEY_ROW3		Level shifter on module, 5V tolerant
17	GND		GND	
18	VGA_RED			Not connected
19	GND		GND	
20	VGA_GREEN			Not connected
21	GND		GND	
22	VGA_BLUE			Not connected
23	VGA_VSYNC			Not connected
24	VGA_HSYNC			Not connected

4. I/O Pins

4.1 Function Multiplexing

The Freescale i.MX6 SoC I/O pins can be configured for any of up to nine alternate functions. Most of the pins can also be used as "normal" GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). For example, the i.MX6 signal pin on the SODIMM pin 33 has the primary function UART1_TX_DATA (Colibri standard function UART_A_RXD), but can also provide the following alternate functions: GPIO5_IO28 (GPIO), IPU1_CSI0_DATA10 (serial camera input), AUD3_RXC (digital audio interface), or ECSPI2_MISO (SPI interface).

The default setting for this pin is the primary function uart1.UART1_TX_DATA. It is strongly recommended to, whenever possible, use the primary interfaces before any alternate interfaces. This ensures the best compatibility with Toradex standard software and operating systems/BSPs and with the other modules in the Colibri family.

Most of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behaviour.

In the table in chapter 4.4 you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

Some of the i.MX6 pins are paired and share the same SODIMM pin. When using one of these pins, make sure that the unused pin the pair is tri-stated or configurator as input to avoid undesired behaviour and/or hardware damage. The following table list all SODIMM pins that have more than one i.MX6 pin connected:

Table 4-1 Multiplexed pins

X1 Pin #	i.MX 6 Pin 1	i.MX 6 Pin 2	Remarks
59	SD4_DATA1	EIM_ADDR22	
67	GPIO01	EIM_ADDR21	
93	SD2_CLK	EIM_RW	GMI_WR_N is connected via a 3-State buffer with SD2_CLK. To tri-state the buffer set RGMII_TD3 (GPIO6_IO23) to high. (default state). For more information see Figure 4
99	SD2_DATA3	EIM_RW	GMI_WR_N is connected via a 3-State buffer with SD2_DATA3. To tri-state the buffer set RGMII_TD2 (GPIO6_IO22) to high. (default state). For more information see Figure 4.
137	GPIO17	USB_OTG_VBUS	SODIMM pin 137 is connected via a 3-State buffer and a level shifter to the USB_OTG_VGUS input of the i.MX 6. For more information see Figure 5. Using this pin as GPIO requires additional software modifications. Therefore, it is preferable to us other GPIO capable pins instead.
180	GPIO02	JTAG_MOD	JTAG mode strapping is sampled during test reset. For more information see section 5.28

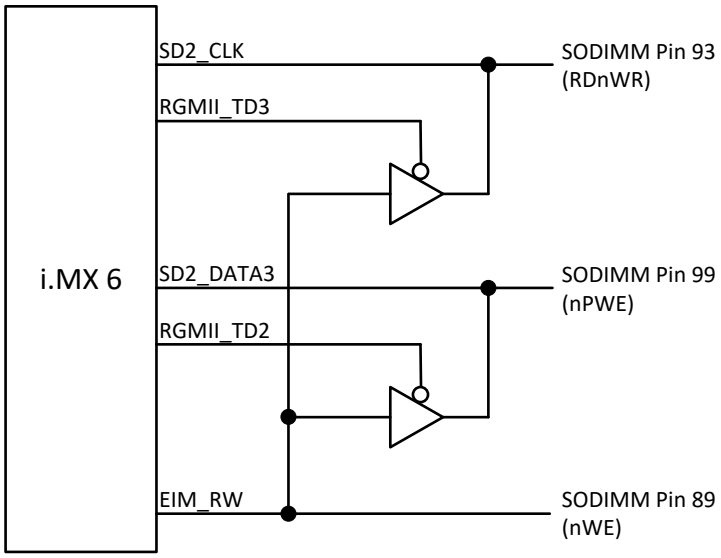

Figure 4: nWE output circuit

The output of the 3-State buffer is enabled if the buffer control input is 0. The output is tri-stated when the control is 1.

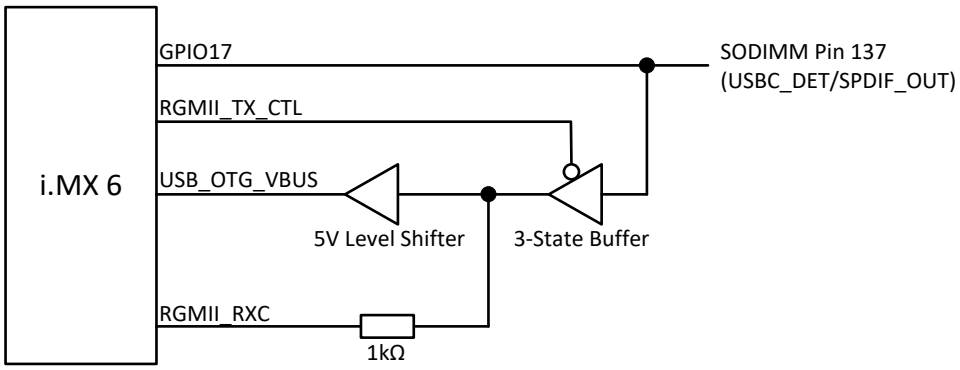

Figure 5: USBC_DET/SPDIF_OUT circuit

If the 3-State buffer is disabled by setting the RGMII_TX_CTL (GPIO6_IO26) pin high, the RGMII_RXC (GPIO6_IO30) can be used for overwriting the USB_OTG_VBUS.

4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC_SW_MUX_CTL_PAD_x where x is the name of the i.MX6 pin. More information about the available register settings can be found in the i.MX6 Reference Manual.

Table 4-2 Pad Mux Registor

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port 111 Select mux mode: ALT7 mux port:	Check chapter 4.4 for the available alternate function of the pin

The pins have an additional register which allows configuration of pull up/down resistors, drive strength and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x where x is the name of the i.MX6 pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX6 Reference Manual.

Table 4-3 Pad Control Registor

Bit	Field	Description	Remarks
31-17	Reserved		
16	HYS	0 CMOS input 1 Schmitt trigger input	
15-14	PUS	00 100 kOhm Pull Down 01 47 kOhm Pull Up 10 100 kOhm Pull Up 11 22 kOhm Pull Up	
13	PUE	0 Keeper enable 1 Pull enable	Selection between keeper and pull up/down function
12	PKE	0 Pull/Keeper Disabled 1 Pull/Keeper Enabled	Enable keeper or pull up/down function
11	ODE	0 Output is CMOS 1 Output is open drain	
10-8	Reserved		
7-6	SPEED	00 Reserved 01 Low (50 MHz) 10 Medium (100 MHz) 11 High (200 MHz)	
5-3	DSE	000 output driver disabled (Hi Z) 001 240 Ohm 010 120 Ohm 011 80 Ohm 100 60 Ohm 101 48 Ohm 110 40 Ohm 111 34 Ohm	If possible decrease the drive strength by increasing the resistance in order to reduce EMC problems
2-1	Reserved		
0	SRE	0 Slow Slew Rate 1 Fast Slew Rate	Use slow slew rate if possible for reducing EMC problems

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x _SELECT_INPUT where x is the name of the input function. More information about this register can be found in the i.MX6 Reference Manual.

4.3 Pin Reset State

After a reset, the pins can be in different modes. Most of them are configured as GPIO input with a 100k pull up resistor enabled. Please check the i.MX6 Reference Manual for the corresponding default configuration state. As soon as the bootloader is executing, it is possible to reconfigure the pins and their states.

Please be aware, the pin reset status is only guaranteed during the release of the reset signal. During the power up sequence the states of the pins might be undefined until the IO bank voltage is enabled on the module.

4.4 Functions List

Below is a list of all the i.MX6 pins which are available on the SODIMM connector. It shows the alternate functions that are available for each pin. The GPIO functionality is always defined as the ALT5 function. The alternate functions which are used to provide the primary interfaces to ensure best compatibility with other Colibri modules are highlighted.

Function Short Forms

AUD:	Synchronous Serial Interface for Audio (I2S and AC97)
CCM:	Clock Control Module
CE-ATA:	Consumer Electronics-Advanced Technology Attachment, specification for attaching mass storage drives over the MMC-interface
CSI:	Camera Sensor Interface
ECSPI:	Enhanced Configurable Serial Peripheral Interface Bus
EIM:	External Interface Module (External Memory Bus)
eMMC:	*Embedded MultiMediaCard, device down memory chip that uses the MMC interface*
ESAI:	Enhanced Serial Audio Interface
FLEXCAN:	Flexible Controller Area Network
GPIO:	General Purpose Input Output
HDMI:	High Definition Multimedia Interface
I2C:	Inter Integrated Circuit
IPU:	Image Processing Units
MIPI/CSI:	Mobile Industry Processor Interface / Camera Serial Interface
MMC:	MultiMediaCard
NAND:	Interface for NAND Flash
PWM:	Pulse Width Modulation output
SD:	Secure Digital Memory Card (related to SDHC, MMC, CE-ATA, eMMC)
SDHC:	Secure Digital High Capacity (SD cards with capacity from 4 to 32 GB)
SPDIF:	S/PDIF (Sony-Philips Digital Interface I/O)
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus

4.4.1 SODIMM 200

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8*	ALT9*	Reset State
19	SD4_CMD	SD4_CMD	NAND_RE_B	UART3_TX_DATA[1)]			GPIO7_IO09					ALT5
21	SD4_CLK	SD4_CLK	NAND_WE_B	UART3_RX_DATA[1)]			GPIO7_IO10					ALT5
23	EIM_DATA24	EIM_DATA24	ECSPI4_SS2	UART3_TX_DATA	ECSPI1_SS2	ECSPI2_SS2	GPIO3_IO24	AUD5_RXFS	UART1_DTR_B	EPDC_SDCE7		ALT5
25	EIM_DATA19	EIM_DATA19	ECSPI1_SS1	IPU1_DI0_PIN08	IPU1_CSI1_DATA16	UART1_CTS_B	GPIO3_IO19	EPIT1_OUT		EPDC_DATA12		ALT5
27	EIM_DATA20	EIM_DATA20	ECSPI4_SS0	IPU1_DI0_PIN16	IPU1_CSI1_DATA15	UART1_RTS_B	GPIO3_IO20	EPIT2_OUT				ALT5
29	EIM_DATA25	EIM_DATA25	ECSPI4_SS3	UART3_RX_DATA	ECSPI1_SS3	ECSPI2_SS3	GPIO3_IO25	AUD5_RXC	UART1_DSR_B	EPDC_SDCE8		ALT5
31	EIM_DATA23	EIM_DATA23	IPU1_DI0_D0_CS	UART3_CTS_B	UART1_DCD_B	IPU1_CSI1_DATA_EN	GPIO3_IO23	IPU1_DI1_PIN02	IPU1_DI1_PIN14	EPDC_DATA11		ALT5
33	CSI0_DATA10	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	UART1_TX_DATA[1)]		GPIO5_IO28		ARM_TRACE07			ALT5
35	CSI0_DATA11	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	UART1_RX_DATA[1)]		GPIO5_IO29		ARM_TRACE08			ALT5
37	NAND_DATA07	NAND_DATA07	SD2_DATA7				GPIO2_IO07					ALT5
43	NAND_DATA05	NAND_DATA05	SD2_DATA5				GPIO2_IO05					ALT5
45	EIM_ADDR16	EIM_ADDR16	IPU1_DI1_DISP_CLK	IPU1_CSI1_PIXCLK			GPIO2_IO22		SRC_BOOT_CFG16	EPDC_DATA00		ALT0
47	SD1_CLK	SD1_CLK			GPT_CLKIN		GPIO1_IO20					ALT5
49	SD1_DATA1	SD1_DATA1		PWM3_OUT	GPT_CAPTURE2		GPIO1_IO17					ALT5
51	SD1_DATA2	SD1_DATA2		GPT_COMPARE2	PWM2_OUT	WDOG1_B	GPIO1_IO19	WDOG1_RESET_B_DEB				ALT5
53	SD1_DATA3	SD1_DATA3		GPT_COMPARE3	PWM1_OUT	WDOG2_B	GPIO1_IO21	WDOG2_RESET_B_DEB				ALT5
55	GPIO07	ESAI_TX4_RX1		EPIT1_OUT	FLEXCAN1_TX	UART2_TX_DATA	GPIO1_IO07	SPDIF_LOCK	USB_OTG_HOST_MODE	I2C4_SCL		ALT5
57	DISP0_DATA16	IPU1_DISP0_DATA16	LCD_DATA16	ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_EVENT0	GPIO5_IO10					ALT5
59	SD4_DATA1		SD4_DATA1	PWM3_OUT			GPIO2_IO09					ALT5
	EIM_ADDR22	EIM_ADDR22	IPU1_DISP1_DATA17	IPU1_CSI1_DATA17			GPIO2_IO16		SRC_BOOT_CFG22	EPDC_GDSP		ALT0
61	DISP0_DATA17	IPU1_DISP0_DATA17	LCD_DATA17	ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11					ALT5
63	GPIO08	ESAI_TX5_RX0	XTALOSC_REF_CLK_32K	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	USB_OTG_PWR_CTL_WAKE	I2C4_SDA		ALT5
65	EIM_ADDR24	EIM_ADDR24	IPU1_DISP1_DATA19	IPU1_CSI1_DATA19		IPU1_SISG2	GPIO5_IO04		SRC_BOOT_CFG24	EPDC_GDRL		ALT0
67	GPIO01	ESAI_RX_CLK	WDOG2_B	KEY_ROW5	USB_OTG_ID	PWM2_OUT	GPIO1_IO01	SD1_CD_B				ALT5
	EIM_ADDR21	EIM_ADDR21	IPU1_DISP1_DATA16	IPU1_CSI1_DATA16			GPIO2_IO17		SRC_BOOT_CFG21	EPDC_GDCLK		ALT0
69	SD2_CMD	SD2_CMD		KEY_ROW5	AUD4_RXC		GPIO1_IO11					ALT5
71	EIM_DATA26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01	IPU1_CSI1_DATA14	UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22	EPDC_SDOED		ALT5
73	EIM_DATA27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00	IPU1_CSI1_DATA13	UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23	EPDC_SDOE		ALT5
75	NAND_CS2_B	NAND_CE2_B	IPU1_SISG0	ESAI_TX0	EIM_CRE	CCM_CLKO2	GPIO6_IO15					ALT5
77	EIM_DATA18	EIM_DATA18	ECSPI1_MOSI	IPU1_DI0_PIN07	IPU1_CSI1_DATA17	IPU1_DI1_D0_CS	GPIO3_IO18	I2C3_SDA		EPDC_VCOM1		ALT5
79	EIM_ADDR19	EIM_ADDR19	IPU1_DISP1_DATA14	IPU1_CSI1_DATA14			GPIO2_IO19		SRC_BOOT_CFG19	EPDC_PWR_CTRL1		ALT0
81	EIM_DATA29	EIM_DATA29	IPU1_DI1_PIN15	ECSPI4_SS0		UART2_RTS_B	GPIO3_IO29	IPU1_CSI1_VSYNC	IPU1_DI0_PIN14	EPDC_PWR_WAKE		ALT5
85	EIM_ADDR23	EIM_ADDR23	IPU1_DISP1_DATA18	IPU1_CSI1_DATA18		IPU1_SISG3	GPIO6_IO06		SRC_BOOT_CFG23	EPDC_GDOE		ALT0
89	EIM_RW	EIM_RW	IPU1_DI1_PIN08	ECSPI2_SS0			GPIO2_IO26		SRC_BOOT_CFG29	EPDC_DATA07		ALT0
91	EIM_OE	EIM_OE	IPU1_DI1_PIN07	ECSPI2_MISO			GPIO2_IO25			EPDC_PWR_IRQ		ALT0

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8*	ALT9*	Reset State
93	SD2_CLK	SD2_CLK		KEY_COL5	AUD4_RXFS		GPIO1_IO10					ALT5
95	EIM_WAIT	EIM_WAIT	EIM_DTACK_B				GPIO5_IO00		SRC_BOOT_CFG25			ALT0
97	EIM_ADDR20	EIM_ADDR20	IPU1_DISP1_DATA15	IPU1_CSI1_DATA15			GPIO2_IO18		SRC_BOOT_CFG20	EPDC_PWR_CTRL2		ALT0
99	SD2_DATA3	SD2_DATA3		KEY_COL6	AUD4_TXC		GPIO1_IO12					ALT5
101	EIM_ADDR17	EIM_ADDR17	IPU1_DISP1_DATA12	IPU1_CSI1_DATA12			GPIO2_IO21		SRC_BOOT_CFG17	EPDC_PWR_STAT		ALT0
103	EIM_ADDR18	EIM_ADDR18	IPU1_DISP1_DATA13	IPU1_CSI1_DATA13			GPIO2_IO20		SRC_BOOT_CFG18	EPDC_PWR_CTRL0		ALT0
105	EIM_CS0	EIM_CS0	IPU1_DI1_PIN05	ECSPI2_SCLK			GPIO2_IO23			EPDC_DATA06		ALT0
107	EIM_CS1	EIM_CS1	IPU1_DI1_PIN06	ECSPI2_MOSI			GPIO2_IO24			EPDC_DATA08		ALT0
111	EIM_AD00	EIM_AD00	IPU1_DISP1_DATA09	IPU1_CSI1_DATA09			GPIO3_IO00		SRC_BOOT_CFG00	EPDC_SDCLK_N		ALT0
113	EIM_AD01	EIM_AD01	IPU1_DISP1_DATA08	IPU1_CSI1_DATA08			GPIO3_IO01		SRC_BOOT_CFG01	EPDC_SDLE		ALT0
115	EIM_AD02	EIM_AD02	IPU1_DISP1_DATA07	IPU1_CSI1_DATA07			GPIO3_IO02		SRC_BOOT_CFG02	EPDC_BDR0		ALT0
117	EIM_AD03	EIM_AD03	IPU1_DISP1_DATA06	IPU1_CSI1_DATA06			GPIO3_IO03		SRC_BOOT_CFG03	EPDC_BDR1		ALT0
119	EIM_AD04	EIM_AD04	IPU1_DISP1_DATA05	IPU1_CSI1_DATA05			GPIO3_IO04		SRC_BOOT_CFG04	EPDC_SDCE0		ALT0
121	EIM_AD05	EIM_AD05	IPU1_DISP1_DATA04	IPU1_CSI1_DATA04			GPIO3_IO05		SRC_BOOT_CFG05	EPDC_SDCE1		ALT0
123	EIM_AD06	EIM_AD06	IPU1_DISP1_DATA03	IPU1_CSI1_DATA03			GPIO3_IO06		SRC_BOOT_CFG06	EPDC_SDCE2		ALT0
125	EIM_AD07	EIM_AD07	IPU1_DISP1_DATA02	IPU1_CSI1_DATA02			GPIO3_IO07		SRC_BOOT_CFG07	EPDC_SDCE3		ALT0
127	NAND_DATA06	NAND_DATA06	SD2_DATA6				GPIO2_IO06					ALT5
129	EIM_DATA31	EIM_DATA31	IPU1_DISP1_DATA20	IPU1_DI0_PIN12	IPU1_CSI0_DATA02	UART3_RTS_B	GPIO3_IO31	USB_H1_PWR		EPDC_SDCLK_P	EIM_ACLK_FREERUN	ALT5
131	EIM_DATA30	EIM_DATA30	IPU1_DISP1_DATA21	IPU1_DI0_PIN11	IPU1_CSI0_DATA03	UART3_CTS_B	GPIO3_IO30	USB_H1_OC		EPDC_SDOEZ		ALT5
133	NAND_DATA03	NAND_DATA03	SD1_DATA7				GPIO2_IO03					ALT5
135	NAND_DATA02	NAND_DATA02	SD1_DATA6				GPIO2_IO02					ALT5
137	GPIO17	ESAI_TX0	ENET_1588_EVENT3_IN	CCM_PMIC_READY	SDMA_EXT_EVENT0	SPDIF_OUT	GPIO7_IO12					ALT5
139	USB_H1_DP											
141	USB_H1_DN											
143	USB_OTG_DP											
145	USB_OTG_DN											
149	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	EIM_DATA00				GPIO5_IO20		ARM_TRACE_CLK			ALT5
151	CSI0_VSYNC	IPU1_CSI0_VSYNC	EIM_DATA01				GPIO5_IO21		ARM_TRACE00			ALT5
153	CSI0_DATA04	IPU1_CSI0_DATA04	EIM_DATA02	ECSPI1_SCLK	KEY_COL5	AUD3_TXC	GPIO5_IO22		ARM_TRACE01			ALT5
155	CSI0_DATA05	IPU1_CSI0_DATA05	EIM_DATA03	ECSPI1_MOSI	KEY_ROW5	AUD3_TXD	GPIO5_IO23		ARM_TRACE02			ALT5
157	CSI0_DATA06	IPU1_CSI0_DATA06	EIM_DATA04	ECSPI1_MISO	KEY_COL6	AUD3_TXFS	GPIO5_IO24		ARM_TRACE03			ALT5
159	CSI0_DATA07	IPU1_CSI0_DATA07	EIM_DATA05	ECSPI1_SS0	KEY_ROW6	AUD3_RXD	GPIO5_IO25		ARM_TRACE04			ALT5
161	CSI0_DATA08	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	I2C1_SDA	GPIO5_IO26		ARM_TRACE05			ALT5
163	CSI0_DATA09	IPU1_CSI0_DATA09	EIM_DATA07	ECSPI2_MOSI	KEY_ROW7	I2C1_SCL	GPIO5_IO27		ARM_TRACE06			ALT5
165	CSI0_DATA12	IPU1_CSI0_DATA12	EIM_DATA08		UART4_TX_DATA		GPIO5_IO30		ARM_TRACE09			ALT5
167	CSI0_DATA13	IPU1_CSI0_DATA13	EIM_DATA09		UART4_RX_DATA		GPIO5_IO31		ARM_TRACE10			ALT5
169	CSI0_DATA14	IPU1_CSI0_DATA14	EIM_DATA10		UART5_TX_DATA		GPIO6_IO00		ARM_TRACE11			ALT5
171	CSI0_DATA15	IPU1_CSI0_DATA15	EIM_DATA11		UART5_RX_DATA		GPIO6_IO01		ARM_TRACE12			ALT5
173	CSI0_DATA16	IPU1_CSI0_DATA16	EIM_DATA12		UART4_RTS_B		GPIO6_IO02		ARM_TRACE13			ALT5
175	CSI0_DATA17	IPU1_CSI0_DATA17	EIM_DATA13		UART4_CTS_B		GPIO6_IO03		ARM_TRACE14			ALT5

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8*	ALT9*	Reset State
177	CSI0_DATA18	IPU1_CSI0_DATA18	EIM_DATA14		UART5_RTS_B		GPIO6_IO04		ARM_TRACE15			ALT5
179	CSI0_DATA19	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		GPIO6_IO05					ALT5
22	ENET_REF_CLK		ENET_TX_CLK	ESAI_RX_FS			GPIO1_IO23	SPDIF_SR_CLK				ALT5
24	DI0_PIN04	IPU1_DI0_PIN04	LCD_BUSY	AUD6_RXD	SD1_WP		GPIO4_IO20			LCD_RESET		ALT5
28	GPIO09	ESAI_RX_FS	WDOG1_B	KEY_COL6	CCM_REF_EN_B	PWM1_OUT	GPIO1_IO09	SD1_WP				ALT5
30	SD4_DATA2		SD4_DATA2	PWM4_OUT			GPIO2_IO10					ALT5
32	SD4_DATA6		SD4_DATA6	UART2_CTS_B			GPIO2_IO14					ALT5
34	SD4_DATA5		SD4_DATA5	UART2_RTS_B			GPIO2_IO13					ALT5
36	SD4_DATA7		SD4_DATA7	UART2_TX_DATA[1)]			GPIO2_IO15					ALT5
38	SD4_DATA4		SD4_DATA4	UART2_RX_DATA[1)]			GPIO2_IO12					ALT5
44	DI0_PIN15	IPU1_DI0_PIN15	LCD_ENABLE	AUD6_TXC			GPIO4_IO17			LCD_RD_E		ALT5
46	DISP0_DATA07	IPU1_DISP0_DATA 07	LCD_DATA07	ECSPI3_RDY			GPIO4_IO28					ALT5
48	DISP0_DATA09	IPU1_DISP0_DATA 09	LCD_DATA09	PWM2_OUT	WDOG2_B		GPIO4_IO30					ALT5
50	DISP0_DATA11	IPU1_DISP0_DATA 11	LCD_DATA11				GPIO5_IO05					ALT5
52	DISP0_DATA12	IPU1_DISP0_DATA 12	LCD_DATA12				GPIO5_IO06					ALT5
54	DISP0_DATA13	IPU1_DISP0_DATA 13	LCD_DATA13		AUD5_RXFS		GPIO5_IO07					ALT5
56	DI0_DISP_CLK	IPU1_DI0_DISP_CL K	LCD_CLK				GPIO4_IO16			LCD_WR_RWN		ALT5
58	DISP0_DATA03	IPU1_DISP0_DATA 03	LCD_DATA03	ECSPI3_SS0			GPIO4_IO24					ALT5
60	DISP0_DATA02	IPU1_DISP0_DATA 02	LCD_DATA02	ECSPI3_MISO			GPIO4_IO23					ALT5
62	DISP0_DATA08	IPU1_DISP0_DATA 08	LCD_DATA08	PWM1_OUT	WDOG1_B		GPIO4_IO29					ALT5
64	DISP0_DATA15	IPU1_DISP0_DATA 15	LCD_DATA15	ECSPI1_SS1	ECSPI2_SS1		GPIO5_IO09					ALT5
66	DISP0_DATA14	IPU1_DISP0_DATA 14	LCD_DATA14		AUD5_RXC		GPIO5_IO08					ALT5
68	DI0_PIN02	IPU1_DI0_PIN02	LCD_HSYNC	AUD6_TXD			GPIO4_IO18			LCD_RS		ALT5
70	DISP0_DATA01	IPU1_DISP0_DATA 01	LCD_DATA01	ECSPI3_MOSI			GPIO4_IO22					ALT5
72	DISP0_DATA05	IPU1_DISP0_DATA 05	LCD_DATA05	ECSPI3_SS2	AUD6_RXFS		GPIO4_IO26					ALT5
74	DISP0_DATA10	IPU1_DISP0_DATA 10	LCD_DATA10				GPIO4_IO31					ALT5
76	DISP0_DATA00	IPU1_DISP0_DATA 00	LCD_DATA00	ECSPI3_SCLK			GPIO4_IO21					ALT5
78	DISP0_DATA04	IPU1_DISP0_DATA 04	LCD_DATA04	ECSPI3_SS1			GPIO4_IO25					ALT5
80	DISP0_DATA06	IPU1_DISP0_DATA 06	LCD_DATA06	ECSPI3_SS3	AUD6_RXC		GPIO4_IO27					ALT5
82	DI0_PIN03	IPU1_DI0_PIN03	LCD_VSYNC	AUD6_TXFS			GPIO4_IO19			LCD_CS		ALT5
86	EIM_ADDR25	EIM_ADDR25	ECSPI4_SS1	ECSPI2_RDY	IPU1_DI1_PIN12	IPU1_DI0_D1_CS	GPIO5_IO02	HDMI_TX_CEC_LI NE		EPDC_DATA15	EIM_ACLK_FREER UN	ALT0
88	EIM_DATA21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU1_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN			ALT5
90	EIM_DATA22	EIM_DATA22	ECSPI4_MISO	IPU1_DI0_PIN01	IPU1_CSI1_DATA10	USB_OTG_PWR	GPIO3_IO22	SPDIF_OUT		EPDC_SDCE6		ALT5
92	EIM_DATA28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI	IPU1_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13	EPDC_PWR_CTRL 3		ALT5
94	EIM_EB3	EIM_EB3	ECSPI4_RDY	UART3_RTS_B	UART1_RI_B	IPU1_CSI1_HSYNC	GPIO2_IO31	IPU1_DI1_PIN03	SRC_BOOT_CFG3 1	EPDC_SDCE0	EIM_ACLK_FREER UN	ALT5
96	EIM_DATA17	EIM_DATA17	ECSPI1_MISO	IPU1_DI0_PIN06	IPU1_CSI1_PIXCLK	DCIC1_OUT	GPIO3_IO17	I2C3_SCL		EPDC_VCOM0		ALT5
98	SD2_DATA0	SD2_DATA0			AUD4_RXD	KEY_ROW7	GPIO1_IO15	DCIC2_OUT				ALT5

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8*	ALT9*	Reset State
100	SD4_DATA3		SD4_DATA3				GPIO2_IO11					ALT5
102	NAND_DATA04	NAND_DATA04	SD2_DATA4				GPIO2_IO04					ALT5
104	SD4_DATA0		SD4_DATA0	NAND_DQS			GPIO2_IO08					ALT5
106	SD2_DATA1	SD2_DATA1		EIM_CS2	AUD4_TXFS	KEY_COL7	GPIO1_IO14					ALT5
110	EIM_AD08	EIM_AD08	IPU1_DISP1_DATA01	IPU1_CSI1_DATA01			GPIO3_IO08		SRC_BOOT_CFG08	EPDC_SDCE4		ALT0
112	EIM_AD09	EIM_AD09	IPU1_DISP1_DATA00	IPU1_CSI1_DATA00			GPIO3_IO09		SRC_BOOT_CFG09	EPDC_SDCE5		ALT0
114	EIM_AD10	EIM_AD10	IPU1_DI1_PIN15	IPU1_CSI1_DATA_EN			GPIO3_IO10		SRC_BOOT_CFG10	EPDC_DATA01		ALT0
116	EIM_AD11	EIM_AD11	IPU1_DI1_PIN02	IPU1_CSI1_HSYNC			GPIO3_IO11		SRC_BOOT_CFG11	EPDC_DATA03		ALT0
118	EIM_AD12	EIM_AD12	IPU1_DI1_PIN03	IPU1_CSI1_VSYNC			GPIO3_IO12		SRC_BOOT_CFG12	EPDC_DATA02		ALT0
120	EIM_AD13	EIM_AD13	IPU1_DI1_D0_CS				GPIO3_IO13		SRC_BOOT_CFG13	EPDC_DATA13		ALT0
122	EIM_AD14	EIM_AD14	IPU1_DI1_D1_CS				GPIO3_IO14		SRC_BOOT_CFG14	EPDC_DATA14		ALT0
124	EIM_AD15	EIM_AD15	IPU1_DI1_PIN01	IPU1_DI1_PIN04			GPIO3_IO15		SRC_BOOT_CFG15	EPDC_DATA09		ALT0
126	EIM_EB0	EIM_EB0	IPU1_DISP1_DATA11	IPU1_CSI1_DATA11		CCM_PMIC_READY	GPIO2_IO28		SRC_BOOT_CFG27	EPDC_PWR_COM		ALT0
128	EIM_EB1	EIM_EB1	IPU1_DISP1_DATA10	IPU1_CSI1_DATA10			GPIO2_IO29		SRC_BOOT_CFG28	EPDC_SDSHR		ALT0
130	SD2_DATA2	SD2_DATA2		EIM_CS3	AUD4_TXD	KEY_ROW6	GPIO1_IO13					ALT5
132	NAND_DATA00	NAND_DATA00	SD1_DATA4				GPIO2_IO00					ALT5
134	NAND_DATA01	NAND_DATA01	SD1_DATA5				GPIO2_IO01					ALT5
136	DISP0_DATA18	IPU1_DISP0_DATA18	LCD_DATA18	ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2			ALT5
138	DISP0_DATA19	IPU1_DISP0_DATA19	LCD_DATA19	ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3			ALT5
140	DISP0_DATA20	IPU1_DISP0_DATA20	LCD_DATA20	ECSPI1_SCLK	AUD4_TXC		GPIO5_IO14					ALT5
142	DISP0_DATA21	IPU1_DISP0_DATA21	LCD_DATA21	ECSPI1_MOSI	AUD4_TXD		GPIO5_IO15					ALT5
144	DISP0_DATA22	IPU1_DISP0_DATA22	LCD_DATA22	ECSPI1_MISO	AUD4_TXFS		GPIO5_IO16					ALT5
146	DISP0_DATA23	IPU1_DISP0_DATA23	LCD_DATA23	ECSPI1_SS0	AUD4_RXD		GPIO5_IO17					ALT5
150	EIM_LBA	EIM_LBA	IPU1_DI1_PIN17	ECSPI2_SS1			GPIO2_IO27		SRC_BOOT_CFG26	EPDC_DATA04		ALT0
152	EIM_BCLK	EIM_BCLK	IPU1_DI1_PIN16				GPIO6_IO31			EPDC_SDCE9		ALT0
154	NAND_CS3_B	NAND_CE3_B	IPU1_SISG1	ESAI_TX1	EIM_ADDR26		GPIO6_IO16				I2C4_SDA	ALT5
156	NAND_CS1_B	NAND_CE1_B	SD4_VSELECT	SD3_VSELECT			GPIO6_IO14					ALT5
158	NAND_READY	NAND_READY					GPIO6_IO10					ALT5
160	NAND_ALE	NAND_ALE	SD4_RESET				GPIO6_IO08					ALT5
162	NAND_WP_B	NAND_WP_B					GPIO6_IO09				I2C4_SCL	ALT5
164	NAND_CS0_B	NAND_CE0_B					GPIO6_IO11					ALT5
166	NAND_CLE	NAND_CLE					GPIO6_IO07					ALT5
168	GPIO19	KEY_COL5	ENET_1588_EVENT0_OUT	SPDIF_OUT	CCM_CLKO1	ECSPI1_RDY	GPIO4_IO05	ENET_TX_ER				ALT5
170	CSI0_HSYNC	IPU1_CSI0_HSYNC			CCM_CLKO1		GPIO5_IO19		ARM_TRACE_CTL			ALT5
172	CSI0_PIXCLK	IPU1_CSI0_PIXCLK					GPIO5_IO18		ARM_EVENTO			ALT5
174	GPIO04	ESAI_TX_HF_CLK		KEY_COL7			GPIO1_IO04	SD2_CD_B				ALT5
176	GPIO05	ESAI_TX2_RX3		KEY_ROW7	CCM_CLKO1		GPIO1_IO05	I2C3_SCL	ARM_EVENTI			ALT5
178	KEY_COL4	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	GPIO4_IO14					ALT5

X1 Pin	i.MX6 Ball Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8*	ALT9*	Reset State
180	GPIO02	ESAI_TX_FS		KEY_ROW6			GPIO1_IO02	SD2_WP	MLB_DATA			ALT5
	JTAG_MOD											
184	KEY_COL2	ECSPI1_SS1	ENET_RX_DATA2	FLEXCAN1_TX	KEY_COL2	ENET_MDC	GPIO4_IO10	USB_H1_PWR_CTL_WAKE				ALT5
186	KEY_ROW2	ECSPI1_SS2	ENET_TX_DATA2	FLEXCAN1_RX	KEY_ROW2	SD2_VSELECT	GPIO4_IO11	HDMI_TX_CEC_LINE				ALT5
188	KEY_ROW4	FLEXCAN2_RX	IPU1_SISG5	USB_OTG_PWR	KEY_ROW4	UART5_CTS_B	GPIO4_IO15					ALT5
190	SD1_CMD	SD1_CMD		PWM4_OUT	GPT_COMPARE1		GPIO1_IO18					ALT5
192	SD1_DATA0	SD1_DATA0			GPT_CAPTURE1		GPIO1_IO16					ALT5
194	GPIO06	ESAI_TX_CLK		I2C3_SDA			GPIO1_IO06	SD2_LCTL	MLB_SIG			ALT5
196	GPIO03	ESAI_RX_HF_CLK		I2C3_SCL	XTALOSC_REF_CLK_24M	CCM_CLKO2	GPIO1_IO03	USB_H1_OC	MLB_CLK			ALT5

*Alternate function ALT8 and ALT9 are only available on the Solo and DualLite variant of the i.MX 6.

1) UART is configured in DTE mode. The function name is according the DCE mode. Therefore names for RX and TX are swapped (see section 5.11)

5. Interface Description

5.1 Power Signals

5.1.1 Digital Supply

Table 5-1 Digital Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
42, 84,108, 148,182,198, 200	3V3	I	3.3V main power supply	Use decoupling capacitors on all pins.
39, 41, 83, 109,147, 181, 197, 199	GND	I	Digital Ground	
40	VCC_BATT	I	RTC Power supply can be connected to a backup battery.	Connect this pin to 3.3V even if the internal RTC is not used.

5.1.2 Analogue Supply

Table 5-2 Analogue Supply Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
10, 12	AVDD_AUDIO	I	3.3V Analogue supply	Connect this pin **to a 3.3V supply**. For better Audio accuracy we recommend filtering this supply separately from the digital supply. This pin is only connected to the Audio Codec. If audio is not used, connect these pins to the 3V3 input supply.
9, 11	VSS_AUDIO	I	Analogue Ground	Connect this pin to GND. For better Audio accuracy we recommend filtering this supply separate from the digital supply. Internally this pin is connected with Digital GND on the Colibri iMX6.

5.1.3 Power Management Signals

Table 5-3 Power Management Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Remarks
26	nRESET_EXT	I	Reset Input	This pin is active low and resets the Colibri module. There is a 100k Ohm pull-up on this pin.
87	nRESET_OUT	O	Reset Output	This pin is active low. This pin is driven low at boot up. This signal is a push/pull output.

On the Colibri iMX6 V1.0, the nRESET_OUT (pin 87) is a buffered output of the PMIC reset output (RESETBMCU). Since the PMIC reset output cannot be triggered by a software initiated reset cycle, the circuit has been updated on module version 1.1 (see also Colibri iMX6 errata document). An additional transistor circuit allows driving the external nRESET_OUT signal low by driving high the RGMII_RD1 pin of the SoC (GPIO6_IO27). The circuit is compatible with older software versions which leave the RGMII_RD1 pin unused.

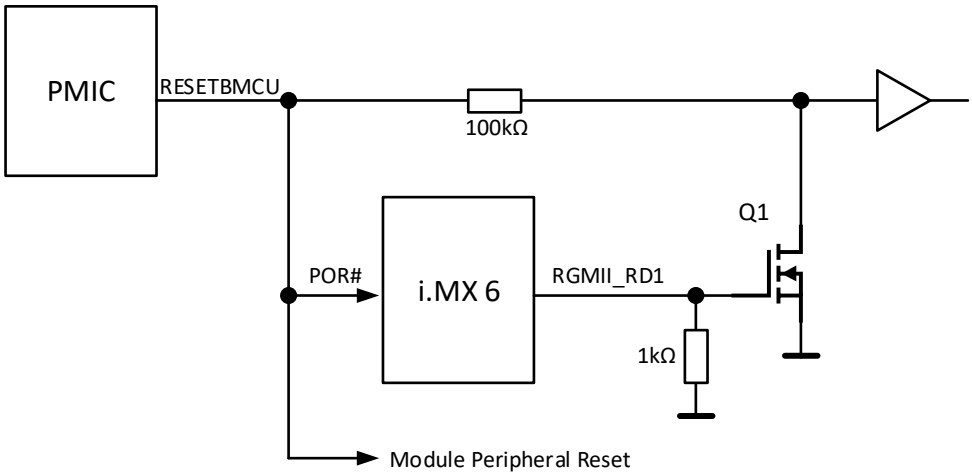

Figure 6: nRESET_OUT circuit

5.2 GPIOs

Most of the pins have a GPIO (General Purpose Input/Output) function. The GPIO functionality is configured by selecting the alternate function ALT5. All GPIO pins can be used as interrupt source.

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Colibri module from a suspend state. In the Colibri module standard, Pin 43 (WAKEUP Source<0>) and 45 (WAKEUP Source<1>) are the default wakeup source.

The touch pen down interrupt signal from the touch controller is connected to the GPIO6_IO20 (RGMII_TD0 ball) and can therefore also be used to wake up the system.

5.3 Ethernet

The Colibri iMX6 features a 10/100 Mbit/s Ethernet interface. The MAC is integrated in the i.MX 6 SoC and connected to a separate PHY located on the module, therefore only the magnetics are required on the carrier board. The Micrel KSZ8041 Fast Ethernet Transceiver chip is connected via RMII to the Freescale i.MX 6.

The Fast Ethernet MAC in the SoC features an accurate IEEE 1588 compliant timer for clock synchronisation commonly used in industrial automation applications.

Table 5-4 Ethernet Pins

X1 Pin#	Colibri Signal Name	PHY Signal Name	I/O	Description
189	TXO+	TX+	O	100BASE-TX: Transmit + (Auto MDIX: Receive +)
187	TXO-	TX-	O	100BASE-TX: Transmit - (Auto MDIX: Receive -)
195	RXI+	RX+	I	100BASE-TX: Receive + (Auto MDIX: Transmit +)
193	RXI-	RX-	I	100BASE-TX: Receive - (Auto MDIX: Transmit -)
191	AGND_LAN	GND		Ethernet ground, on VFxx connected to common GND
183	LINK_AKT	LED0	O	Link activity indication LED
185	SPEED100	LED1	O	100Mbit/s indication LED

5.4 USB

The Colibri iMX6 provides two USB 2.0 High Speed (480 Mbit/s) ports. One of the two ports (USBC) can be configured as host or client through firmware interfaces. The port cannot be used as a true OTG controller. The USBC controller is also used for the serial loader mode (recovery mode). For more information, see chapter 6.

5.4.1 USB Data Signal

Table 5-5 USB Data Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	I/O	Description
139	USBH_P	USB_H1_DP	I/O	Positive Differential Signal for USB Host port
141	USBH_N	USB_H1_DN	I/O	Negative Differential Signal for USB Host port
143	USBC_P	USB_OTG_DP	I/O	Positive Differential Signal for the shared USB Host / Client port
145	USBC_N	USB_OTG_DN	I/O	Negative Differential Signal for the shared USB Host / Client port

5.4.2 USB Control Signals

Table 5-6 USB OTG Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	I/O	Description
135	USB_ID	NAND_DATA02	I	Use this pin to detect the ID pin if you use USB OTG jack. This is not a dedicated function, it provides the function only as GPIO
137	USBC_DET	USB_OTG_VBUS/ GPIO17	I	Use this pin to detect if VBUS is present (5V USB supply). Please note that this pin is only 3.3V tolerant This signal is connected to two pins of the i.MX 6 SoC. For more information about the configuration, see section 4.1.

If you use the USB Host function you need to generate the 5V USB supply voltage on your carrier board. The Colibri iMX6 provides two optional signals for USB power supply control. We recommend using the following pins to ensure best possible compatibility, however, use of these signals is not mandatory and other GPIOs may be used instead. The USB OTG jack features an ID pin which allows detecting whether a type A or type B plug is plugged in. The Colibri iMX6 module does not support true OTG, but the interface can be configured as host or client.

Table 5-7 USB Power Control Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	I/O	Description
129	USBH_PEN	EIM_DATA31	O	This pin enables the external USB voltage supply.
131	USBH_OC	EIM_DATA30	I	USB overcurrent, this pin can Signal an over current condition in the USB supply

5.5 Display

The Colibri iMX6 features one Image Processing Unit (IPU). The unit provides camera and display connectivity and related processing synchronization and control. The output of the IPU can be routed individually to each of the display output interfaces such as the two parallel LCD and HDMI. The IPU has 2 display ports (not to be confused with the DisplayPort standard). This means up to two external display output ports can be active at any given time.

Features of the Video Graphics Sub System include:
- Video Processing Unit (multi-standard video encoder/decoder)
- OpenGL ES 2.0
- 3D GPU
- 2D GPU
- OpenVG acceleration
- Fully programmable display timing and resolution

5.5.1 Parallel RGB LCD interface

The Colibri iMX6 provides up to two parallel LCD interfaces on the SODIMM connector. They support up to 24-bit colour per pixel. One of the two 24bit parallel interfaces is provided as a standard interface which is compatible with the entire Colibri family. The 24bit colour mapping is different from other Colibri modules, and therefore only the 18bit mode is ensured to be compatible with the other modules. The second parallel RGB interface is available as an alternate function.

Features
- Up to WUXGA (1920x1200) resolution
- Up to 24-bit colour
- Supports parallel TTL displays and smart displays
- Max pixel clock 165MHz

Table 5-8 Standard Parallel RGB LCD Interface Pins

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	24bit RGB Interface	18bit RGB Interface	16bit RGB Interface
76	LCD RGB Data<0>	IPU1_DISP0_DATA00	O	B0	B0	B0
70	LCD RGB Data<1>	IPU1_DISP0_DATA01	O	B1	B1	B1
60	LCD RGB Data<2>	IPU1_DISP0_DATA02	O	B2	B2	B2
58	LCD RGB Data<3>	IPU1_DISP0_DATA03	O	B3	B3	B3
78	LCD RGB Data<4>	IPU1_DISP0_DATA04	O	B4	B4	B4
72	LCD RGB Data<5>	IPU1_DISP0_DATA05	O	B5	B5	G0
80	LCD RGB Data<6>	IPU1_DISP0_DATA06	O	B6	G0	G1
46	LCD RGB Data<7>	IPU1_DISP0_DATA07	O	B7	G1	G2
62	LCD RGB Data<8>	IPU1_DISP0_DATA08	O	G0	G2	G3
48	LCD RGB Data<9>	IPU1_DISP0_DATA09	O	G1	G3	G4
74	LCD RGB Data<10>	IPU1_DISP0_DATA10	O	G2	G4	G5
50	LCD RGB Data<11>	IPU1_DISP0_DATA11	O	G3	G5	R0
52	LCD RGB Data<12>	IPU1_DISP0_DATA12	O	G4	R0	R1
54	LCD RGB Data<13>	IPU1_DISP0_DATA13	O	G5	R1	R2
66	LCD RGB Data<14>	IPU1_DISP0_DATA14	O	G6	R2	R3
64	LCD RGB Data<15>	IPU1_DISP0_DATA15	O	G7	R3	R4
57	LCD RGB Data<16>	IPU1_DISP0_DATA16	O	R0	R4	
61	LCD RGB Data<17>	IPU1_DISP0_DATA17	O	R1	R5	
136	ADDRESS24	IPU1_DISP0_DATA18	O	R2		
138	ADDRESS23	IPU1_DISP0_DATA19	O	R3		
140	ADDRESS22	IPU1_DISP0_DATA20	O	R4		
142	ADDRESS21	IPU1_DISP0_DATA21	O	R5		
144	ADDRESS20	IPU1_DISP0_DATA22	O	R6		
146	ADDRESS19	IPU1_DISP0_DATA23	O	R7		
44	LCD RGB DE	IPU1_DI0_PIN15	O	Data Enable (other names: Output Enable, L_BIAS)		
68	LCD RGB HSYNC	IPU1_DI0_PIN02	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
82	LCD RGB VSYNC	IPU1_DI0_PIN03	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
56	LCD RGB PCLK	IPU1_DI0_DISP_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

Many applications will also require some signals to control the backlight and/or display enabling. You can use any free GPIO for these functions but we recommend using the same signals as used on our standard carrier boards to ensure minimal software configuration overhead. PWM capable signals can be used to control the backlight brightness on many display panels - see section 5.13.

A secondary LCD interface is available as alternate function. This alternate function is not compatible with other Colibri modules. Therefore, use the secondary LCD interface with caution.

Table 5-9 Additional Parallel RGB LCD Interface Pins on alternate functions

X1 Pin#	Colibri Signal Name	Vybrid Signal Name	I/O	24bit RGB Interface	18bit RGB Interface	16bit RGB Interface
112	ADDRESS9	IPU1_DISP1_DATA00	O	B0	B0	B0
110	ADDRESS8	IPU1_DISP1_DATA01	O	B1	B1	B1
125	ADDRESS7	IPU1_DISP1_DATA02	O	B2	B2	B2
123	ADDRESS6	IPU1_DISP1_DATA03	O	B3	B3	B3
121	ADDRESS5	IPU1_DISP1_DATA04	O	B4	B4	B4
119	ADDRESS4	IPU1_DISP1_DATA05	O	B5	B5	G0
117	ADDRESS3	IPU1_DISP1_DATA06	O	B6	G0	G1
115	ADDRESS2	IPU1_DISP1_DATA07	O	B7	G1	G2
113	ADDRESS1	IPU1_DISP1_DATA08	O	G0	G2	G3
111	ADDRESS0	IPU1_DISP1_DATA09	O	G1	G3	G4
128	DQM1	IPU1_DISP1_DATA10	O	G2	G4	G5
126	DQM0	IPU1_DISP1_DATA11	O	G3	G5	R0
101	Camera Input Data<2>	IPU1_DISP1_DATA12	O	G4	R0	R1
103	Camera Input Data<3>	IPU1_DISP1_DATA13	O	G5	R1	R2
79	Camera Input Data<4>	IPU1_DISP1_DATA14	O	G6	R2	R3
97	Camera Input Data<5>	IPU1_DISP1_DATA15	O	G7	R3	R4
67	PWM<D>,Camera Input Data<6>	IPU1_DISP1_DATA16	O	R0	R4	
59	PWM<A>,Camera Input Data<7>	IPU1_DISP1_DATA17	O	R1	R5	
85	Camera Input Data<8>, Keypad_Out<4>	IPU1_DISP1_DATA18	O	R2		
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	IPU1_DISP1_DATA19	O	R3		
129	USB Host Power Enable	IPU1_DISP1_DATA20	O	R4		
131	Usb Host Over-Current Detect	IPU1_DISP1_DATA21	O	R5		
71	Camera Input Data<0>,LCD Back-Light GPIO	IPU1_DISP1_DATA22	O	R6		
73		IPU1_DISP1_DATA23	O	R7		
114	ADDRESS10	IPU1_DI1_PIN15	O	Data Enable (other names: Output Enable, L_BIAS)		
116	ADDRESS11	IPU1_DI1_PIN02	O	Horizontal Sync (other names: Line Clock, L_LCKL)		
118	ADDRESS12	IPU1_DI1_PIN03	O	Vertical Sync (other names: Frame Clock, L_FCLK)		
45	WAKEUP Source<1>	IPU1_DI1_DISP_CLK	O	Pixel Clock (other names: Dot Clock, L_PCLK_WR)		

5.5.2 LVDS

Colibri iMX6 does not have a native LVDS interface. However, it is very easy to use the parallel LCD port with an LVDS transmitter. The Colibri Evaluation board provides a reference design for an LVDS interface implementation. Contact Toradex if you have any questions about how to connect a LVDS transmitter. The i.MX 6 SoC has an integrated LVDS interface, but these signals are not available on the Colibri module.

5.5.3 HDMI

HDMI provides a unified method of transferring both video and audio data over a TMDS compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI standard. The HDMI interface is available on the X2 FFC connector on the bottom of the Colibri iMX6 module. This interface is compatible with the Colibri T20 and T30 modules.

Features
- HDMI 1.4a up to 1080p60
- Pixel Clock from 13.5MHz up to 266MHz
- Supports digital sound
- High-bandwidth Content Protection (HDCP, separate license needed)
- CEC interface

Table 5-10 HDMI Interface Signals (FFC)

X2 Pin#	Colibri Signal Name	iMX6 Ball Name	I/O	Description
2	TMDS_CLK_P	HDMI_TX_CLK_P	O	HDMI Differential Clock
3	TMDS_CLK_N	HDMI_TX_CLK_N	O	
5	TMDS_DATA0_P	HDMI_TX_DATA0_P	O	HDMI Differential Data
6	TMDS_DATA0_N	HDMI_TX_DATA0_N	O	
8	TMDS_DATA1_P	HDMI_TX_DATA1_P	O	HDMI Differential Data
9	TMDS_DATA1_N	HDMI_TX_DATA1_N	O	
11	TMDS_DATA2_P	HDMI_TX_DATA2_P	O	HDMI Differential Data
12	TMDS_DATA2_N	HDMI_TX_DATA2_N	O	
14	HOTPLUG_DETECT	HDMI_TX_HPD	I	Hot Plug Detect
16	DDC_DATA	KEY_ROW3	I/O	Display Data Channel, level shifter on module, 5V tolerant
15	DDC_CLOCK	KEY_COL3	O	

Table 5-11 Additional Display Signals (SODIMM)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
186	ADDRESS17	KEY_ROW2	HDMI_TX_CEC_LINE	I/O	HDMI Consumer Electronic Control (not primary function of these pins)
86	SPI CS	EIM_ADDR25			

5.5.4 Analogue VGA

The Colibri iMX6 does not have a native Analogue VGA interface. However, it is possible to implement a VGA interface on the carrier board using a VGA DAC. The Colibri Evaluation board features a reference design for such a VGA DAC.

5.5.5 DDC (Display Data Channel)

The Colibri iMX6 provides a dedicated DDC interface for the HDMI port. These signals are located on the FFC connector on the bottom of the module. The DDC is a 5V logic level signal. A bidirectional level shifter is on the module which is 5V tolerant. A pull up resistor to the 5V supply of the DDC is required on the carrier board. If an additional DDC is required for the parallel RGB LCD interfaces, one of the I²C interfaces can be used. Please note that the other I²C interfaces have a logic level of 3.3V and will therefore require a level shifter if used for this purpose.

Table 5-12 HDMI DDC

X2 Pin#	Colibri Signal Name	iMX6 Ball Name	I/O	Description
16	DDC_DATA	KEY_ROW3	I/O	Display Data Channel, level shifter on module, 5V tolerant
15	DDC_CLOCK	KEY_COL3	O	

5.5.6 Display Serial Interface (DSI)

The Colibri iMX6 does not support the Display Serial Interface that is available on the Freescale i.MX 6 SoC.

5.6 PCI Express

The Colibri iMX6 does not support the PCI Express Interface that is available on the Freescale i.MX 6 SoC.

5.7 SATA

The Colibri iMX6 does not support the SATA Interface that is available on some of the Freescale i.MX 6 SoC variants.

5.8 IDE

The Colibri iMX6 does not support the Integrated Drive Electronics interface (IDE).

5.9 External Memory Bus

The Colibri iMX6 features an external memory bus. Freescale refers to this bus in their documentation as the "External Interface Module" EIM. No internal devices are connected to the external memory bus. Hence the memory bus configuration can be optimized for any application specific requirements without restrictions. The external memory bus is typically used to connect high speed devices like FPGAs, DSPs, secondary Ethernet controllers, CAN controllers, etc.

Features
- Non-multiplexed mode: 16-bit data bus width (compatible with other Colibri modules)
- Multiplexed mode up to 32-bit data bus width (not compatible with other Colibri modules)
- Up to 26-bit address bus width (16 bit compatible with other modules)
- Asynchronous and burst mode
- Multiplexed and de-multiplexed address/data mode
- Maximum main clock frequency of 133 MHz
- Up to four chip select signals

5.9.1 Non-Multiplexed Mode

This mode uses different pins for the address and data signals. The interface is compatible with other Colibri modules. The interface cannot be used with 32bit data bus width as the EIM_DATA16 signal is not present on the SODIMM edge connector. The following configurations can be used in the non-multiplexed mode:

Table 5-13 Non-Multiplexed Signal Mapping

Peripheral Signals	8bit		16Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 001
A[15:0]	EIM_AD[15:0]	EIM_AD[15:0]	EIM_AD[15:0]
A[25:16]	EIM_A[25:16]	EIM_A[25:16]	EIM_A[25:16]
D[7:0]	EIM_D[7:0]	EIM_D[15:8]	EIM_D[7:0]
DQM0	EIM_EB0	EIM_EB1	EIM_EB0
D[15:8]			EIM_D[15:8]
DQM1			EIM_EB1

5.9.2 Multiplexed Mode

In multiplexed mode, AD[15:0] are used for both the data and address signals. This reduces the number of signals required to connect to a device. Multiplexed mode is not compatible with the Colibri T20/T30 and Colibri PXA270 modules due to different signal mapping. The EIM_LBA signal (X1 pin 150) is used for selecting between address and data.

Table 5-14 Multiplexed Signal Mapping

Peripheral Signals (demultiplexed)	16Bit	32Bit
	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	EIM_AD[15:0]	EIM_AD[15:0]
A[25:16]	EIM_A[25:16]	EIM_D[9:0]
D[7:0]	EIM_AD[7:0]	EIM_AD[7:0]
DQM0	EIM_EB0	EIM_EB0
D[15:8]	EIM_AD[15:8]	EIM_AD[15:8]
DQM1	EIM_EB1	EIM_EB1
D[23:16]		EIM_D[7:0]
DQM2		Not available
D[31:24]		EIM_D[15:8]
DQM3		EIM_EB3

5.9.3 Memory Bus Signals

Table 5-15 Standard Memory Bus Signals (compatible with other Colibri modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
111	ADDRESS0	EIM_AD00	EIM_AD00	I/O	
113	ADDRESS1	EIM_AD01	EIM_AD01	I/O	Non-multiplexed mode: address bits 15 to 0
115	ADDRESS2	EIM_AD02	EIM_AD02	I/O	Multiplexed mode: address and data bits 15 to 0
117	ADDRESS3	EIM_AD03	EIM_AD03	I/O	

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
119	ADDRESS4	EIM_AD04	EIM_AD04	I/O	
121	ADDRESS5	EIM_AD05	EIM_AD05	I/O	
123	ADDRESS6	EIM_AD06	EIM_AD06	I/O	
125	ADDRESS7	EIM_AD07	EIM_AD07	I/O	
110	ADDRESS8	EIM_AD08	EIM_AD08	I/O	
112	ADDRESS9	EIM_AD09	EIM_AD09	I/O	
114	ADDRESS10	EIM_AD10	EIM_AD10	I/O	
116	ADDRESS11	EIM_AD11	EIM_AD11	I/O	
118	ADDRESS12	EIM_AD12	EIM_AD12	I/O	
120	ADDRESS13	EIM_AD13	EIM_AD13	I/O	
122	ADDRESS14	EIM_AD14	EIM_AD14	I/O	
124	ADDRESS15	EIM_AD15	EIM_AD15	I/O	
149	DATA0	CSI0_DATA_EN	EIM_DATA00	I/O	
151	DATA1	CSI0_VSYNC	EIM_DATA01	I/O	
153	DATA2	CSI0_DATA04	EIM_DATA02	I/O	
155	DATA3	CSI0_DATA05	EIM_DATA03	I/O	
157	DATA4	CSI0_DATA06	EIM_DATA04	I/O	
159	DATA5	CSI0_DATA07	EIM_DATA05	I/O	
161	DATA6	CSI0_DATA08	EIM_DATA06	I/O	
163	DATA7	CSI0_DATA09	EIM_DATA07	I/O	Non-multiplexed mode: data bits 15 to 0
165	DATA8	CSI0_DATA12	EIM_DATA08	I/O	Multiplexed mode: data bits 32 to 16
167	DATA9	CSI0_DATA13	EIM_DATA09	I/O	
169	DATA10	CSI0_DATA14	EIM_DATA10	I/O	
171	DATA11	CSI0_DATA15	EIM_DATA11	I/O	
173	DATA12	CSI0_DATA16	EIM_DATA12	I/O	
175	DATA13	CSI0_DATA17	EIM_DATA13	I/O	
177	DATA14	CSI0_DATA18	EIM_DATA14	I/O	
179	DATA15	CSI0_DATA19	EIM_DATA15	I/O	
91	nOE	EIM_OE	EIM_OE	O	Output Enable
89	nWE	EIM_RW	EIM_RW	O	Write Enable
93	RDnWR		EIM_RW	O	Buffered Write Enable, see section 4.1
99	nPWE		EIM_RW	O	Buffered Write Enable, see section 4.1
95	RDY	EIM_WAIT	EIM_WAIT	I	Ready/Busy/Wait signal
105	nCS0	EIM_CS0	EIM_CS0	O	
107	nCS1	EIM_CS1	EIM_CS1	O	Chip select signals
106	nCS2	SD2_DATA1	EIM_CS2	O	
126	DQM0	EIM_EB0	EIM_EB0	O	Byte Enable Mask, corresponds to D[7:0]
128	DQM1	EIM_EB1	EIM_EB1	O	Byte Enable Mask, corresponds to D[15:8]
152	DATA17	EIM_BCLK	EIM_BCLK	O	Burst Clock
150	DATA16	EIM_LBA	EIM_LBA	O	Address Valid, used for multiplexed bus only

Table 5-16 Additional Memory Bus Signals (not compatible with other Colibri modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
94	Camera Input HSYNC	EIM_EB3	EIM_EB3	O	Byte Enable Mask, corresponds to D[31:24]
136	ADDRESS24	DISP0_DATA18	EIM_CS2	O	Alternative CS2 output
130	DQM2	SD2_DATA2	EIM_CS3	O	Chip select Signal
138	ADDRESS23	DISP0_DATA19			
75	Camera Input MCLK	NAND_CS2_B	EIM_CRE	O	CRE/PS signal for CellularRam memory
95	RDY	EIM_WAIT	EIM_DTACK_B	I	Data Acknowledge, pin is shared with the Ready/Busy/Wait signal
45	WAKEUP Source<1>	EIM_ADDR16	EIM_ADDR16	O	Additional address bits 26 to 16, can be used for multiplexed and non-multiplexed mode
101	Camera Input Data<2>	EIM_ADDR17	EIM_ADDR17	O	
103	Camera Input Data<3>	EIM_ADDR18	EIM_ADDR18	O	
79	Camera Input Data<4>	EIM_ADDR19	EIM_ADDR19	O	
97	Camera Input Data<5>	EIM_ADDR20	EIM_ADDR20	O	
67	PWM<D>,Camera Input Data<6>	EIM_ADDR21	EIM_ADDR21	O	
59	PWM<A>,Camera Input Data<7>	EIM_ADDR22	EIM_ADDR22	O	
85	Camera Input Data<8>, Keypad_Out<4>	EIM_ADDR23	EIM_ADDR23	O	
65	Camera Input Data<9>, Keypad_Out<3>, PS2 SDA2	EIM_ADDR24	EIM_ADDR24	O	
86	SPI CS	EIM_ADDR25	EIM_ADDR25	O	
154	DATA18	NAND_CS3_B	EIM_ADDR26	O	

5.10 I²C

The Freescale i.MX 6 SoC provides up to four I²C controllers and an additional DDC controller. They implement the I²C V2.1 specification. All can be used in master or slave mode. The port I2C2 is used for power management and is not available externally. Port I2C3 is available as standard I²C on the module connector. Port I2C1 is only available as alternate function. The fourth port I2C4 is only available on the Solo and DualLite variant of the i.MX 6 and only as an alternate function.

The HDMI DDC controller is a dedicated I²C controller. It is intended to be used for the DDC or EDID interface. It cannot be used as a general purpose I²C interface. The pins are located on the X2 FFC connector on the bottom of the Colibri iMX6 module.

Features:
- Supports 100kbit/s and fast mode 400kbit/s data transfer
- Multimaster operation
- Software-selectable acknowledge bit
- Interrupt driven, byte-by-byte data transfer
- Start and stop signal generation and detection
- Repeated start signal generation
- Acknowledge bit generation and detection
- Bus-busy detection
- Calling address identification interrupts
- Master supports clock stretching by the slave

There are a lot of low speed devices which use I²C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB Bus devices.

Table 5-17 I²C Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
194	I2C SDA	GPIO06	I2C3_SDA	I/O	Open Drain Data Signal Port 3
196	I2C SCL	GPIO03	I2C3_SCL	I/O	Clock Signal Port 3

Table 5-18 HDMI DDC Signals (FFC)

X2 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
16	DDC_DATA	KEY_ROW3	HDMI_TX_DDC_SDA	I/O	Display Data Channel, level shifter on module, 5V tolerant
15	DDC_CLOCK	KEY_COL3	HDMI_TX_DDC_SCL	O	

Table 5-19 Alternate I²C Signals (additional, not compatible with other Colibri family modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
92	SPI TXD	EIM_DATA28	I2C1_SDA	I/O	Open Drain Data Signal Port 1
161	DATA6	CSI0_DATA08			
88	SPI CLK	EIM_DATA21	I2C1_SCL	I/O	Clock Signal Port 1
163	DATA7	CSI0_DATA09			
77		EIM_DATA18	I2C3_SDA	I/O	Alternate Open Drain Data Signal Port 3
176	DATA29	GPIO05	I2C3_SCL	I/O	Alternate Clock Signal Port 3
96	Camera Input PCLK	EIM_DATA17			
63	PS2 SCL1	GPIO08	I2C4_SDA	I/O	Open Drain Data Signal Port 4
154	DATA18	NAND_CS3_B			
55	PS2 SDA1	GPIO07	I2C4_SCL	I/O	Clock Signal Port 4
162	DATA22	NAND_WP_B			

5.10.1 Real-Time Clock (RTC) recommendation

The Colibri iMX6 module features a RTC circuit which is located inside the SoC. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for time keeping. The RTC is sourced from the VCC_BATT (pin 40) supply pin.

The RTC on the module is not designed for ultra-low power consumption (typical current consumption can be found in section 8.2). Therefore, a standard lithium coin cell battery can be drain faster than required for certain designs. If a rechargeable RTC battery is not a solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I2C1 interface of the module and source the VCC_BACKUP pin from the 3.3V rail that sources also the main module rail. A suitable reference schematic can be found in the schematic diagram of the Colibri evaluation board.

5.11 UART

The Colibri iMX6 provides up to five serial UART interfaces. Three of them are available on dedicated UART pins which are compatible with other Colibri modules. The fourth and fifth UARTs are only available as an alternate function. These UARTs are not compatible with other Colibri modules. Therefore, the fourth and fifth UART should only be used if compatibility with other Colibri modules is not required.

The i.MX 6 UART1 (defined as Colibri UART_A interface) is the only full featured UART and is used as standard debug interface for the Toradex Embedded Linux and Windows Embedded Compact operating systems. It is recommended that at least the RXD and TXD lines of this port are kept accessible for system debugging.

The ring indicator (RI) of UART_A is not available at its dedicated pin 37. This signal is only available as an alternate function. If this signal is required and compatibility with the Colibri family is mandatory, then it needs to be emulated by using the GPIO located at SODIMM pin 37.
The UARTs of the i.MX 6 can be configured either in DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Colibri family, the UARTs need to be configured in DTE mode.

Particular attention should be paid to the names of the i.MX 6 data signals. In DTE mode, the UARTx_RX_DATA port is transmitting data from the SoC while the UARTx_TX_DATA port is receiving

it. Therefore, the RX and TX signals need to be swapped. In the following signal descriptions, the port direction is always described for DTE mode.

UART Features
- High-speed TIA/EIA-232F compatible (up to 5 Mbit/s)
- IrDA-compatible (up to 115.2kbit/s
- 7 or 8 data bits (9 bit for RS485)
- 1 or 2 stop bits
- Optional parity bit (even or odd)
- Hardware flow control
- Auto detect baud rate
- 32 entries FIFO for receive and transmit

Table 5-20 UART_A Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
33	UART_A RXD	CSI0_DATA10	UART1_TX_DATA	I	Received Data
35	UART_A TXD	CSI0_DATA11	UART1_RX_DATA	O	Transmitted
27	UART_A RTS	EIM_DATA20	UART1_RTS_B	O	Request to Send
25	UART_A CTS, Keypad_In<0>	EIM_DATA19	UART1_CTS_B	I	Clear to Send
23	UART_A DTR	EIM_DATA24	UART1_DTR_B	O	Data Terminal Ready
29	UART_A DSR	EIM_DATA25	UART1_DSR_B	I	Data Set Ready
31	UART_A DCD	EIM_DATA23	UART1_DCD_B	I	Data Carrier Detect
37	UART_A RI, Keypad_In<4>	NAND_DATA07	GPIO2_IO07	I	Ring Indicator, GPIO only, RI need to be emulated

Table 5-21 UART_B Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
36	UART_B RXD	SD4_DATA7	UART2_TX_DATA	I	Received Data
38	UART_B TXD	SD4_DATA4	UART2_RX_DATA	O	Transmitted Data
34	UART_B RTS	SD4_DATA5	UART2_RTS_B	O	Request to Send
32	UART_B CTS	SD4_DATA6	UART2_CTS_B	I	Clear to Send

Table 5-22 UART_C Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
19	UART_C RXD	SD4_CMD	UART3_TX_DATA	I	Received Data
21	UART_C TXD	SD4_CLK	UART3_RX_DATA	O	Transmitted Data

Table 5-23 Signal Pins of additional UART Ports

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
165	DATA8	CSI0_DATA12	UART4_TX_DATA	I	Received Data
167	DATA9	CSI0_DATA13	UART4_RX_DATA	O	Transmitted Data
173	DATA12	CSI0_DATA16	UART4_RTS_B	O	Request to Send
175	DATA13	CSI0_DATA17	UART4_CTS_B	I	Clear to Send
169	DATA10	CSI0_DATA14	UART5_TX_DATA	I	Received Data
171	DATA11	CSI0_DATA15	UART5_RX_DATA	O	Transmitted Data
177	DATA14	CSI0_DATA18	UART5_RTS_B	O	Request to Send
179	DATA15	CSI0_DATA19	UART5_CTS_B	I	Clear to Send

These UART ports are only available as alternate functions. Compatibility with other Colibri modules cannot be guaranteed, as they are not standard Colibri module interfaces.

Table 5-24 Alternate UART Signals (additional, not compatible with other Colibri family modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
94	Camera Input HSYNC	EIM_EB3	UART1_RI_B	I	Ring Indicator
55	PS2 SDA1	GPIO07	UART2_TX_DATA	I	Alternate Received Data
71	Camera Input Data<0>,LCD Back-Light GPIO	EIM_DATA26			
63	PS2 SCL1	GPIO08	UART2_RX_DATA	O	Alternate Transmitted Data
73		EIM_DATA27			
81	Camera Input VSYNC	EIM_DATA29	UART2_RTS_B	O	Alternate Request to Send
92	SPI TXD	EIM_DATA28	UART2_CTS_B	I	Clear to Send
23	UART_A DTR	EIM_DATA24	UART3_TX_DATA	I	Alternate Received Data
29	UART_A DSR	EIM_DATA25	UART3_RX_DATA	O	Alternate Transmitted Data
94	Camera Input HSYNC	EIM_EB3	UART3_RTS_B	O	Alternate Request to Send
129	USB Host Power Enable	EIM_DATA31			
31	UART_A DCD	EIM_DATA23	UART3_CTS_B	I	Clear to Send
131	USB Host Over-Current Detect	EIM_DATA30			

5.12 SPI

The i.MX 6 Solo and DualLite provide 4 SPI controllers (in the reference manual called Enhanced Configurable SPI, ECSPI) all of which are available on the module edge connector. One SPI interface is available as standard Colibri module interface. This interface is compatible with other Colibri modules. The other SPI interfaces are available as alternate functions. These interfaces are not compatible with other Colibri modules. Please first use the standard Colibri SPI interface before using the others.

The SPI ports operate at up to 23 Mbps and provide full duplex, synchronous, serial communication between the Colibri module and internal or external peripheral devices. Each SPI port consists of

four signals; clock, chip select (frame), data in and data out. There are additional chip select signals available as alternate functions to support multiple peripherals.

Features:
- Up to 23 Mbps
- 32bit x 64 deep FIFO (RX and TX)
- Master/Slave configurable
- Simultaneous receive and transmit
- Low power mode

Each SPI channel supports four different modes of the SPI protocol:

Table 5-25 SPI Modes

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	Clock is positive polarity and the data is latched on the positive edge of SCK
1	0	1	Clock is positive polarity and the data is latched on the negative edge of SCK
2	1	0	Clock is negative polarity and the data is latched on the positive edge of SCK
4	1	1	Clock is negative polarity and the data is latched on the negative edge of SCK

SPI can be used as a fast interface for ADCs, DACs, FPGAs, etc. Some LCD displays require configuration over SPI prior to being driven via the RGB or LVDS interface.

Pay attention to the data direction of the signals in master respectively slave mode. The following table describes the data direction of the signals at the module side.

Table 5-26 SPI Signal Direction in Master and Slave Mode

iMX6 Port Name	Master Mode		Slave Mode	
	I/O	Description	I/O	Description
ECSPIx_MOSI	O	Master Output, Slave Input	I	Master Output, Slave Input
ECSPIx_MISO	I	Master Input, Slave Output	O	Master Input, Slave Output
ECSPIx_SS0	O	Slave Select	I	Slave Select
ECSPIx_SCLK	O	Serial Clock	I	Serial Clock

In the Colibri module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-27 SPI Signals (Colibri family compatible interface)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
92	SPI TXD	EIM_DATA28	ECSPI4_MOSI	O	Master Output, Slave Input
90	SPI RXD	EIM_DATA22	ECSPI4_MISO	I	Master Input, Slave Output
86	SPI CS	EIM_ADDR25	ECSPI4_SS1	O	Slave Select
88	SPI CLK	EIM_DATA21	ECSPI4_SCLK	O	Serial Clock

Table 5-28 SPI Signals (additional, not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
27	UART_A RTS	EIM_DATA20	ECSPI4_SS0	O	Slave Select 0
81	Camera Input VSYNC	EIM_DATA29			
23	UART_A DTR	EIM_DATA24	ECSPI4_SS2	O	Slave Select 2
29	UART_A DSR	EIM_DATA25	ECSPI4_SS3	O	Slave Select 3
94	Camera Input HSYNC	EIM_EB3	ECSPI4_RDY	I	Data ready signal
142	ADDRESS21	DISP0_DATA21	ECSPI1_MOSI	O	Master Output, Slave Input
155	DATA3	CSI0_DATA05			
77	0	EIM_DATA18			
144	ADDRESS20	DISP0_DATA22	ECSPI1_MISO	I	Master Input, Slave Output
157	DATA4	CSI0_DATA06			
96	Camera Input PCLK	EIM_DATA17			
146	ADDRESS19	DISP0_DATA23	ECSPI1_SS0	O	Slave Select 0
159	DATA5	CSI0_DATA07			
184	ADDRESS18	KEY_COL2	ECSPI1_SS1	O	Slave Select 1
25	UART_A CTS, Keypad_In<0>	EIM_DATA19			
64	LCD RGB Data<15>	DISP0_DATA15			
186	ADDRESS17	KEY_ROW2	ECSPI1_SS2	O	Slave Select 2
23	UART_A DTR	EIM_DATA24			
29	UART_A DSR	EIM_DATA25	ECSPI1_SS3	O	Slave Select 3
140	ADDRESS22	DISP0_DATA20	ECSPI1_SCLK	O	Serial Clock
153	DATA2	CSI0_DATA04			
168	DATA25	GPIO19	ECSPI1_RDY	I	Data ready signal
107	nCS1	EIM_CS1	ECSPI2_MOSI	O	Master Output, Slave Input
57	LCD RGB Data<16>	DISP0_DATA16			
163	DATA7	CSI0_DATA09			
91	nOE	EIM_OE	ECSPI2_MISO	I	Master Input, Slave Output
61	LCD RGB Data<17>	DISP0_DATA17			
33	UART_A RXD	CSI0_DATA10			
89	nWE	EIM_RW	ECSPI2_SS0	O	Slave Select 0
136	ADDRESS24	DISP0_DATA18			
35	UART_A TXD	CSI0_DATA11			
150	DATA16	EIM_LBA	ECSPI2_SS1	O	Slave Select 1
64	LCD RGB Data<15>	DISP0_DATA15			
23	UART_A DTR	EIM_DATA24	ECSPI2_SS2	O	Slave Select 2
29	UART_A DSR	EIM_DATA25	ECSPI2_SS3	O	Slave Select 3
105	nCS0	EIM_CS0	ECSPI2_SCLK	O	Serial Clock
138	ADDRESS23	DISP0_DATA19			

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
161	DATA6	CSI0_DATA08			
86	SPI CS	EIM_ADDR25	ECSPI2_RDY	I	Data ready signal
70	LCD RGB Data<1>	DISP0_DATA01	ECSPI3_MOSI	O	Master Output, Slave Input
60	LCD RGB Data<2>	DISP0_DATA02	ECSPI3_MISO	I	Master Input, Slave Output
58	LCD RGB Data<3>	DISP0_DATA03	ECSPI3_SS0	O	Slave Select 0
78	LCD RGB Data<4>	DISP0_DATA04	ECSPI3_SS1	O	Slave Select 1
72	LCD RGB Data<5>	DISP0_DATA05	ECSPI3_SS2	O	Slave Select 2
80	LCD RGB Data<6>	DISP0_DATA06	ECSPI3_SS3	O	Slave Select 3
76	LCD RGB Data<0>	DISP0_DATA00	ECSPI3_SCLK	O	Serial Clock
46	LCD RGB Data<7>	DISP0_DATA07	ECSPI3_RDY	I	Data ready signal

5.13 PWM (Pulse Width Modulation)

The Colibri iMX6 features a four channel Pulse Width Modulator (PWM). Each PWM channel features a 16-bit up-counter with clock source selection. There is a 16bit 4 level deep FIFO available in order to minimize the interrupt overhead. There is a 12-bit prescaler available for dividing the clock.

The PWM interface can be used as an easy way to emulate a DAC and generate a variable DC voltage if used with a suitable RC circuit. Other uses include control of LED brightness, display backlights or servo motors.

Table 5-29 PWM Interface Signals

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Remarks
28	PWM<B>	GPIO09	PWM1_OUT	O	PWM Output 1
67	PWM<D>,Camera Input Data<6>	GPIO01	PWM2_OUT	O	PWM Output 2
59	PWM<A>,Camera Input Data<7>	SD4_DATA1	PWM3_OUT	O	PWM Output 3
30	PWM<C>	SD4_DATA2	PWM4_OUT	O	PWM Output 4

Table 5-30 Alternate Locations of PWM Interface Signals (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Remarks
53	SDCard DAT<3>	SD1_DATA3	PWM1_OUT	O	Alternate PWM Output 1
62	LCD RGB Data<8>	DISP0_DATA08			
51	SDCard DAT<2>	SD1_DATA2	PWM2_OUT	O	Alternate PWM Output 2
48	LCD RGB Data<9>	DISP0_DATA09			
49	SDCard DAT<1>	SD1_DATA1	PWM3_OUT	O	Alternate PWM Output 3
190	SDCard CMD	SD1_CMD	PWM4_OUT	O	Alternate PWM Output 4

5.14 OWR (One Wire)

The Colibri iMX6 does not feature a One Wire interface.

5.15 SD/MMC

The i.MX 6 SoC provides four SDIO interfaces; one is used internally for the eMMC Flash and the other 3 are available on the module edge connector. To ensure carrier board design compatibility with other Colibri modules, only the standard Colibri SD/MMC interface should be used. The second and third SD/MMC interfaces are available as alternate functions.

The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, CE-ATA cards and eMMC devices. The controllers can act as both master and slave simultaneously.

The Colibri iMX6 supports UHS-I which allows up to 104 Mbyte/s transfer speed on its standard SD card interface. However, UHS-I requires 1.8V IO level, which is not in the Colibri module specification. Since the 1.8V capability is not mandatory in the Colibri module specification, other modules may support only 3.3V logic level. Pay attention to the SD card signal pull-up resistors on the carrier board. If the interface is used in the 1.8V mode, it is recommended to remove the pullup resistors on the carrier board. The iMX6 features internal pull-up resistors, which can be used instead.

Buss Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MBytes/s	3.3V	Colibri Standard
High Speed	50 MHz	25 MBytes/s	3.3V	
SDR12	25 MHz	12.5 MBytes/s	1.8V	UHS-I May not be compatible with other modules
SDR25	50 MHz	25 MBytes/s	1.8V	
DDR50	50 MHz	50 MBytes/s	1.8V	
SDR50	100 MHz	50 MBytes/s	1.8V	
SDR104	208 MHz	104 MBytes/s	1.8V	

Features
- Supports SD Memory Card Specification 3.0
- Supports SDIO Card Specification Version 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, and 4.41
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TByte
- Support SPI mode
- Supports SD UHS-I mode (up to ….) with 1.8V IO voltage level (only standard SD port)

i.MX 6 SDIO interface	Max Bus Width	Description
USDHC1	4bit (8bit)	Colibri Standard SD/MMC interface, additional data bits for 8bit interface available as alternate function
USDHC2	8bit	Available as alternate function, not compatible with Colibri standard
USDHC3	8bit	Connected to internal eMMC. Not available at the module edge connector
USDHC4	8bit	Available as secondary function, not compatible with Colibri standard

Table 5-31 Colibri SD/MMC Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
190	SDCard CMD	SD1_CMD	SD1_CMD	I/O	Command
192	SDCard DAT<0>	SD1_DATA0	SD1_DATA0	I/O	Serial Data 0
49	SDCard DAT<1>	SD1_DATA1	SD1_DATA1	I/O	Serial Data 1
51	SDCard DAT<2>	SD1_DATA2	SD1_DATA2	I/O	Serial Data 2
53	SDCard DAT<3>	SD1_DATA3	SD1_DATA3	I/O	Serial Data 3
47	SDCard CLK	SD1_CLK	SD1_CLK	O	Serial Clock
43	WAKEUP Source<0>,SDCard CardDetect	NAND_DATA05	GPIO2_IO05	I	Card Detect (only GPIO)

Table 5-32 Additional SD/MMC Signals (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
132	DQM3	NAND_DATA00	SD1_DATA4	I/O	Serial Data 4 (only for 8bit MMC)
134	ADDRESS25	NAND_DATA01	SD1_DATA5	I/O	Serial Data 5 (only for 8bit MMC)
135	SPDIF_IN	NAND_DATA02	SD1_DATA6	I/O	Serial Data 6 (only for 8bit MMC)
133		NAND_DATA03	SD1_DATA7	I/O	Serial Data 7 (only for 8bit MMC)
67	PWM<D>,Camera Input Data<6>	GPIO01	SD1_CD_B	I	Dedicated Card Detect
28	PWM<B>	GPIO09	SD1_WP	I	Write Protect
24	Battery Fault Detect	DI0_PIN04			

The additional SD/MMC signals allow the SD/MMC interface to be used as an 8bit interface. The pins are not compatible with other Colibri modules, as it is not part of the Colibri module specification.

Table 5-33 Additional SD/MMC interfaces (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
69	PS2 SCL2	SD2_CMD	SD2_CMD	I/O	Command
98	Camera Input Data<1>	SD2_DATA0	SD2_DATA0	I/O	Serial Data 0
106	nCS2	SD2_DATA1	SD2_DATA1	I/O	Serial Data 1
130	DQM2	SD2_DATA2	SD2_DATA2	I/O	Serial Data 2
99	nPWE	SD2_DATA3	SD2_DATA3	I/O	Serial Data 3
102		NAND_DATA04	SD2_DATA4	I/O	Serial Data 4 (only for 8bit MMC)
43	WAKEUP Source<0>,SDCard CardDetect	NAND_DATA05	SD2_DATA5	I/O	Serial Data 5 (only for 8bit MMC)
127		NAND_DATA06	SD2_DATA6	I/O	Serial Data 6 (only for 8bit MMC)
37	UART_A RI, Keypad_In<4>	NAND_DATA07	SD2_DATA7	I/O	Serial Data 7 (only for 8bit MMC)
93	RDnWR	SD2_CLK	SD2_CLK	O	Serial Clock
174	DATA28	GPIO04	SD2_CD_B	I	Card Detect
180	DATA31	GPIO02	SD2_WP	I	Write Protect
19	UART_C RXD	SD4_CMD	SD4_CMD	I/O	Command
104		SD4_DATA0	SD4_DATA0	I/O	Serial Data 0
59	PWM<A>,Camera Input Data<7>	SD4_DATA1	SD4_DATA1	I/O	Serial Data 1
30	PWM<C>	SD4_DATA2	SD4_DATA2	I/O	Serial Data 2
100	Keypad_Out<1>	SD4_DATA3	SD4_DATA3	I/O	Serial Data 3
38	UART_B TXD	SD4_DATA4	SD4_DATA4	I/O	Serial Data 4 (only for 8bit MMC)
34	UART_B RTS	SD4_DATA5	SD4_DATA5	I/O	Serial Data 5 (only for 8bit MMC)
32	UART_B CTS	SD4_DATA6	SD4_DATA6	I/O	Serial Data 6 (only for 8bit MMC)
36	UART_B RXD	SD4_DATA7	SD4_DATA7	I/O	Serial Data 7 (only for 8bit MMC)
21	UART_C TXD	SD4_CLK	SD4_CLK	O	Serial Clock

5.16 Analogue Audio

The Colibri iMX6 offers analogue audio input and output channels. On the module, a Freescale SGTL5000 chip provides the analogue audio interface. The SGTL5000 is connected over I2S (AUD5) with the i.MX 6 SoC. Please consult the Freescale SGTL5000 datasheet for more information.

Table 5-34 Analogue Audio Interface Pins

X1 Pin #	Colibri Signal Name	I/O	Description	Pin on the SGTL5000 (20pin QFN)
1	MIC_IN	I	Microphone input	10
3	MIC_GND		Microphone pseudo-ground. Possible to connect to GND. Controlled by GPIO6_IO21 (ball RGMII_TD1)	
5	LINEIN_L	I	Left Line Input	9
7	LINEIN_R	I	Right Line Input	8
15	HEADPHONE_L	O	Headphone Left Output	4
17	HEADPHONE_R	O	Headphone Right Output	1
13	HEADPHONE_GND		Headphone pseudo-ground (do not connect to ground!)	2

5.17 Audio Codec Interface

The Colibri module does not feature an audio codec interface as standard. Nevertheless, it is possible to access the internal three synchronous serial interfaces (SSI) of the i.MX 6 SoC at the module edge connector as alternate functions. The interfaces can be used as Intel® Audio Codec '97 (also known as AC'97 or AC97) or as I2S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS). The interfaces can be used to connect an additional external audio codec that can provide up to 5.1 channel audio.

The three internal SSI controllers are connected to a digital audio multiplexer (AUDMUX). This multiplexer has four ports which are available at the X1 SODIMM connector. In total, the multiplexer has seven ports which are essentially equal. All ports can be configured as four (input synchronous to the output stream) or six wire interfaces (input and output stream with independent clocks and frame signal). The multiplexer has the full flexibility to connect any port to another (independent whether it is an internal or external port). Each host can be connected to one (point to point) or many (point to multipoint) hosts. With the TXRXEN bit, it is possible to reverse transmit and receive data lines.

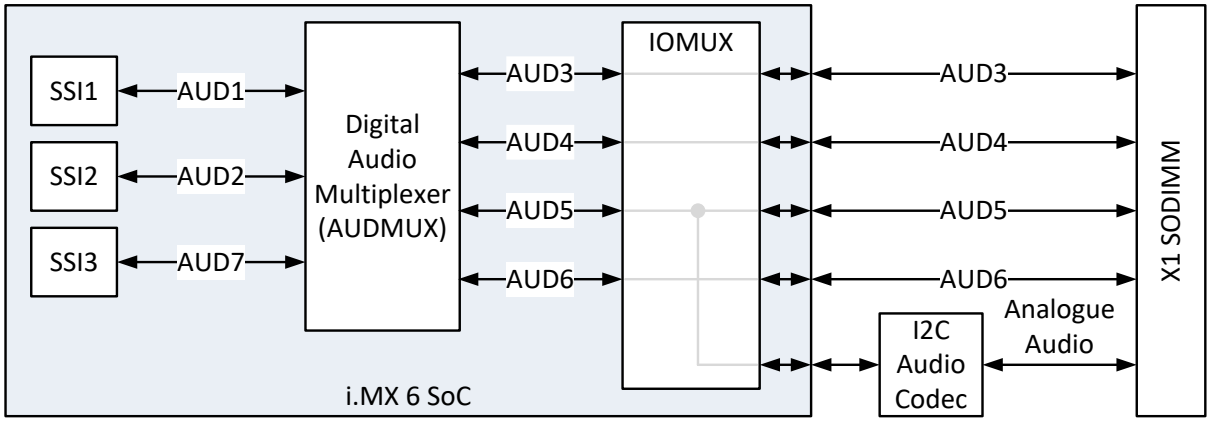

Figure 7 Audio Multiplexing

The audio codec on the module which provides the analogue audio interface is connected to the AUD5 interface of the digital audio multiplexer and is used in the I²S mode. If the analogue audio interface is in use, the external AUD5 signal pins cannot be used externally.

Table 5-35 Synchronous Serial Interface (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
159	DATA5	CSI0_DATA07	AUD3_RXD	I/O	Data Receive
35	UART_A TXD	CSI0_DATA11	AUD3_RXFS	I/O	Receive Frame Sync
33	UART_A RXD	CSI0_DATA10	AUD3_RXC	I/O	Receive Clock
155	DATA3	CSI0_DATA05	AUD3_TXD	I/O	Data Transmit
157	DATA4	CSI0_DATA06	AUD3_TXFS	I/O	Transmit Frame Sync
153	DATA2	CSI0_DATA04	AUD3_TXC	I/O	Transmit Clock
98	Camera Input Data<1>	SD2_DATA0	AUD4_RXD	I/O	Data Receive
146	ADDRESS19	DISP0_DATA23			
93	RDnWR	SD2_CLK	AUD4_RXFS	I/O	Receive Frame Sync
136	ADDRESS24	DISP0_DATA18			
69	PS2 SCL2	SD2_CMD	AUD4_RXC	I/O	Receive Clock
138	ADDRESS23	DISP0_DATA19			
130	DQM2	SD2_DATA2	AUD4_TXD	I/O	Data Transmit
142	ADDRESS21	DISP0_DATA21			
106	nCS2	SD2_DATA1	AUD4_TXFS	I/O	Transmit Frame Sync
144	ADDRESS20	DISP0_DATA22			
99	nPWE	SD2_DATA3	AUD4_TXC	I/O	Transmit Clock
140	ADDRESS22	DISP0_DATA20			
138	ADDRESS23	DISP0_DATA19	AUD5_RXD	I/O	Data Receive
23	UART_A DTR	EIM_DATA24	AUD5_RXFS	I/O	Receive Frame Sync
54	LCD RGB Data<13>	DISP0_DATA13			
29	UART_A DSR	EIM_DATA25	AUD5_RXC	I/O	Receive Clock
66	LCD RGB Data<14>	DISP0_DATA14			
61	LCD RGB Data<17>	DISP0_DATA17	AUD5_TXD	I/O	Data Transmit
136	ADDRESS24	DISP0_DATA18	AUD5_TXFS	I/O	Transmit Frame Sync
57	LCD RGB Data<16>	DISP0_DATA16	AUD5_TXC	I/O	Transmit Clock
24	Battery Fault Detect	DI0_PIN04	AUD6_RXD	I/O	Data Receive
72	LCD RGB Data<5>	DISP0_DATA05	AUD6_RXFS	I/O	Receive Frame Sync
80	LCD RGB Data<6>	DISP0_DATA06	AUD6_RXC	I/O	Receive Clock
68	LCD RGB HSYNC	DI0_PIN02	AUD6_TXD	I/O	Data Transmit
82	LCD RGB VSYNC	DI0_PIN03	AUD6_TXFS	I/O	Transmit Frame Sync
44	LCD RGB DE	DI0_PIN15	AUD6_TXC	I/O	Transmit Clock

5.17.1 Digital Audio Port used as I²S

The SSI interfaces can be used as I²S interfaces with the following features:

- PCM, Network and TDM mode Support
- Master or Slave
- 15x32 bit FIFO for Transmitter and Receiver
- Maximum audio sampling rate 196 kHz

The following signals are used for the I²S interface:

Table 5-36 Digital Audio port used as Master I²S

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_TXD	SDIN	O	Serial Data Output from i.MX 6 SoC
AUDx_RXD	SDOUT	I	Serial Data Input to i.MX 6 SoC
AUDx_TXFS	WS	O	Word Select, also known as Field Select or LRCLK
AUDx_TXC	SCK	O	Serial Continuous Clock

Table 5-37 Digital Audio port used as Slave I²S

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_RXD	SDOUT	I	Serial Data Input to i.MX 6 SoC
AUDx_TXD	SDIN	O	Serial Data Output from i.MX 6 SoC
AUDx_TXFS	WS	I	Word Select, also known as Field Select or LRCLK
AUDx_TXC	SCK	I	Serial Continuous Clock

The audio codecs often require an additional I²C interface for control and a master clock input. Any of the available I²C interfaces can be used (see section 5.10). The master clock can be provided by the clock output signal (see section 5.23). The internal audio codec uses the I2C2 port of the i.MX 6 SoC which is also used for power management purposes. The master clock is provided by the CCM_CLKO1.

5.17.2 Digital Audio Port used as AC'97

The SSI interface can be configured as an AC'97 compatible interface with a maximum frame rate of 48kHz. The AC'97 Audio interface does not require an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec does require a master reference clock, however, a separate crystal/oscillator can be used. Please take care with the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host (e.g. i.MX 6 SoC), and not to the signal direction.

Table 5-38 Digital Audio port used as AC'97

iMX6 Port Name	I²S Signal Name (Names at Codec)	I/O (at iMX6)	Description
AUDx_RXD	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 6
AUDx_TXD	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 6
AUDx_TXFS	SYNC	O	AC'97 Audio Sync
AUDx_TXC	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.18 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for communication with a variety of serial audio devices including industry-standard codecs, S/PDIF transceivers, and other DSPs. The interface is only available as an alternate function as it is not part of the Colibri module standard.

Features
- Independent (asynchronous) mode or shared (synchronous) mode of the transmitter and receiver
- Master or slave mode
- Up to 5 transmitters and up to 3 receivers at the module edge connector available
- Programmable data interface modes (I2S, LSB aligned, MSB aligned)
- Programmable word length (8, 12, 16, 20 or 24bit)
- AC97 support
- 128word FIFO shared by all transmitters
- 128word FIFO shared by all receivers

Table 5-39 ESAI Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
194	I2C SDA	GPIO06	ESAI_TX_CLK	I/O	TX serial bit clock
180	DATA31	GPIO02	ESAI_TX_FS	I/O	Frame sync for transmitters and receivers in the synchronous mode and for the transmitters only in asynchronous mode
174	DATA28	GPIO04	ESAI_TX_HF_CLK	I/O	TX high frequency clock
75	Camera Input MCLK	NAND_CS2_B	ESAI_TX0	I/O	TX data 0
137	USB Client Cable Detect,SPDIF_OUT	GPIO17			
154	DATA18	NAND_CS3_B	ESAI_TX1	I/O	TX data 1
176	DATA29	GPIO05	ESAI_TX2_RX3	I/O	TX data 2 or RX data 3
55	PS2 SDA1	GPIO07	ESAI_TX4_RX1	I/O	TX data 4 or RX data 1
63	PS2 SCL1	GPIO08	ESAI_TX5_RX0	I/O	TX data 5 or RX data 0
67	PWM<D>,Camera Input Data<6>	GPIO01	ESAI_RX_CLK	I/O	RX serial bit clock
28	PWM<B>	GPIO09	ESAI_RX_FS	I/O	RX frame sync signal in asynchronous mode
22	VDD Fault Detect	ENET_REF_CLK			
196	I2C SCL	GPIO03	ESAI_RX_HF_CLK	I/O	RX high frequency clock

5.19 S/PDIF (Sony-Philips Digital Interface I/O)

The S/PDIF interface supports both input and output of serial audio digital interface format data. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard. The S/PDIF out is available at a module edge pin that is compatible with some other Colibri modules (currently Colibri T20 and Colibri T30). The S/PDIF input signal is only available as an alternate function and not on the pin that would be compatible with other modules.

Features:
- Internal data width: 24-bit
- Left and right channel 16x24bit FIFO (receive and transmit)

Table 5-40 S/PDIF Data Pins (compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
137	USB Client Cable Detect,SPDIF_OUT	GPIO17	SPDIF_OUT	O	Serial data output

Table 5-41 Additional S/PDIF Data Pins (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
168	DATA25	GPIO19	SPDIF_OUT	O	Alternate serial data output
90	SPI RXD	EIM_DATA22			
88	SPI CLK	EIM_DATA21	SPDIF_IN	I	Serial data input

5.20 Touch Panel Interface

The Colibri iMX6 provides a 4-wire resistive touch interface using the ST Microelectronics STMPE811. It is connected with the i.MX 6 SoC via the power management I2C interface (I2C2). The STMPE811 does not support 5-wire operation mode. Please consult the ST Microelectronics STMPE811 documentation for more information.

Table 5-42 Touch Interface Pins

X1 Pin#	Colibri Signal Name	STMPE811 Pin#	STMPE811 Pin Name	I/O	Description
14	TSPX	13	X+	I/O	X+ (4-wire)
16	TSMX	16	X-	I/O	X- (4-wire)
18	TSPY	15	Y+	I/O	Y+ (4-wire)
20	TSMY	1	Y-	I/O	Y- (4-wire)

5.21 Analogue Inputs

The ST Microelectronics STMPE811 provides 4 analogue input channels. Please consult the ST Microelectronics STMPE811 documentation for more information. All channels are protected with a 47k Ohm series resistor between the module edge connector pins and the input.

Features
- 12-bit ADC
- 0 to 3.3V rail to rail

Table 5-43 Analogue Inputs Pins

X1 Pin#	Colibri Signal Name	STMPE811 Pin#	STMPE811 Pin Name	I/O	Description
8	Analogue Input <0>	8	IN0_GPIO0	I/O	ADC input 0
6	Analogue Input <1>	9	IN0_GPIO1	I/O	ADC input 1
4	Analogue Input<2>	11	IN0_GPIO2	I/O	ADC input 2
2	Analogue Input<3>	12	IN0_GPIO3	I/O	ADC input 3

5.22 Camera Interface

The i.MX 6 DualLite/Solo SoC features one Image Processing Units (IPU). The IPU can receive data from TV decoder chips, CMOS sensors, graphics accelerators, and other devices. The IPU is also responsible for sending image data to a display device (see also section 5.5).

The IPU has two camera sensor interfaces (CSI). The SoC itself features three camera input ports, two parallel and one MIPI/CSI-2. The first parallel camera port (IPU1.CSI0) is available on pins that are compatible with other Colibri modules. The second parallel camera port is only available as alternate function of other pins. The MIPI/CSI-2 port is not available at all at the module edge connector.

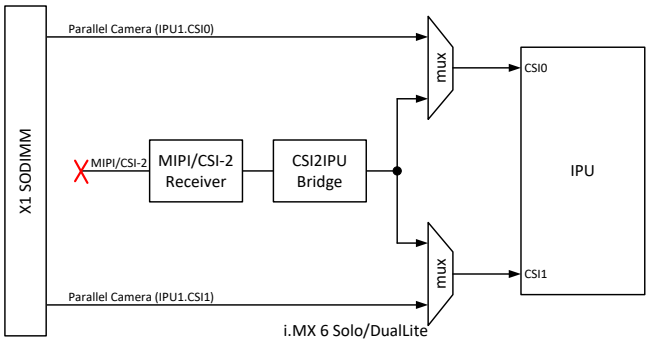

Figure 8: Camera Interface input connectivity

5.22.1 Parallel Camera Interface

The Colibri iMX6 features up to two 20 bit parallel camera interfaces. Only 8 bits of the first camera interface (IPU1.CSI0) are available on pins that are compatible with other Colibri modules. The remaining bits and the second parallel camera interface are only available as alternate functions. These pins are not guaranteed to be compatible with other Colibri modules.

Features
- Raw (Bayer), RGB, YUV input
- Frame size up to 8192x4096 pixels
- 8/16/20bit parallel video interface
- Dedicated synchronisation signals (VSYNC, HSYNC) or embedded in data stream (BT.656)

Although the location for the 8 bits of the camera interface is equal to other modules, the colour mapping might be different. Please carefully read the datasheets for the other Colibri modules for more information regarding available colour modes.

Table 5-44 Parallel Camera Interface Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
101	Camera Input Data<2>	EIM_ADDR17	IPU1_CSI1_DATA12	I	Camera pixel data
103	Camera Input Data<3>	EIM_ADDR18	IPU1_CSI1_DATA13	I	Camera pixel data
79	Camera Input Data<4>	EIM_ADDR19	IPU1_CSI1_DATA14	I	Camera pixel data
97	Camera Input Data<5>	EIM_ADDR20	IPU1_CSI1_DATA15	I	Camera pixel data
67	PWM<D>,Camera Input Data<6>	EIM_ADDR21	IPU1_CSI1_DATA16	I	Camera pixel data
59	PWM<A>,Camera Input Data<7>	EIM_ADDR22	IPU1_CSI1_DATA17	I	Camera pixel data
85	Camera Input Data<8>, Keypad_Out<4>	EIM_ADDR23	IPU1_CSI1_DATA18	I	Camera pixel data
65	Camera Input Data<9>, Keypad_Out<3>,PS2 SDA2	EIM_ADDR24	IPU1_CSI1_DATA19	I	Camera pixel data
96	Camera Input PCLK	EIM_DATA17	IPU1_CSI1_PIXCLK	I	Camera pixel clock
94	Camera Input HSYNC	EIM_EB3	IPU1_CSI1_HSYNC	I	Camera horizontal sync
81	Camera Input VSYNC	EIM_DATA29	IPU1_CSI1_VSYNC	I	Camera vertical sync
75	Camera Input MCLK	NAND_CS2_B	CCM_CLKO2	O	Camera reference clock output

The camera modules often require an additional I²C interface for control purposes. Any available I²C interface can be used (see section 5.10). The following table shows the additional signals for the IPU1_CSI1 camera interface for up to 20 bit connections. Please be aware that these signals are alternate functions and are not compatible with other modules.

Table 5-45 Additional IPU1_CS1 Signals for 20bit Interface on nonstandard Colibri Pin

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
112	ADDRESS9	EIM_AD09	IPU1_CSI1_DATA00	I	Additional camera pixel data
110	ADDRESS8	EIM_AD08	IPU1_CSI1_DATA01	I	Additional camera pixel data
125	ADDRESS7	EIM_AD07	IPU1_CSI1_DATA02	I	Additional camera pixel data
123	ADDRESS6	EIM_AD06	IPU1_CSI1_DATA03	I	Additional camera pixel data
121	ADDRESS5	EIM_AD05	IPU1_CSI1_DATA04	I	Additional camera pixel data
119	ADDRESS4	EIM_AD04	IPU1_CSI1_DATA05	I	Additional camera pixel data
117	ADDRESS3	EIM_AD03	IPU1_CSI1_DATA06	I	Additional camera pixel data
115	ADDRESS2	EIM_AD02	IPU1_CSI1_DATA07	I	Additional camera pixel data
113	ADDRESS1	EIM_AD01	IPU1_CSI1_DATA08	I	Additional camera pixel data
111	ADDRESS0	EIM_AD00	IPU1_CSI1_DATA09	I	Additional camera pixel data
128	DQM1	EIM_EB1	IPU1_CSI1_DATA10	I	Additional camera pixel data
90	SPI RXD	EIM_DATA22			
126	DQM0	EIM_EB0	IPU1_CSI1_DATA11	I	Additional camera pixel data
88	SPI CLK	EIM_DATA21			
92	SPI TXD	EIM_DATA28	IPU1_CSI1_DATA12	I	Alternative pin for camera pixel data 12
73		EIM_DATA27	IPU1_CSI1_DATA13	I	Alternative pin for camera pixel data 13
71	Camera Input Data<0>,LCD Back-Light GPIO	EIM_DATA26	IPU1_CSI1_DATA14	I	Alternative pin for camera pixel data 14
27	UART_A RTS	EIM_DATA20	IPU1_CSI1_DATA15	I	Alternative pin for camera pixel data 15
25	UART_A CTS, Keypad_In<0>	EIM_DATA19	IPU1_CSI1_DATA16	I	Alternative pin for camera pixel data 16
77		EIM_DATA18	IPU1_CSI1_DATA17	I	Alternative pin for camera pixel data 17
45	WAKEUP Source<1>	EIM_ADDR16	IPU1_CSI1_PIXCLK	I	Alternative pin for pixel clock
116	ADDRESS11	EIM_AD11	IPU1_CSI1_HSYNC	I	Alternative pin for horizontal sync
118	ADDRESS12	EIM_AD12	IPU1_CSI1_VSYNC	I	Alternative pin for vertical sync
114	ADDRESS10	EIM_AD10	IPU1_CSI1_DATA_EN	I	Pixel data enable
31	UART_A DCD	EIM_DATA23			

Table 5-46 IPU2_CS0 Signals 20bit Interface on non-standard Colibri Pin

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
71	Camera Input Data<0>,LCD Back-Light GPIO	EIM_DATA26	IPU1_CSI0_DATA01	I	Camera pixel data
73		EIM_DATA27	IPU1_CSI0_DATA00	I	Camera pixel data
129	USB Host Power Enable	EIM_DATA31	IPU1_CSI0_DATA02	I	Camera pixel data
131	Usb Host Over-Current Detect	EIM_DATA30	IPU1_CSI0_DATA03	I	Camera pixel data
153	DATA2	CSI0_DATA04	IPU1_CSI0_DATA04	I	Camera pixel data
155	DATA3	CSI0_DATA05	IPU1_CSI0_DATA05	I	Camera pixel data
157	DATA4	CSI0_DATA06	IPU1_CSI0_DATA06	I	Camera pixel data
159	DATA5	CSI0_DATA07	IPU1_CSI0_DATA07	I	Camera pixel data
161	DATA6	CSI0_DATA08	IPU1_CSI0_DATA08	I	Camera pixel data
163	DATA7	CSI0_DATA09	IPU1_CSI0_DATA09	I	Camera pixel data
33	UART_A RXD	CSI0_DATA10	IPU1_CSI0_DATA10	I	Camera pixel data
35	UART_A TXD	CSI0_DATA11	IPU1_CSI0_DATA11	I	Camera pixel data
165	DATA8	CSI0_DATA12	IPU1_CSI0_DATA12	I	Camera pixel data
167	DATA9	CSI0_DATA13	IPU1_CSI0_DATA13	I	Camera pixel data
169	DATA10	CSI0_DATA14	IPU1_CSI0_DATA14	I	Camera pixel data
171	DATA11	CSI0_DATA15	IPU1_CSI0_DATA15	I	Camera pixel data
173	DATA12	CSI0_DATA16	IPU1_CSI0_DATA16	I	Camera pixel data
175	DATA13	CSI0_DATA17	IPU1_CSI0_DATA17	I	Camera pixel data
177	DATA14	CSI0_DATA18	IPU1_CSI0_DATA18	I	Camera pixel data
179	DATA15	CSI0_DATA19	IPU1_CSI0_DATA19	I	Camera pixel data
172	DATA27	CSI0_PIXCLK	IPU1_CSI0_PIXCLK	I	Camera pixel clock
170	DATA26	CSI0_HSYNC	IPU1_CSI0_HSYNC	I	Camera horizontal sync
151	DATA1	CSI0_VSYNC	IPU1_CSI0_VSYNC	I	Camera vertical sync
149	DATA0	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	I	Pixel data enable

Table 5-47 Camera Interface Colour Pin Mapping

iMX6 Port Name	RGB565 8bit 2 cycle	RGB565 8bit 3 cycle	RGB666 8bit 3 cycle	RGB888 8bit 3 cycle	YCbCr 8bit 2 cycle	RGB565 16bit 1 cycle	YCbCr 16bit 1 cycle	YCbCr 16bit 1 cycle	YCbCr 20bit 1 cycle
IPUx_CSIx_DATA00								0	C0
IPUx_CSIx_DATA01								0	C1
IPUx_CSIx_DATA02								C0	C2
IPUx_CSIx_DATA03								C1	C3
IPUx_CSIx_DATA04						B0	C0	C2	C4
IPUx_CSIx_DATA05						B1	C1	C3	C5
IPUx_CSIx_DATA06						B2	C2	C4	C6
IPUx_CSIx_DATA07						B3	C3	C5	C7
IPUx_CSIx_DATA08						B4	C4	C6	C8
IPUx_CSIx_DATA09						G0	C5	C7	C9
IPUx_CSIx_DATA10						G1	C6	0	Y0
IPUx_CSIx_DATA11						G2	C7	0	Y1
IPUx_CSIx_DATA12	B0,G3	R2,G4,B2	R/G/B4	R/G/B0	Y/C0	G3	Y0	Y0	Y2
IPUx_CSIx_DATA13	B1,G4	R3,G5,B3	R/G/B5	R/G/B1	Y/C1	G4	Y1	Y1	Y3
IPUx_CSIx_DATA14	B2,G5	R4,G0,B4	R/G/B0	R/G/B2	Y/C2	G5	Y2	Y2	Y4
IPUx_CSIx_DATA15	B3,R0	R0,G1,B0	R/G/B1	R/G/B3	Y/C3	R0	Y3	Y3	Y5
IPUx_CSIx_DATA16	B4,R1	R1,G2,B1	R/G/B2	R/G/B4	Y/C4	R1	Y4	Y4	Y6
IPUx_CSIx_DATA17	G0,R2	R2,G3,B2	R/G/B3	R/G/B5	Y/C5	R2	Y5	Y5	Y7
IPUx_CSIx_DATA18	G1,R3	R3,G4,B3	R/G/B4	R/G/B6	Y/C6	R3	Y6	Y6	Y8
IPUx_CSIx_DATA19	G2,R4	R4,G5,B4	R/G/B5	R/G/B7	Y/C7	R4	Y7	Y7	Y9

5.22.2 Camera Serial Interface (MIPI/CSI-2)

The Colibri iMX6 does not support the MIPI/CSI-2 interface available on the i.MX 6 SoC. The associated signals are not available on the module edge connector.

5.23 Clock Output

The i.MX 6 SoC has two general purpose clock output channels (CLKO1 and CLKO2) which are available on different SoC pins. The audio codec on the module requires a reference clock which is provided by CLKO1 on the GPIO00 pin of the SoC. The CLKO1 can only be used on the module edge connector pins if the internal audio codec is not used.

The CLKO2 is provided on the module edge connector. The signal is available at the master clock output for the camera interface as well as an alternate function of the I2C CLK signal (pin 196). It is recommended that is it used on the camera interface master clock output pin to increase compatibility with other Colibri modules.

Table 5-48 Clock Output Signal Pin (compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
75	Camera Input MCLK	NAND_CS2_B	CCM_CLKO2	O	Master clock output for camera

Table 5-49 Alternate Clock Output Signal Pins (not compatible with other modules)

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
176	DATA29	GPIO05	CCM_CLKO1	O	General purpose clock output. Same clock source is also used for audio codec on module. Can only be used if audio codec is not used.
168	DATA25	GPIO19			
170	DATA26	CSI0_HSYNC			
196	I2C SCL	GPIO03	CCM_CLKO2	O	Alternate output for CLKO2

5.24 Keypad

You can use any free GPIOs to realize a matrix keypad interface. Additionally, the i.MX 6 SoC features a keyboard controller. As the keyboard controller is only available as an alternate function, this interface is not compatible with other Colibri modules and can only be used if the required pins are being used for their primary function.

The keyboard controller eliminates the requirement for de-bounce capacitors and pull up resistors. It can handle up to two buttons being pressed without the need for de-ghosting diodes. If the diodes are available, any combination of pressed keys can be detected. The row and column pins can be configured for a keyboard matrix of up to 5 by 5, as not all signals are available on the module edge connector.

Features
- Open drain design
- Glitch suppression circuit
- Multiple-key detection
- Long key-press detection
- Standby key-press detection

Table 5-50 Keyboard Matrix Interface Signals

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
186	ADDRESS17	KEY_ROW2	KEY_ROW2	I	Keyboard row 2
188	ADDRESS16	KEY_ROW4	KEY_ROW4	I	Keyboard row 4
67	PWM<D>,Camera Input Data<6>	GPIO01	KEY_ROW5	I	Keyboard row 5
69	PS2 SCL2	SD2_CMD			
155	DATA3	CSI0_DATA05			
180	DATA31	GPIO02	KEY_ROW6	I	Keyboard row 6
130	DQM2	SD2_DATA2			
159	DATA5	CSI0_DATA07			
176	DATA29	GPIO05	KEY_ROW7	I	Keyboard row 7
98	Camera Input Data<1>	SD2_DATA0			
163	DATA7	CSI0_DATA09			
184	ADDRESS18	KEY_COL2	KEY_COL2	O	Keyboard column 2
178	DATA30	KEY_COL4	KEY_COL4	O	Keyboard column 4
93	RDnWR	SD2_CLK	KEY_COL5	O	Keyboard column 5
168	DATA25	GPIO19			
153	DATA2	CSI0_DATA04			
28	PWM<B>	GPIO09	KEY_COL6	O	Keyboard column 6
99	nPWE	SD2_DATA3			
157	DATA4	CSI0_DATA06			
174	DATA28	GPIO04	KEY_COL7	O	Keyboard column 7
106	nCS2	SD2_DATA1			
161	DATA6	CSI0_DATA08			

5.25 Controller Area Network (CAN)

The Flexible Controller Area Network (FlexCAN) peripheral of the Freescale i.MX 6 SoC implements the CAN protocol according to the CAN 2.0B specification. It features a buffer for up to 64 messages and supports both standard and extended message frames. The interfaces are located as secondary functions on the SODIMM pins. The interface is therefore not compatible with all the modules in the Colibri family. If only one CAN interface is required, the interface on Pin 63/55 is preferable as it is compatible with the Colibri VFxx modules. In order to be compliant with the CAN standard, a transceiver on the carrier board is required.

Features
- Bit rate up to 1Mb/s
- Content-related addressing
- Flexible mailboxes of eight bytes data length (configurable as RX or TX)
- Powerful Rx FIFO ID filtering
- Listen-only mode
- Loop-back mode
- Time stamp based on 16bit free running timer
- Low power modes, wake up on bus activity
- Maskable interrupts

Table 5-51 CAN Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
63	PS2 SCL1	GPIO08	FLEXCAN1_RX	I	CAN receive pin, compatible with Colibri VFxx
186	ADDRESS17	KEY_ROW2			Alternate CAN receive pin
55	PS2 SDA1	GPIO07	FLEXCAN1_TX	O	CAN transmit pin, compatible with Colibri VFxx
184	ADDRESS18	KEY_COL2			Alternate CAN transmit pin
188	ADDRESS16	KEY_ROW4	FLEXCAN2_RX	I	CAN receive pin
178	DATA30	KEY_COL4	FLEXCAN2_TX	O	CAN transmit pin

5.26 NAND

The Colibri iMX6 supports the connection of up to four NAND flash devices on the carrier board. As the NAND interface is not part of the Colibri module standard, this interface is not compatible with other Colibri modules. In the Freescale documentation, the NAND interface is called General Purpose Media Interface (GPMI). It is compatible with ONFI 2.2 specifications and supports DDR mode. It is also compatible with the Samsung/Toshiba Toggle NAND protocol. It is not possible to boot from the NAND interface as the Colibri iMX6 is fused to boot from the on module eMMC.

Table 5-52 NAND Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
160	DATA21	NAND_ALE	NAND_ALE	O	Address latch enable
164	DATA23	NAND_CS0_B	NAND_CE0_B	O	Chip Enable 0
156	DATA19	NAND_CS1_B	NAND_CE1_B	O	Chip Enable 1
75	Camera Input MCLK	NAND_CS2_B	NAND_CE2_B	O	Chip Enable 2
154	DATA18	NAND_CS3_B	NAND_CE3_B	O	Chip Enable 3
166	DATA24	NAND_CLE	NAND_CLE	O	Command latch enable
132	DQM3	NAND_DATA00	NAND_DATA00	I/O	Data signal 0
134	ADDRESS25	NAND_DATA01	NAND_DATA01	I/O	Data signal 1
135	SPDIF_IN	NAND_DATA02	NAND_DATA02	I/O	Data signal 2
133		NAND_DATA03	NAND_DATA03	I/O	Data signal 3
102		NAND_DATA04	NAND_DATA04	I/O	Data signal 4
43	WAKEUP Source<0>,SDCard CardDetect	NAND_DATA05	NAND_DATA05	I/O	Data signal 5
127		NAND_DATA06	NAND_DATA06	I/O	Data signal 6
37	UART_A RI, Keypad_In<4>	NAND_DATA07	NAND_DATA07	I/O	Data signal 7
104		SD4_DATA0	NAND_DQS	I/O	Data strobe
158	DATA20	NAND_READY	NAND_READY	I/O	Ready signal
19	UART_C RXD	SD4_CMD	NAND_RE_B	O	Read enable
21	UART_C TXD	SD4_CLK	NAND_WE_B	O	Write enable
162	DATA22	NAND_WP_B	NAND_WP_B	O	Wait polarity

5.27 Media Local Bus (MLB150)

The Media Local Bus is predominantly used in automotive for high-bandwidth audio video and control information transport. MLB is a standardized on-PCB, inter-chip communication bus for MOST (Media Oriented Systems Transport) based devices. The MLB is not available for all variants of the i.MX 6 SoC. The industrial temperature (IT) graded variants do not support this interface. As MLB is not part of the Colibri module standard, the interface is not compatible with other Colibri modules. The Colibri iMX6 features only the 3-pin (single ended) interface of the MLB. The signals required for the 6-pin (differential pair) interface are not available on the module edge connector.

Table 5-53 UART1 Signal Pins

X1 Pin#	Colibri Signal Name	iMX6 Ball Name	iMX6 Port Name	I/O	Description
196	I2C SCL	GPIO03	MLB_CLK	I	Single ended clock
180	DATA31	GPIO02	MLB_DATA	I/O	Single ended data
194	I2C SDA	GPIO06	MLB_SIG	I/O	Single ended signal

5.28 JTAG

The JTAG interface is not normally required for software development with the Colibri iMX6. There is always the possibility of reprogramming the module using the Recovery Mode over USB. To flash the module in recovery mode and for debug reasons, it is strongly recommended that the USBO1 interface is accessible even if not needed in the production system. Additionally, UART1 should also be accessible.

The JTAG interface is located on test points on the bottom side of the module. The location is the same for all modules in the Colibri family. On the Evaluation Board 3.1 the signals are accessible through pogo pins. The interface voltage is 3.3V, hence jumper JP 29 must be in position 2-3.

The JTAG on the i.MX 6 knows two different modes which can be strapped by the JTAG_MODE pin. Beginning with the module version V1.1, this pin is connected to the SODIMM pin 180 together with the GPIO02 pin of the SoC. If the JTAG_MODE pin is high during JTAG reset, the mode is set to IEEE1149.1 compliant boundary scan. This is the default mode since the pin 180 features an internal pull up resistor of around 100kΩ. If the pin is strapped low, the JTAG interface can be set to a common SW debugging.

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Colibri iMX6 even if the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in the recovery mode, the USBC interface is used to connect it to a host computer. You will find additional information at our Developer Centre: http://developer.toradex.com.

In order to enter recovery mode, short circuit the recovery mode pads on the front of the module and power-up the module. Figure 8 (below) show the location of the pads that need to be shorted for entering the recovery mode. The recovery button on the Colibri Evaluation board cannot be used for entering the recovery mode. Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module will try to boot from the external SD card instead of the USB serial loader.

Figure 9 Location of recovery mode pads

7. Known Issues

Up-to-date information about all known hardware issues. can be found in the errata document which can be downloaded on our website at:
http://docs.toradex.com/103380-colibri-imx6-errata.pdf

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
Vmax_3V3	Main power supply	-0.3	3.6	V
Vmax_AVDD	Analogue power supply	-0.3	3.6	V
Vmax_VCC_BATT	RTC power supply	-0.3	3.6	V
Vmax_IO	IO pins with GPIO function	-0.5	3.6	V
Vmax_AN1	ADC and touch analogue input	-0.3	3.9	V

8.2 Electrical Characteristics

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
3V3	Main power supply	3.135	3.3	3.465	V
AVDD	Analogue power supply	3.0	3.3	3.6	V
VCC_BATT	RTC power supply	2.8	3.3	3.6	V

Table 8-3 Typical Power Consumption (Colibri iMX6DL 512MB IT)

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	245	mA
IDD_HIGHCPU	Maximal CPU Load	490	mA
IDD_HD	Full HD Video on HDMI	615	mA
IDD_SUSPEND	Module in Suspend State	37	mA
IDD_BATT	Current consumption of internal RTC	51	µA

Table 8-4 Typical Power Consumption (Colibri iMX6DL 512MB)

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	230	mA
IDD_HIGHCPU	Maximal CPU Load	535	mA
IDD_HD	Full HD Video on HDMI	750	mA
IDD_SUSPEND	Module in Suspend State	36	mA
IDD_BATT	Current consumption of internal RTC	50	µA

Table 8-5 Typical Power Consumption (Colibri iMX6S 256MB IT)

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	230	mA
IDD_HIGHCPU	Maximal CPU Load	350	mA
IDD_HD	Full HD Video on HDMI	545	mA
IDD_SUSPEND	Module in Suspend State	30	mA
IDD_BATT	Current consumption of internal RTC	50	µA

Table 8-6 Typical Power Consumption (Colibri iMX6S 256MB)I

Symbol	Description (VCC = 3.3V)	Typical	Unit
IDD_IDL	CPU Idle	220	mA
IDD_HIGHCPU	Maximal CPU Load	370	mA
IDD_HD	Full HD Video on HDMI	560	mA
IDD_SUSPEND	Module in Suspend State	25	mA
IDD_BATT	Current consumption of internal RTC	45	µA

8.3 Mechanical Characteristics

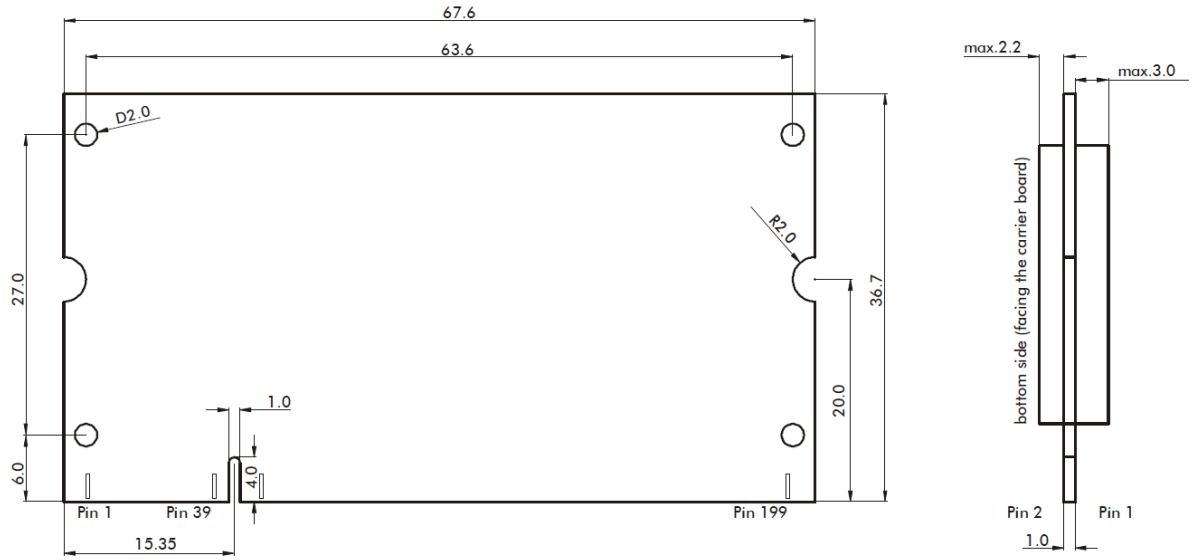

Figure 10 Mechanical dimensions of the Colibri module (top view)
Tolerance for all measures: +/- 0.1mm

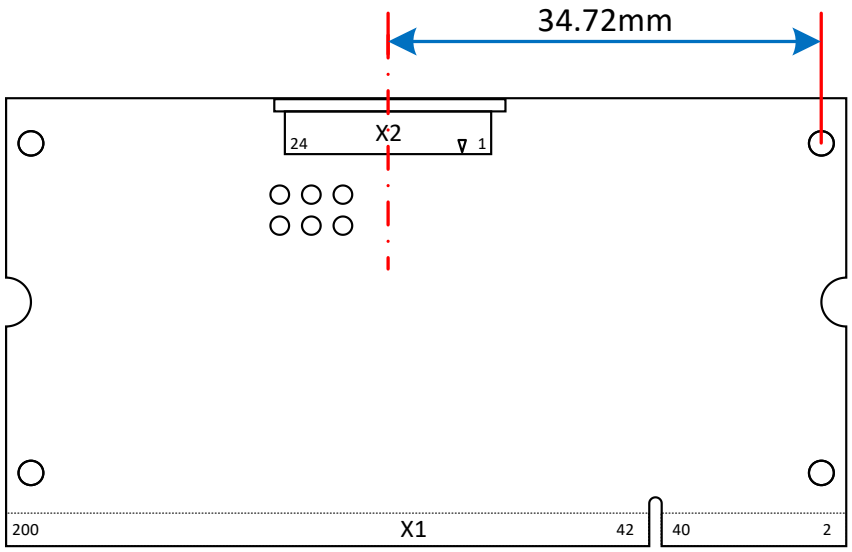

Figure 11 Mechanical position of FFC connectors (bottom view)
Tolerance for all measures: +/- 0.1mm

8.3.1 Sockets for the Colibri Modules

The Colibri modules fit into a regular 2.5V (DDR1) SODIMM200 memory socket.
A selection of SODIMM200 socket manufacturers is detailed below:

AUK Connectors:	http://www.aukconnector.com/
CONCRAFT:	http://www.concraft.com.tw/connector_products_ddr.html
Morethanall Co Ltd.:	http://www.morethanall.com/
Tyco Electronics (AMP):	http://www.tycoelectronics.com
NEXUS COMPONENTS GmbH	http://www.nexus-de.com

8.4 Thermal Specification

The Colibri iMX6 incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. This allows the Colibri iMX6 to deliver higher performance at lower average power consumption compared to other solutions. The Freescale i.MX 6 SoC has an integrated temperature sensor for monitoring the temperature of the CPU.

Here some general considerations:

- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to smaller leakage currents.
- If you need the full CPU/Graphics performance over a long period of time, make sure that you are able to dissipate sufficient thermal energy to the environment.

In general, the more effective the generated thermal energy is transported to the environment, the more performance you can get out of the Colibri iMX6 Module.

Table 8-7 1.1 Thermal Specification

Module	Description	Min	Typ	Max	Unit
Colibri iMX6x	Operating temperature range	0		70[1]	°C
Colibri iMX6x IT	Operating temperature range	-40		85[1]	°C
Colibri iMX6x Colibri iMX6x IT	Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Colibri iMX6x	Junction temperature SoC	0		95	°C
Colibri iMX6x IT	Junction temperature SoC	-40		105	°C
Colibri iMX6x Colibri iMX6x IT	Thermal Resistance Junction-to-Ambient, i.MX 6 only. (Theta-JA)[2]		23		°C/W
Colibri iMX6x Colibri iMX6x IT	Thermal Resistance Junction-to-Top of i.MX 6 chip case. (Psi-JCtop)[2]		2		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four layer Board as defined by JEDEC Standard JESD51-6, board mounted horizontal, natural convection.

8.5 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance