Attracting Tomorrow

Ceramic Capacitor Technology

CeraLink® Opens New Dimensions in Power Electronics

TDK Electronics AG
Piezo and Protection Devices Business Group
Product Marketing PI AE/IE Munich, Germany
June 2021

CeraLink in a shot - optimized for conditions under operation in power electronics

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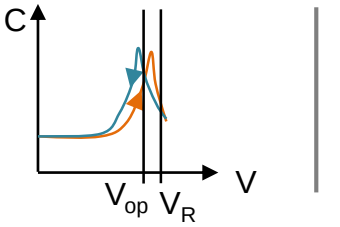
Use CeraLink when
- Space requirement is tight
- Temperature is demanding (+150 °C)
- High current rating is vital
- Requirements for capacitance density are tough
- High switching frequencies are applied (SiC, GaN)

Main Application
- Snubber capacitor
- DC-Link capacitor
- Filter capacitor

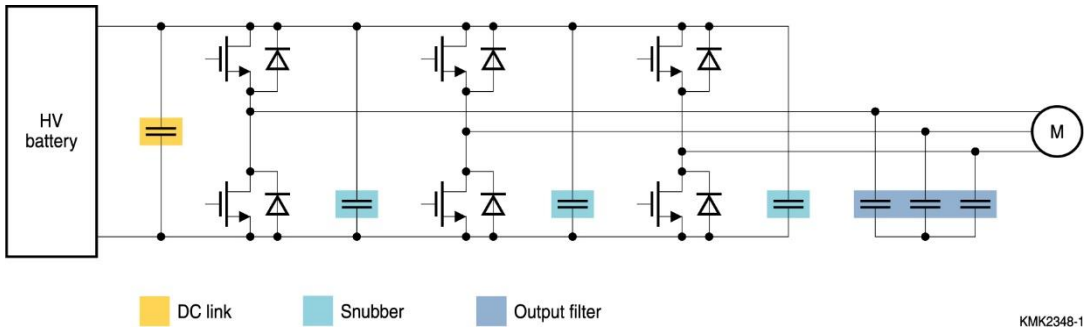
CeraLink technology supports
- Increasing capacitance with DC bias and best in class capacitance density at operating point (V_{op} + T_{op})
- High current capability due to low losses at high frequencies (up to several MHz) and high temperatures (up to +150 °C)
- No limitation of dV/dt
- Good self-regulating properties
- Qualification based on AEC-Q200 rev. D

RoHS Compliant

Full Performance Potential



Main Application



Measurement condition	Film capacitor	Class 2 MLCC	CeraLink
Typical capacitance density @ DC link voltage, 20 V_{RMS}, 25°C	0.7 µF/cm³	2.5 µF/cm³	**4.9 µF/cm³**
Typical current rating per capacitance @ 100 kHz, 105°C	< 1 A/µF	< 4.5 A/µF	**11 A/µF**

CeraLinks Special Behaviour

At High Temperature

- Operating temperature up to +150 °C
- Low losses at high temperature
- Low leakage current
- No thermal runaway

- Generally low self-heating AND self-heating supports CeraLink to come to temperature for good performance

At High Frequency

- Optimal frequency in the range of 100 kHz to 1 MHz
- Minimal ESR due to low-loss copper electrodes and HF-suited backend
- Typ. ESR @ 25 °C, 1 MHz*: 3-45 mOhm
- Typ. ESL*: 2-4 nH
- Temperature decrease with rising frequency

Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

Measurement condition	MKP film capacitor	BTO Class 2 MLCC	CeraLink
Typical capacitance density @ DC link voltage, 20 V_{RMS}, 25 °C	0.7 µF/cm³	2.5 µF/cm³	**4.9 µF/cm³**
Typical current rating per capacitance @ 100 kHz, 105 °C	< 1 A/µF	< 4.5 A/µF	**11 A/µF**

* varies with series and voltage class

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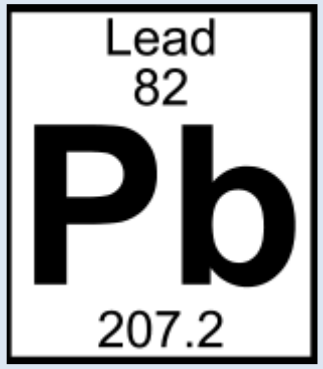
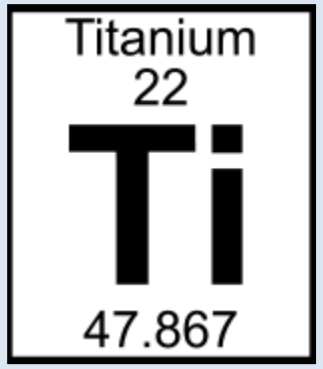
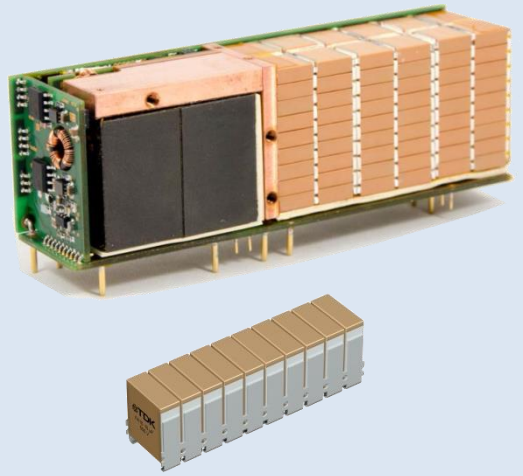
Technology Insights

PZT – a highly flexible ceramic material class



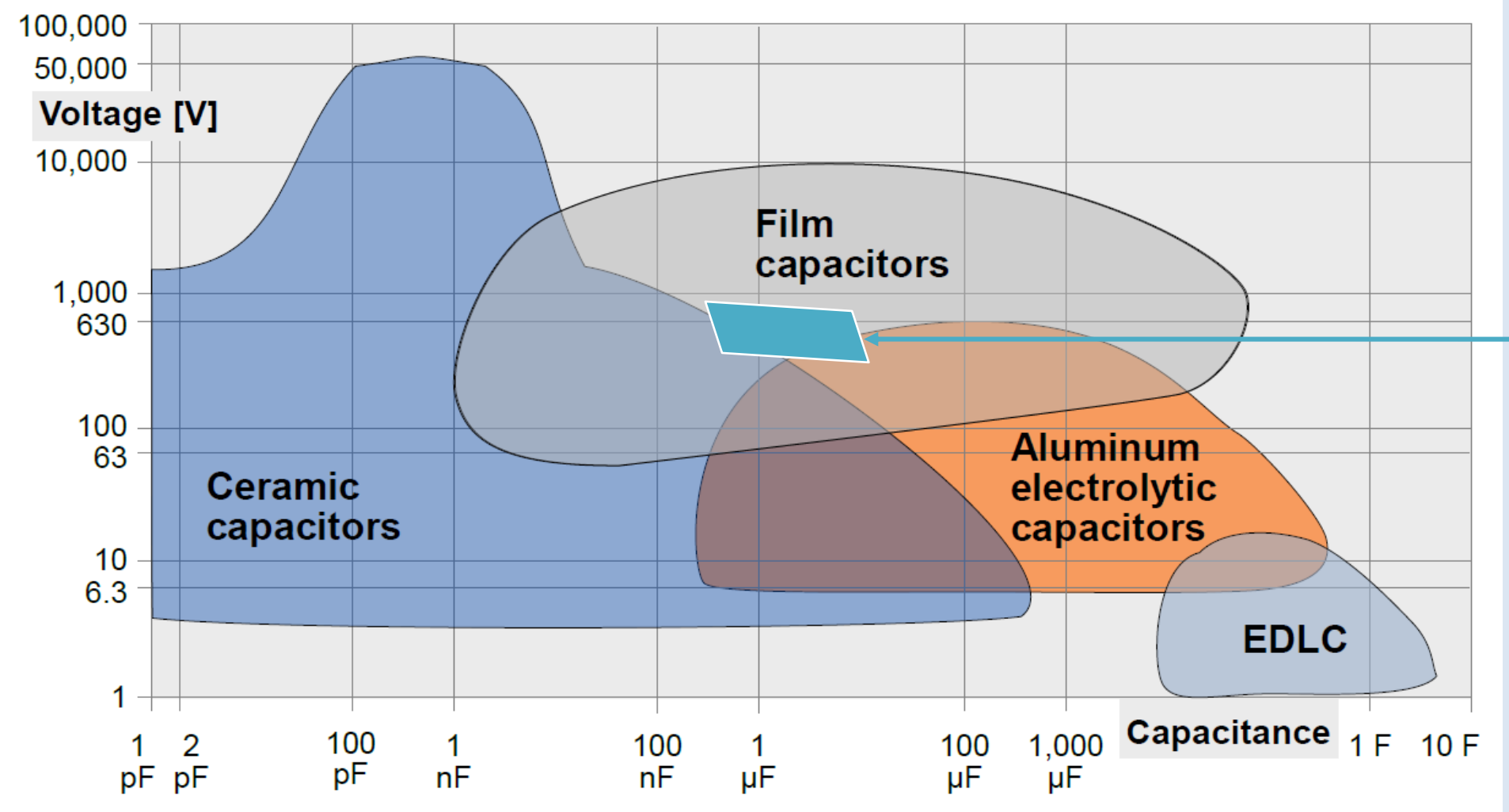


Piezo actuators



Capacitors

Capacitor technology landscape

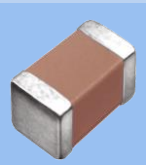


Technology guideline

Film capacitors

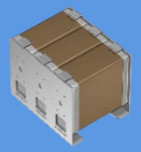
- Smaller
- Higher operating temperature
- Lower ESL
- Higher frequency
- SMD
- Higher ripple current ratings

Large MLCC chips



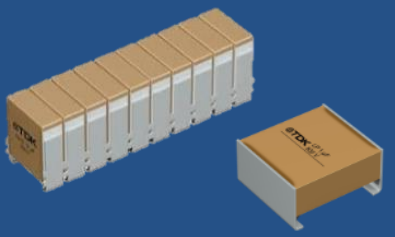
- Lower ESL
- Mechanically more robust

Stacked MLCC



- Smaller solution
- Higher operating temperature
- Lower ESL
- Higher ripple current ratings

CeraLink

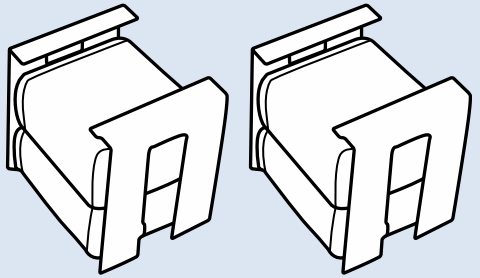


Si IGBT → SiC / GaN

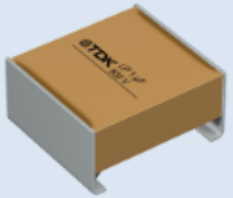
CeraLink LP versus class II MLCC

Capacitance
@ 400 V + 20 V ripple

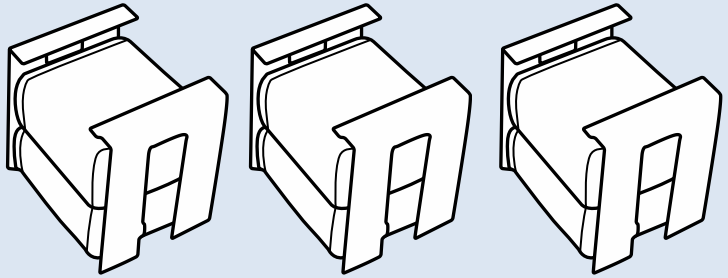
Similar like



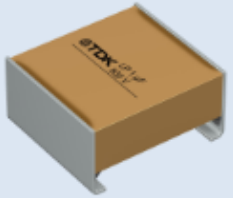
Ripple current
@ 100 kHz & 85 °C



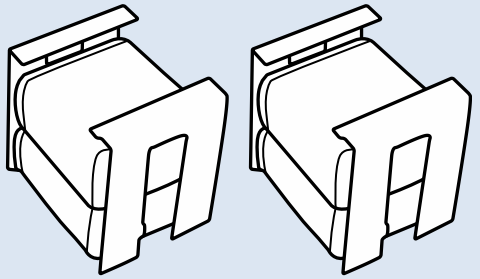
Similar like



Added value of
CeraLink LP series

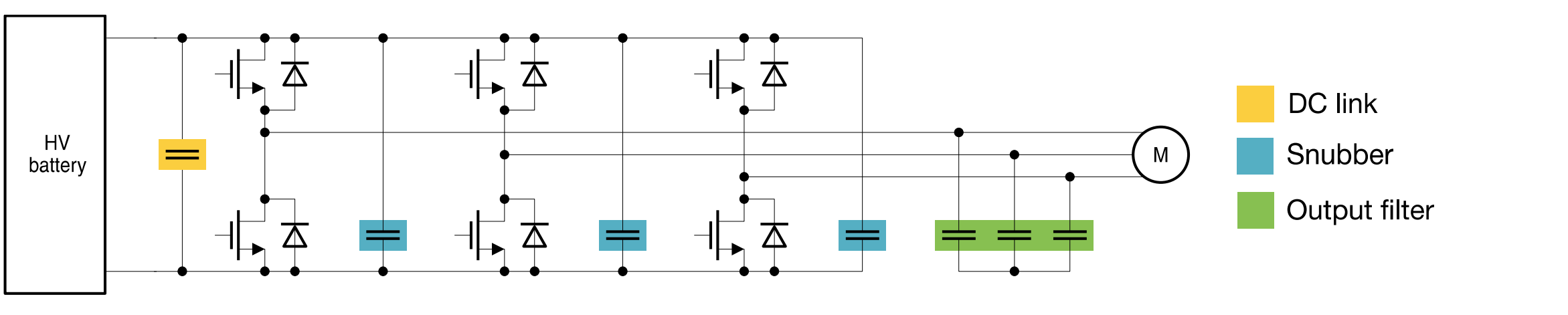


- Less PCB space
- Higher temperature
- Low ESL



Stacked MLCC based on case size 2220

CeraLink target applications

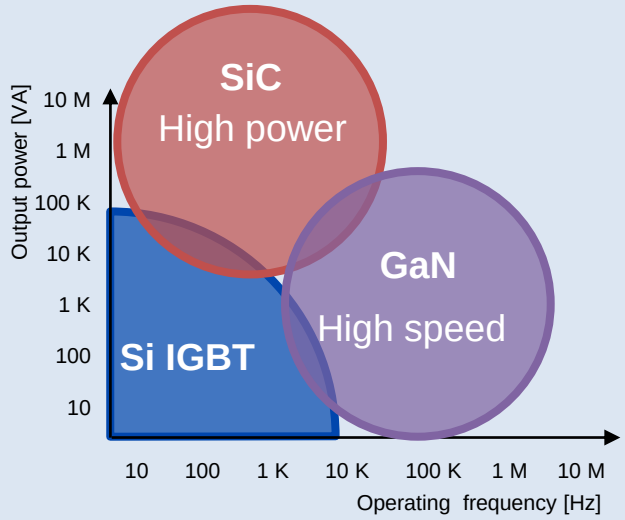


Main applications

- Snubber capacitors
- DC-link capacitors
- Filter capacitors

Scope

- High power density
- High efficiency
- High temperature



Material
PLZT – an antiferroelectric material

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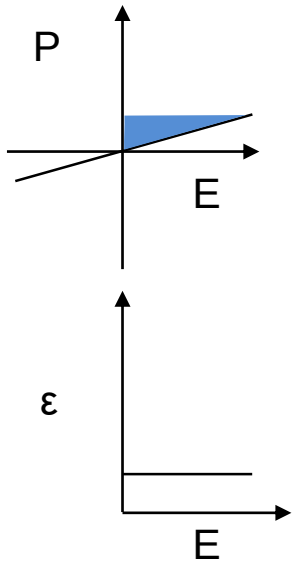
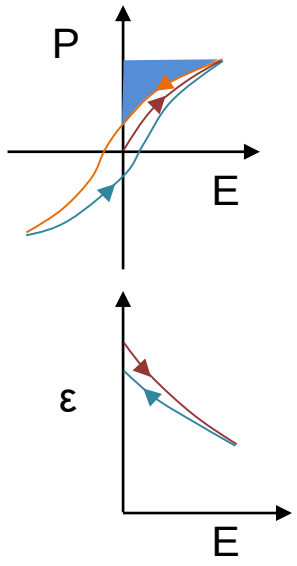
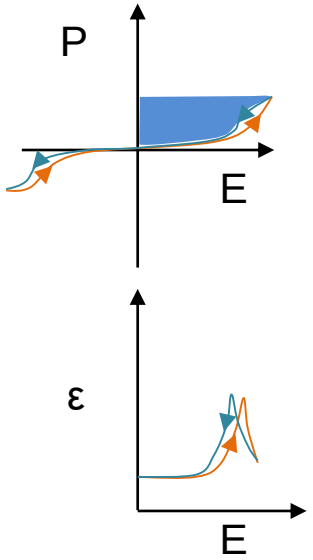
Linear	Ferroelectric	Antiferroelectric
		

Nature of electrical polarization	Electronic, ionic	Permanent dipoles form ferroelectric domains	Permanent dipoles form antiparallel zones
Material class	(Ba,Nd)TiO, typ. NP0, C0G	$BaTiO_3$ (BTO), typ. X7R	$(Pb,La)(Zr,Ti)O_3$ (PLZT)
Advantages	ε constant over electric field and temperature	ε up to 10,000 is possible	ε increases with field
Disadvantages	ε < 100	ε decreases strongly with electrical field	ε low at zero bias

P Dielectric polarization

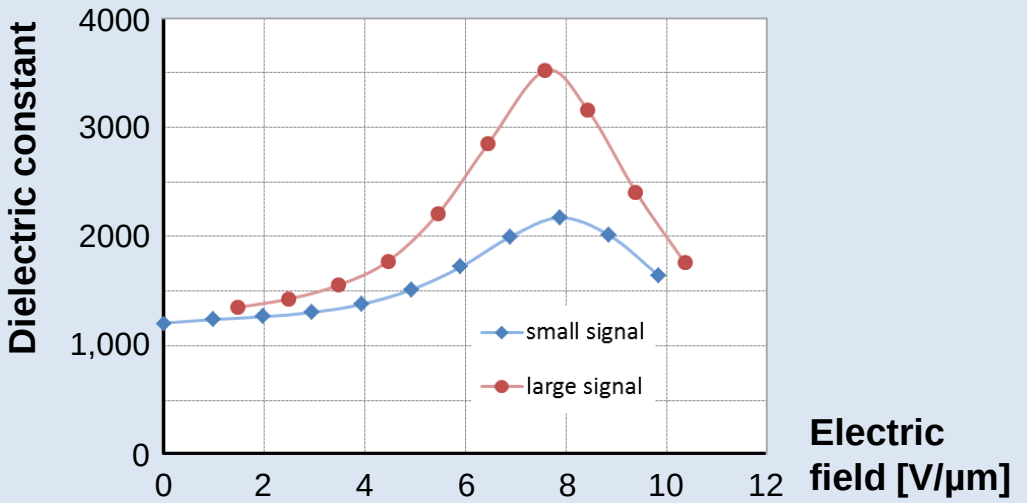
E Electrical field strength

ε Permittivity

High capacitance density at operating condition

- Due to antiferroelectric behavior, the characteristics of CeraLink are strongly non-linear and optimized for conditions under operation in power electronics
- Film capacitors and class 1 ceramics have a dielectric constant (nearly) independent on the electrical field (ε < 100)
- The permittivity of ferroelectric (e.g. X7R) MLCC capacitors is decreasing with electrical field
- CeraLink features an increasing dielectric constant up to the operating voltage
- At higher AC voltage (peaks), the material is able to provide even higher permittivities

DC bias characteristics at room temperature

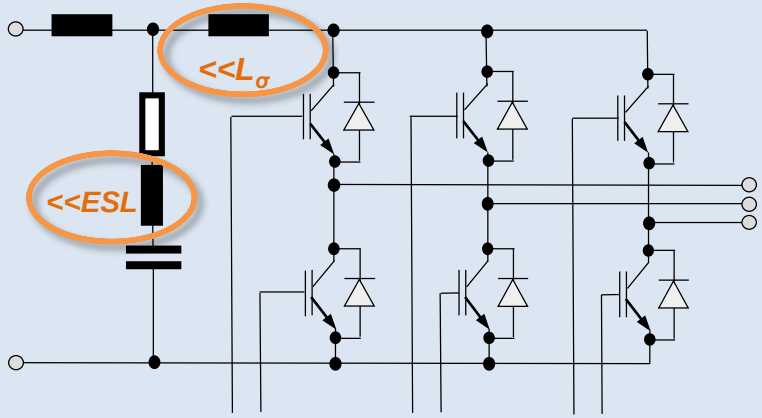


	Film capacitor	Class 2 MLCC	CeraLink	
Nominal / rated capacitance	100 %	100 %	**100 %**	
No bias voltage 0.5 V_{RMS}	100%	100 %	**35 %**	
DC link voltage 0.5 V_{RMS}	100 %	35 %	**60 %**	**DC link (energy)**
DC link voltage 20 V_{RMS}	100 %	35 %	**100 %**	**Snubber**

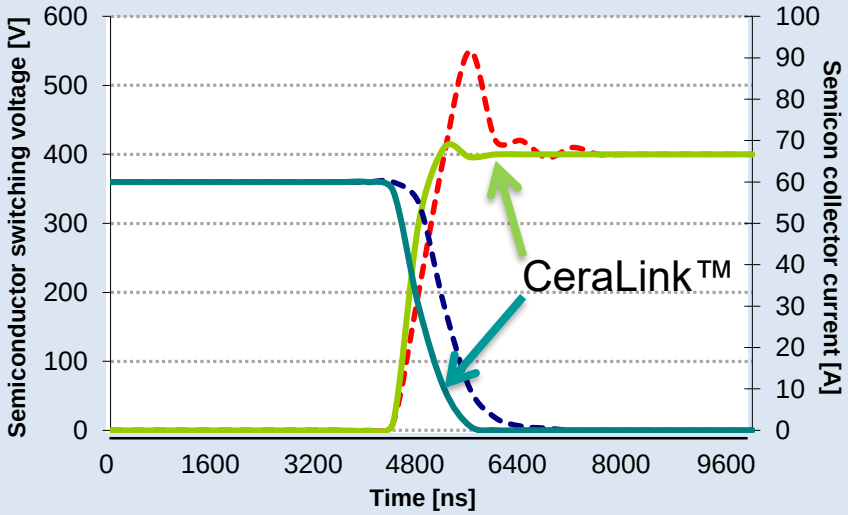
CeraLink is ideal for fast switching

Device characteristics lead to a low inductive commutation loop

- High capacitance density of 2 to 5 µF/cm³
- **Low self-inductance (ESL) of 2.5 to 4 nH**
- High thermal robustness allows CeraLink to be placed very close to the semi-conductor with operation up to 150 °C permissible
- **No limitation of dV/dt**

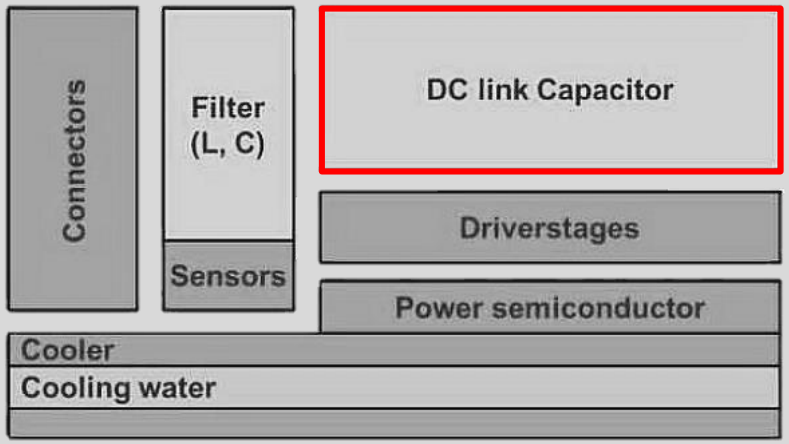


Semiconductor overshoot principle



New demands for DC link capacitors

Improvements in power density and efficiency were mainly driven by semiconductor technology in the last decade.



Example: principle block picture and size comparison of a motor inverter

"Today the package of a motor inverter is mainly driven by the size of the capacitor, the bus bars, the terminal box and the filter components."

Source: Plikat, Mertens, Koch, Volkswagen AG, Corporate Research, 2013

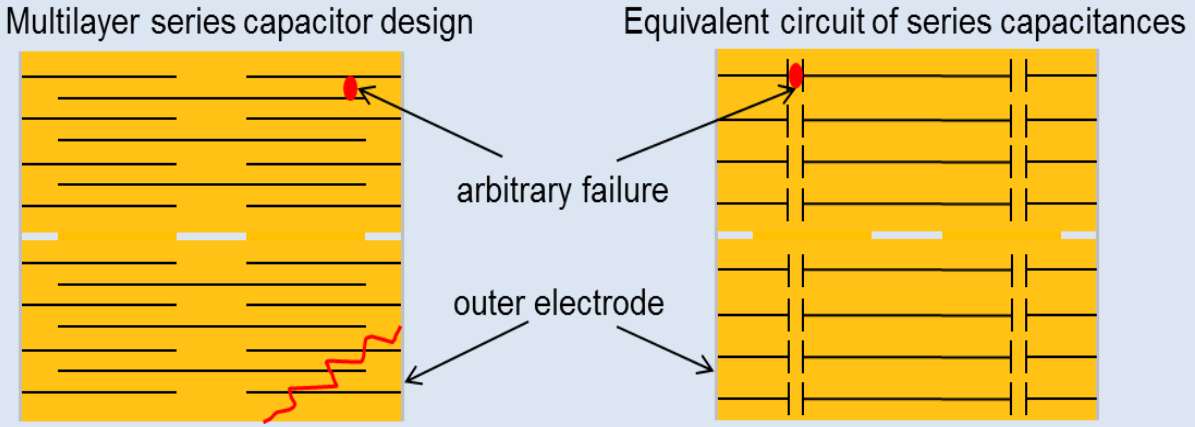
Requirements for a DC link capacitor

- High capacitance density
- High current density
- Low parasitic values (ESR/ESL) for fast switching
- Low losses in operation
- High operating and peak temperatures
- High cooling efficiency due to high thermal conductivity
- Support of distributed DC link capacitor topologies with low inductance components (modular design)

Ceramic Chip Features
Design for robustness against ceramic cracks

MLSC design

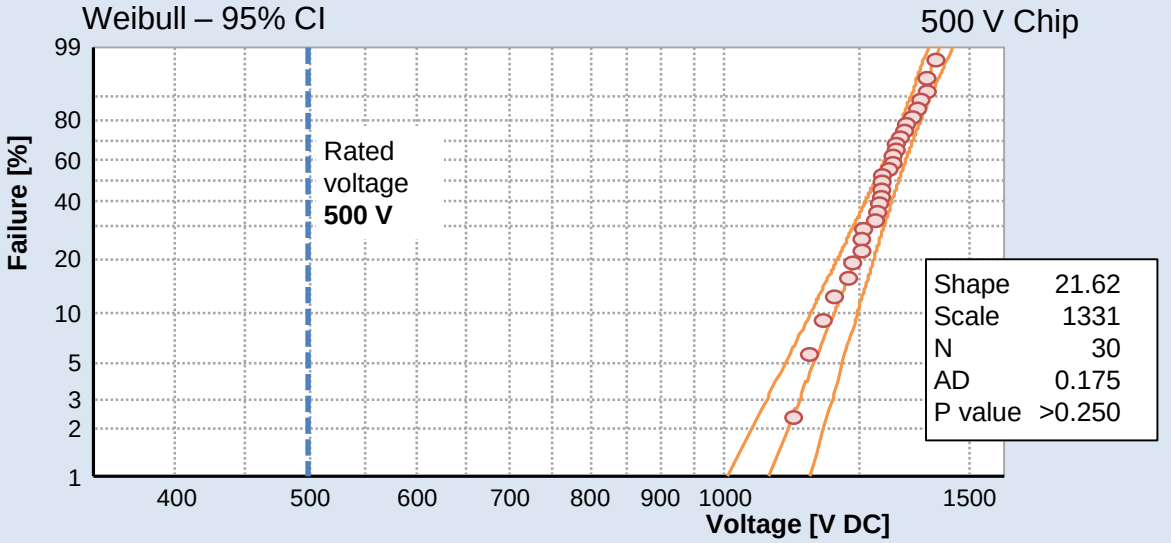
- Series connection of two MLCC geometries in one component.
- **MLSC** design prevents short circuits caused by cracks from mechanical overstress



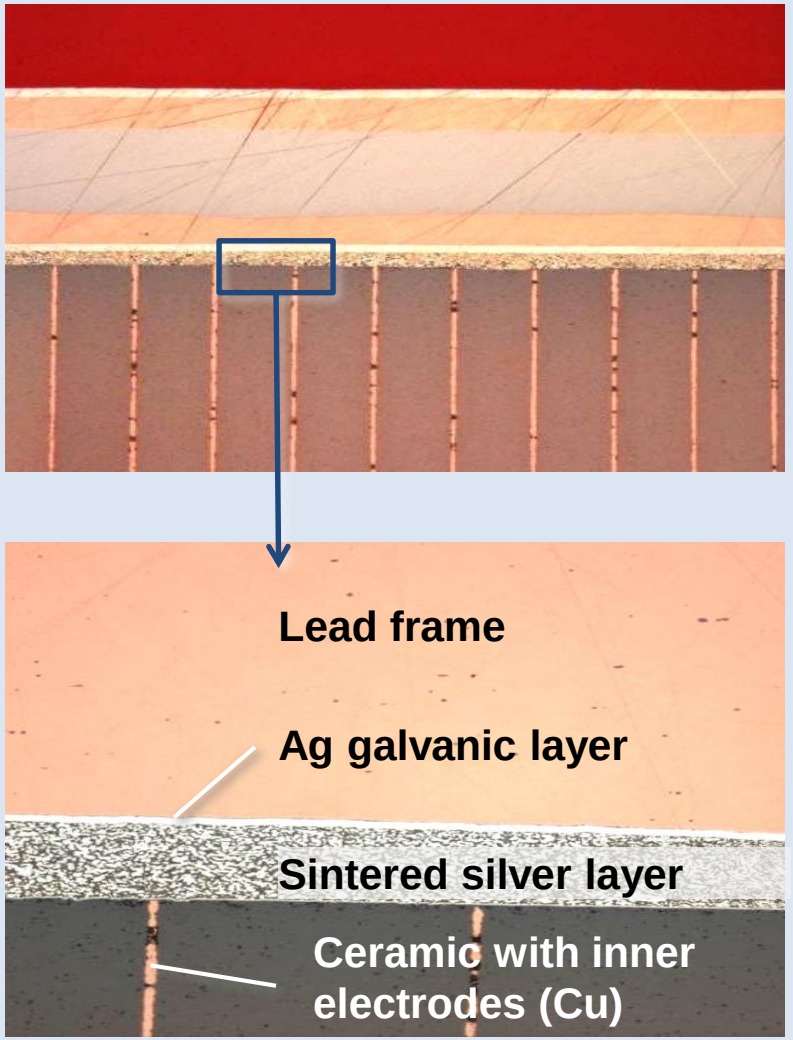
MFD design

- Chip is segmented in height to reduce piezoelectric stress between active and inactive area

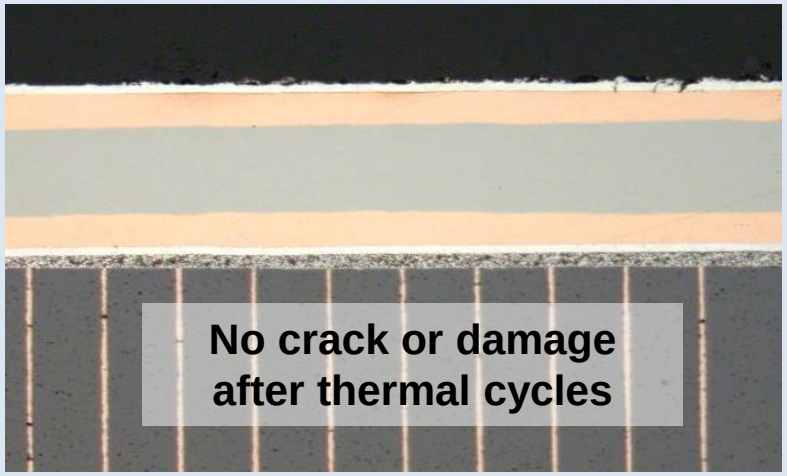
Breakdown voltage measurement



Packaging
Robust interconnection of metallic contacts



10,000 cycles thermal shock test
(-55 °C to +150 °C)

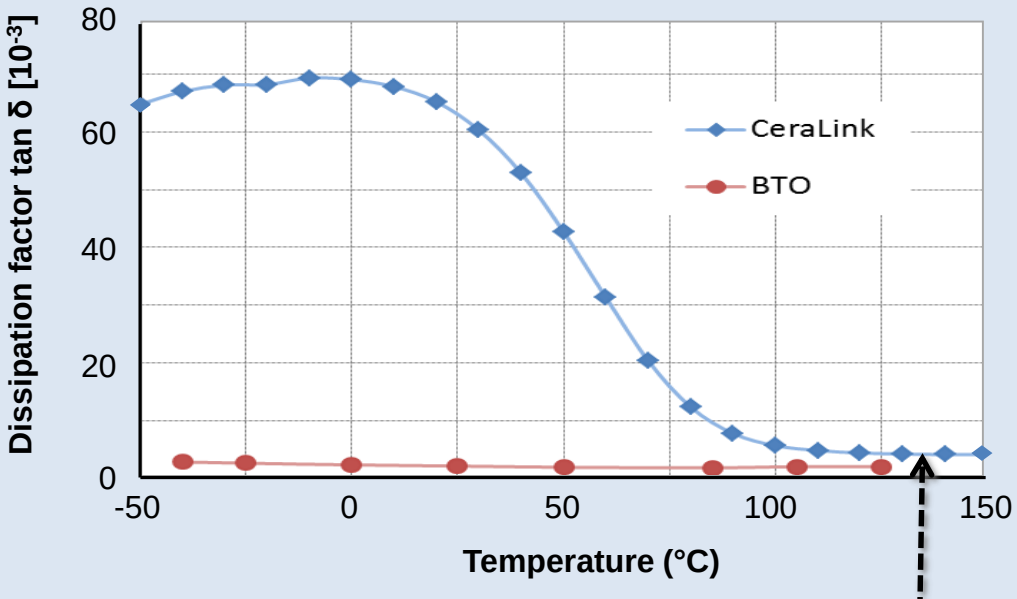


- Silver sinter connection between ceramic body and lead frame
- Outer contacts made of CIC (copper invar* copper), to combine high electrical and thermal conductivity with low coefficient of thermal expansion
- All materials are excellent thermal and electrical conductors (lowest thermal and electrical resistance)
- Silver layer prevents cracking of the ceramic in case of mechanical overstress or solder shock → open mode!

*Invar: 36Ni-Fe

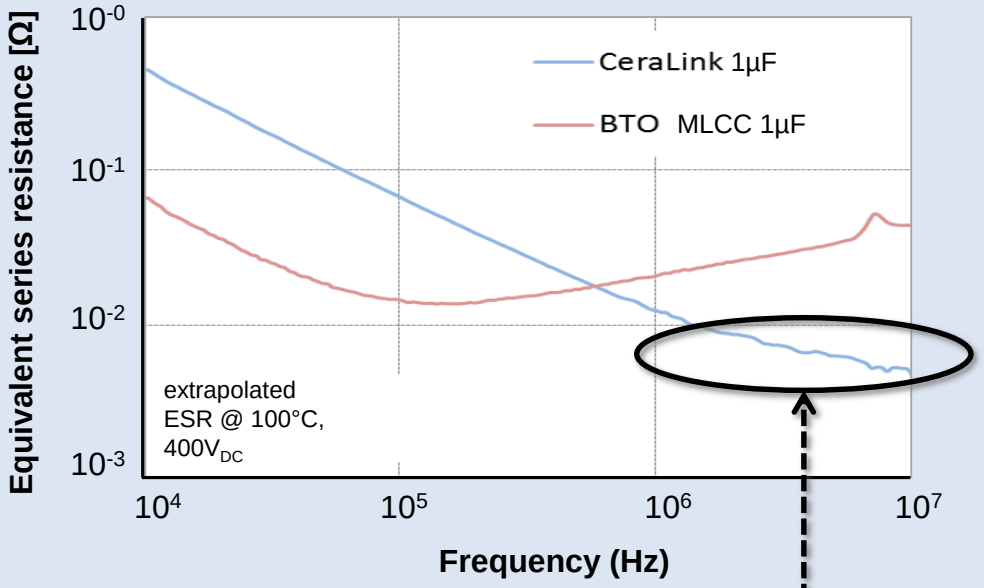
Low losses at high temperatures and frequencies

Comparison @ 1 V_{AC}, 1 kHz, 400 V_{DC}, 25 °C



Low dielectric loss at high temperatures

Comparison @ 0.1 V_{AC}, 0 V_{DC}, 25 °C



Minimal ESR due to low-loss copper electrodes and HF-suited backend

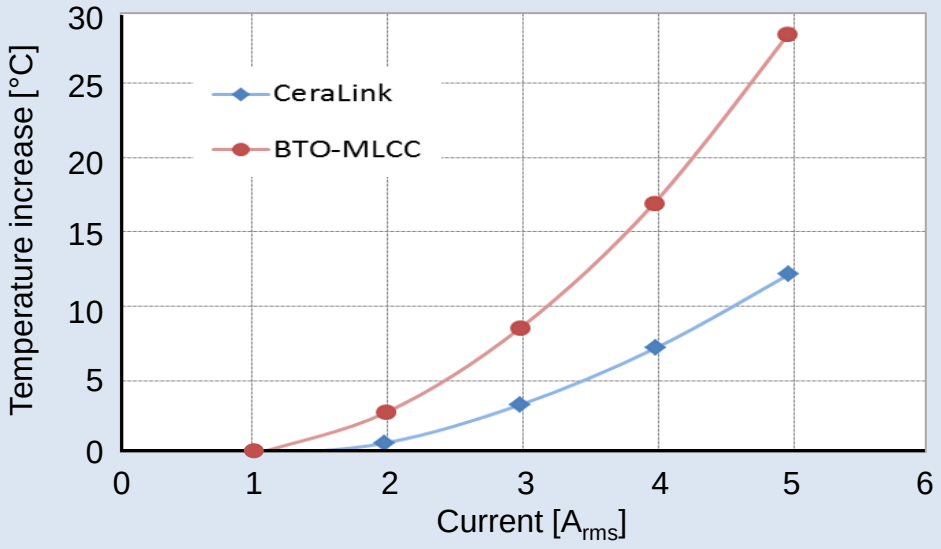
BTO = barium titanate oxide = standard MLCC material

Low self-heating and high current capability

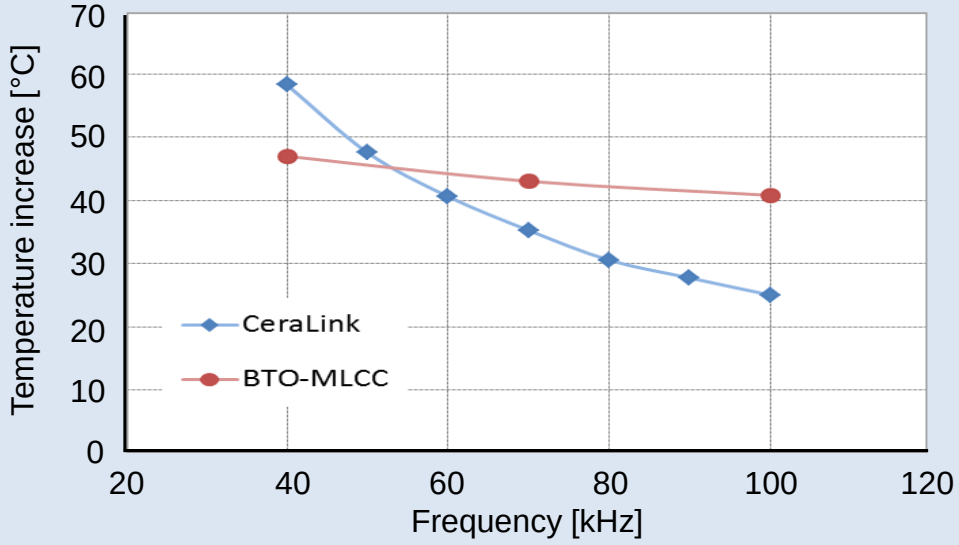
Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

Measurement condition	MKP film capacitor	BTO Class 2 MLCC	CeraLink
Typical capacitance density @ DC link voltage, 20 V_{RMS}, 25 °C	0.7 µF/cm³	2.5 µF/cm³	**4.9 µF/cm³**
Typical current rating per capacitance @ 100 kHz, 105 °C	< 1 A/µF	< 4.5 A/µF	**11 A/µF**

Comparison @ 400 V_{DC}, 105 °C, 200 kHz

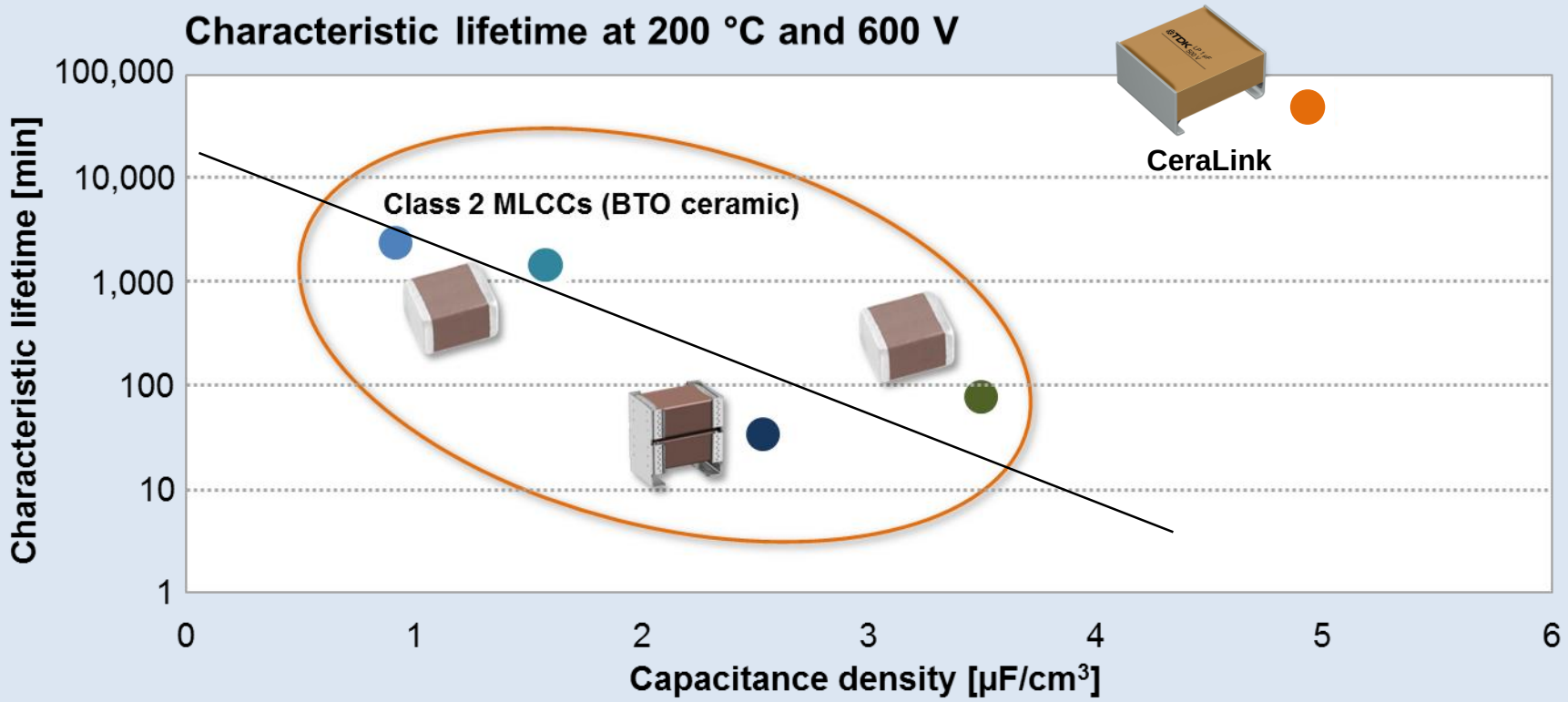


Comparison @ 400 V_{DC}, 85 °C, 5 A_{rms}



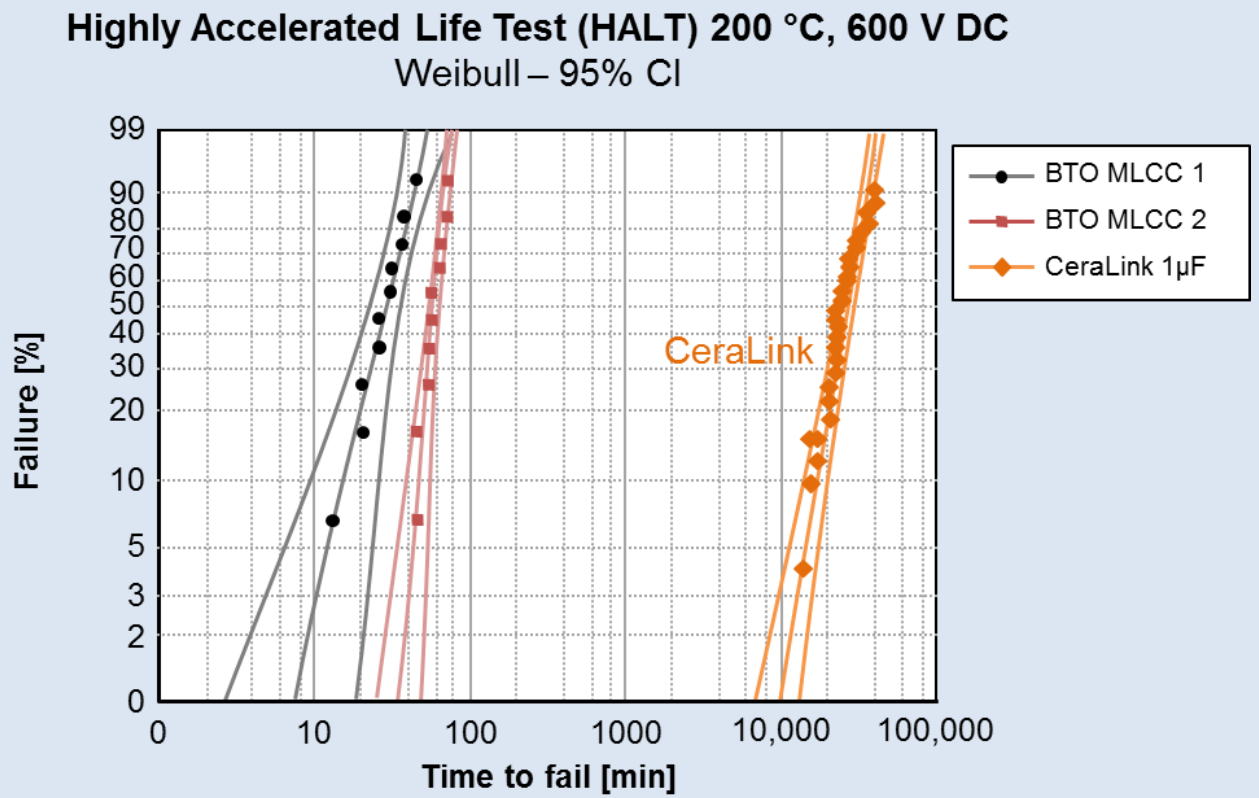
Measurements were carried out without active cooling (no forced air flow, no heat sink)

Lifetime at high temperatures – comparison of ceramic capacitors



CeraLink offers highest lifetime and capacitance density compared to conventional ceramic capacitors

Exceptional lifetime at high temperatures



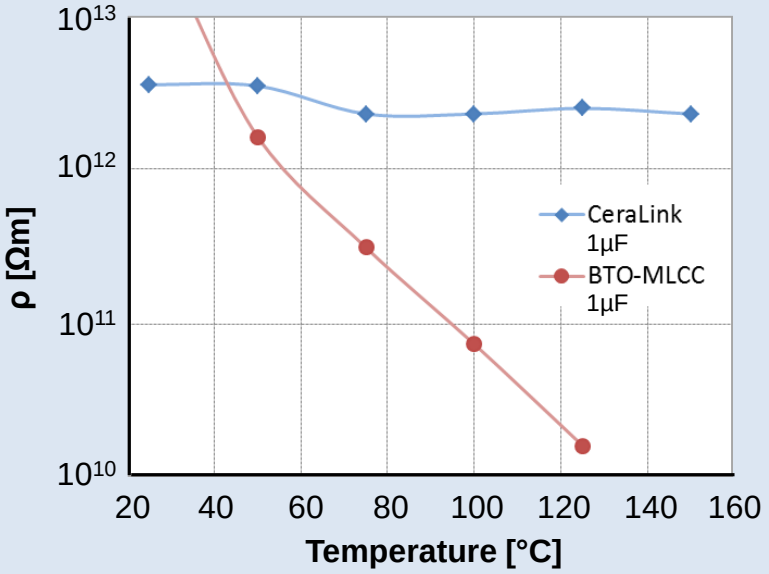
Lifetime @ 200 °C three orders of magnitude higher than that of conventional ceramic capacitors

Low leakage current at high temperatures

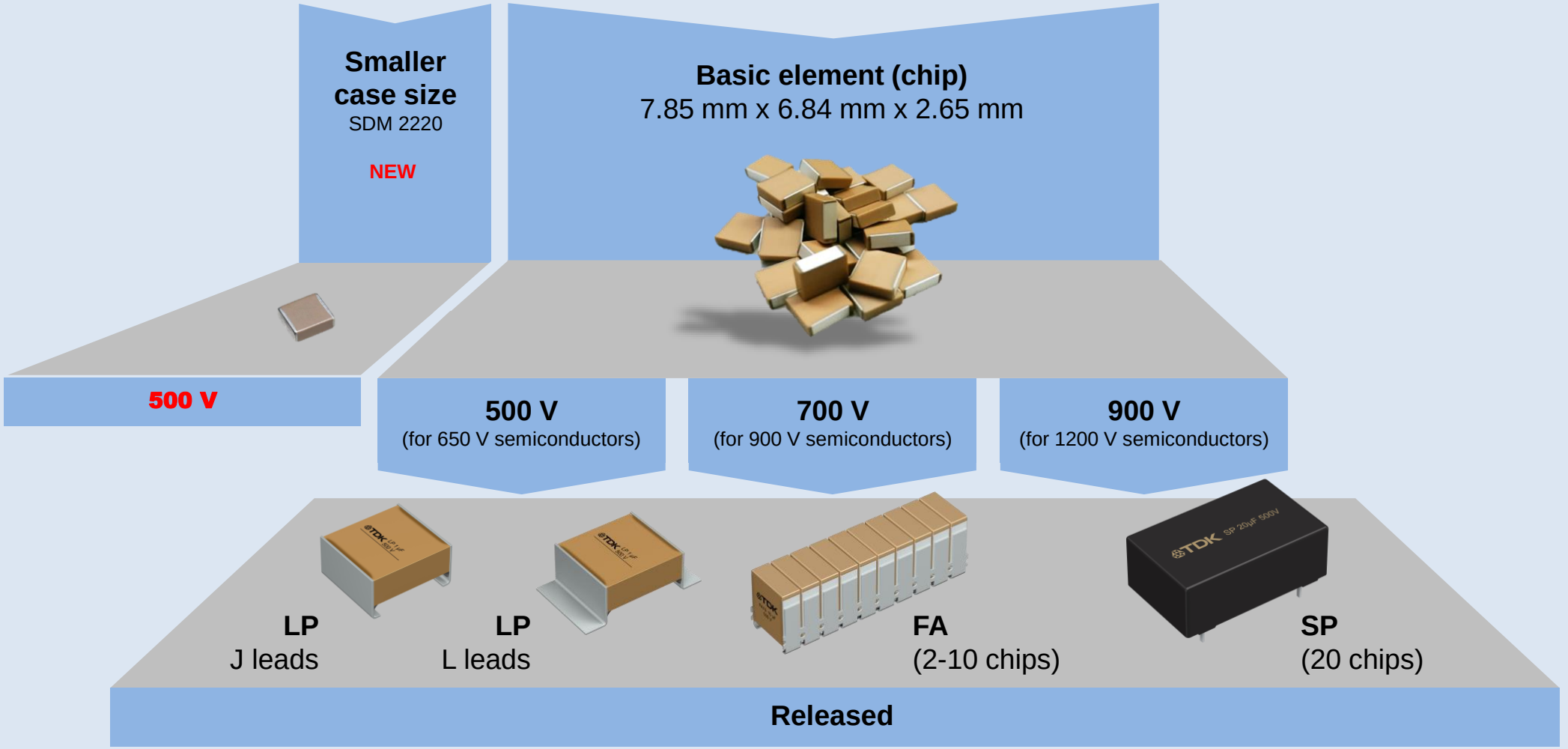
CeraLink shows stable and outstanding high isolation properties compared to all existing capacitor technologies

- low leakage current at elevated temperatures even above 150 °C
- No thermal runaway observed for CeraLink ceramic material

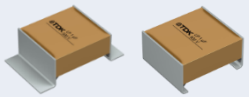
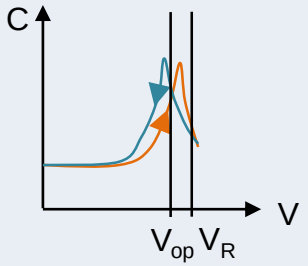
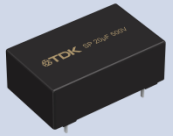
Comparison @ 400 V_{DC}



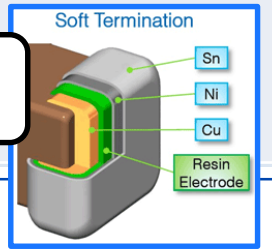
CeraLink Product portfolio – modular design



CeraLink product range

Series	Maximum voltage ratings			Features
	650 V	1000 V	1300 V	
Low Profile **LP (L /J leads)** 	**1 µF / 500 V**	**0.5 µF / 700 V**	**0.25 µF / 900 V**	Innovative anti-ferroelectric ceramic material  $V_{op} = V_R - 100$ V
Flex Assembly **FA2 / FA3** 	**2/3 µF / 500 V**	**1/1.5 µF / 700 V**	**0.5/0.75 µF / 900 V**	
Flex Assembly **FA10** 	**10 µF / 500 V**	**5 µF / 700 V**	**2.5 µF / 900 V**	Use CeraLink when • Temperature is demanding (+150 °C) • High current rating is vital • Requirements for capacitance density are tough • High switching frequencies are applied (SiC, GaN)
Solder Pin **SP** 	**20 µF / 500 V**	**10 µF / 700 V**	**5 µF / 900 V**	Qualified based on AEC-Q200 and RoHS Compliant
SMD **SMD 2220 - New** 	**0.25 µF / 500V**			

Soft Electrode samples avail.



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Application Insights

Application examples
Ideal for demanding applications

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High voltage applications in xEV

Power supplies for medical equipment

Test and measurement

Drives

Welding

Traction (SiC)

- Temperature
- High voltage
- High current capability
- Compact design
- Low weight/ Low size
- Low ESL
- Robust design

Application examples
Integrated servo drive

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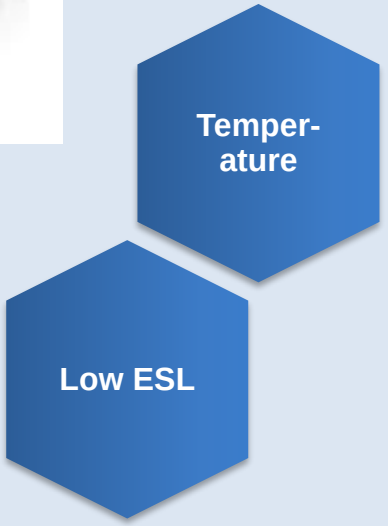
Traditional design

Integrated servo drive

Electronics integrated into the motor housing (outside of inverter)
→ A lot of space
→ Separated from main temperature driver

Electronics integrated into inverter box
→ Tight space requirements
→ Challenging temperatures
SiC based design
→ Low ESL requirements



CeraLink inside Automotive
… some Success Stories

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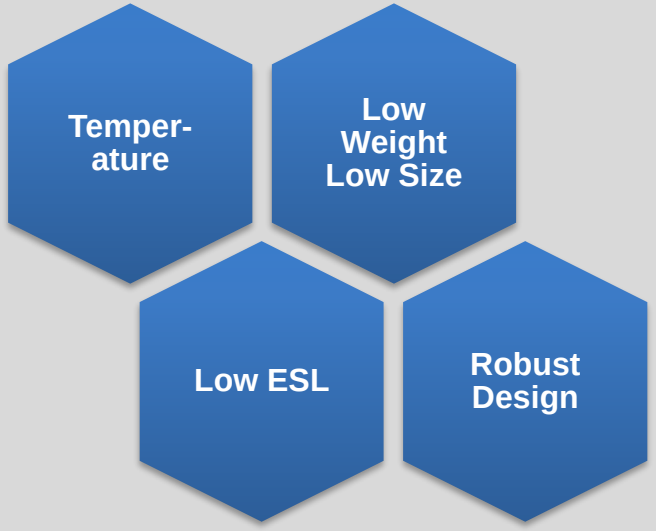
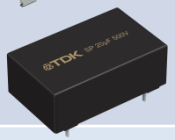
Target Application

- OBC
- DC/DC
- Auxiliary inverters
  - HV heater
  - HV pump
  - HV compressor

Often chosen due to

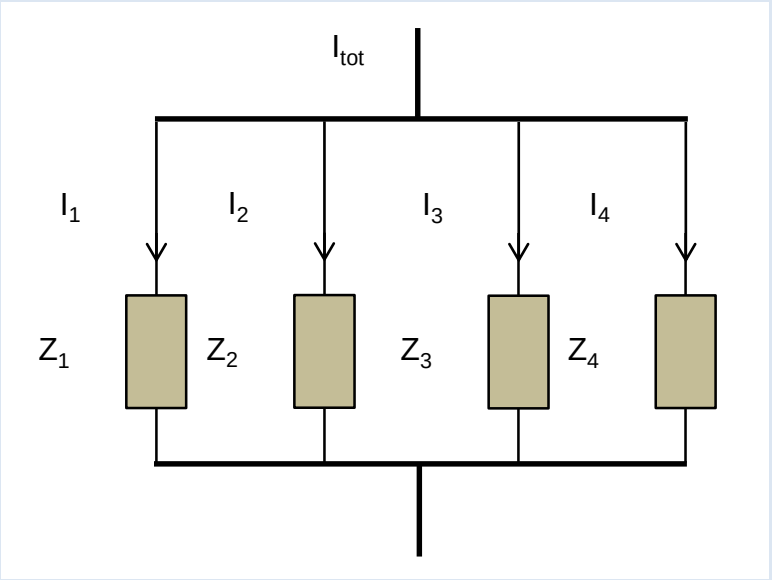


CeraLink as DC Link

Series	Maximum voltage ratings			Features
	650 V	1000 V	1300 V	
Flex Assembly **FA10** 	**10 µF / 500 V**	**5 µF / 700 V**	**2.5 µF / 900 V**	The capacitance characteristic and low ESR of CeraLink avoid a thermal runaway
Solder Pin **SP** 	**20 µF / 500 V**	**10 µF / 700 V**	**5 µF / 900 V**	

In parallel connection, higher temperature leads to:

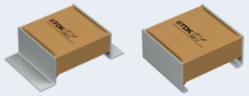
- Lower capacitance
- Higher impedance
- Lowest current through the **hottest** capacitor → self-regulating properties



CeraLink as Snubber

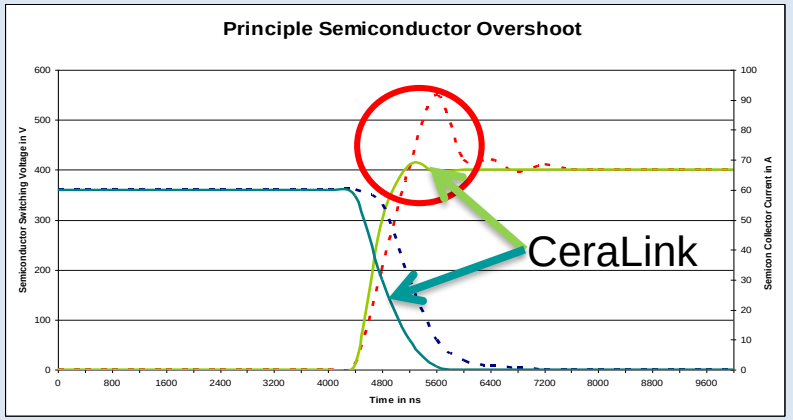
1 per half bridge - *mounted close to the semiconductor*

Attracting Tomorrow

Series	Maximum voltage ratings			Features
	650 V	1000 V	1300 V	
Low Profile **LP (L /J leads)** 	**1 µF / 500 V**	**0.5 µF / 700 V**	**0.25 µF / 900 V**	• Low ESL (typ. 3 nH) • Low losses at high frequencies and high temperatures (up to +150 °C) • No limitation of dV/dt
Flex Assembly **FA2 / FA3** 	**2/3 µF / 500 V**	**1/1.5 µF / 700 V**	**0.5/0.75 µF / 900 V**	
SMD **SMD 2220 - New** 	**0.25 µF / 500 V**			

Over-voltages or over-shoots occur when switching off a Semiconductor.
This will cause an overvoltage according the formula (see left)
The low inductance of the CeraLink enables a faster switching of the semiconductor resulting in lower switching losses, enabling a reduction of switching losses of up to **40%**!

$$V = -L \cdot \frac{di}{dt}$$



CeraLink: Ideal Capacitors for Wide Bandgap Semiconductors

Attracting Tomorrow

Target Application

- OBC
- DC/DC
- SiC Power Modules
- Auxiliary inverters for xEV
  (HV compressor, HV pump, HV heater)
- Wireless charging of vehicle

- Suitable for designs of **400 V / 800 V** xEV
- Increasing capacitance with DC bias and best in class capacitance density at operating point (Vop + Top)
- Supports **miniaturization** with low inductive design

Basic Facts

Qualification based on AECQ-200

Manufacturing site in EU (Deutschlandsberg, AT)

Quality management system according to IATF 16949:2016

Soldering Method: Reflow

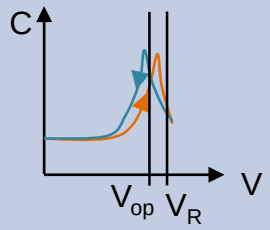
RoHS Compliant

Unique Feature

Innovative anti-ferroelectric ceramic material

High cooling efficiency due to high thermal conductivity

Good self-regulating properties



Resulting Advantages

High capacitance density

High current capability

Low ESL (typ. 3 nH)

Low losses at high frequencies and high temperatures (up to +150 °C)

No limitation in dV/dt

→ Ideal as snubber or filter cap for SiC and GaN applications

Applications
SiC & GaN

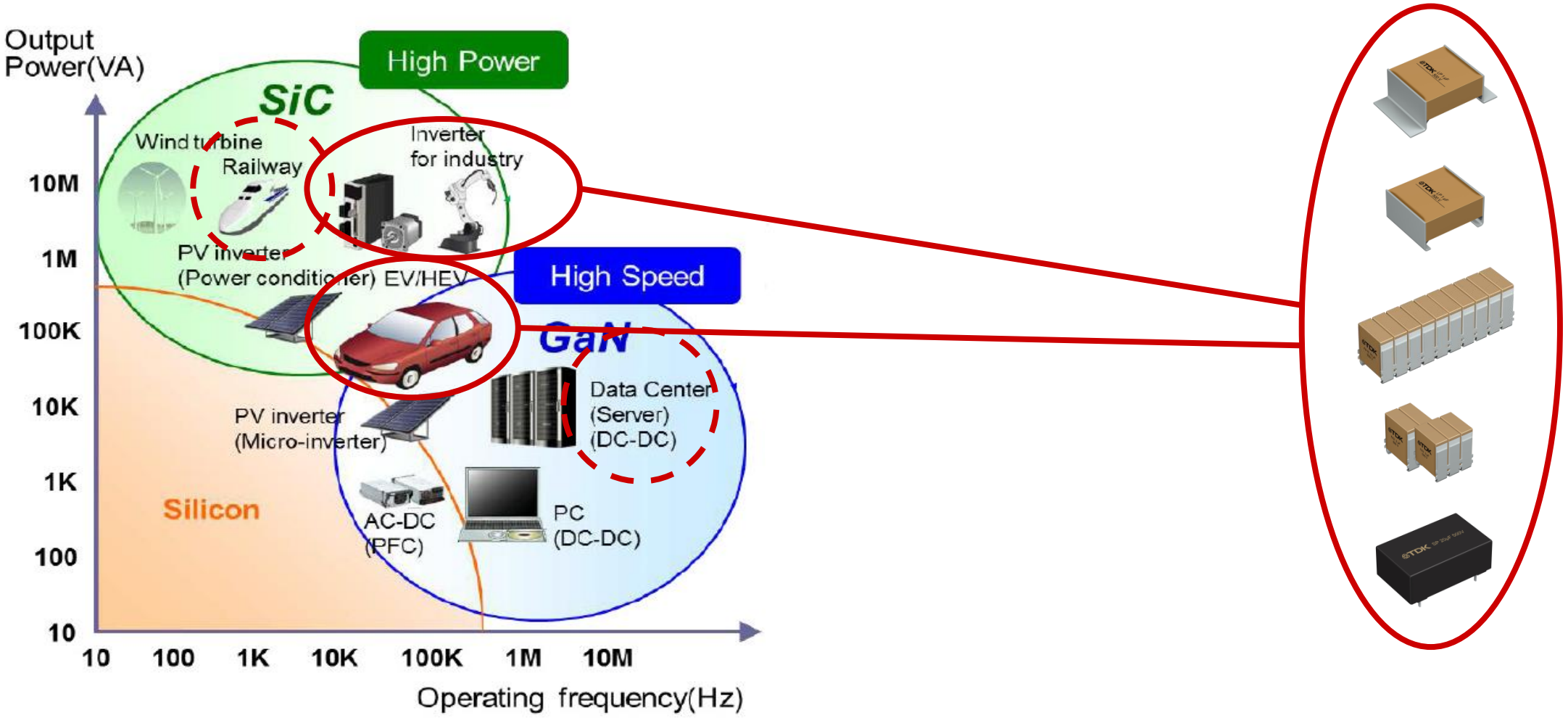


Image: Panasonic

SiC based DC/DC Converter
CeraLink as Snubber

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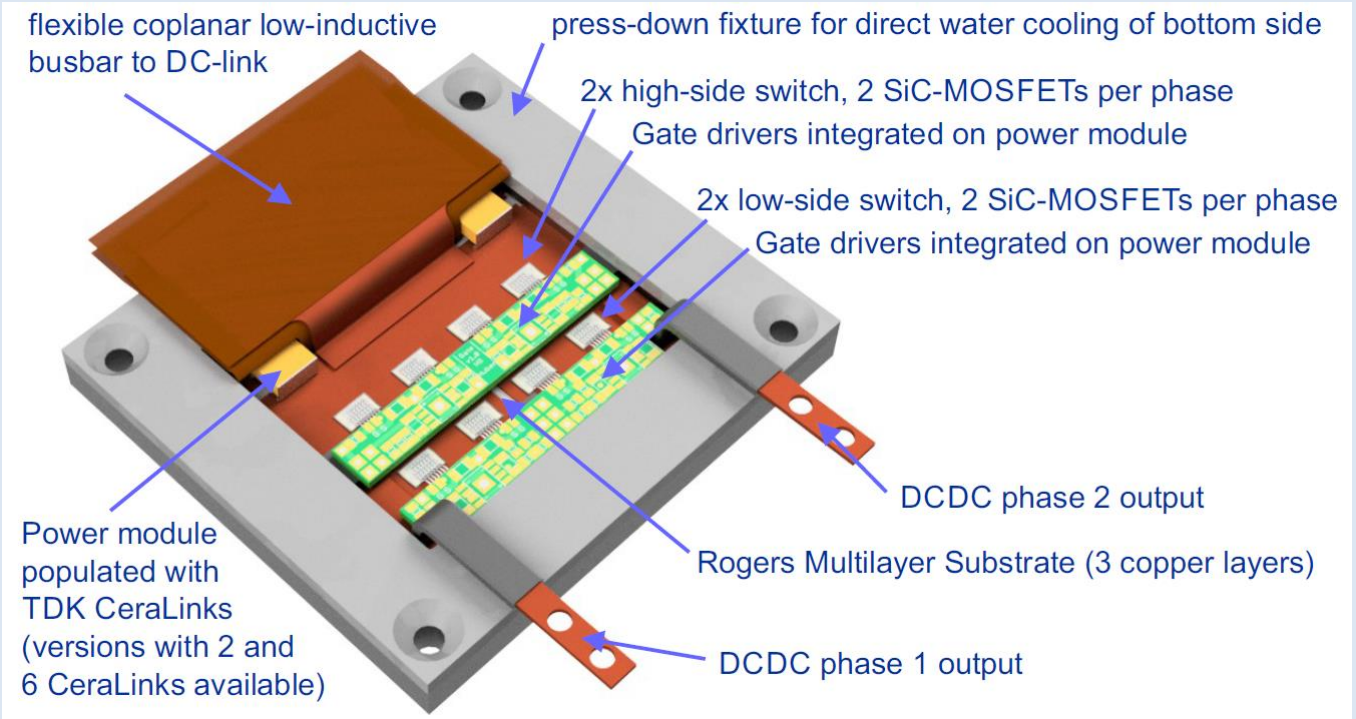
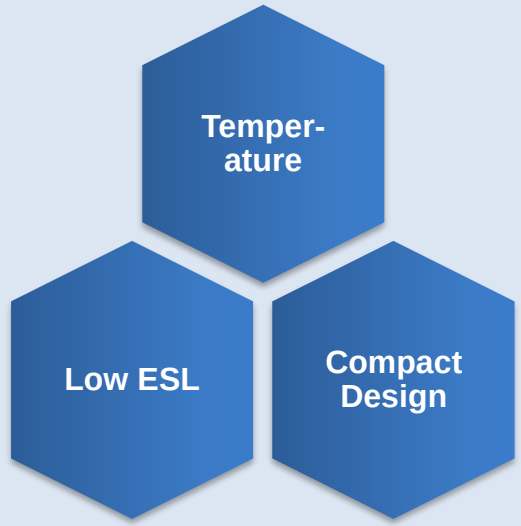
Fast Power Electronics with Low Inductive Module Design

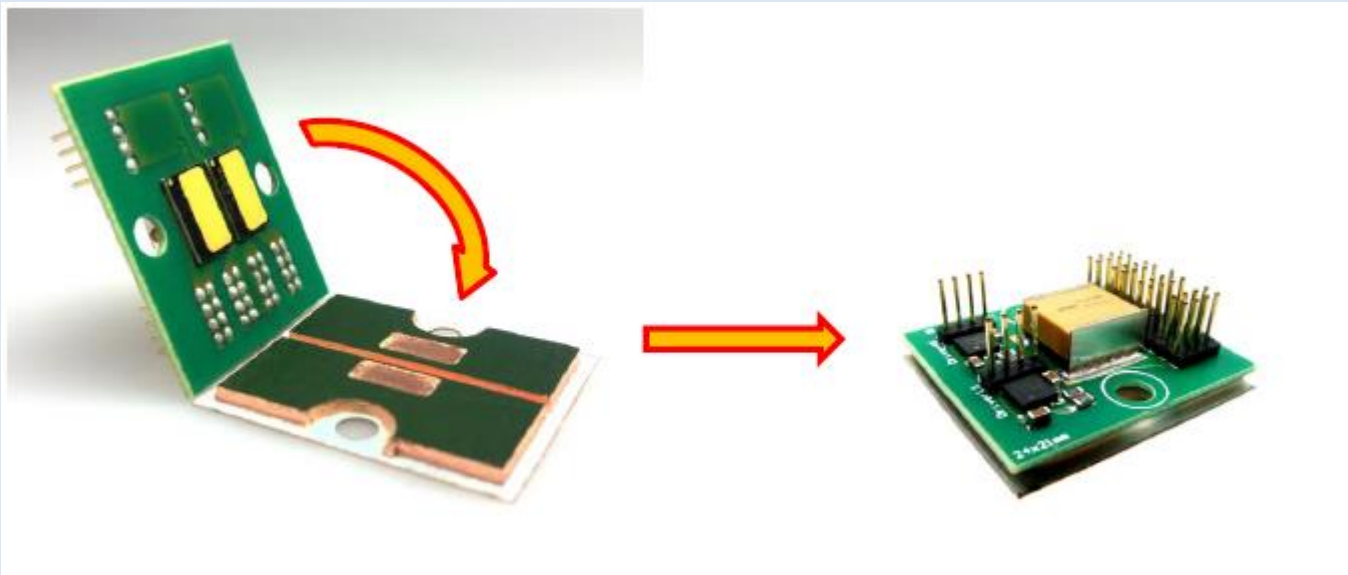
- DC/DC SiC power module: 2 phases - 800V, 100A, 130kHz each
- Ultra-low inductive commutation loop - inductance in low single-digit range realized with CeraLink LP 900 V 0.25 µF (B58031U9254M062)





Source: Hochschule Landshut

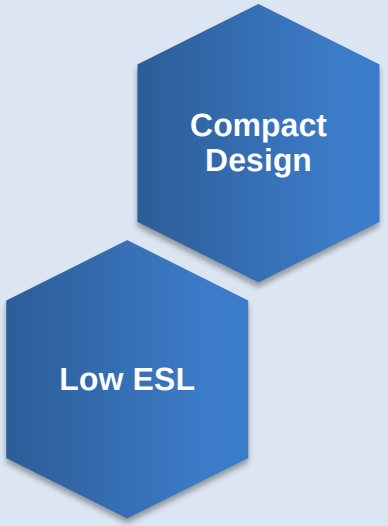
GaN power module with integrated driver and DC-Link capacitor



- 1x CeraLink LP 500 V, 1 µF → low inductive commutation loop ~3nH
- 2x integrated driver for 2x GaN systems 650 V

CeraLink as DC-Link capacitors

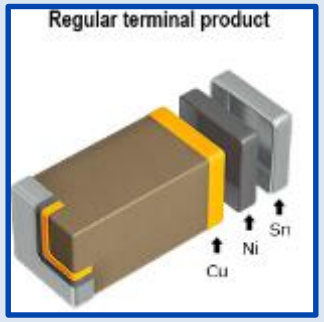
- Supports **miniaturization** with low inductive design
- Supports **fast-switching GaN** and high switching frequencies

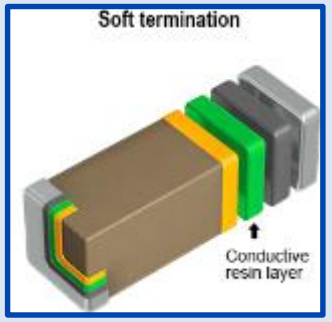


Source: Fraunhofer IZM

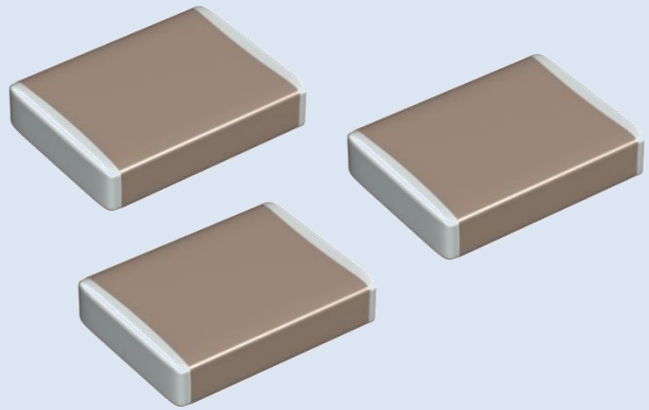
NEW CeraLink® SMD 2220 series

- Optimized for capacitance density (MLCC design)
- Termination
  - ¬ Standard: Cu cap with Ni/Sn galvanics
  - ¬ Soft electrode: coming soon





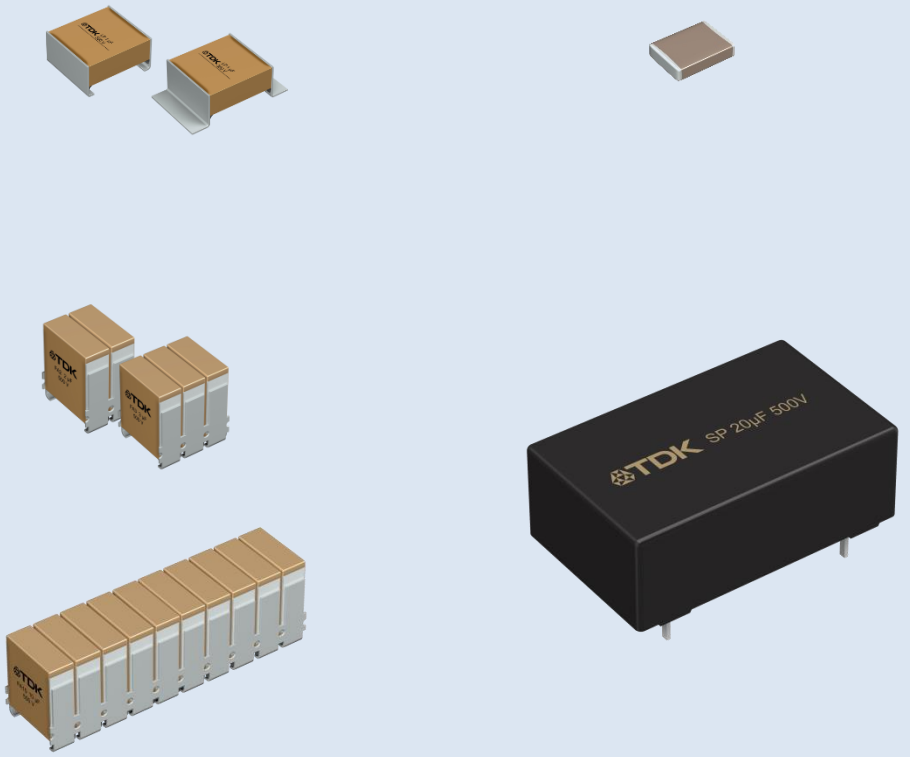
- 500 V component with
  - ¬ $C_{nom, typ}$: 250 nF
  - ¬ I_{RMS} @100 kHz and 85 °C: about 5 A for standard termination, -5% (max.) for soft termination



Summary

Key benefits of CeraLink®

- Effective capacitance increases with rising voltage and leads to **high capacitance density**
- **Low ESL** and low inductive connection
- **Low ESR** especially at high frequencies and high temperatures
- **High current density**
- **High operating and peak temperatures** with temperature excursions up to 150 °C
- **High robustness against high temperatures**
- Supports **fast-switching semiconductors** and high switching frequencies
- Supports further **miniaturization** of power electronics at the system level



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