

DATA SHEET

SURFACE MOUNT MULTILAYER CERAMIC CAPACITORS

Embedded Capacitance

Class 2, X5R

4 V TO 25 V

10 nF to 220 nF

RoHS compliant & Halogen free



YAGEO

Product Specification – May 24, 2024 v.0



SCOPE

The thickness and termination dimension can be customized for the purpose of embedded the MLCCs into substrates under the ICs.

APPLICATIONS

IC design
Module

FEATURES

- To save space for module assembly.
- To reduce parasitic inductance.
- To ensure good electrical bonding with advanced.
- Cu termination technologies.

ORDERING INFORMATION - GLOBAL PART NUMBER, PHYCOMPCTC & I2NC

All part numbers are identified by the series, size, tolerance, TC material, packing style, voltage, process code, termination and capacitance value.

YAGEO BRAND ordering code**GLOBAL PART NUMBER (PREFERRED)**

CE XXXX X X X5R X BB XXX

(1) (2) (3) (4) (5) (6)

(1) SIZE – INCH BASED (METRIC)

01 : 0201 (0603)

02 : 0402 (1005)

(2) THICKNESS

1B = 0.13 ±0.02mm

2B = 0.2 ±0.02mm

(3) TOLERANCE

K = ±10%

M = ±20%

(4) PACKING STYLE

R = Paper taping reel; Reel 7 inch

(5) RATED VOLTAGE

4 = 4 V

5 = 6.3 V

6 = 10 V

7 = 16 V

8 = 25 V

(6) CAPACITANCE VALUE

2 significant digits+number of zeros

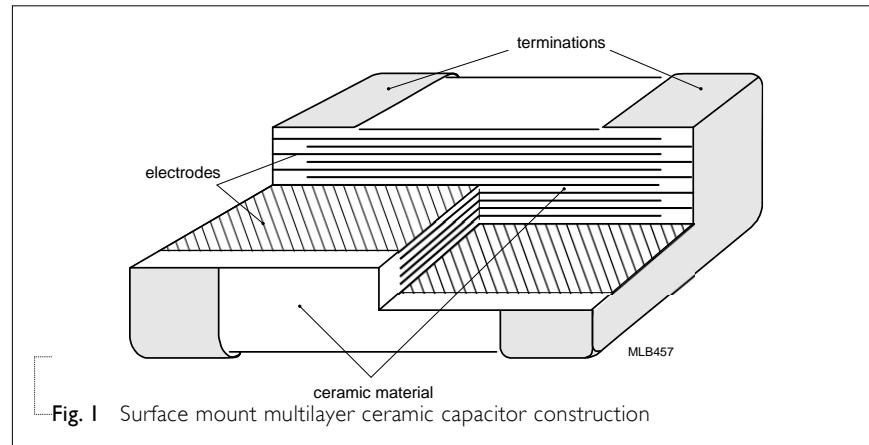
The 3rd digit signifies the multiplying factor, and letter R is decimal point

Example: 103 = $10 \times 10^3 = 10,000 \text{ pF} = 10 \text{ nF}$

CONSTRUCTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated copper. A cross section of the structure is shown in Fig.1.



DIMENSION

Table I For outlines see fig. 2

TYPE	L ₁ (mm)	W (mm)	T (mm)	L ₂ / L ₃ (mm)		L ₄ (mm) min.
				min.	max.	
0201	0.6 ±0.09	0.3 ±0.09	Refer to Table 2	0.1	0.25	0.2
0402	1.0 ±0.2	0.5 ±0.2		0.15	0.35	0.3

OUTLINES

For dimension see Table I

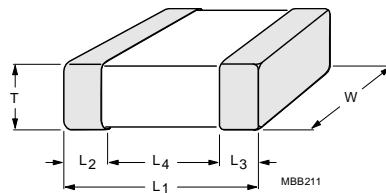


Fig. 2 Surface mount multilayer ceramic capacitor dimension

CAPACITANCE RANGE & THICKNESS FOR X5R

Table 2 Sizes from 0201 to 0402

CAP.	0201					0402				
	4 V	6.3 V	10 V	16 V	25 V	4 V	6.3 V	10 V	16 V	25 V
10 nF	0.13±0.02									
100 nF	0.2±0.02	0.2±0.02				0.13±0.02				
220 nF	0.2±0.02									

NOTE

1. Values in shaded cells indicate thickness class in mm

THICKNESS CLASSES AND PACKING QUANTITY

Table 3

SIZE CODE	THICKNESS CLASSIFICATION	TAPE WIDTH	Ø180 MM / 7 INCH		Ø330 MM / 13 INCH		QUANTITY PER BULK CASE
			Paper	Blister	Paper	Blister	
0201	0.15 mm max 0.22 mm max	8 mm	15,000	---	50,000	---	---
0402	0.15 mm max 0.22 mm max	8 mm	10,000	---	50,000	---	---

ELECTRICAL CHARACTERISTICS**X5R DIELECTRIC CAPACITORS; NISN TERMINATIONS**

Unless otherwise specified, all tests and measurements shall be made under standard atmospheric conditions for testing as given in 5.3 of IEC 60068-1:

- Temperature: 15 ° C to 35 ° C
- Relative humidity: 25% to 75%
- Air pressure: 86 kPa to 106 kPa

Before the measurements are made, the capacitor shall be stored at the measuring temperature for a time sufficient to allow the entire capacitor to reach this temperature.

The period as prescribed for recovery at the end of a test is normally sufficient for this purpose.

Table 4

DESCRIPTION	VALUE
Capacitance range	10 nF to 220 nF
Capacitance tolerance	±10% and ±20%
Dissipation factor (D.F.)	≤10%
Insulation resistance after 1 minute at Ur (DC)	Rins ≥ 10 GΩ or Rins × Cr ≥ 50 seconds whichever is less
Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):	±15%
Operating temperature range:	-55 °C to +85 °C

TESTS AND REQUIREMENTS**Table 5** Test procedures and requirements

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Mounting	IEC 60384- 21/22	4.3 The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage
Visual Inspection and Dimension Check	4.4	Any applicable method using $\times 10$ magnification	In accordance with specification
Capacitance ⁽¹⁾	4.5.1	Class 2:	Within specified tolerance
Dissipation Factor (D.F.) ⁽¹⁾	4.5.2	At 20 °C, 24 hrs after annealing Cap $\leq 1 \mu\text{F}$, f = 1 KHz, measuring at voltage 1 Vrms at 20 °C Cap $> 1 \mu\text{F}$, f = 1 KHz for C $\leq 10 \mu\text{F}$, rated voltage $> 6.3 \text{ V}$, measuring at voltage 1 Vrms at 20 °C f = 1 KHz, for C $\leq 10 \mu\text{F}$, rated voltage $\leq 6.3 \text{ V}$, measuring at voltage 0.5 Vrms at 20 °C f = 120 Hz for C $> 10 \mu\text{F}$, measuring at voltage 0.5 Vrms at 20 °C	
Insulation Resistance	4.5.3	At U _r (DC) for 1 minute	In accordance with specification

NOTE

- I. The figure indicates typical inspection. Please refer to individual specifications.

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS												
Temperature Characteristic	4.6	<p>Capacitance shall be measured by the steps shown in the following table.</p> <p>The capacitance change should be measured after 5 min at each specified temperature stage.</p> <table border="1"> <thead> <tr> <th>Step</th><th>Temperature(°C)</th></tr> </thead> <tbody> <tr> <td>a</td><td>25±2</td></tr> <tr> <td>b</td><td>Lower temperature±3°C</td></tr> <tr> <td>c</td><td>25±2</td></tr> <tr> <td>d</td><td>Upper Temperature±2°C</td></tr> <tr> <td>e</td><td>25±2</td></tr> </tbody> </table> <p>(1) Class I</p> <p>Temperature Coefficient shall be calculated from the formula as below</p> $\text{Temp, Coefficient} = \frac{C_2 - C_1}{C_1 \times \Delta T} \times 10^6 \text{ [ppm/°C]}$ <p>C1: Capacitance at step c C2: Capacitance at 125°C ΔT: 100°C (=125°C -25°C)</p> <p>(2) Class II</p> <p>Capacitance Change shall be calculated from the formula as below</p> $\Delta C = \frac{C_2 - C_1}{C_1} \times 100\%$ <p>C1: Capacitance at step c C2: Capacitance at step b or d</p>	Step	Temperature(°C)	a	25±2	b	Lower temperature±3°C	c	25±2	d	Upper Temperature±2°C	e	25±2	<p>Class2: X5R: $\Delta C/C: \pm 15\%$</p> <p>Measurement Voltage: Less than 1.0Vrms</p>
Step	Temperature(°C)														
a	25±2														
b	Lower temperature±3°C														
c	25±2														
d	Upper Temperature±2°C														
e	25±2														
Adhesion	4.7	A force applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate	<p>Force size ≥ 0603: 5N size = 0402: 2.5N size = 0201: 1N</p>												
Rapid Change of Temperature	IEC 60384-21/22	<p>4.11 Preconditioning: 150 +0/-10 °C for 1 hour, then keep for 24 ±1 hours at room temperature</p> <p>5 cycles with following detail: 30 minutes at lower category temperature 30 minutes at upper category temperature</p> <p>Recovery time 24 ±2 hours</p>	<p>No visual damage $\Delta C/C$ Class2: X5R: $\pm 15\%$</p> <p>D.F. meet initial specified value R_{ins} meet initial specified value</p>												

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Voltage Proof	IEC 60384-1 4.6	<ol style="list-style-type: none"> 1. Specified stress voltage applied for 1~5 seconds 2. $U_r \leq 100$ V: series applied 2.5 U_r 3. $100 V < U_r \leq 200$ V series applied ($1.5 U_r + 100$) 4. $200 V < U_r \leq 500$ V series applied ($1.3 U_r + 100$) <p>Charge/Discharge current is less than 50 mA</p>	No breakdown or flashover
Endurance	4.14	<ol style="list-style-type: none"> 1. Preconditioning, class 2 only: $150 +0/-10$ °C / 1 hour, then keep for 24 ± 1 hour at room temp 2. Initial measure: Spec: refer to initial spec C, D, IR 3. Endurance test: Temperature: X5R: 85 °C Specified stress voltage applied $1.5 \times U_r$ for 1,000 hours 4. Recovery time: 24 ± 2 hours 5. Final measure: C, D, IR <p>P.S. If the capacitance value is less than the minimum value permitted, then after the other measurements have been made the capacitor shall be preconditioned according to "IEC 60384 4.1" and then the requirements shall be met.</p>	<p>No visual damage</p> <p>ΔC/C</p> <p>Class2: X5R: $\pm 15\%$</p> <p>D.F.</p> <p>Class2: X5R: $2 \times$ initial value</p> <p>R_{ins}</p> <p>Class2: $R_{ins} \times C_r \geq 10s$ whichever is less</p>

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 0	May 24, 2024	-	- New datasheet for embedded capacitance X5R series with RoHS compliant

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