Cyclone® 10 GX Device Overview

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Intel® Cyclone® 10 GX Device Overview

The Intel® Cyclone® 10 GX device family consists of high-performance and power-efficient 20 nm low cost FPGAs.

Intel Cyclone 10 GX device family delivers higher core, transceiver, and I/O performance than the previous generation of low cost FPGAs.

The Intel Cyclone 10 GX devices are ideal for high bandwidth, low-cost applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Cyclone 10 GX Devices

Market	Applications
Industrial	• Machine vision • Robotics • Programmable logic controller and drivers
Broadcast	Professional audiovisual

Key Advantages of Intel Cyclone 10 GX Devices

Table 2. Key Advantages of the Intel Cyclone 10 GX Device Family

Advantage	Supporting Feature
Enhanced core architecture	• Built on TSMC's 20 nm process technology • Twice the performance of the previous generation of low cost FPGAs
High-bandwidth integrated transceivers	• Short-reach rates up to 12.5 Gigabits per second (Gbps) • Backplane capability up to 6.6 Gbps • Hard PCI Express IP blocks supporting up to Gen2 ×4 applications
Improved logic integration and hard IP blocks	• 8-input adaptive logic module (ALM) • Up to 11.74 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks • Fractional synthesis phase-locked loops (PLLs) • Hard memory controllers and PHY up to 1,866 Megabits per second (Mbps)
Advanced power savings	• Comprehensive set of advanced power saving features • Power-optimized MultiTrack routing and core architecture

Summary of Intel Cyclone 10 GX Features

Table 3. Summary of Features for Intel Cyclone 10 GX Devices

Feature	Description	
Technology	TSMC's 20-nm process technology	
Packaging	• 1.0 mm ball-pitch FineLine BGA packaging • 0.8 mm ball-pitch Ultra FineLine BGA packaging • Multiple devices with identical package footprints for seamless migration between different FPGA densities • RoHS6-compliance	
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved multi-track routing architecture to reduce congestion and improve compilation time • Hierarchical core clocking architecture • Fine-grained partial reconfiguration	
Internal memory blocks	• M20K—20-Kb memory blocks with hard error correction code (ECC), cascadable • Memory logic array block (MLAB)—640-bit memory, cascadable	
Embedded Hard IP blocks	Variable-precision DSP	• Native support for signal processing precision levels from 18 x 19 to 54 x 54, cascadable • Native support for 27 x 27 multiplier mode • 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) • Internal coefficient memory banks • Preadder/subtractor for improved efficiency • Additional pipeline register to increase performance and reduce power • Supports floating point arithmetic: — Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication. — Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability. — Dynamic accumulator reset control. — Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.
	Memory controller	DDR3, DDR3L, and LPDDR3
	PCI Express®	PCI Express (PCIe®) Gen2 (x1, x2, or x4) and Gen1 (x1, x2, or x4) hard IP with complete protocol stack, endpoint, and root port.
	Transceiver I/O	• PCS hard IPs that support: — 10 Gbps Ethernet (10GbE) (1) — PCIe PIPE interface — Interlaken — Gbps Ethernet (GbE) — 6G Common Public Radio Interface (CPRI) with deterministic latency support — Gigabit-capable passive optical network (GPON) with fast lock-time support • 12G Serial Digital Interface (SDI) • 8B/10B, 64B/66B, 64B/67B encoders and decoders • Custom mode support for proprietary protocols

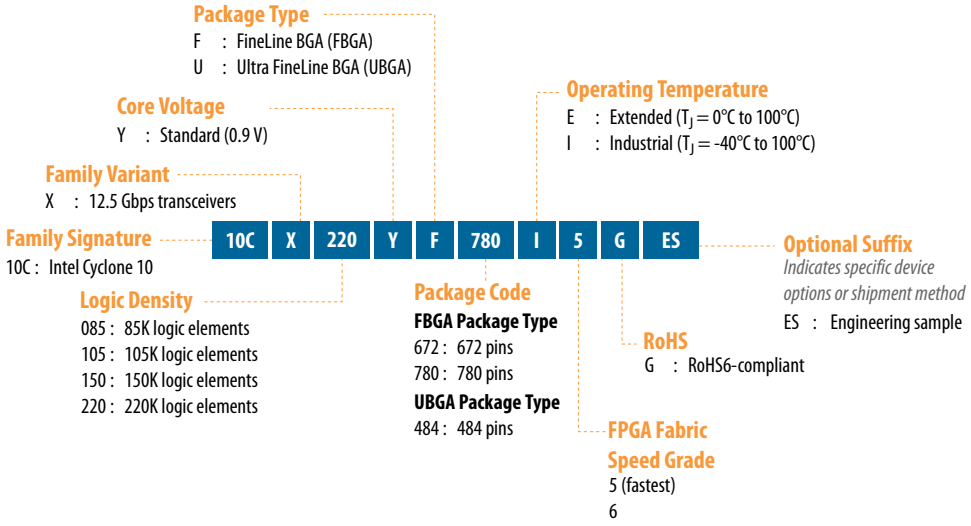
continued...

(1) 10GBASE-KR is not supported.

Feature	Description
Core clock networks	• Up to 300 MHz fabric clocking, depending on the application: — 467 MHz external memory interface clocking with 1,866 Mbps DDR3 interface — 300 MHz LVDS interface clocking with 1.434 Gbps LVDS interface • Global, regional, and peripheral clock networks • Clock networks that are not used can be gated to reduce dynamic power
Phase-locked loops (PLLs)	• High-resolution fractional synthesis PLLs: — Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB) — Support integer mode and fractional mode — Fractional mode support with third-order delta-sigma modulation • Integer PLLs: — Adjacent to general purpose I/Os — Support external memory and LVDS interfaces
FPGA General-purpose I/Os (GPIOs)	• One 3 V I/O bank supporting up to 3.0 V I/O standards • Up to 1.434 Gbps LVDS—every pair can be configured as receiver or transmitter • On-chip termination (OCT) • 1.2 V to 3.0 V single-ended LVTTL/LVCMOS interfaces using LVDS I/O or 3 V I/O banks
External Memory Interface	• Hard memory controller—DDR3, DDR3L, and LPDDR3 support • DDR3 speeds up to 933 MHz/1,866 Mbps
Low-power serial transceivers	• Continuous operating range up to 12.5 Gbps • Backplane support up to 6.6 Gbps • Extended range down to 125 Mbps with oversampling • ATX transmit PLLs with user-configurable fractional synthesis capability • Transmitter pre-emphasis and de-emphasis • Dynamic reconfiguration of individual transceiver channels
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced 256-bit advanced encryption standard (AES) design security with authentication • Configuration via protocol (CvP) using PCIe Gen1 or Gen2 • Dynamic reconfiguration of the transceivers and PLLs • Fine-grained partial reconfiguration of the core fabric • Active Serial ×4 Interface
Power management	• Programmable Power Technology • Intel Quartus® Prime Pro Edition integrated power analysis tool
Software and tools	• Intel Quartus Prime Pro Edition design suite • Transceiver toolkit • Platform Designer (Standard) system integration tool • DSP Builder advanced blockset • OpenCL* support

Intel Cyclone 10 GX Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Cyclone 10 GX Devices



Intel Cyclone 10 GX Maximum Resources

Table 4. Maximum Resource Counts for Intel Cyclone 10 GX Devices

Resource		Product Line			
		10CX085	10CX105	10CX150	10CX220
Logic Elements (LE) (K)		85	104	150	220
ALM		31,000	38,000	54,770	80,330
Register		124,000	152,000	219,080	321,320
Memory (Kb)	M20K	5,820	7,640	9,500	11,740
	MLAB	653	799	1,152	1,690
Variable-precision DSP Block		84	125	156	192
18 x 19 Multiplier		168	250	312	384
Hard Floating-point Arithmetic		Yes	Yes	Yes	Yes
PLL	Fractional Synthesis	2	4	4	4
	I/O	4	6	6	6
12.5 Gbps Transceiver		6	12	12	12
GPIO (2)		216	284	284	284
LVDS Pair (3)		84	118	118	118
PCIe Hard IP Block		1	1	1	1
Hard Memory Interfaces		1	2	2	2

Intel Cyclone 10 GX Package Plan

Table 5. Package Plan for Intel Cyclone 10 GX Devices

The GPIO numbers include the I/O pins in the LVDS and 3 VI/O banks. In each device package, there is one 3 VI/O bank (48 pins).

Product Line	Type	U484 484-pin UBGA			F672 672-pin FBGA			F780 780-pin FBGA		
	Size	19 mm × 19 mm			27 mm × 27 mm			29 mm × 29 mm		
	Ball Pitch	0.8 mm			1.0 mm			1.0 mm		
	I/O Type	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR
10CX085		188	70	6	216	84	6	—	—	—
10CX105		188	70	6	236	94	10	284	118	12
10CX150		188	70	6	236	94	10	284	118	12
10CX220		188	70	6	236	94	10	284	118	12

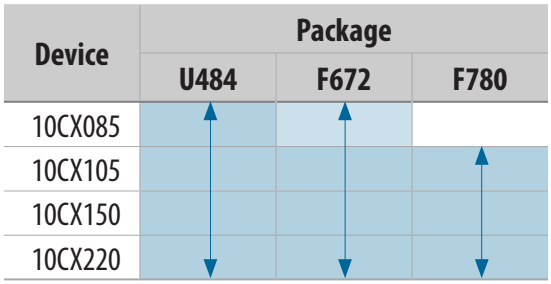
(2) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime Pro Edition software, the number of user I/Os includes transceiver I/Os.

(3) Each LVDS I/O pair can be used as differential input or output.

I/O Vertical Migration for Intel Cyclone 10 GX Devices

Figure 2. Migration Capability Across Intel Cyclone 10 GX Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.



Note: To verify the pin migration compatibility, use the Pin Migration View window in the Intel Quartus Prime Pro Edition software Pin Planner.

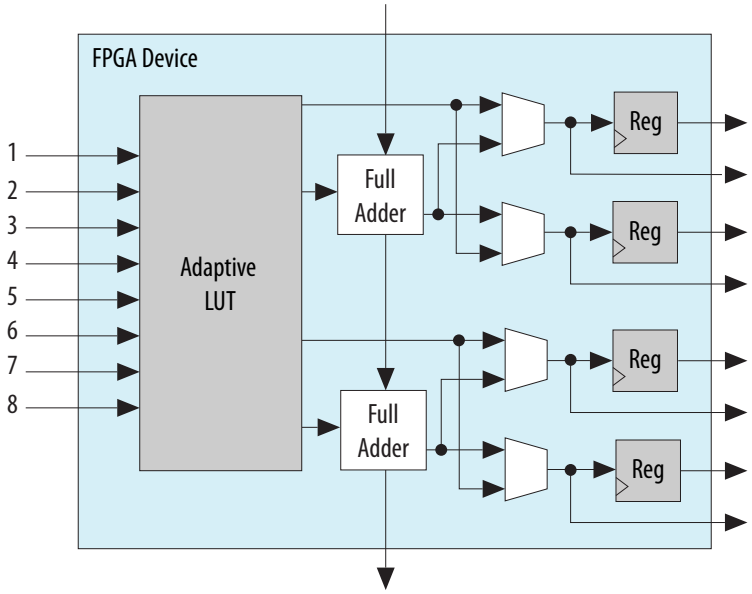
Adaptive Logic Module

Intel Cyclone 10 GX devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

Figure 3. ALM for Intel Cyclone 10 GX Devices



The Intel Quartus Prime Pro Edition software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Cyclone 10 GX ALM architecture.

Variable-Precision DSP Block

The Intel Cyclone 10 GX variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support

Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 6. Variable-Precision DSP Block Configurations for Intel Cyclone 10 GX Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 7. Resources for Fixed-Point Arithmetic in Intel Cyclone 10 GX Devices

Device	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18×19 Multiplier Adder Sum Mode	18×18 Multiplier Adder Summed with 36-bit Input
		18×19 Multiplier	27×27 Multiplier		
10CX085	84	168	84	84	84
10CX105	125	250	125	125	125
10CX150	156	312	156	156	156
10CX220	192	384	192	192	192

Table 8. Resources for Floating-Point Arithmetic in Intel Cyclone 10 GX Devices

Device	Variable-precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single-Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating-Point Operations per Second (GFLOPs)
10CX085	84	84	84	84	76
10CX105	125	125	125	125	113
10CX150	156	156	156	156	140
10CX220	192	192	192	192	173

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Types of Embedded Memory

The Intel Cyclone 10 GX devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Cyclone 10 GX devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Intel Cyclone 10 GX Devices

Table 9. Embedded Memory Capacity and Distribution in Intel Cyclone 10 GX Devices

Product Line	M20K		MLAB		Total RAM Bit (Kb)
	Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
10CX085	291	5,820	1,044	653	6,473
10CX105	382	7,640	1,278	799	8,439
10CX150	475	9,500	1,843	1,152	10,652
10CX220	587	11,740	2,704	1,690	13,430

Embedded Memory Configurations for Single-port Mode

Table 10. Single-port Embedded Memory Configurations for Intel Cyclone 10 GX Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 (4)	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8

continued...

(4) Supported through software emulation and consumes additional MLAB blocks.

Memory Block	Depth (bits)	Programmable Width
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Cyclone 10 GX core clock networks are capable of up to 300 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 1,866 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime Pro Edition software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Cyclone 10 GX devices contain up to 4 fractional synthesis PLLs and up to 6 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Cyclone 10 GX devices support PLL-to-PLL cascading.

FPGA General Purpose I/O

Intel Cyclone 10 GX devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - One 3 V I/O bank that supports up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.434 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

Related Information

I/O and Differential I/O Buffers in Intel Cyclone 10 GX Devices, Intel Cyclone 10 GX Core Fabric and General Purpose I/Os Handbook
Provides more information about the GPIOs in Intel Cyclone 10 GX devices.

External Memory Interface

Intel Cyclone 10 GX devices offer external memory bandwidth of up to 1×72-bit or 2×40-bit DDR3 memory interfaces running at up to 1,866 Mbps. This bandwidth provides ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Cyclone 10 GX FPGAs delivers the highest performance and ease of use. You can configure up to a maximum width of 72 bits when using the hard memory controllers.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontroller based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Cyclone 10 GX device to compensate for any changes in process, voltage, or temperature either within the Intel Cyclone 10 GX device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

Memory Standards Supported by Intel Cyclone 10 GX Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

Table 11. Memory Standards Supported by the Hard Memory Controller

This table lists the capability of the hard memory controller and the maximum speed achievable in different I/O bank types. For specific details, refer to the External Memory Interface Spec Estimator and Intel Cyclone 10 GX Device Datasheet.

Memory Standard	Rate Support	Device Speed Grade	Ping Pong PHY Support	Frequency (MHz)	
				LVDS I/O Bank	3 V I/O Bank
DDR3 SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
				933	450
		–6	Yes	933	333
				933	333
DDR3L SDRAM	Half rate	–5	Yes	533	225
			—	533	225
		–6	Yes	466	166
			—	466	166
	Quarter rate	–5	Yes	933	450
			—	933	450
		–6	Yes	933	333
			—	933	333
LPDDR3	Half rate	–5	—	400	225

continued...

Memory Standard	Rate Support	Device Speed Grade	Ping Pong PHY Support	Frequency (MHz)	
				LVDS I/O Bank	3 V I/O Bank
		–6	—	333	166
	Quarter rate	–5	—	800	450
		–6	—	666	333

PCIe Gen1 and Gen2 Hard IP

Intel Cyclone 10 GX devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen2 Endpoint and Root Port in x1, x2, or x4 lane configuration(5).
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Cyclone 10 GX device completes loading the programming file for the rest of the FPGA.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen2 or Gen1 speed.

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Intel Cyclone 10 GX enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 12.5 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Cyclone 10 GX devices.

10 Gbps Ethernet Support

The Intel Cyclone 10 GX enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks. This simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.

(5) For the PCIe hard IP, only x2 lane configuration is available for the U484 package of the 10CX085, 10CX105, 10CX150, and 10CX220 devices, and the F672 package of the 10CX085 device.

Low Power Serial Transceivers

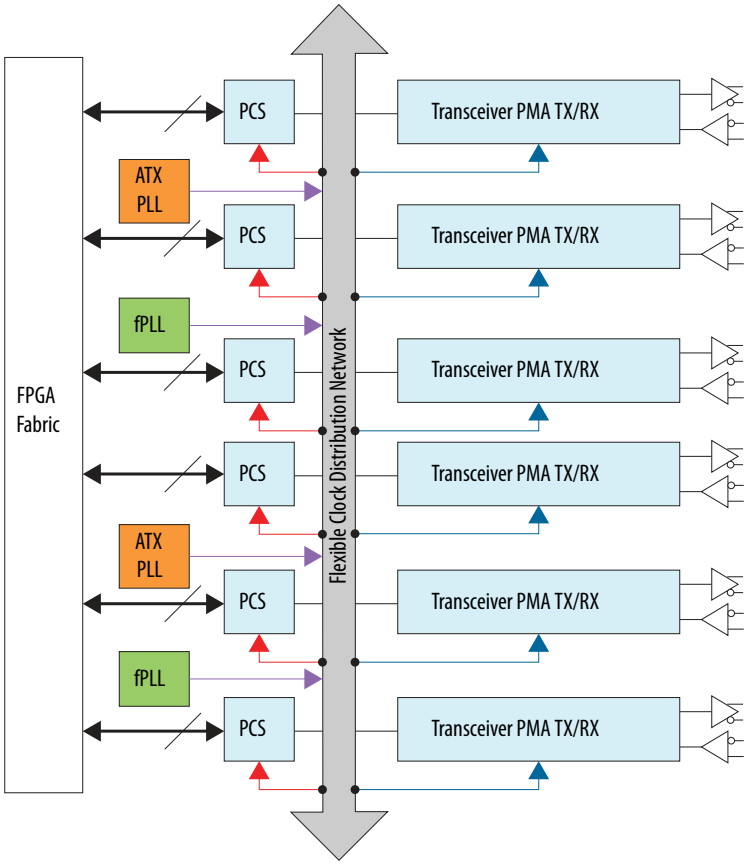
Intel Cyclone 10 GX FPGAs offer transceivers that deliver high bandwidth, throughput, and low latency at very low power consumption per channel. The transceivers support various data rates from 125 Mbps up to 12.5 Gbps in chip-to-chip applications.

- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 12 transceiver channels
- All channels feature continuous data rate support up to the maximum rated speed

Figure 4. Intel Cyclone 10 GX Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

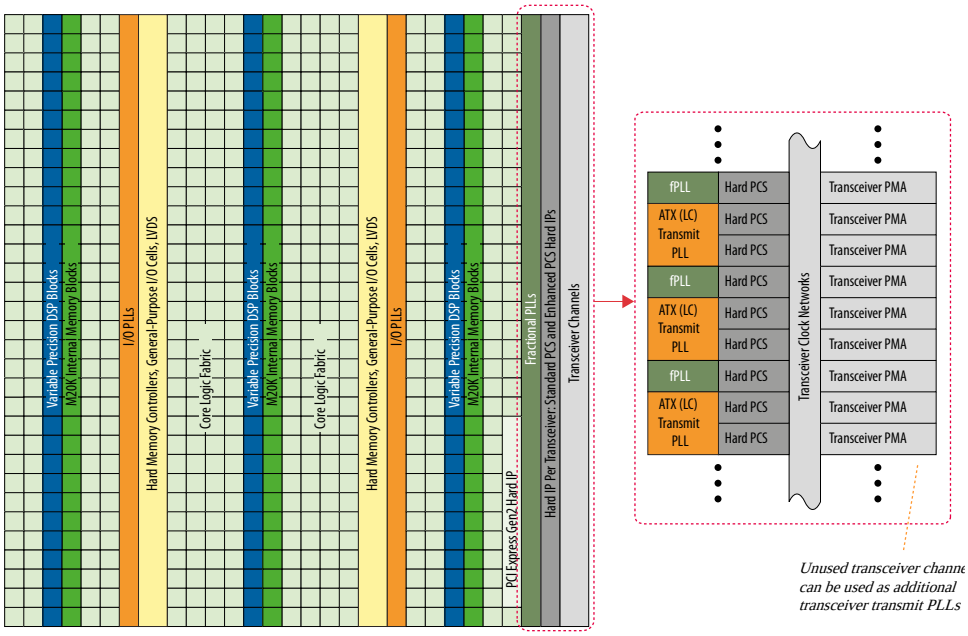
- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 4 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network.

Figure 5. Device Chip Overview for Intel Cyclone 10 GX Devices

This figure is a graphical representation of a top view of the silicon die, which corresponds to a reverse view for flip chip packages. Different Intel Cyclone 10 GX devices may have different floorplans than the one shown in this figure.



PMA Features

Intel Cyclone 10 GX transceivers provide exceptional signal integrity at data rates up to 12.5 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel.

Table 12. PMA Features of the Transceivers in Intel Cyclone 10 GX Devices

Feature	Capability
Chip-to-Chip Data Rates	125 Mbps to 12.5 Gbps
Backplane Support	Drive backplanes at data rates up to 6.6 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
	continued...

Feature	Capability
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	High-gain linear receive equalization to compensate for system channel loss
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

You can use the transceiver PCS to support a wide range of protocols ranging from 125 Mbps to 12.5 Gbps.

Table 13. PCS Features of the Transceivers in Intel Cyclone 10 GX Devices

This table summarizes the Intel Cyclone 10 GX transceiver PCS features.

PCS	Description
Standard PCS	• Operates at a data rate up to 12.5 Gbps • Supports protocols such as PCI-Express, CPRI 4.2+, and GigE • Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.
Enhanced PCS	• Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA • Handles data transfer to and from the FPGA fabric • Handles data transfer internally to and from the PMA • Provides frequency compensation • Performs channel bonding for multi-channel low skew applications
PCIe Gen2 PCS	• Supports the seamless switching of Data and Clock between the Gen1 and Gen2 data rates • Provides support for PIPE 3.0 features • Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed

PCS Protocol Support

Table 14. Protocols Supported by Intel Cyclone 10 GX Transceiver PCS

This table lists some of the protocols supported by the Intel Cyclone 10 GX transceiver PCS.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen2 x1, x2, x4	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS
1000BASE-X Gigabit Ethernet with IEEE 1588v2	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R with IEEE 1588v2	10.3125	Native PHY	Enhanced PCS
Interlaken (CEI-6G-SR/CEI-11G-SR)	3.125 to 12.5	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	6.25	Native PHY	Enhanced PCS
12G SDI	11.88	Native PHY	Enhanced PCS
CPRI 6.0 (64B/66B)	0.6144 to 6.144	Native PHY	Enhanced PCS
CPRI 4.2 (8B/10B)	0.6144 to 6.144	Native PHY	Standard PCS
OBSAI RP3 v4.2	0.6144 to 6.144	Native PHY	Standard PCS
SD-SDI/HD-SDI/3G-SDI	0.143[6] to 2.97	Native PHY	Standard PCS

Dynamic and Partial Reconfiguration

The Intel Cyclone 10 GX devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

(6) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime Pro Edition design software, making such time-intensive task simple.

Intel Cyclone 10 GX devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)].
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interfaces.

Enhanced Configuration and Configuration via Protocol

Table 15. Configuration Schemes and Features of Intel Cyclone 10 GX Devices

Intel Cyclone 10 GX devices support 1.8 V programming voltage and several configuration schemes.

Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) (7)	Decompression	Design Security (8)	Partial Reconfiguration (9)	Remote System Update
JTAG	1 bit	33	33	—	—	Yes(10)	—
Active Serial (AS) through the EPCQ-L configuration device	1 bit, 4 bits	100	400	Yes	Yes	Yes(10)	Yes
Passive serial (PS) through CPLD or external microcontroller	1 bit	100	100	Yes	Yes	Yes(10)	Parallel Flash Loader (PFL) IP core
Fast passive parallel (FPP) through CPLD or external microcontroller	8 bits	100	3200	Yes	Yes	Yes(11)	PFL IP core
	16 bits			Yes	Yes		
	32 bits			Yes	Yes		
Configuration via Protocol [CvP (PCIe)]	x1, x2, x4 lanes	—	5000	Yes	Yes	Yes(10)	—

(7) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Cyclone 10 GX Device Datasheet for more information.

(8) Encryption and compression cannot be used simultaneously.

(9) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(10) Partial configuration can be performed only when it is configured as internal host.

(11) Supported at a maximum clock rate of 100 MHz.

You can configure Intel Cyclone 10 GX devices through PCIe using Configuration via Protocol (CvP). The Intel Cyclone 10 GX CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Intel Cyclone 10 GX devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Cyclone 10 GX CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

Intel Cyclone 10 GX devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption.

Intel Cyclone 10 GX devices use Programmable Power Technology for power reduction. The Intel Quartus Prime Pro Edition software identifies non-critical timing paths and biases the logic in these paths for low power instead of high performance

Furthermore, Intel Cyclone 10 GX devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Intel Quartus Prime Pro Edition software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Cyclone 10 GX devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History for Intel Cyclone 10 GX Device Overview

Document Version	Changes
2019.04.01	Added support for partial reconfiguration.
2019.01.01	Updated I/O resource count for package F672 of the 10CX085 device.
2018.07.11	Removed mentions of Single Root I/O Virtualization (SR-IOV). The Intel Cyclone 10 GX devices do not support SR-IOV.
2018.05.07	Added footnote to the PCIe hard IP topic to list device and package combinations that support only x2 lane configuration.

Date	Version	Changes
November 2017	2017.11.06	• The document is no longer preliminary. • Updated the 10 Gbps Ethernet Support section. • Updated the features supported in the PMA Features of the Transceivers in Intel Cyclone 10 GX Devices table. • Removed automotive support. • Removed the note about the migration paths in the I/O Vertical Migration for Intel Cyclone 10 GX Devices.
May 2017	2017.05.08	Initial release.