

AC/DC Controller IC

CRM Totem Pole PFC Controller IC

BM85060FV

General Description

The BM85060FV is a critical conduction mode (CRM) power factor correction (PFC) controller IC designed to drive a bridgeless totem pole PFC topology. Bridgeless totem pole PFC consists of two totem pole legs: a fast-switching leg driven at high switching frequencies and a second leg operating at AC line frequency. This topology eliminates the need for a diode bridge, which is essential in conventional PFC circuits, and significantly improves efficiency and power density.

Key Specifications

- Operating Power Supply Voltage Range
 VCC Pin Voltage: 8.0 V to 36 V (rated 40 V)
 HV Pin Voltage: 80 V to 600 V
- Frequency Range: 25 kHz to 1 MHz
- Operating Temperature Range: -40 °C to +125 °C

Package

SSOP-B20

W (Typ) x D (Typ) x H (Max)

6.5 mm x 6.4 mm x 1.45 mm

Features

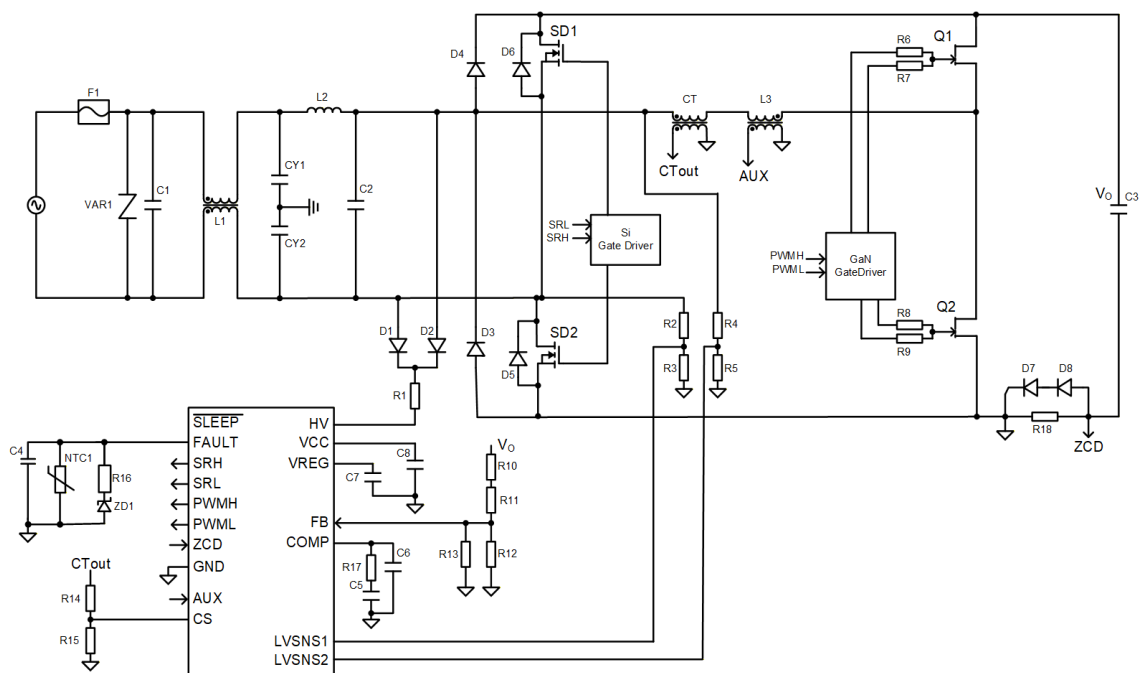
- Critical Conduction Mode (CRM) and Discontinuous Conduction Mode (DCM) Operation
- Burst Mode Operation at Very Light Loads
- Brownout Detection
- X Capacitor Discharge Function
- High Voltage Startup
- Dynamic Response Enhancer
- Protections
 - Output Over Voltage Protection (Fast Over Voltage, Second Over Voltage)
 - Output Under Voltage Protection (UVP)
 - Input Over Voltage Protection (VAC OVP)
 - Overload and Peak Current Limit Protection (Peak Current Limit, Soft Over Current)
 - Inrush Current Limit
 - Open Loop Detection
 - Internal TSD
 - AC Voltage Sudden Change Detection
 - Negative Over Current Limiter



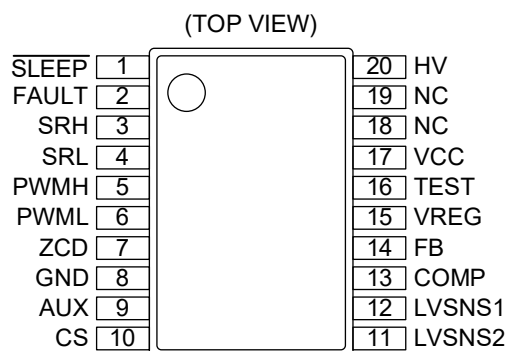
Applications

- Power Supplies for 5G / Telecom
- Power Supplies for Industrial Applications
- Power Supplies for Gaming Consoles
- Ultra-High Definition (UHD) Power Supplies
- Commercial Power Supplies

Typical Application Circuit



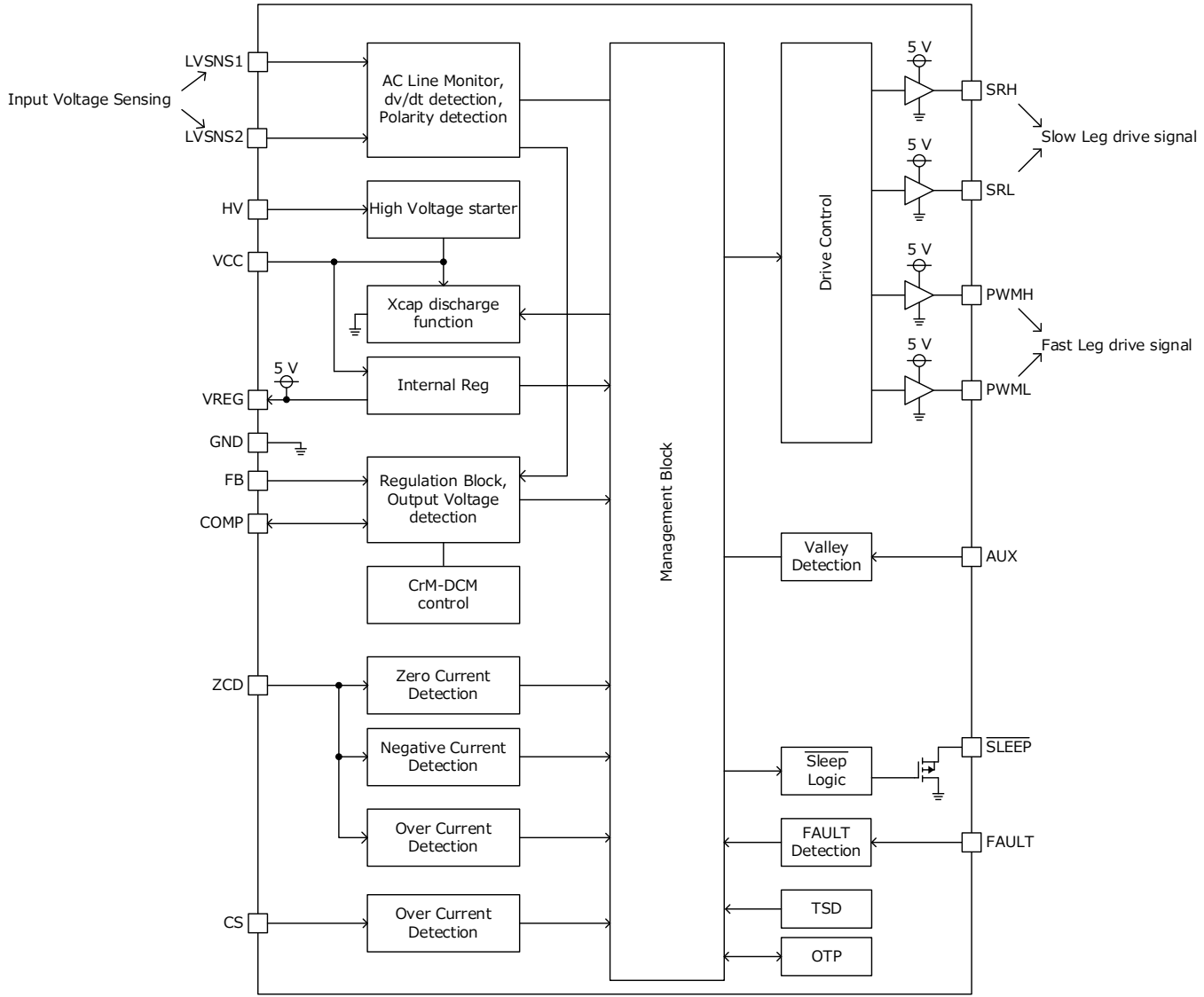
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	SLEEP	I	The pin is held high after VCC UVLO is released except SLEEP or burst mode condition. When burst mode condition is satisfied, this pin is held low immediately.
2	FAULT	O	Dedicated fault trigger pin.
3	SRH	O	Control signal for high side Slow Leg device.
4	SRL	O	Control signal for low side Slow Leg device.
5	PWMH	O	PWM logic level output for control of high side Fast Leg switch.
6	PWML	O	PWM logic level output for control of low side Fast Leg switch.
7	ZCD	I	The pin senses the inductor downslope current and short-circuit current of half-bridge.
8	GND	-	Ground connection
9	AUX	I	The pin is used to monitor the switch node resonance on the auxiliary winding and enable valley turn-on during CRM.
10	CS	I	Connected to current sensing transformer. Current limit is based on the signal on this pin.
11	LVSNS2	I	Low voltage input for AC line voltage monitoring. The LVSNS2 resistor divider should be connected to the neutral of the AC line voltage.
12	LVSNS1	I	Low voltage input for AC line voltage monitoring. The LVSNS1 resistor divider should be connected to AC line side of the boost inductor.
13	COMP	I	Connection pin to the loop compensation network.
14	FB	I	This pin senses the PFC output voltage for loop regulation.
15	VREG	I	Internal regulator output. Capacitor must be connected.
16	TEST	I	Test pin. This pin must be connected to ground.
17	VCC	I	Bias supply input
18	NC	-	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
19	NC	-	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
20	HV	I	High voltage startup and X capacitor discharge function.

Block Diagram



Description of Blocks

1 Basic Operation of Totem Pole PFC

The Totem Pole PFC (TPPFC) circuit consists of two half-bridges, “Fast Leg” switches at the PWM frequency and “Slow Leg” switches at the AC line frequency.

Fast Leg switches perform the role of switches and diodes in conventional boost-type PFC.

In other words, these switches adjust the output voltage and shape the input current to achieve high power factor and low harmonic distortion.

Slow Leg switches perform the role of the diode bridge in a classical boost PFC.

Efficiency is improved by using low on-resistance active switches instead of diodes.

The TPPFC operates with bidirectional current flow in the inductor, and the command of the fast and Slow Leg switches change depending on the polarity of the AC line cycle.

Operation of the TPPFC during the positive and negative half line cycles is shown in Figure 1.

positive AC line cycle:

During the positive AC line cycle the PWML signal is responsible for performing pulse width modulation or duty cycle control of the converter.

PWML toggles high turning on the low side Fast Leg device, allowing current to charge and store energy in the inductor, as shown (1) in Figure 1.

When the PWML signal toggles low the inductor current diverts through the high side Fast Leg switch, transferring energy from the inductor to the load, as shown (2) in Figure 1.

In this half line cycle the high side Fast Leg device does not need to conduct for proper PFC operation, however the PWMH signal can toggle high turn on the high side device, providing enhanced system efficiency at medium to high load levels.

Throughout the positive half line cycle current is flowing left to right through the inductor and always returning to the source through the low side Slow Leg device, hence the SRL signal can toggle high to turn on the low side Slow Leg device for optimum converter efficiency.

negative AC line cycle:

During a negative AC line cycle, the following points change from a positive AC line cycle.

The roles of PWMH and PWML are interchanged.

The roles of SRH and SRL are interchanged. The direction of the inductor current is reversed.

In summary:

Positive Half Cycle Operation

Output PWM (d) signal to the PWML pin

Output SYNC (1-d) signal to the PWMH pin at medium to high load level

Output a high level to the SRL pin and a low level to the SRH pin

Negative Half Cycle Operation

Output SYNC (1-d) signal to the PWML pin at medium to high load level

Output PWM (d) signal to the PWMH pin

Output a low level to the SRL pin and a high level to the SRH pin

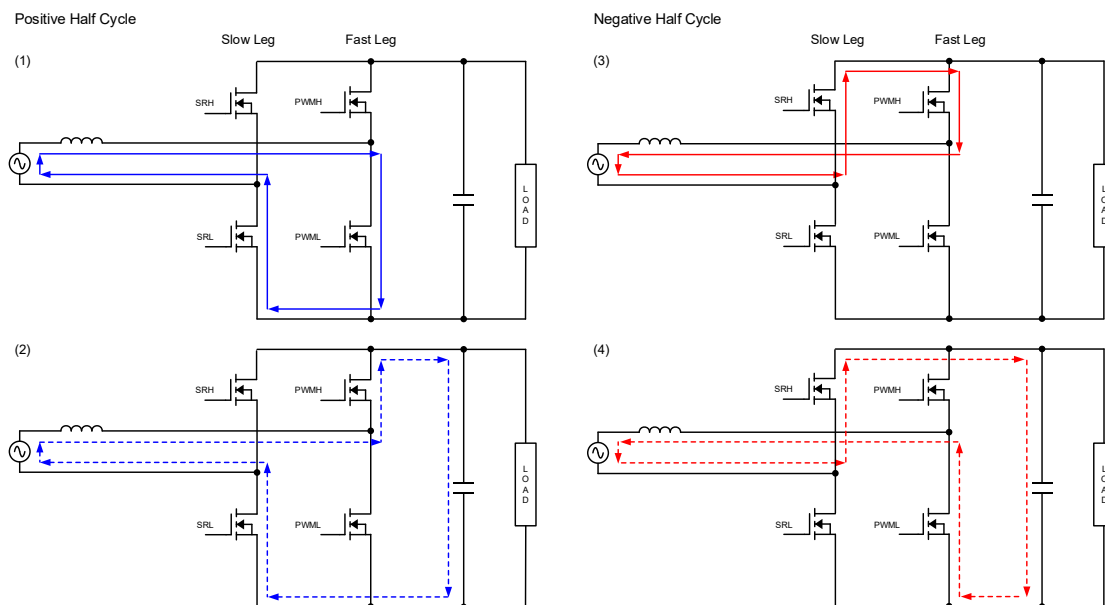


Figure 1. Cycle operation

Description of Blocks - continued

2 High Voltage Startup, X capacitor discharge function

Figure 2 shows the IC has built-in starter circuit with an absolute maximum voltage of 650 V.

Two diode rectifiers and current limiting resistor must be placed between AC lines and the HV pin to use this function.

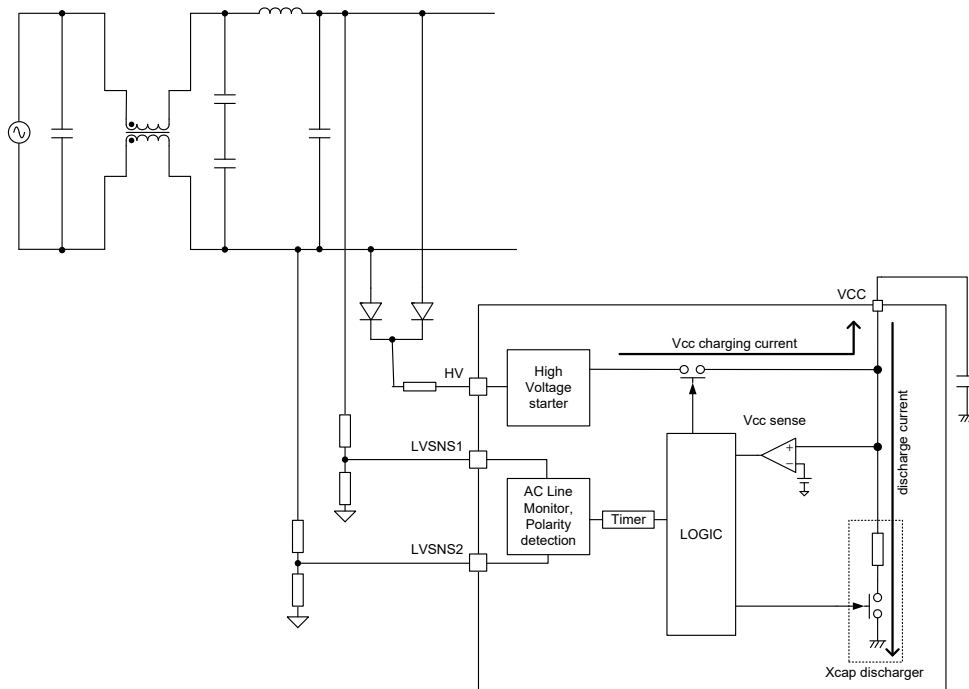


Figure 2. Configuration of HV startup circuit

Figure 2 shows the operation of the startup circuit.

A protection circuit is built-in to prevent overheating of the startup circuit.

If the external circuit becomes short-circuited, the startup circuit will continue to operate for an extended period of time, causing the startup circuit to overheat.

If $t_{\text{CHARGE_MAX}}$ elapses after the startup circuit starts operating, this circuit automatically stops.

The startup circuit is restarted when $t_{\text{CHARGE_RESTART}}$ is exceeded.

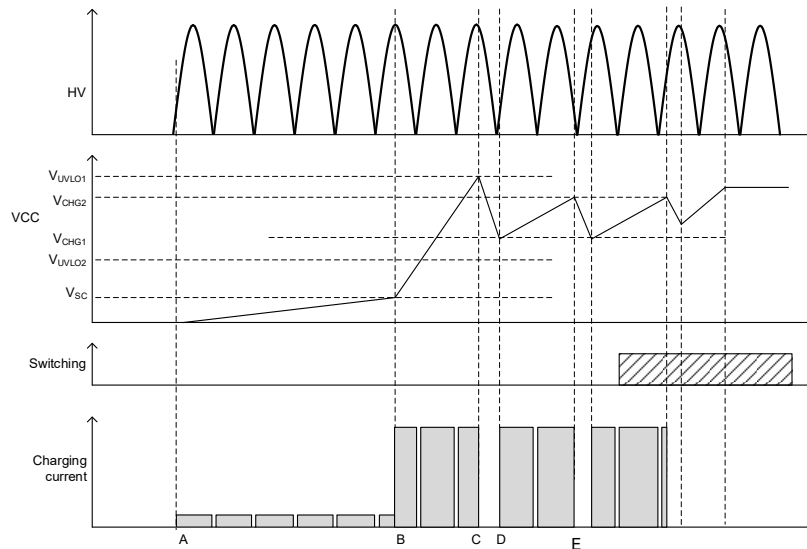


Figure 3. VCC startup charging operation

A: When the HV pin voltage is higher than $V_{\text{HV-START (ON)}}$, starter circuit is enabled and initial current flow to the VCC pin.

B: VCC charging current will increase to higher level when the VCC pin voltage (V_{CC}) reaches V_{SC} .

C: IC stops charging when V_{CC} reaches V_{UVLO1} .

D: If the VCC pin voltage drops to $V_{\text{CC}} < V_{\text{CHG1}}$ after starting with $V_{\text{CC}} > V_{\text{UVLO1}}$, the VCC charging function starts again.

E: After charging the VCC pin again, charging is terminated when the VCC pin rises to V_{CHG2} .

Description of Blocks - continued

2 High Voltage Startup, X capacitor discharge function - continued

Figure 4 shows when IC detects the disconnection of AC input, X capacitor discharge function starts operation. This function is achieved by repeatedly charging from the HV pin to the VCC pin and discharging from the VCC pin.

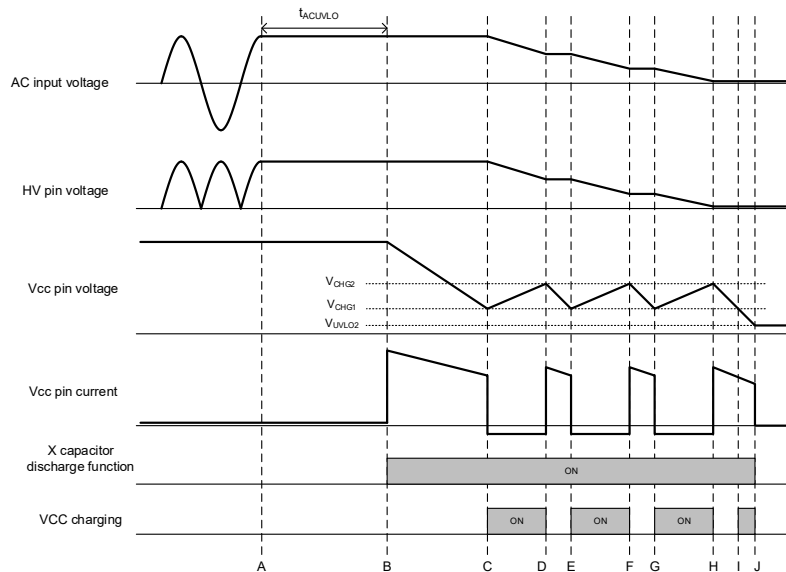


Figure 4. Timing Chart of X Capacitor Discharge Function.

- A: The AC input voltage is turned OFF.
- B: After t_{ACUVLO} (128 ms) from A, X capacitor discharge function is enabled. VCC capacitor is discharged until VCC voltage reaches V_{CHG1} .
- C: When the VCC pin voltage becomes less than V_{CHG1} , the VCC recharge operation starts and discharging starts from the HV pin.
- D: When the VCC pin voltage becomes more than V_{CHG2} , the VCC recharge operation stops and VCC capacitor is discharged.
- E: The Same as C.
- F: The Same as D.
- G: The Same as C.
- H: The Same as D.
- I: When the VCC pin voltage becomes less than V_{CHG1} , the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low HV pin voltage.
- J: When the VCC pin voltage becomes less than V_{UVLO2} , IC stops operation.

Description of Blocks - continued

3 Startup Sequence

Figure 5 shows startup sequence when AC voltage (V_{AC}) is applied to circuit.

High voltage startup circuit is activated and V_{CC} begins to rise. Switching operation is initiated when the following four conditions are met.

- A: Brownout protection is cleared.
- B: V_{CC} reaches V_{UVLO1} even once.
- C: Detects 4 consecutive polarity edges that are within the expected AC line frequency range.
- D: Polarity rising edge

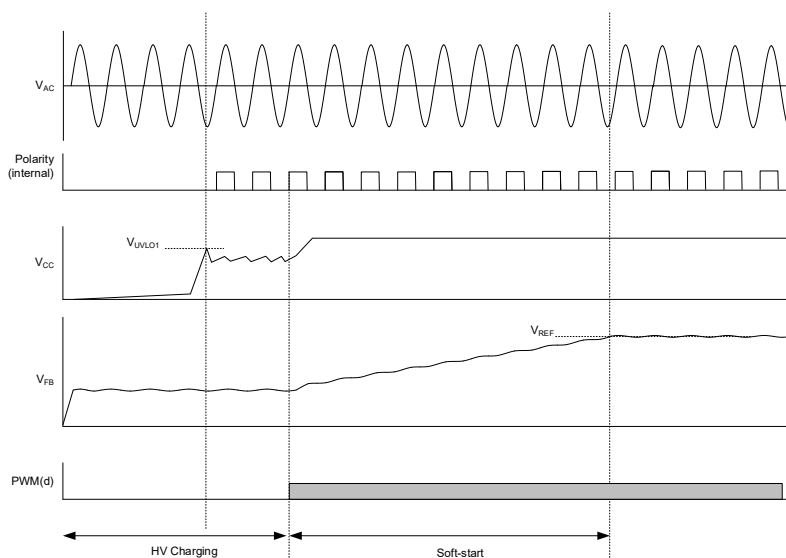


Figure 5. Startup Sequence

Soft-start sequence starts after switching started. Internal V_{REF} signal gradually increases from 0 V. This allows a gradual increase in V_{FB} voltage and suppresses inrush current on the input side. Soft-start period is 80 ms (Typ).

Description of Blocks - continued

4 PWM generation

Figure 6 shows the structure of PWM generation circuit.

This IC operates with a constant on-time control algorithm and on-time of the main PWM switch is determined by the compensation voltage, a ramp voltage and integrated functions.

FB pin monitors a divided voltage of the output voltage.

This voltage and V_{REF} voltage are connected to GmAMP.

GmAMP controls base signal of PWM on time.

The gain and phase characteristics of the GmAMP can be adjusted using the RC circuit network on the terminal (COMP) and the internal gain switching function (DRE and Vin-Range control function).

Output of GmAMP is controlled by Digital Limiter. This function is used to realize AC zero cross control and SoftOVP.

The PWM reset timing (PWM_RST) is determined by comparing the two signals V_{RAMP} and Digital Limiter out.

V_{RAMP} is a sawtooth wave for outputting PWM.

The waveform can be adjusted by Frequency control function (f_{MAX} , f_{MIN}), ZCD over-current control and feed forward control of input voltage.

When COMP voltage rises, width of PWM_RST signal becomes shorter.

This means increase of on-time of PWM.

The PWM reset signal is input to the PWM generator.

In PWM generator, there are several functions for default PWM operation, zero current detection and circuit protection.

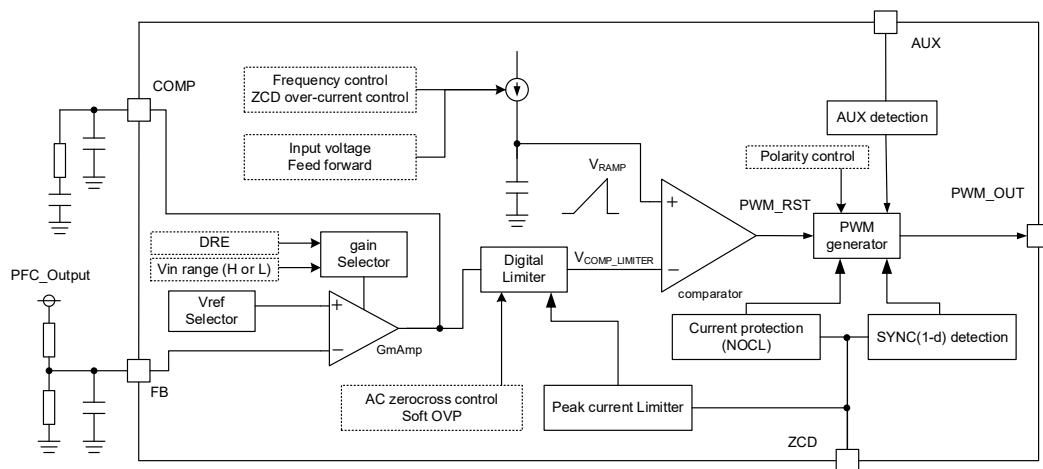


Figure 6. Structure of PWM generation circuit

5 AUX Detection

This IC uses an auxiliary winding that detects the valley of the ringing waveform of the drain voltage and turns on the switching device at that timing.

Figure 7 shows block diagram and waveform of the AUX pin.

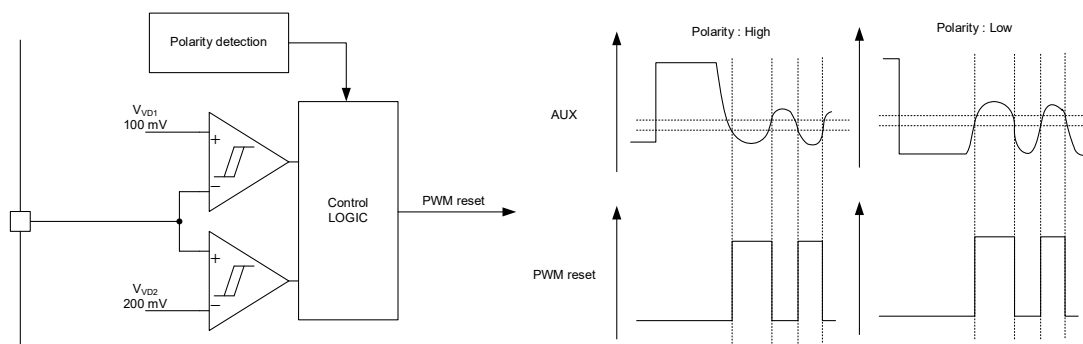


Figure 7. Block diagram and waveform of AUX pin

The voltage waveform of the AUX pin becomes the opposite waveform depending on the input voltage polarity.

Two comparators are used to detect the troughs of the ringing waveform so that either of these two waveforms can detect the troughs.

Comparator outputs are connected internal logic circuit, and this generates PWM reset signal to restart PWM on-time.

Description of Blocks - continued

6 GmAMP

Figure 8 shows the FB pin monitors a divided point for resistance of the output voltage.

The ripple voltage of the AC frequency (50 Hz/60 Hz) overlaps with the FB pin.

GmAMP removes this ripple voltage. GmAMP compares V_{REF} (2.5 V Typ) with the removed voltage, GmAMP controls the COMP voltage by difference between these two voltages.

When the COMP pin voltage rises, the ON width of the PWMH/PWML pin becomes wide.

Also, the error amplifier constant must be set so that the AC frequency does not overlap with the amplifier bandwidth. Frequency characteristics should be confirmed with an actual board.

A typical trans-conductance gain is 25 μ S.

Also, the trans-conductance at DRE switches to 150 μ S (Typ) and at DCM switches to 16 μ S (Typ) to adjust the loop gain.

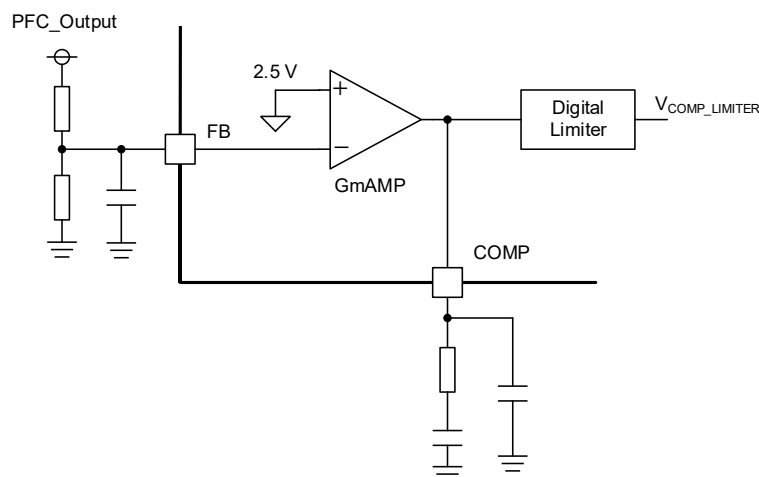


Figure 8. GmAMP Block Diagram

7 Dynamic Response Enhancer (DRE)

This IC has a function to suppress output undershoot.

When the FB pin voltage falls below ratio R_{DRE_LO} of V_{REF} , the control loop gain is increased to suppress output undershoot.

This high gain continues until the FB pin voltage returns to ratio R_{DRE_HI} of V_{REF} .

If an overcurrent is detected while the function is active, this function will be immediately disabled.

This state will persist for the duration of the same input voltage polarity.

When the input voltage polarity changes, this function will be re-enabled.

Description of Blocks - continued

8 Light load operation (DCM)

Figure 9 shows transition between light load operation mode (DCM) and normal operation mode (CRM).

This transition occurs when output load becomes light load and the COMP voltage falls below V_{DCM_TH2} threshold.

In DCM, the interval during which the inductor current becomes 0 A (t_{HIZ}) becomes longer and the switching frequency gradually decreases.

t_{HIZ} becomes longer in proportion to the difference between the COMP and V_{DCM_TH2} voltage, the COMP- V_{DCM_TH2} voltage.

If ON pulse width are equal in DCM and CRM, entering DCM from CRM reduces the switching frequency and current supply to the output capacitor, so the COMP voltage rises in the next AC half cycle and returns to CRM mode.

To prevent such CRM and DCM from alternating in the AC half cycle and worsening THD, the ON pulse width of DCM is controlled to be thicker than that of CRM.

During the t_{HIZ} interval, the V_{DS} voltage resonates.

The next turn-on is initiated at the valley of the V_{DS} resonance.

When the load current increases and the COMP voltage rise above the V_{DCM_TH1} voltage, it enters CRM.

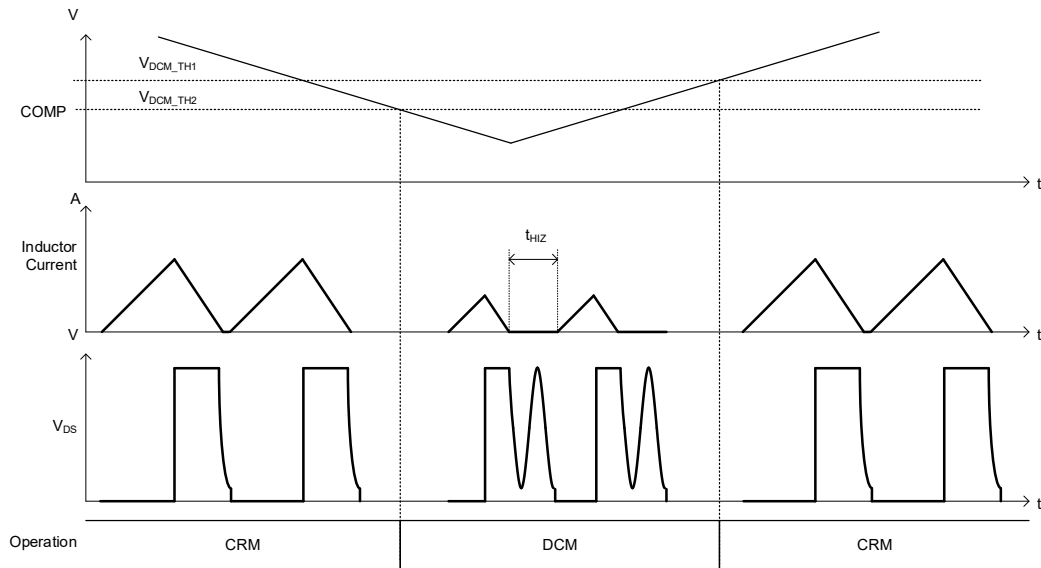


Figure 9. Transition from CRM Mode to DCM Mode

Description of Blocks - continued

9 Burst Mode Operation

Burst mode operation at light load is implemented to reduce I_{CC} current.

Figure 10 shows when the load becomes light and the COMP voltage reaches V_{CLAMP_TH} , the error amplifier output COMP pin clamps and the FB voltage increases, after the FB voltage reaches $V_{SOFTOVP}$, the controller enters the sleep state.

The quiescent current in sleep state is reduced to I_{CC3} .

When the FB voltage reaches V_{BURST_TH} , the controller automatically returns from sleep state and starts PWM.

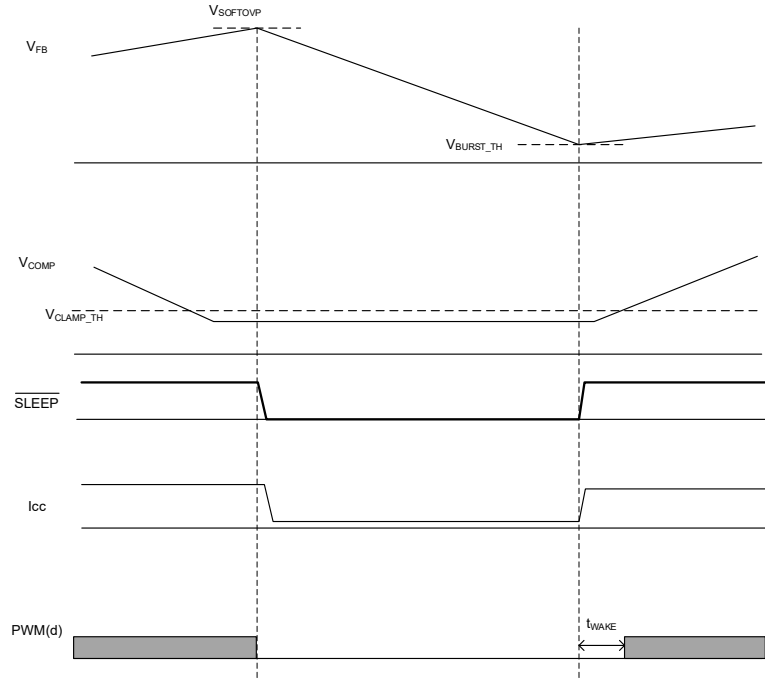


Figure 10. Burst mode operation

$\overline{\text{SLEEP}}$ pin is set low when the controller enters the sleep state.

This can help reduce power consumption of external gate drivers by disabling external IC or power supply.

Figure 11 shows typical connections when using this function.

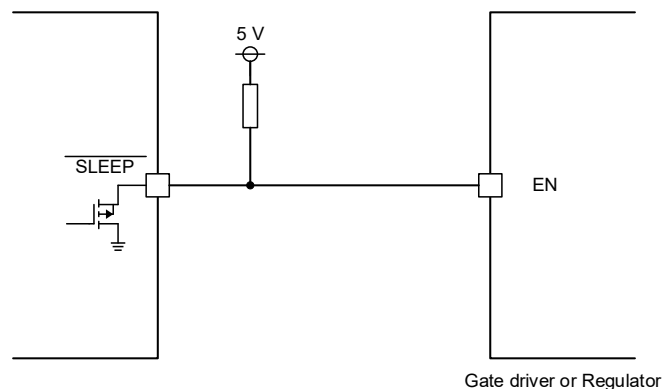


Figure 11. Typical connections when using $\overline{\text{SLEEP}}$ function

$\overline{\text{SLEEP}}$ pin is open-drain connection, and this pin should be pulled up to appropriate voltage.

When controller enters to sleep state, the EN pin of gate-driver is set to Low and gate-driver's power consumption can be decreased.

When controller returns from sleep state, $\overline{\text{SLEEP}}$ pin set to high immediately to enable gate driver or regulator.

The PWM signal is output after t_{WAKE} (400 μs).

Description of Blocks - continued

10 Zero Current Detection and synchronous PWM Drive Control

Figure 12 shows the zero current is detected by using the shunt resistor in series with the output capacitor to detect commutation timing.

The inductor discharge current that flows to the load during the 1-D period of the switching cycle can be monitored by using a series sensing element.

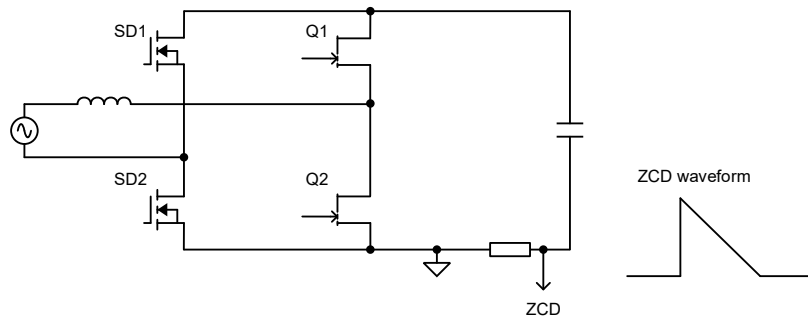


Figure 12. Zero Current Detection via ZCD pin

Figure 13 shows synchronous PWM driving pulses are only enabled at higher loads when the ZCD voltage is above the V_{ZCD_ARM} threshold.

The conditions to enable synchronous PWM drive are as follows.

1. V_{LINE} [absolute value of $(V_{LVSNS1} - V_{LVSNS2})$] voltage exceeds V_{SYNC_START}
2. ZCD voltage crosses the V_{ZCD_ARM} threshold

SYNC (1-D) pulses are enabled only at higher loads for efficiency improvement across all load conditions. This avoids premature enabling of the SYNC (1-D) pulses and enhances efficiency. This also prevents reverse currents during startup.

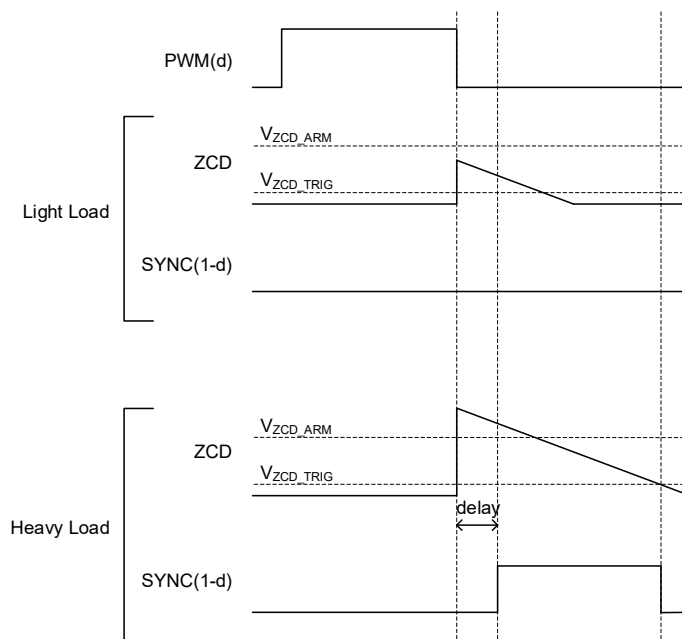


Figure 13. Synchronous PWM Drive Control

11 Line Range Detection

Since PFC must operate correctly over a wide input voltage range, the PFC controller must control and limit the operation of external components as input voltage changes.

When V_{LINE} exceeds the High-Line threshold V_{HL} , the IC transitions to High-Line mode.

When V_{LINE} falls below the Low-Line threshold V_{LL} in High-Line mode, the IC returns to Low-Line mode.

This mode-switch changes the parameters inside the IC.

This allows the control characteristics to be switched according to the input voltage.

Description of Blocks - continued

12 PWM polarity control, AC Zero Crossing Management

Figure 14 shows PWM polarity control and AC zero crossing management is a feature that determines when to enable or disable the various drive signals at the beginning and end of each half line cycle.

This feature is controlled by the LVSNS1 pin and the LVSNS2 pin.

IC detects difference between these 2 pins.

The polarity of PWM depends on the polarity of this difference.

When V_{LINE} voltage (absolute value of $V_{LVSNS1} - V_{LVSNS2}$) is positive, the PWML pin works as PWM (d) signal source and the PWMH pin works as SYNC (1-d) signal.

When V_{LINE} is negative, the PWMH pin works as PWM (d) signal source and the PWML pin works as SYNC (1-d) signal.

The same can be applied for the SRL and SRH pins.

This change is controlled by Polarity signal generated internally from the LVSNS1 pin and the LVSNS2 pin.

Following 2 types of PWM control functions are implemented to avoid large current flow around AC zero crossing.

[ACZ SoftStart]

Function to gradually increase PWM pulse width from minimum value.

Slow Leg signals [SRL, SRH] will not be triggered until ACZ sequence finishes even if V_{LINE} reaches V_{SR} .

This function is triggered when V_{LINE} is larger than V_{ZCB} and stops when following 2 conditions are detected.

- (A) V_{LINE} is larger than V_{SR} .
- (B) $t_{AC_SOFTSTART}$ period timeout.

[ACZ SoftStop]

Function to gradually decrease PWM pulse width to minimum value.

This function is triggered when V_{LINE} is smaller than V_{SR} and stops when following 2 conditions are detected.

- (A) Polarity change is detected.
- (B) $t_{AC_SOFTSTOP}$ period timeout.

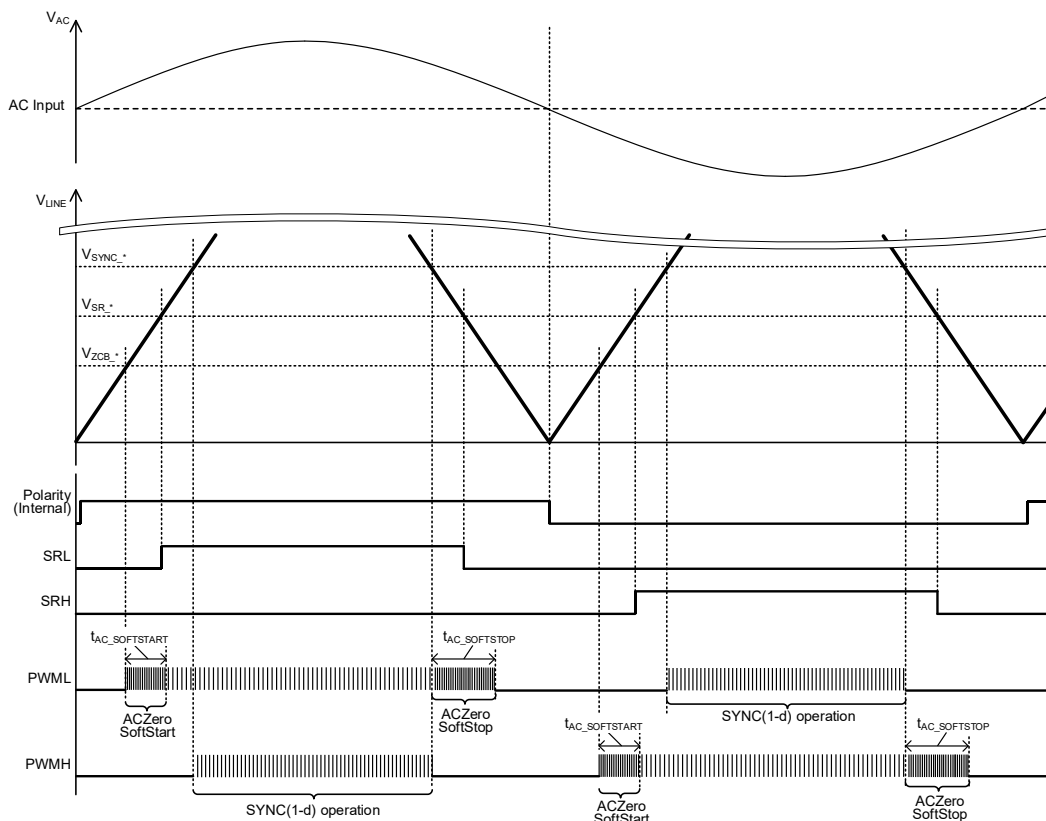


Figure 14. AC Zero Crossing Management

Description of Blocks - continued

13 Over Current Protection

Over current protection is used to protect flowing large current into inductor or transistor.
This function can be achieved by following 2 methods.

[CS pin detection (cycle by cycle protection)]

Figure 15 shows the CS pin connected to current transformer and signal conditioning circuit.

This enables measuring the inductor current at both AC positive cycle and negative cycle.

When the CS pin voltage (V_{CS}) reaches to $V_{CS1_LIM_POS}$ or $V_{CS1_LIM_NEG}$, controller stops PWM (d) state to prevent large current flow.

If the AC line voltage level is changed from Low-line level (100 V_{AC} range) to High-line level (200 V_{AC} range), threshold of V_{CS1_LIM} is decreased.

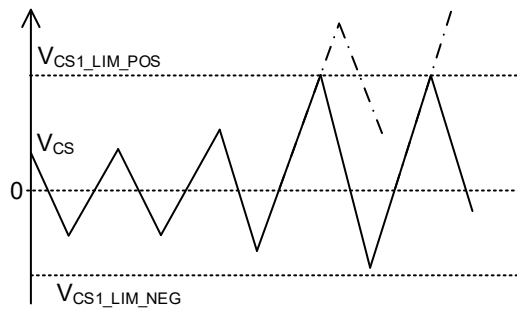


Figure 15. Cycle by Cycle Peak Current Limit Protection at the CS pin

[ZCD pin detection (peak current protection)]

Figure 16 shows the ZCD pin can detect the commutation current.

Internal control logic detects peak voltage and limits PWM on time when the ZCD pin voltage exceeds specified value (V_{ZCD_CLIM}).

When V_{ZCD} exceeds V_{ZCD_CLIM} , limit level of digital limiter in PWM block is increased.

If V_{ZCD} is lower than V_{ZCD_CLIM} at next switching, limit level is decreased.

If the AC line voltage level is changed from Low-line level (100 V_{AC} range) to High-line level (200 V_{AC} range), threshold of V_{ZCD_CLIM} is decreased.

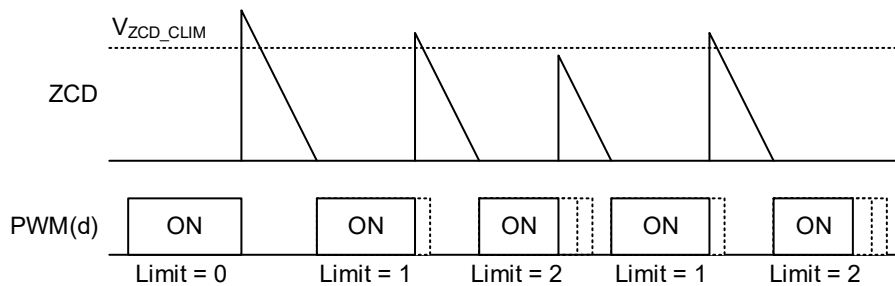


Figure 16. Peak current limiter via the ZCD pin

Description of Blocks - continued

14 Inductor Saturation Protection

Figure 17 shows the CS pin has second voltage threshold ($V_{CS2_LIM_POS}$ and $V_{CS2_LIM_NEG}$) to prevent over current destruction of semiconductors caused by inductor saturation current.

After the CS voltage reaches $V_{CS2_LIM_POS}$ and $V_{CS2_LIM_NEG}$, controller stops all PWM and becomes latch-off state.

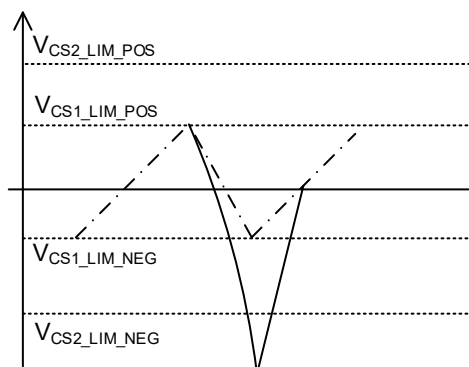


Figure 17. Inductor Saturation Protection

15 Inrush Current Protection

Figure 18 shows after power-on (when waiting for start-up), if the voltage at the ZCD pin is higher than V_{INRUSH} , switching is not performed.

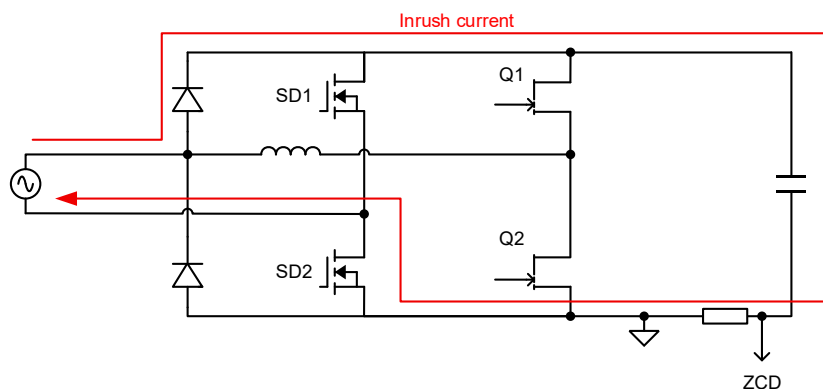


Figure 18. Inrush Current Protection

Description of Blocks - continued

16 Negative Over Current Limiter (NOCL)

Figure 19 shows if SD1 turns on while SD2 has a short-circuit fault, a short circuit occurs between output (+) and GND. This is also the same to Q1 and Q2 Large current flows from the output capacitor (shoot through current). To protect against this, NOCL function stops PWMs and SRL/SRH when negative voltage detects at the ZCD pin.

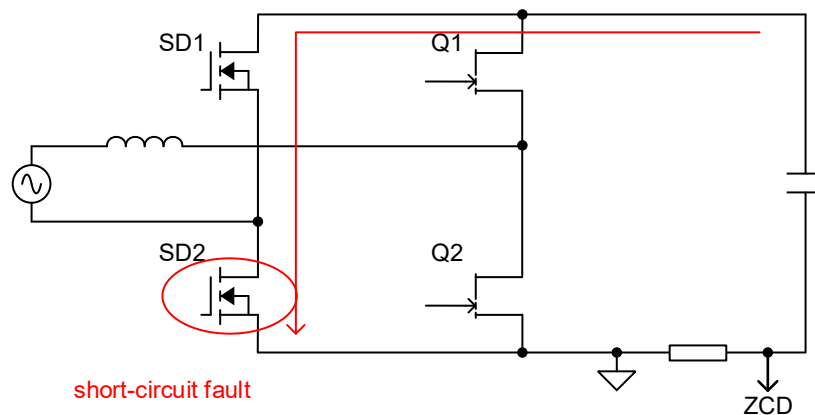


Figure 19. Target current of NOCL function

The (a) in Figure 20 shows the ZCD pin voltage.

When shoot through current occurs and ZCD voltage decrease less than V_{NOCL} , IC stops both PWMs and SRL/SRH. This fault may be temporary, but it can be permanent.

Permanent fault can cause destruction of switching devices.

To prevent destruction, this controller has latch-stop protection.

The (b) in Figure 20 shows latch-stop protection method.

When NOCL protection is activated 4 times in succession, internal fault flag is set and IC stop operation (Latch-stop). This counter is reset in each AC zero crossing timing if counter is less than 4.

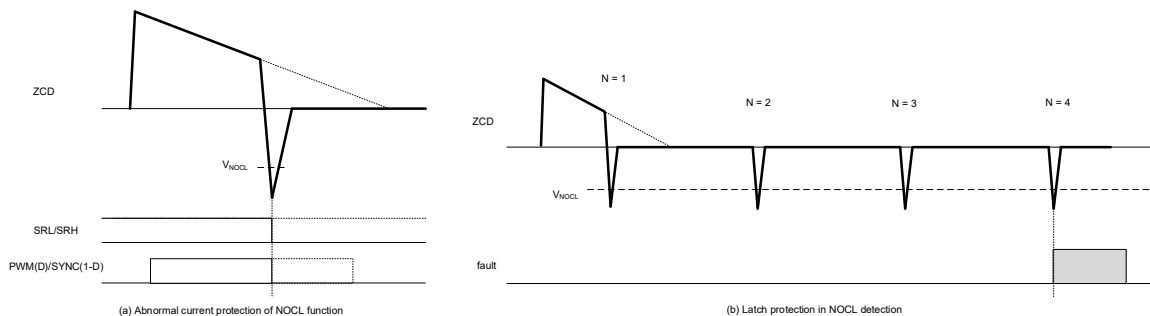


Figure 20. NOCL function

17 UVP, BUV

IC has 2 levels of protection for output under voltage, UVP and BUV.

[UVP (Output Under Voltage Protection)]

UVP is detected when V_{FB} is lower than V_{UVP} .

This protection prevents start-up in the event of short-circuit failure (when the feedback loop is open).

After UVP detected, both Fast Leg and Slow Legs are stopped.

Main reset is needed to reset UVP.

[BUV (Bulk Under Voltage)]

BUV is detected when V_{FB} is lower than V_{BUV} .

After BUV detected, both Fast Leg and Slow Legs are stopped.

After $t_{BUV} = 500$ ms is passed since BUV flag is set, BUV is automatically reset.

DC-DC circuit is usually connected to output of PFC circuit.

Since the DCDC circuit also has a UVLO function, it is necessary to set the UVLO voltage of the DCDC circuit higher than the BUV voltage so that the protection voltages do not overlap.

Description of Blocks - continued

18 OVP (Output Over Voltage Protection)

Figure 21 shows IC has 3 levels of over voltage protection threshold to protect system and circuits.

[StaticOVP]

StaticOVP detects an open-circuit fault on the feedback pin or overvoltage, immediately stopping PWM pulses.

When V_{FB} voltage exceeds ratio $R_{STATICOVP}$ of V_{REF} , StaticOVP is triggered and PWM stops.

This fault cannot be reset until main reset occurs.

[FastOVP]

FastOVP detects a feedback pin anomaly and immediately stops the PWM pulses.

When V_{FB} voltage exceeds ratio $R_{FASTOVP}$ of V_{REF} , FastOVP is triggered and PWM stops.

After FastOVP triggered and V_{FB} voltage decreases to ratio $R_{OVPRECOVER}$ of V_{REF} , FastOVP function is reset and PWM will recover.

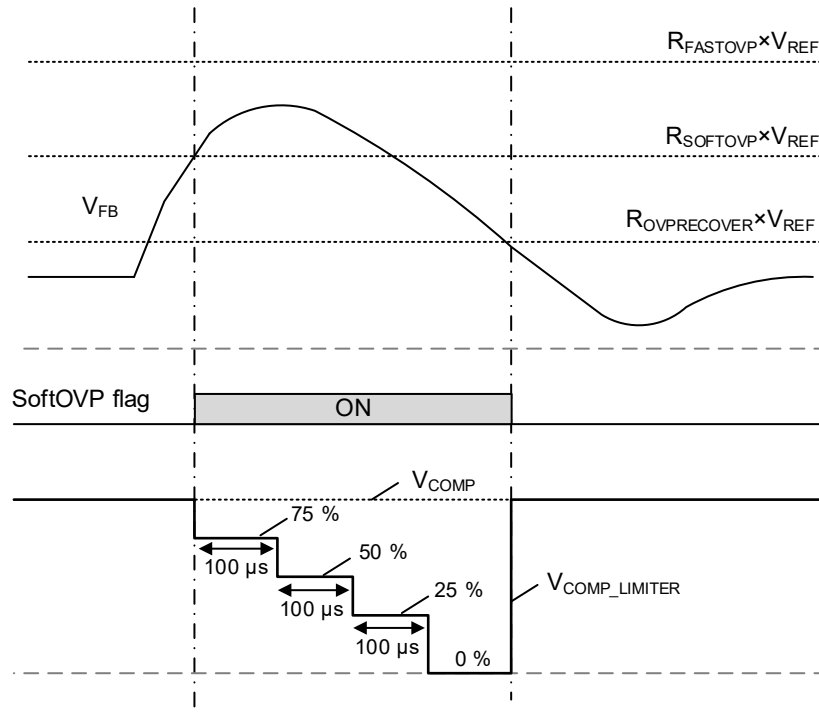
[SoftOVP]

SoftOVP detects feedback pin anomaly and slowly stops the PWM pulses.

This function is achieved by controlling Error amplifier output limiter $V_{COMP_LIMITER}$.

When V_{FB} voltage exceeds ratio $R_{SOFTOVP}$ of V_{REF} , following SoftOVP actions will start.

After SoftOVP triggered and V_{FB} voltage decreases to ratio $R_{OVPRECOVER}$ of V_{REF} , SoftOVP function is reset and PWM will recover.



Step 1: $V_{COMP_LIMITER}$ drops to 75 % of the V_{COMP} value for 100 μs .

Step 2: $V_{COMP_LIMITER}$ drops to 50 % of the V_{COMP} value for 100 μs .

Step 3: $V_{COMP_LIMITER}$ drops to 25 % of the V_{COMP} value for 100 μs .

Step 4: $V_{COMP_LIMITER}$ drops to 0 until the SoftOVP fault is reset.

Figure 21. Soft OVP (Output Over Voltage Protection)

Description of Blocks - continued

19 VAC OVP (Input Over Voltage Protection)

If a higher than typical mains voltage is applied to this IC, the output voltage can easily rise to the FastOVP or StaticOVP. To suppress this fault, a second overvoltage protection is implemented on the input side.

When V_{LINE} voltage exceeds 4 V (Typ), IC detects over voltage of input side and stops PWM operation.

After V_{LINE} decreases 4 V, this fault is reset and PWM will be restarted from AC zero cross timing.

20 Brownout (BO) and Line sag

Figure 22 shows the IC feature set includes line voltage Brownout (BO) and Line sag (SAG) detection.

Both BO and SAG are activated when Line voltage falls below V_{BO_STOP} .

When $V_{LINE} > V_{BO_START}$, the controller will return from the BO or SAG fault state.

[SAG function]

- (1) Detect Condition
 V_{LINE} is lower than V_{BO_STOP} for $t_{SAG (BLANK)}$ or more.
- (2) Action
Soft stop operation is started.
- (3) Release condition
 V_{LINE} is larger than V_{BO_START} .

[BO function]

- (1) Detect Condition
 V_{LINE} is lower than V_{BO_STOP} for $t_{BO (BLANK)}$ or more.
- (2) Action
Disables the polarity detection circuit.
- (3) Release condition
 V_{LINE} is larger than V_{BO_START} .

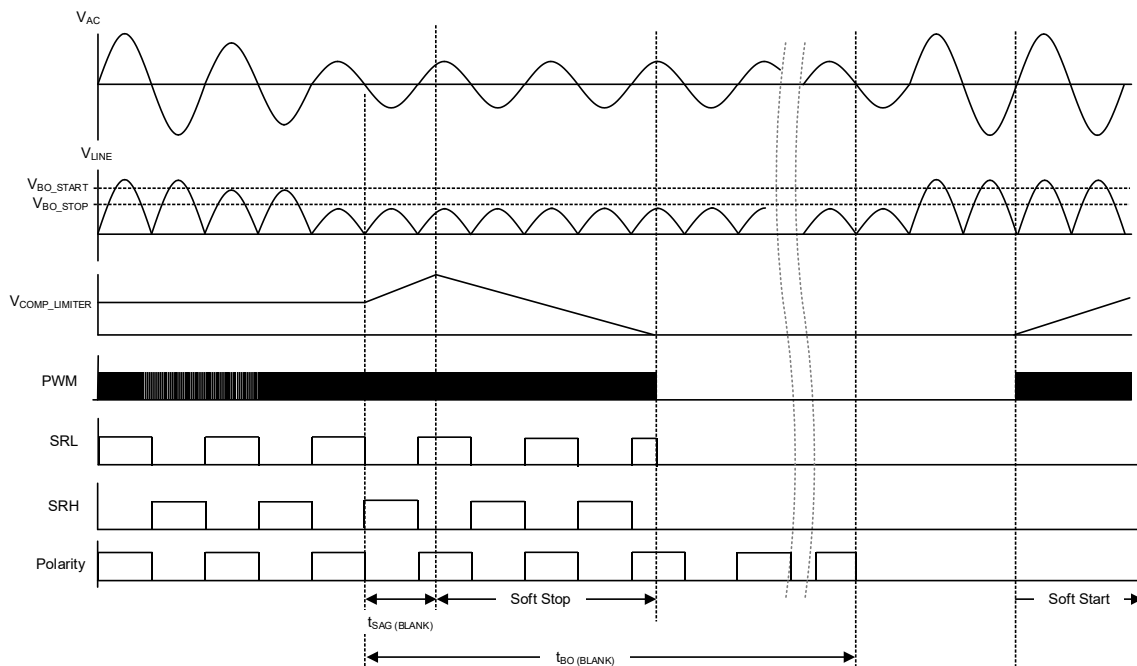


Figure 22. Brownout (BO) and Line sag

Description of Blocks - continued

21 Line Frequency Fault

Figure 23 shows IC monitors whether the AC line frequency is within the mains frequency range ($f_{\text{LINE (LO)}}$ to $f_{\text{LINE (HI)}}$). If abnormal mains frequency is detected, following steps are operated.

[Step1]

If outside of the expected frequency range, stop Slow Leg.
PWM continues operation.

[Step2]

If 100 ms elapsed since abnormal mains frequency detected, both Fast Leg and Slow Leg is stopped.
IC will recover from this fault state if IC detects 4 consecutive polarity edges that are within the expected frequency range (same as a startup).

The IC measures the time between every edge transition of the filtered polarity signal.

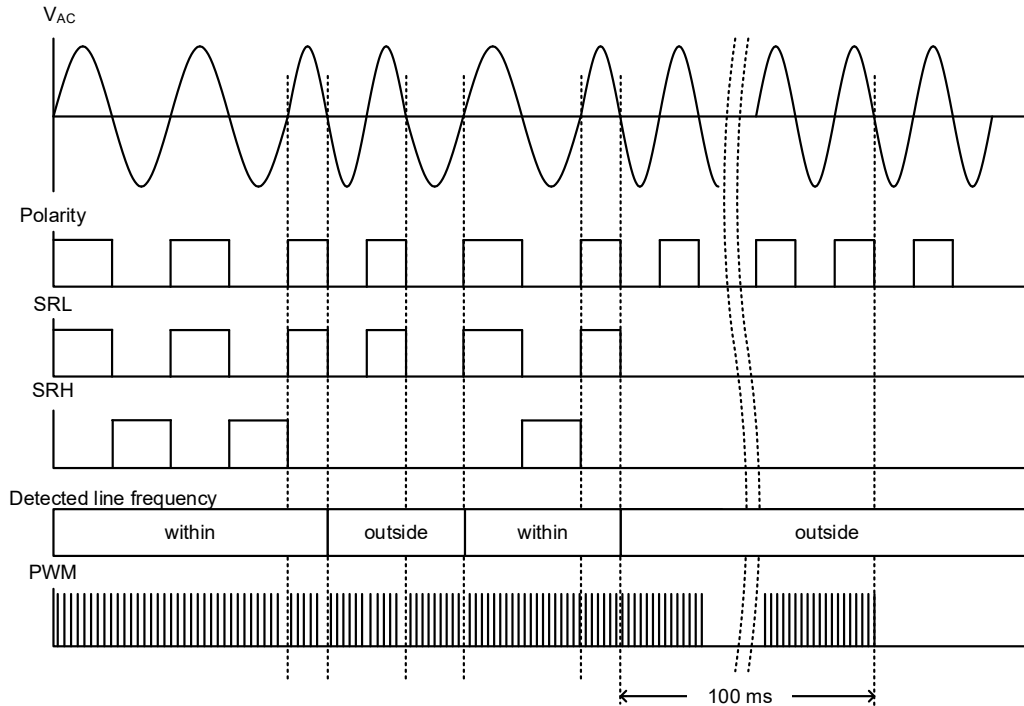


Figure 23. Line Frequency Fault

Description of Blocks - continued

22 AC Line Voltage sudden change protection

Figure 24 shows FET failure conditions when the AC input voltage changes suddenly due to the application of lightning surge voltage.

The sudden voltage change may cause large current to flow from and to the output capacitor via Slow Leg FET.

To prevent FET failure due to excessive current, controller must turn off the gate signals of Slow Leg and SYNC (1-D) when this phenomenon occurs.

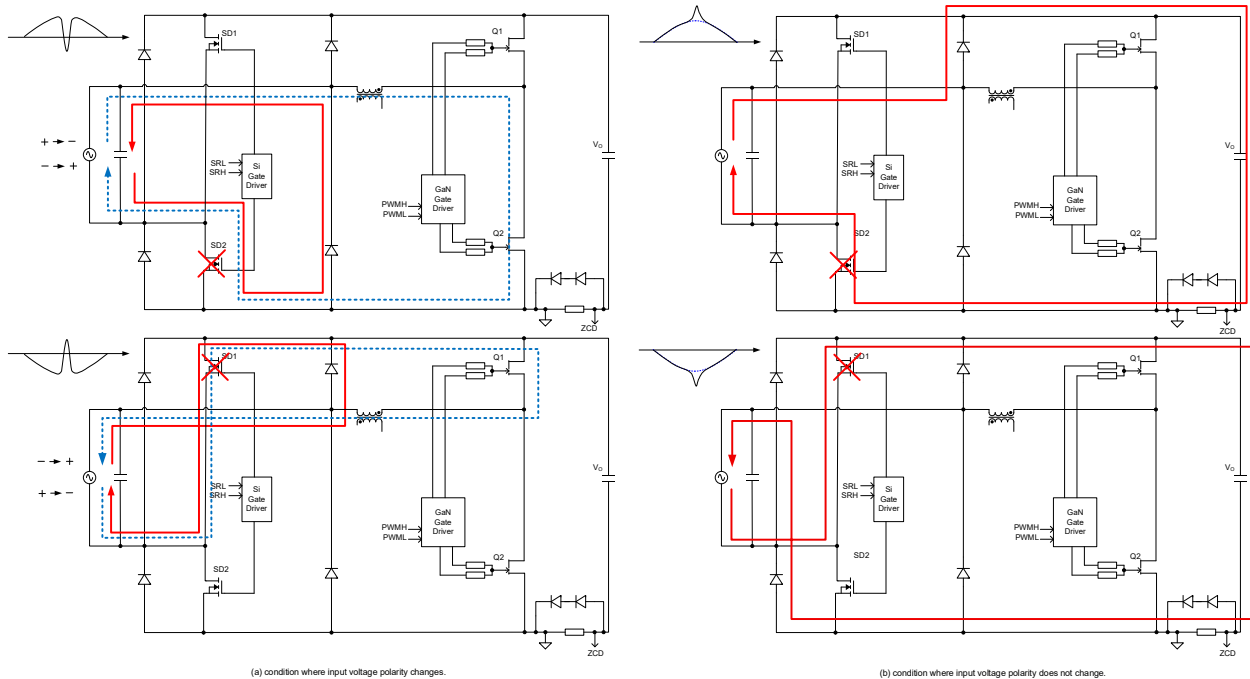


Figure 24. FET failure conditions when Slow Leg FET is on.

Controller uses 2 methods to detect this phenomenon.

In situations where the input voltage polarity changes, large voltage changes can be detected at the LVSNS1 and the LVSNS2 pin.

[Figure 25 (a)]

After detection, all gate signals are set low.

PWM gate signal is recovered after 200 μ s from trigger timing, and Slow Leg gate signals (SRL/SRH) are recovered from next AC zero crossing timing.

In situations where the input voltage polarity does not change, large voltage changes can be detected at the ZCD pin.

[Figure 25 (b)]

After detection, all gate signals are set low.

PWM gate signal is recovered after 200 μ s from trigger timing, and Slow Leg gate signals (SRL/SRH) are recovered from next AC zero crossing timing.

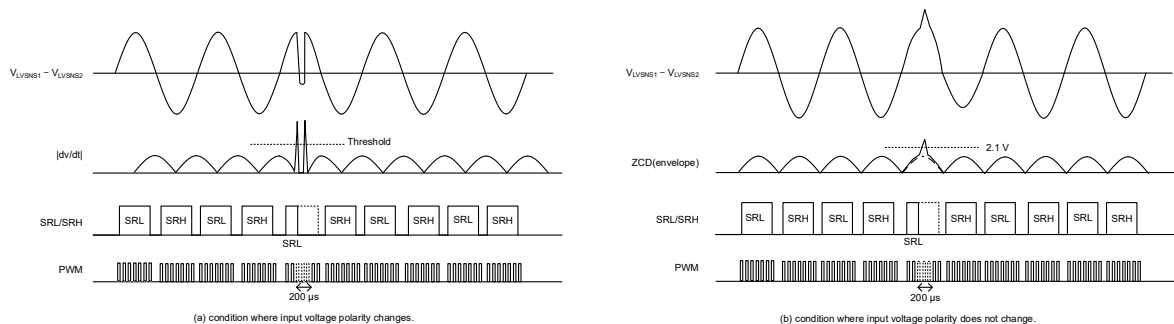


Figure 25. Detection method and timing chart (positive polarity only)

Description of Blocks - continued

23 Internal TSD

An internal thermal shutdown function is implemented to prevent the IC from being damaged under abnormally high temperatures.

This fault is triggered when junction temperature (T_j) exceeds TSD detection temperature.

After triggered, IC stops Fast Leg and Slow Leg operation.

The fault is cleared when the temperature drops below $T_{SD} - T_{SD(HYS)}$.

24 External fault control (FAULT pin)

The FAULT pin has comparator for detecting faults as shown in Figure 26.

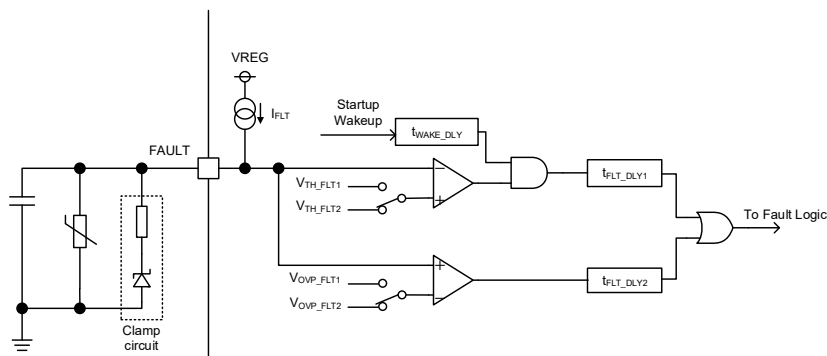


Figure 26. Simplified diagram of FAULT pin function

Internal current source (I_{FLT}) is implemented at the FAULT pin.

External TSD can be achieved by connecting thermistor to the FAULT pin.

Typical voltage to trigger external thermal fault is V_{TH_FLT2} .

After fault detected, comparator threshold changes to V_{TH_FLT1} .

The FAULT pin voltage is normally 0 V during startup and upon wake-up from SLEEP state.

Under these conditions, an external temperature fault may be detected.

Therefore, this function is enabled after a circuit stabilization time t_{WAKE_DLY} following startup.

Clamp circuit must be connected in parallel with thermistor so that voltage does not exceed the OVP protection threshold.

It is recommended to connect filter capacitor to this pin.

This pin also can be used as OVP by adding detection circuit.

Typical voltage to trigger OVP is V_{OVP_FLT2} .

After fault detected, comparator threshold changes to V_{OVP_FLT1} .

Description of Blocks - continued

25 Fault summary

Following table shows protection features, the conditions needed to set or reset the fault, and the action of the IC for the given fault.

Fault	Set condition	Reset condition	Controller Action
Line SAG	$(V_{LINE} < V_{BO (STOP)}) + t_{SAG (BLANK)} \text{ expired}$	$V_{LINE} > V_{BO (START)}$	- Begin soft stop sequence - PWM, SR drives disabled after soft stop - Cancels t_{BUV}
Brownout	$(V_{LINE} < V_{BO (STOP)}) + t_{BO (BLANK)} \text{ expired}$	$V_{LINE} > V_{BO (START)}$	- Disables the polarity detection circuit
Line Frequency1	$t_{LINE} < t_{LINE (45)} \text{ OR } > t_{LINE (65)}$	$t_{LINE (45)} < t_{LINE} < t_{LINE (65)}$	- SR drives disabled - Starts 100 ms timer
Line Frequency2	100 ms timer expired	$N_{DRV_EN} = 4: t_{LINE (45)} < t_{LINE} < t_{LINE (65)} \text{ for 4 consecutive polarity toggles}$	- PWM, SR drives disabled
UVP	$V_{FB} < V_{UVP}$	$V_{FB} > V_{UVP}$	- PWM, SR drives disabled
BUV (Bulk Under Voltage)	$V_{FB} < V_{BUV}$	$t_{BUV} \text{ expires}$	- PWM, SR drives disabled - Automatic restart after t_{BUV}
SoftOVP	$V_{FB} > V_{SOFTOVP}$	$V_{FB} < V_{OVPRECOVER}$	- Begin SoftOVP sequence - PWM Drive disables after SoftOVP Sequence - SR remains active
FastOVP	$V_{FB} > V_{FASTOVP}$	$V_{FB} < V_{OVPRECOVER}$	- PWM Drive disables immediately - SR remains active
StaticOVP	$V_{FB} > V_{STATICOVP}$	Main Reset	- PWM, SR drives disabled
VACOV	$V_{LINE} > V_{ACOV}$	$V_{LINE} < V_{ACOV}$	- PWM, SR drives disabled
V _{CC} UVLO	$V_{CC} < V_{UVLO2}$	$V_{CC} > V_{UVLO1}$	- PWM, SR drives disabled
External Fault	$V_{FAULT} < V_{TH_FLT2}$	$V_{FAULT} > V_{TH_FLT1}$	- PWM, SR drives disabled
CS OCP2	$V_{CS} > V_{CS_LIM2_POS} \text{ OR } V_{CS} < V_{CS_LIM2_NEG}$	Main Reset	- PWM, SR drives disabled
NOCL latch	NOCL detected 3 times	Main Reset	- PWM, SR drives disabled
TSD	$T_j > T_{SD}$	$T_j < (T_{SD} - T_{SD (HYS)})$	- PWM, SR drives disabled
Double Fault1	Both [ZCD-OCP] and [SoftOVP] detected.	Either fault is cleared	- PWM, SR drives disabled - PWM, SR drives restart from next AC Zero Crossing after reset.
Double Fault2	Both [LineSAG] and [SoftOVP] detected.	Either fault is cleared	- PWM and SR drives disabled - PWM and SR drives restart from next AC Zero Crossing after reset.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
High Voltage Start-Up Circuit Input Voltage Range, HV Pin	V_{HV} (MAX)	-0.3 to +650	V
Supply Input Voltage Range, VCC Pin	V_{VCC}	-0.3 to +40	V
Internal Regulator Voltage Range, VREG Pin	V_{VREG}	-0.3 to +7.0	V
Current Sensing Voltage Range, CS ZCD Pins	V_{CS} , V_{ZCD}	-0.9 to $V_{VREG} + 0.3$	V
Other Input Voltage Range LVSNS1, LVSNS2, FB, COMP, FAULT, SLEEP, SRH, SRL, AUX, PWMH, PWML Pins	V_{LVSNS1} , V_{LVSNS2} , V_{FB} , V_{COMP} , V_{FAULT} , V_{SLEEP} , V_{SRH} , V_{SRL} , V_{AUX} , V_{PWMH} , V_{PWML}	-0.3 to $V_{VREG} + 0.3$	V
Maximum Junction Temperature	T_{jmax}	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
SSOP-B20				
Junction to Ambient	θ_{JA}	115.4	57.3	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	10	8	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for HV	V_{HV}	80	-	600	V
Supply Voltage for VCC	V_{CC}	8	-	36	V
Operating Temperature	T_{opr}	-40	+25	+125	°C
VCC Capacitor	C_{VCC}	-	-	70	μ F
VREG Output Capacitor ^(Note 5)	C_{VREG}	1.0	2.2	-	μ F
VREG Output Load Capability	I_{VREG}	-	-	5	mA
Total X Capacitance	C_{XCAP}	-	-	4.7	μ F

(Note 5) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered.

Electrical Characteristics (Unless otherwise specified $V_{HV} = 320\text{ V}$, $V_{CC} = 12\text{ V}$, $T_j = -40\text{ to }+125\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Supply Circuits]						
VCC UVLO Release Voltage	V_{UVLO1}	9.75	10.50	11.25	V	V_{CC} rising
VCC UVLO Detection Voltage	V_{UVLO2}	5.9	6.5	7.1	V	V_{CC} falling
VCC Hysteresis	$V_{CC(HYS)}$	-	4	-	V	$V_{UVLO1} - V_{UVLO2}$
Quiescent Current (Before Startup)	I_{CC1}	-	330	680	μA	$V_{CC} = 9.5\text{ V}$
Quiescent Current (CRM Operation)	I_{CC2}	-	2.2	4.4	mA	Non switching
Quiescent Current (Burst Mode)	I_{CC3}	-	150	350	μA	Burst mode
VREG Voltage	V_{REG1}	4.80	5.00	5.25	V	
VREG UVLO Release Voltage	V_{REG_UVLO1}	3.76	4.25	4.74	V	V_{REG} rising
VREG UVLO Detection Voltage	V_{REG_UVLO2}	3.503	3.630	3.757	V	V_{REG} falling
[High Voltage Startup & X-Capacitor Discharge]						
HV Minimum Operation Voltage	$V_{HV_START(ON)}$	30	-	-	V	
VCC Recharge Start Voltage	V_{CHG1}	8.5	9.5	10.5	V	V_{CC} falling
VCC Recharge Stop Voltage	V_{CHG2}	9.0	10.0	11.0	V	V_{CC} rising
Start Current 1	I_{START1}	0.24	0.60	1.80	mA	$V_{CC} = 0\text{ V}$
Start Current 2	I_{START2}	3.0	6.5	12.0	mA	$V_{CC} = 10\text{ V}$
OFF Current	$I_{START-OFF}$	-	14	25	μA	HV current after V_{UVLO1}
Start Current Charging Voltage	V_{SC}	0.8	1.8	2.8	V	V_{CC} voltage
VCC Charging Timer	t_{CHARGE_MAX}	240	300	360	ms	
VCC Charging Restart Timer	$t_{CHARGE_RESTART}$	360	450	540	ms	
[AC Zero Crossing Management] ^(Note 6)						
Threshold to Stop PWML/H 1	$V_{ZCB_STOP(HL)}$	60	140	220	mV	at High-Line
Threshold to Stop PWML/H 2	$V_{ZCB_STOP(LL)}$	60	140	220	mV	at Low-Line
Threshold to Start PWML/H 1	$V_{ZCB_START(HL)}$	120	200	280	mV	at High-Line
Threshold to Start PWML/H 2	$V_{ZCB_START(LL)}$	120	200	280	mV	at Low-Line
Threshold to Stop SRL/H 1	$V_{SR_STOP(HL)}$	240	320	400	mV	at High-Line
Threshold to Stop SRL/H 2	$V_{SR_STOP(LL)}$	240	320	400	mV	at Low-Line
Threshold to Start SRL/H 1	$V_{SR_START(HL)}$	300	380	460	mV	at High-Line
Threshold to Start SRL/H 2	$V_{SR_START(LL)}$	300	380	460	mV	at Low-Line
Threshold to Stop SYNC 1	$V_{SYNC_STOP(HL)}$	300	380	460	mV	at High-Line
Threshold to Stop SYNC 2	$V_{SYNC_STOP(LL)}$	300	380	460	mV	at Low-Line
Threshold to Start SYNC 1	$V_{SYNC_START(HL)}$	360	440	520	mV	at High-Line
Threshold to Start SYNC 2	$V_{SYNC_START(LL)}$	360	440	520	mV	at Low-Line
Zero Crossing Softstart Time	$t_{AC_SOFTSTART}$	154	192	230	μs	
Zero Crossing Softstop Time	$t_{AC_SOFTSTOP}$	164	202	240	μs	
Polarity Detection Filter	t_{POL_FILTER}	102	128	154	μs	

(Note 6) The threshold voltage is the absolute value of the difference between V_{LVSN1} and V_{LVSN2}

Electrical Characteristics (Unless otherwise specified $V_{HV} = 320\text{ V}$, $V_{CC} = 12\text{ V}$, $T_j = -40\text{ to }+125\text{ }^{\circ}\text{C}$) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[ZCD Pin Detection]						
ZCD Arming Threshold 1	$V_{ZCD_ARM(HL)}$	70	100	130	mV	at High-Line
ZCD Arming Threshold 2	$V_{ZCD_ARM(LL)}$	70	100	130	mV	at Low-Line
ZCD Trigger Threshold 1	$V_{ZCD_TRIG(HL)}$	20	50	80	mV	at High-Line
ZCD Trigger Threshold 2	$V_{ZCD_TRIG(LL)}$	20	50	80	mV	at Low-Line
ZCD Current Limit Detection 1	$V_{ZCD_CLIM(HL)}$	700	800	900	mV	at High-Line
ZCD Current Limit Detection 2	$V_{ZCD_CLIM(LL)}$	1500	1600	1700	mV	at Low-Line
Inrush Current Threshold	V_{INRUSH}	30	60	90	mV	
Negative Over Current Threshold	V_{NOCL}	-790	-700	-610	mV	
[Brownout, Line Sag, Line Fault Detection]						
Line Sag And Brownout Detection Upper Threshold	V_{BO_START}	1.02	1.10	1.18	V	$ V_{LVSNS1} - V_{LVSNS2} $ rising
Line Sag And Brownout Detection Lower Threshold	V_{BO_STOP}	0.92	1.00	1.08	V	$ V_{LVSNS1} - V_{LVSNS2} $ falling
Brownout Detection Hysteresis	V_{BO_HYS}	60	100	-	mV	$V_{BO_START} - V_{BO_STOP}$
Line Sag Detection Blanking Timer	$t_{SAG(BLANK)}$	20	25	30	ms	$ V_{LVSNS1} - V_{LVSNS2} < V_{BO_STOP}$, Delay to Soft Stop Enable
Brownout Detection Blanking Timer	$t_{BO(BLANK)}$	520	650	780	ms	
[Line Range Detection]						
High-Line Level Detection Threshold	V_{HL}	2.20	2.36	2.52	V	$ V_{LVSNS1} - V_{LVSNS2} $ rising, 200 V_{AC} range
Low-Line Level Detection Threshold	V_{LL}	2.07	2.22	2.37	V	$ V_{LVSNS1} - V_{LVSNS2} $ falling, 100 V_{AC} range
Low to High Line Mode Selector Timer Filter	$t_{BLANK(HL)}$	200	300	400	μs	$ V_{LVSNS1} - V_{LVSNS2} > V_{HL}$
High to Low Line Mode Selector Timer Filter	$t_{BLANK(LL)}$	20	25	30	ms	$ V_{LVSNS1} - V_{LVSNS2} < V_{LL}$
[AC Line Frequency Monitoring]						
Line Frequency Upper Threshold	$f_{LINE(HI)}$	66	72	78	Hz	
Line Frequency Lower Threshold	$f_{LINE(LO)}$	37	41	45	Hz	
[AUX Pin Detection]						
Valley Detection Thresholds 1	V_{VD1}	50	100	160	mV	
Valley Detection Thresholds 2	V_{VD2}	150	200	250	mV	
Valley Detection Hysteresis	V_{VD_HYS}	50	100	-	mV	
[DCM And Burst Mode Control]						
DCM-CRM Mode Threshold 1	$V_{DCM_TH1(HL)}$	590	650	710	mV	at High-Line
DCM-CRM Mode Threshold 2	$V_{DCM_TH1(LL)}$	640	700	760	mV	at Low-Line
CRM-DCM Mode Threshold 1	$V_{DCM_TH2(HL)}$	400	450	500	mV	at High-Line
CRM-DCM Mode Threshold 2	$V_{DCM_TH2(LL)}$	550	600	650	mV	at Low-Line
Burst Mode In Threshold 1	$V_{CLAMP_TH(HL)}$	200	220	250	mV	at High-Line
Burst Mode In Threshold 2	$V_{CLAMP_TH(LL)}$	200	220	250	mV	at Low-Line
Burst Mode Out Threshold Ratio	R_{BURST}	92	95	98	%	$R_{BURST} = V_{BURST_TH}/V_{REF}$, at V_{FB} rising

Electrical Characteristics(Unless otherwise specified $V_{HV} = 320\text{ V}$, $V_{CC} = 12\text{ V}$, $T_j = -40\text{ to }+125\text{ }^{\circ}\text{C}$) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Fast Leg DRIVE SIGNALS (PWML & PWMH)]						
Source Resistance	R_{ON_OH1}	-	15	32	Ω	
Sink Resistance	R_{ON_OL1}	-	5	16	Ω	
[Slow Leg DRIVE SIGNALS (SRL & SRH)]						
Source Resistance	R_{ON_OH2}	-	15	32	Ω	
Sink Resistance	R_{ON_OL2}	-	5	16	Ω	
[On-Time Modulation Circuit]						
Maximum Frequency Clamp	f_{MAX}	800	1000	1200	kHz	
Minimum Frequency Clamp	f_{MIN}	22	25	28	kHz	
[GmAMP Circuit]						
Feedback Voltage Reference	V_{REF}	2.45	2.50	2.55	V	
Error Amplifier Sink Current	I_{COMP_SINK}	1.3	2.6	4.2	μA	
Error Amplifier Source Current	I_{COMP_SOURCE}	-4.2	-2.6	-1.3	μA	
[FB Pin Detection]						
FB Input Bias Current	I_{FB}	-0.5	0.0	+0.5	μA	
SoftOVP Threshold Ratio	$R_{SOFTOVP}$	103	105	108	%	$R_{SOFTOVP} = V_{SOFTOVP}/V_{REF}$ V_{FB} rising
FastOVP Threshold Ratio	$R_{FASTOVP}$	105	108	111	%	$R_{FASTOVP} = V_{FASTOVP}/V_{REF}$ V_{FB} rising
OVPRecovery Threshold Ratio	$R_{OVPRECOVER}$	100	103	106	%	$R_{OVPRECOVER} = V_{OVPRECOVER}/V_{REF}$ V_{FB} falling
StaticOVP Threshold Ratio	$R_{STATICOVP}$	118	120	122	%	$R_{STATICOVP} = V_{STATICOVP}/V_{REF}$ V_{FB} rising
Under Voltage Protection Ratio	R_{UVP}	10	12	14	%	$R_{UVP} = V_{UVP}/V_{REF}$ V_{FB} falling
BUV Threshold Ratio	R_{BUV}	77	80	83	%	$R_{BUV} = V_{BUV}/V_{REF}$ V_{FB} falling
DRE Detection Threshold Ratio	R_{DRE_LO}	93.5	95.0	96.5	%	$R_{DRE_LO} = V_{DRE_LO}/V_{REF}$ V_{FB} falling
DRE Recovery Threshold Ratio	R_{DRE_HI}	96.5	98.0	99.5	%	$R_{DRE_HI} = V_{DRE_HI}/V_{REF}$ V_{FB} rising
[SLEEP Pin Detection]						
SLEEP ON Resistance	R_{ON_SLEEP}	12	25	55	Ω	
SLEEP Leak Current	I_{LEAK_SLEEP}	-10	0	+10	μA	
[FAULT Pin Detection]						
Thermal FAULT Threshold 1	V_{TH_FLT1}	855	900	945	mV	V_{FAULT} rising
Thermal FAULT Threshold 2	V_{TH_FLT2}	418	440	462	mV	V_{FAULT} falling
OVP FAULT Threshold 1	V_{OVP_FLT1}	0.874	0.920	0.966	V	V_{FAULT} falling
OVP FAULT Threshold 2	V_{OVP_FLT2}	2.85	3.00	3.15	V	V_{FAULT} rising
Detection Filter Delay (Thermal)	t_{FLT_DLY1}	2	3	4	ms	
Detection Filter Delay (OVP)	t_{FLT_DLY2}	2	3	4	ms	
Startup/Wake Delay	t_{WAKE_DLY}	4	5	6	ms	
FAULT Source Current	I_{FLT}	47	50	53	μA	

Electrical Characteristics(Unless otherwise specified $V_{HV} = 320\text{ V}$, $V_{CC} = 12\text{ V}$, $T_j = -40\text{ to }+125\text{ }^{\circ}\text{C}$) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[CS Pin Detection]						
CBC Current Limit Detection 1	$V_{CS1_LIM_POS(HL)}$	70	120	170	mV	at High-Line, AC = Positive
CBC Current Limit Detection 2	$V_{CS1_LIM_NEG(HL)}$	-170	-120	-70	mV	at High-Line, AC = Negative
CBC Current Limit Detection 3	$V_{CS1_LIM_POS(LL)}$	220	270	320	mV	at Low-Line, AC = Positive
CBC Current Limit Detection 4	$V_{CS1_LIM_NEG(LL)}$	-320	-270	-220	mV	at Low-Line, AC = Negative
Current Protection Threshold 1	$V_{CS2_LIM_POS}$	360	420	480	mV	AC = Positive
Current Protection Threshold 2	$V_{CS2_LIM_NEG}$	-480	-420	-360	mV	AC = Negative
[Thermal Shutdown]						
Thermal Shutdown Threshold	T_{SD}	-	175	-	$^{\circ}\text{C}$	Temperature rising
Thermal Shutdown Hysteresis	$T_{SD(HYS)}$	-	25	-	$^{\circ}\text{C}$	Temperature falling

Typical Performance Curves

(Reference Data)

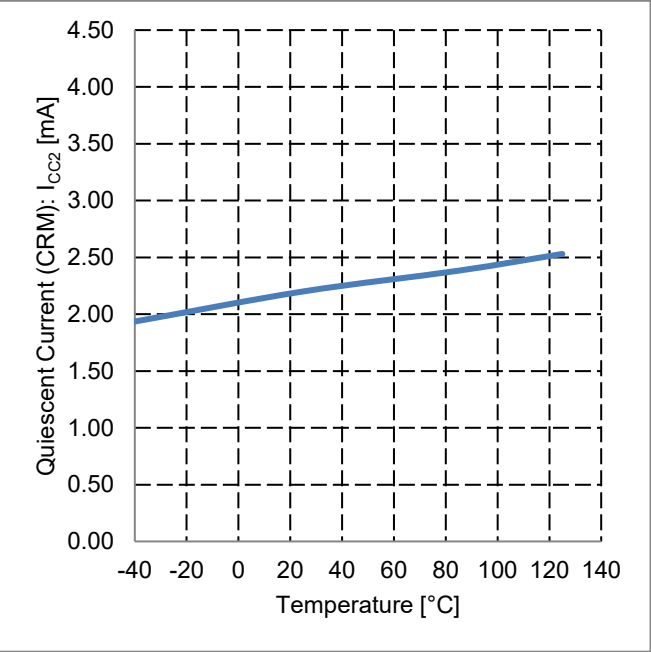


Figure 27. Quiescent Current (CRM) vs Temperature
(VCC = 12 V)

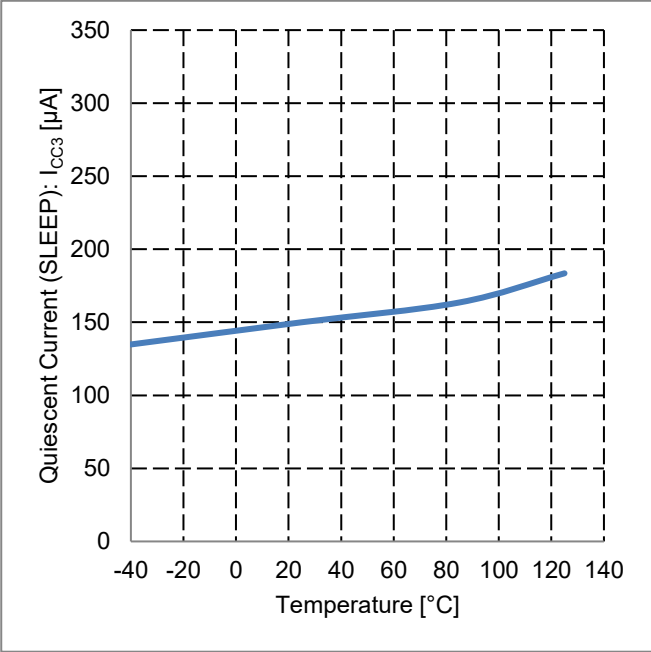


Figure 28. Quiescent Current (SLEEP) vs Temperature
(VCC = 12 V)

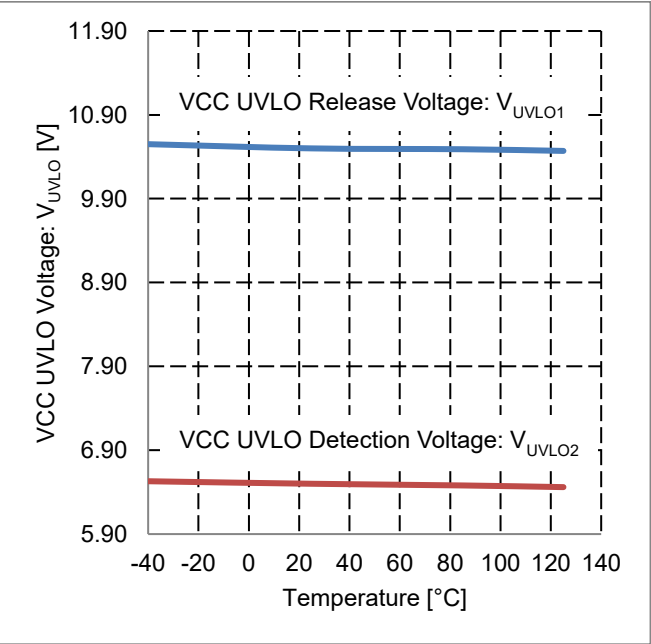


Figure 29. VCC UVLO Voltage vs Temperature

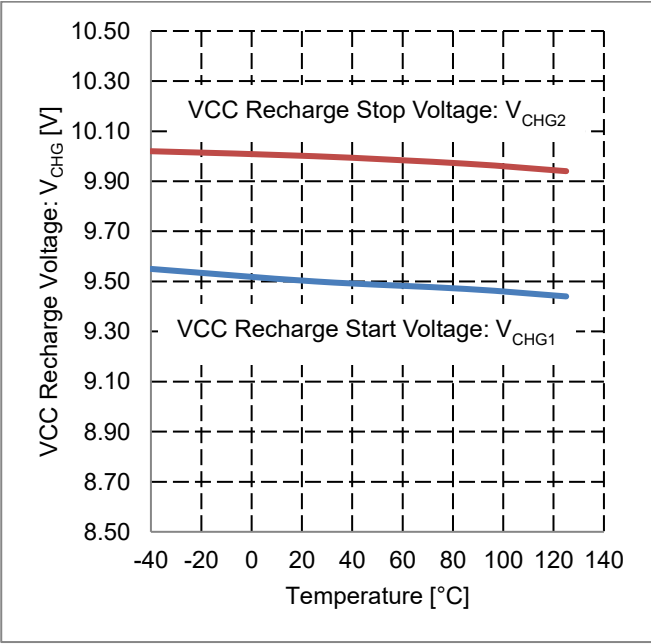


Figure 30. VCC Recharge Voltage vs Temperature

Typical Performance Curves - continued

(Reference Data)

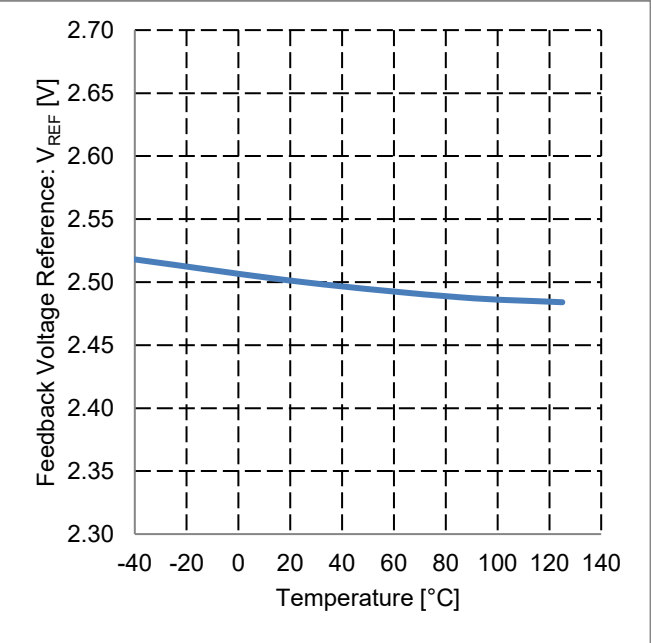


Figure 31. Feedback Voltage Reference vs Temperature
(VCC = 12 V)

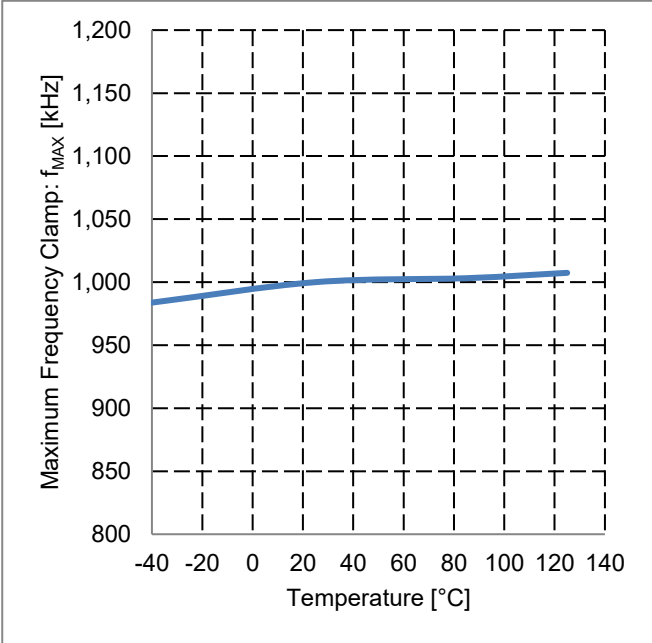


Figure 32. Maximum Frequency Clamp vs Temperature
(VCC = 12 V)

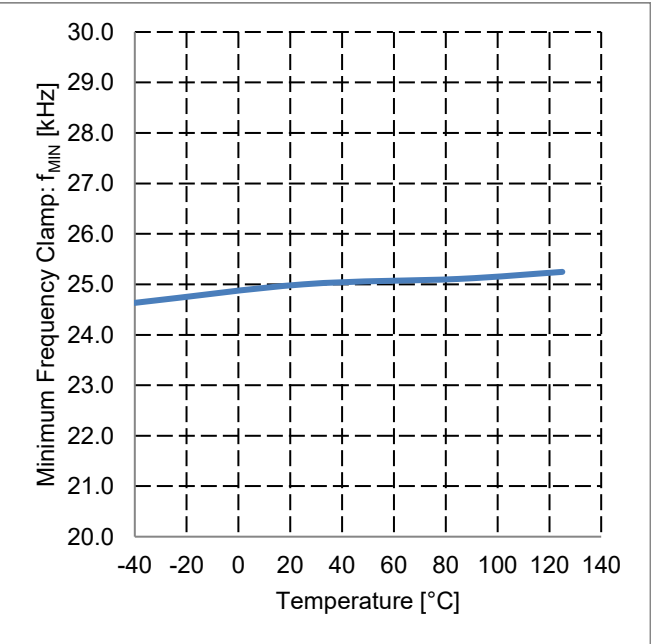


Figure 33. Minimum Frequency Clamp vs Temperature
(VCC = 12 V)

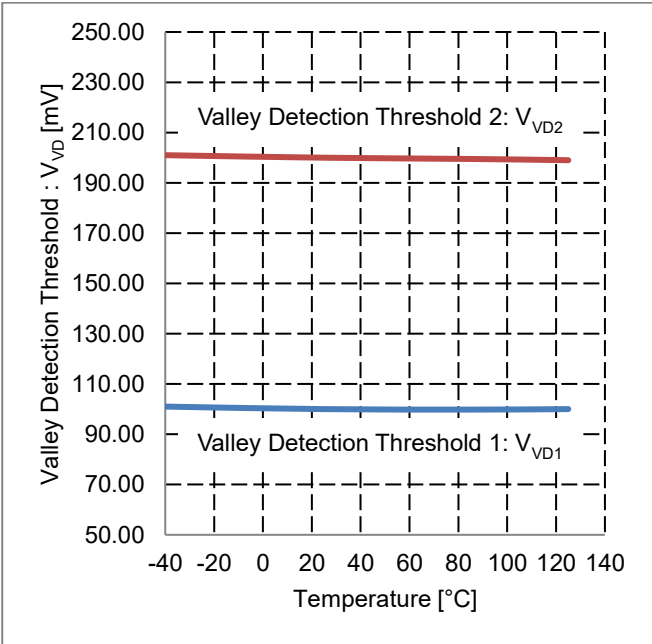


Figure 34. Valley Detection Threshold vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

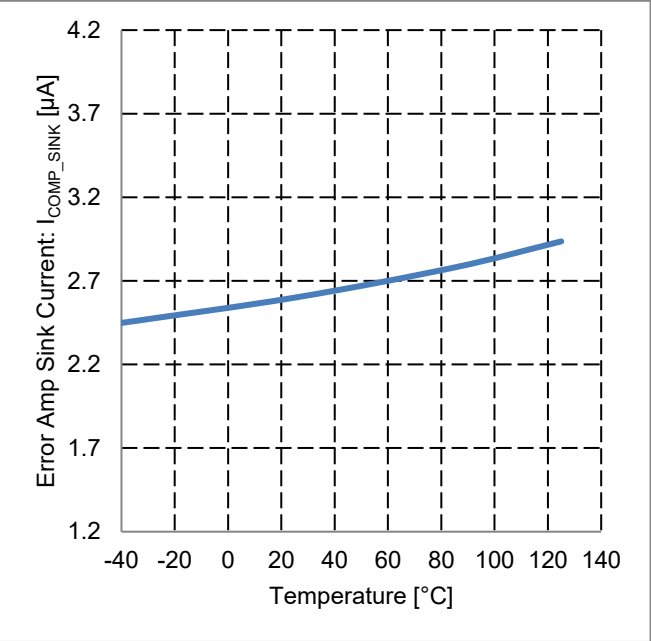


Figure 35. Error Amp Sink Current vs Temperature
(VCC = 12 V)

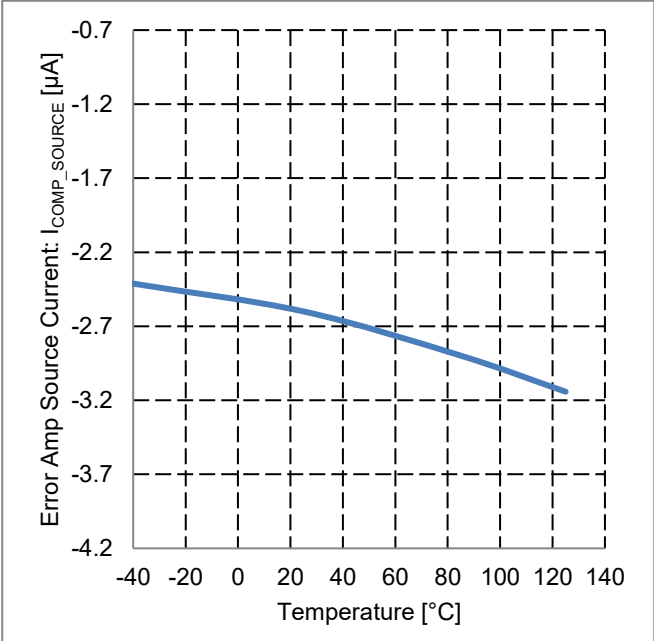


Figure 36. Error Amp Source Current vs Temperature
(VCC = 12 V)

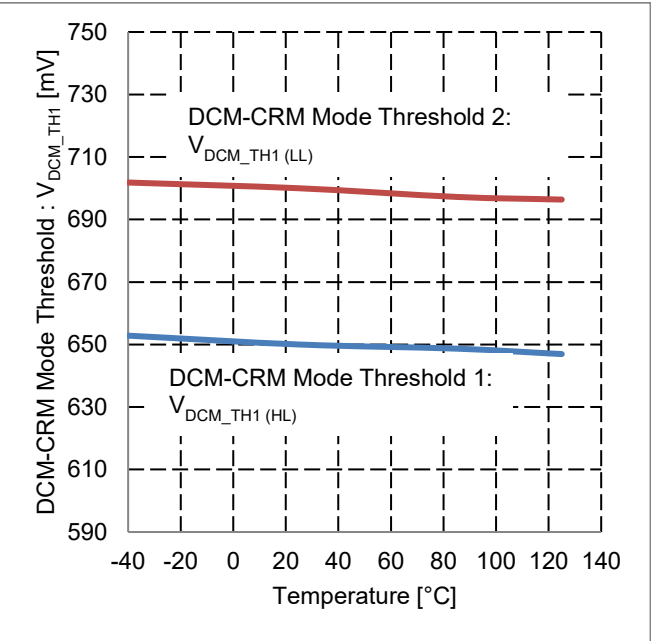


Figure 37. DCM-CRM Mode Threshold vs Temperature
(VCC = 12 V)

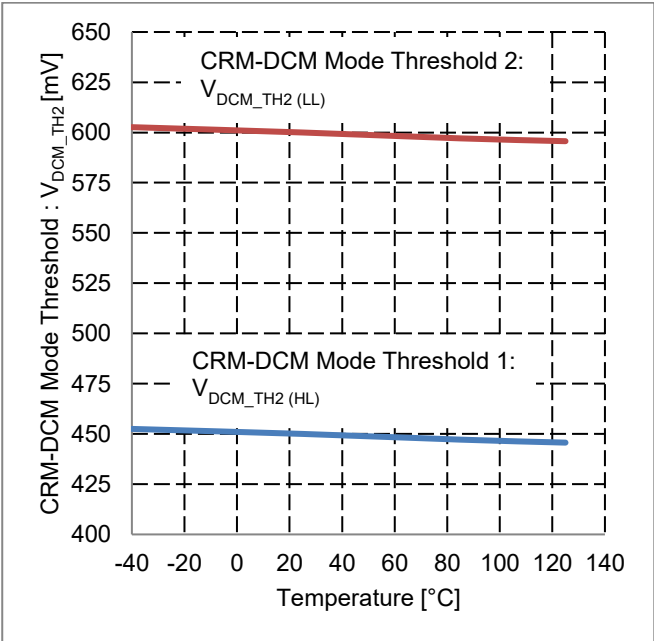


Figure 38. CRM-DCM Mode Threshold vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

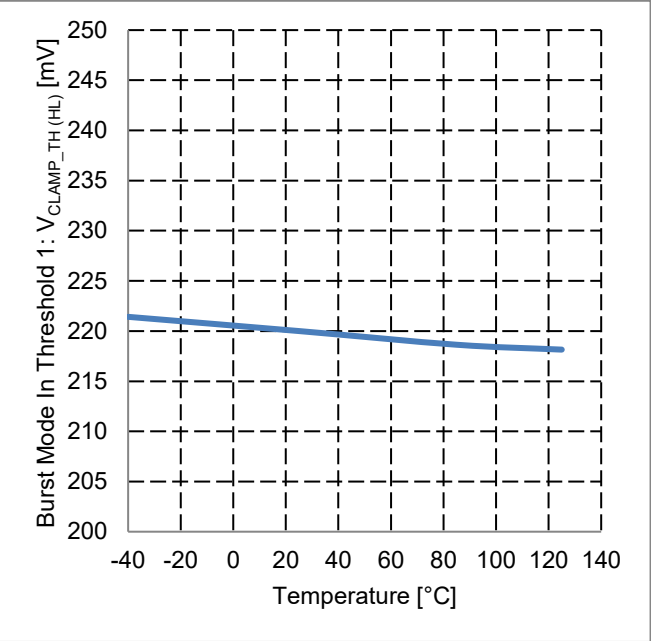


Figure 39. Burst Mode In Threshold 1 vs Temperature
(VCC = 12 V)

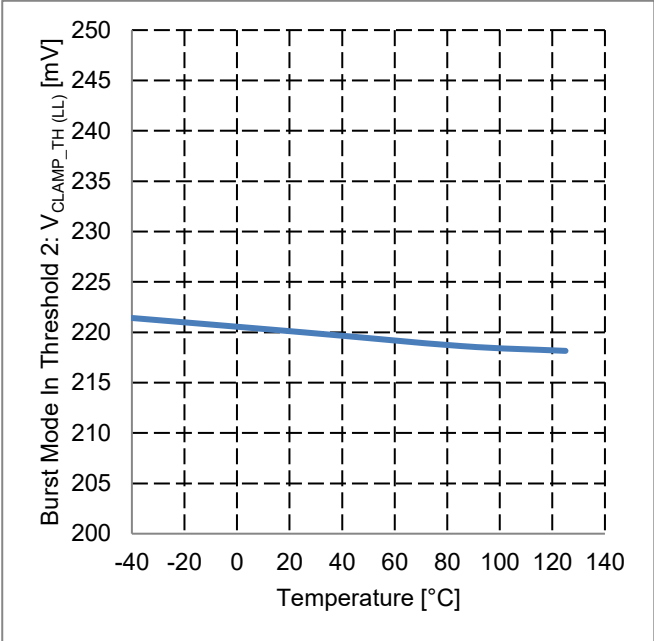


Figure 40. Burst Mode In Threshold 2 vs Temperature
(VCC = 12 V)

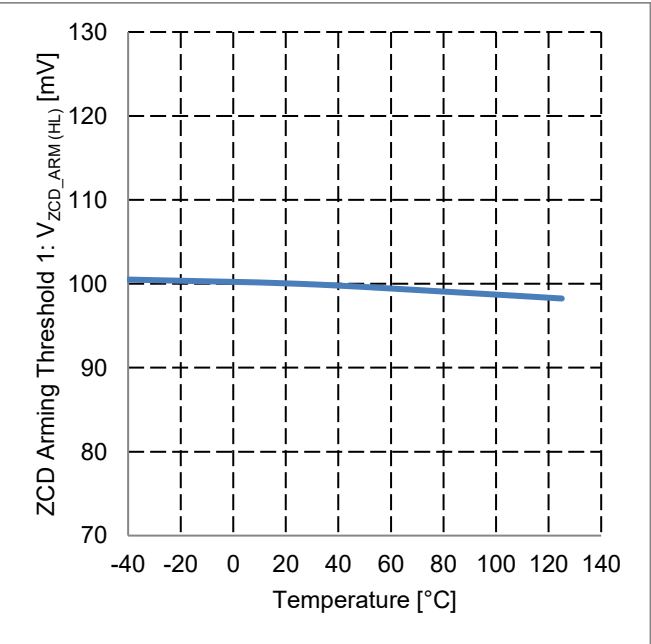


Figure 41. ZCD Arming Threshold 1 vs Temperature
(VCC = 12 V)

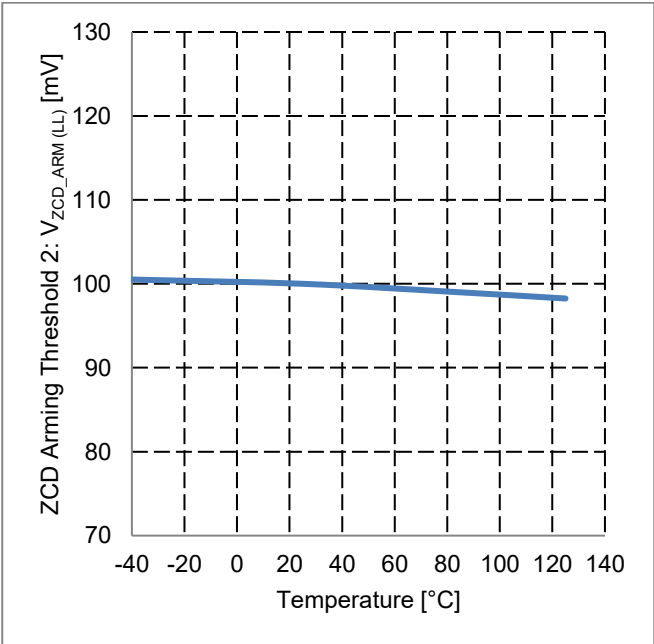


Figure 42. ZCD Arming Threshold 2 vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

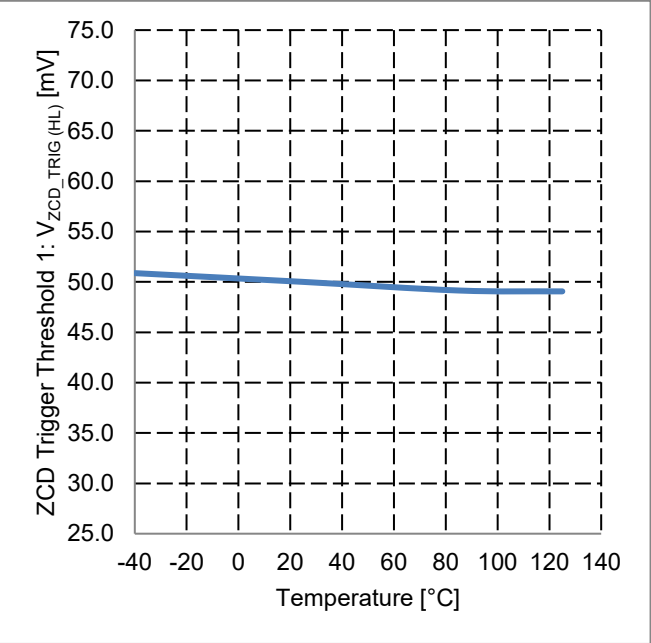


Figure 43. ZCD Trigger Threshold 1 vs Temperature
(VCC = 12 V)

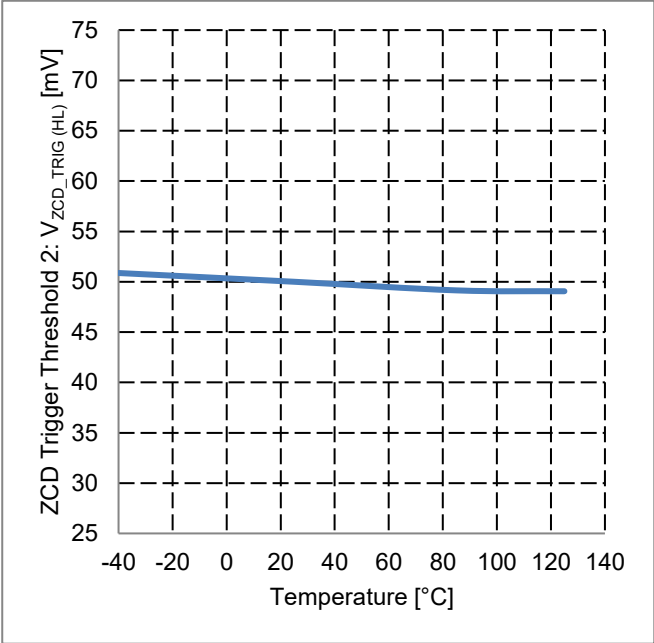


Figure 44. ZCD Trigger Threshold 2 vs Temperature
(VCC = 12 V)

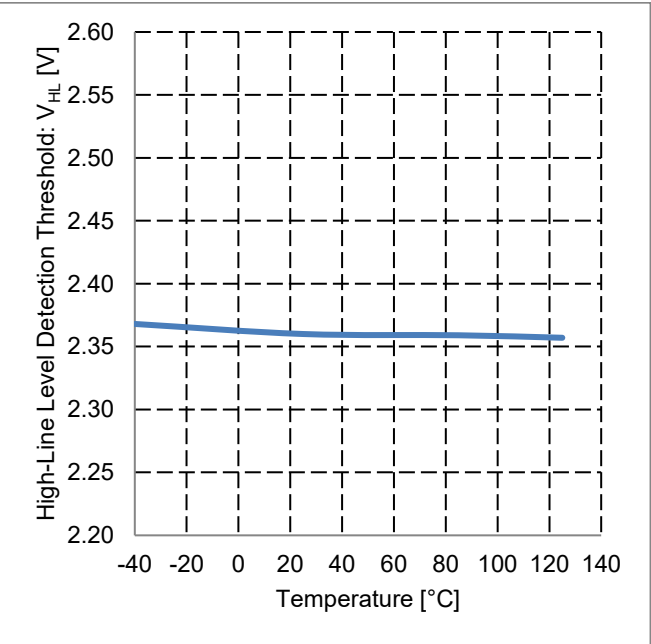


Figure 45. High-Line Level Detection Threshold
vs Temperature
(VCC = 12 V)

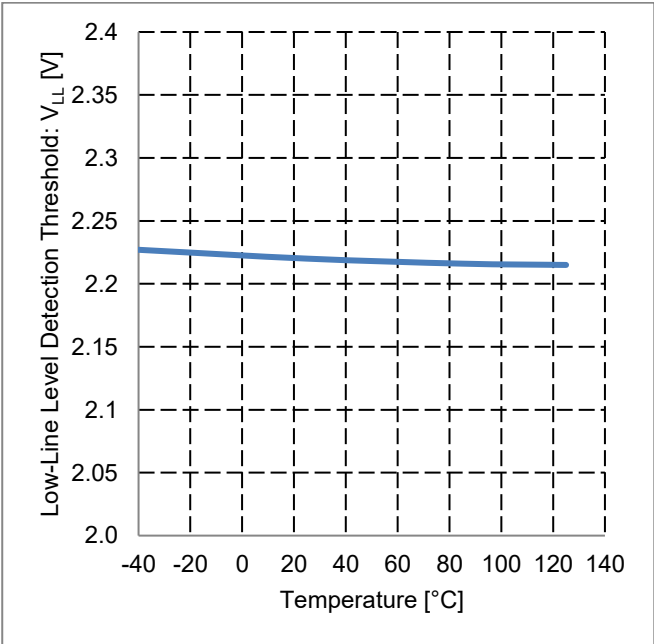


Figure 46. Low-Line Level Detection Threshold
vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

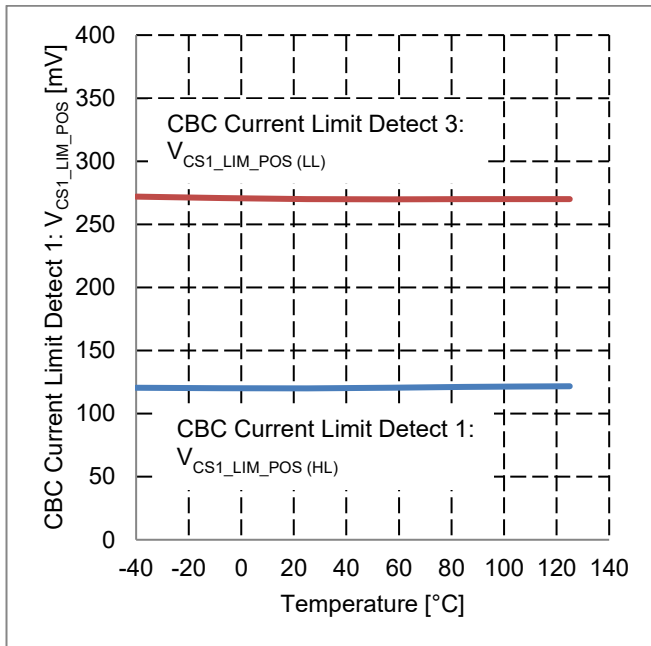


Figure 47. CBC Current Limit Detect (POS) vs Temperature
(VCC = 12 V)

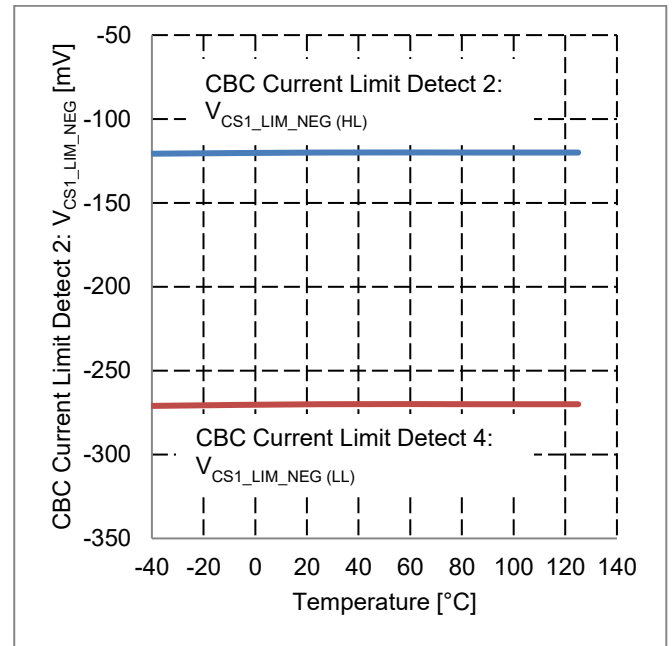


Figure 48. CBC Current Limit Detect (NEG) vs Temperature
(VCC = 12 V)

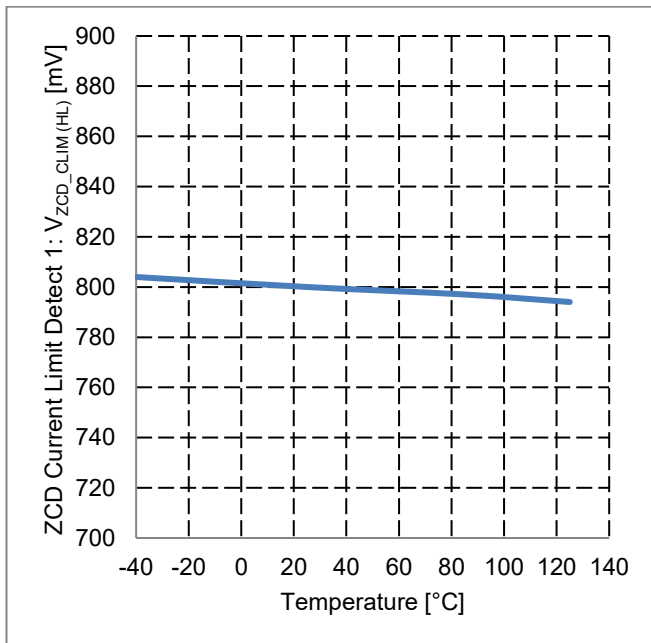


Figure 49. ZCD Current Limit Detect 1 vs Temperature
(VCC = 12 V)

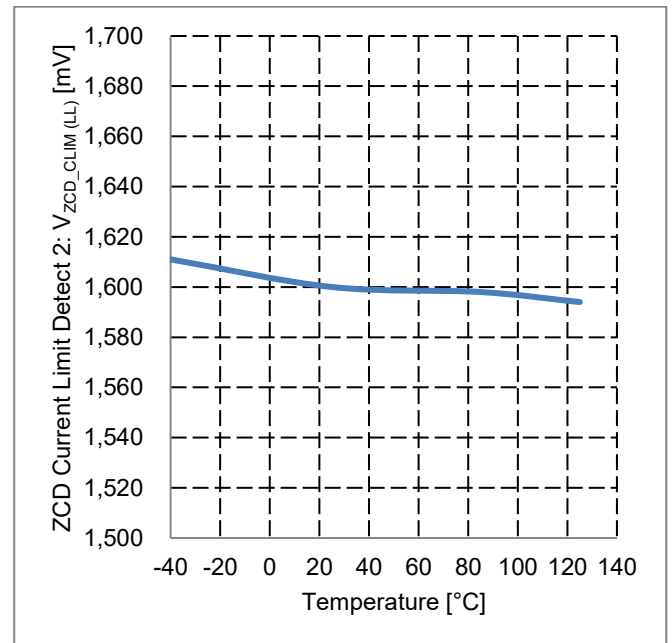


Figure 50. ZCD Current Limit Detect 2 vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

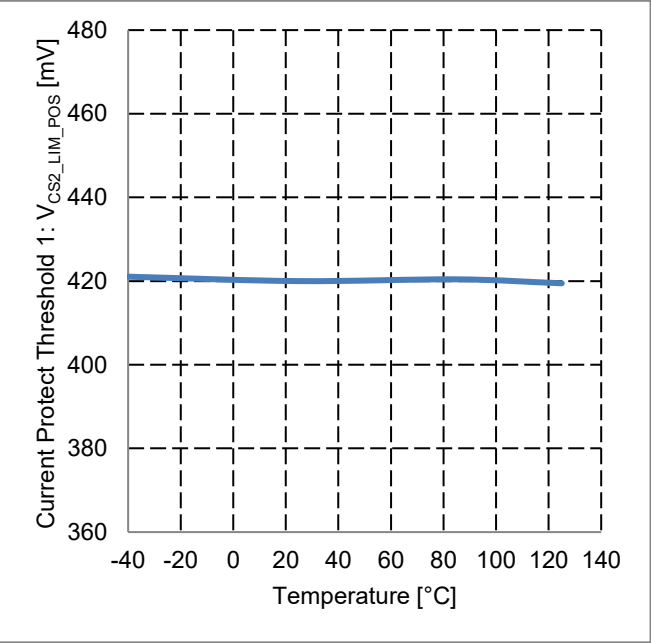


Figure 51. Current Protect Threshold 1 vs Temperature
(VCC = 12 V)

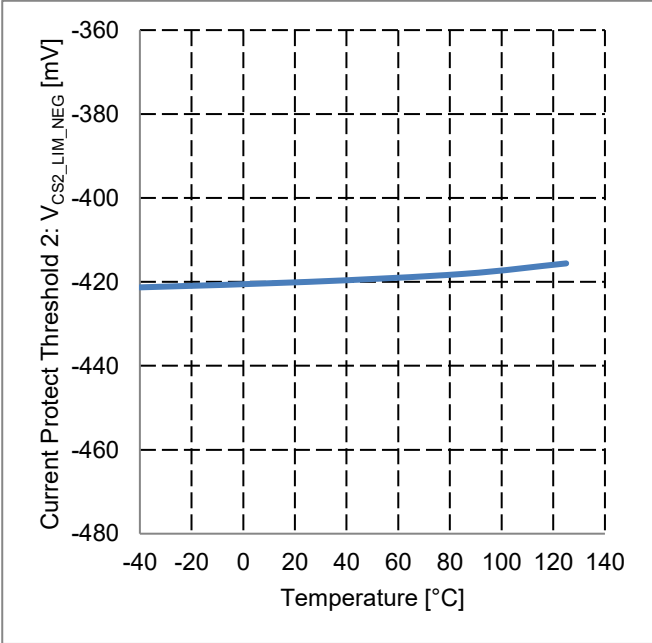


Figure 52. Current Protect Threshold 2 vs Temperature
(VCC = 12 V)

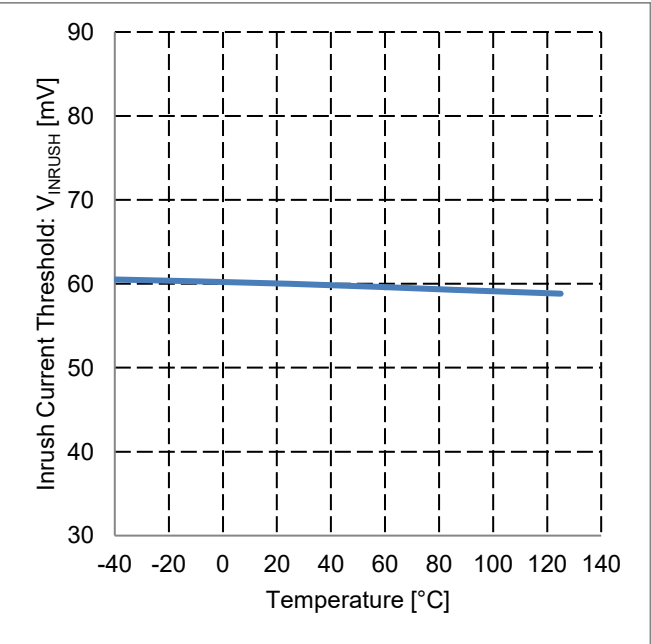


Figure 53. Inrush Current Threshold vs Temperature
(VCC = 12 V)

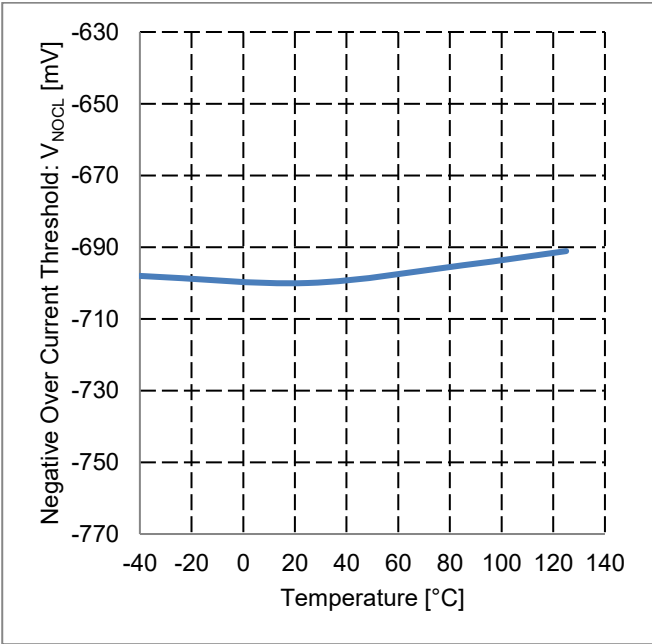


Figure 54. Negative Over Current Threshold vs Temperature
(VCC = 12 V)

Typical Performance Curves - continued

(Reference Data)

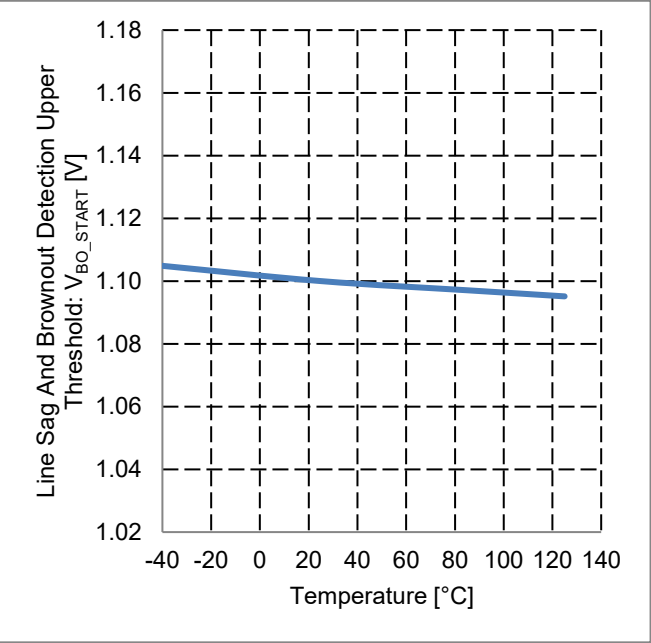


Figure 55. Line Sag And Brownout Detection Upper Threshold vs Temperature (VCC = 12 V)

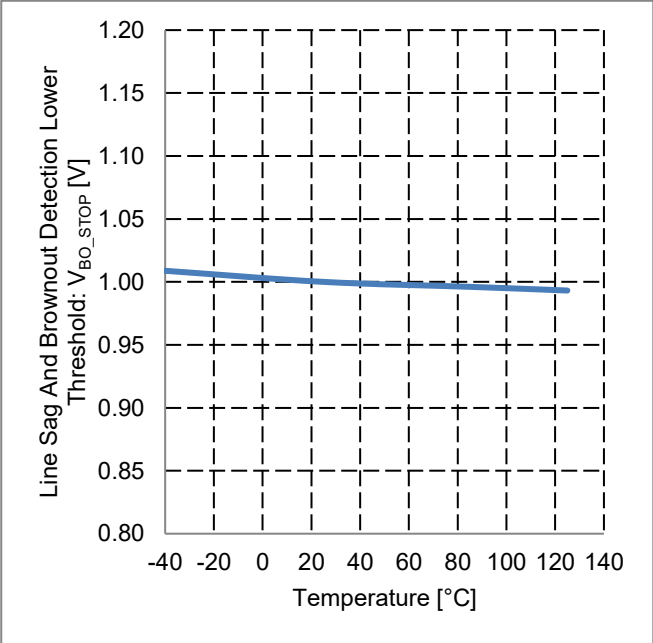


Figure 56. Line Sag And Brownout Detection Lower Threshold vs Temperature (VCC = 12 V)

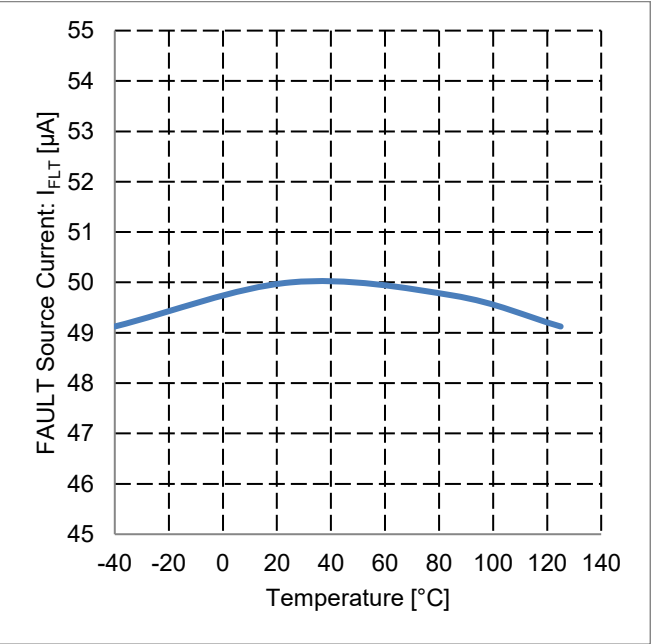


Figure 57. FAULT Source Current vs Temperature (VCC = 12 V)

Application Example

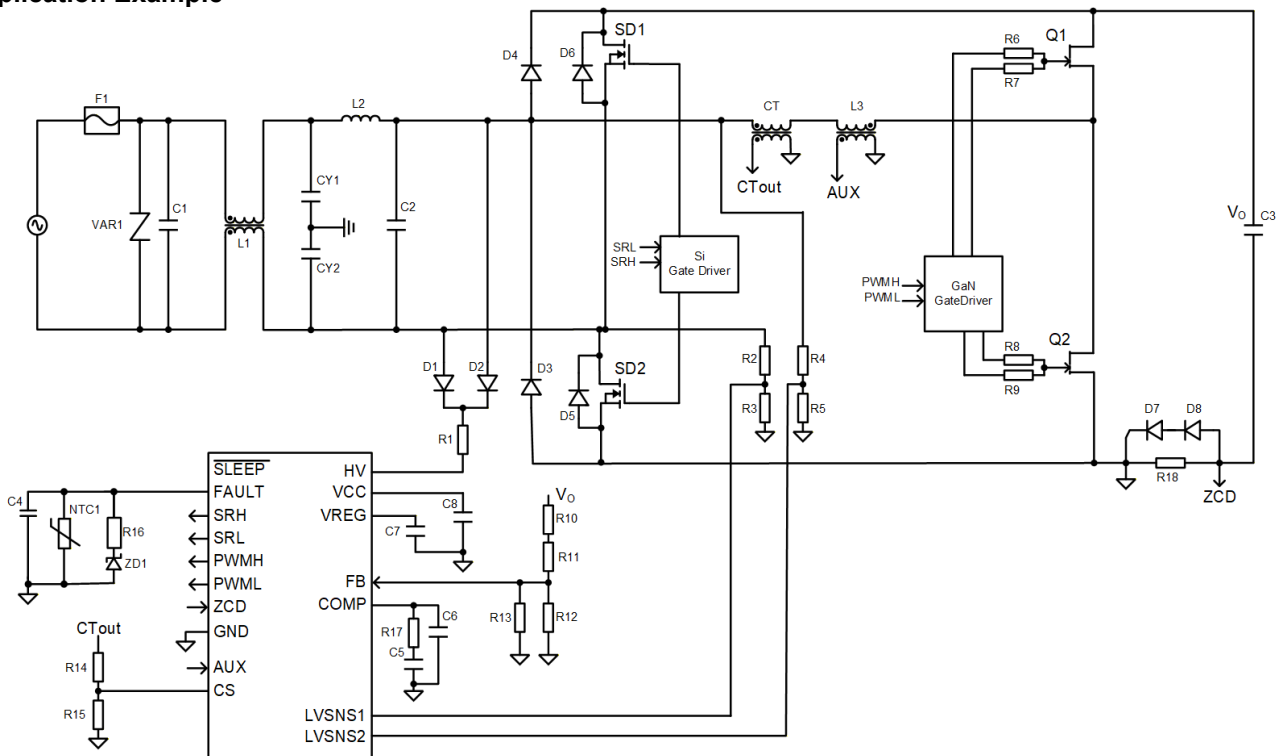


Figure 58. Application Example

1 Output Voltage Setting

The output voltage is determined by the feedback resistor connected to the FB pin.

$$V_{OUT} = \left(1 + \frac{(R_{10} + R_{11})}{(R_{12} // R_{13})}\right) \times V_{REF} = \left(1 + \frac{7.8 M\Omega}{50 k\Omega}\right) \times 2.5 V = 392.5 V$$

where:

$R_{10} + R_{11}$ is the upper resistance value of output feedback

$R_{12} // R_{13}$ is the lower combined resistance value of output feedback

V_{REF} is the Feedback Voltage Reference

2 Calculation of Inductance

Reference when $V_{OUT} = 400 V$ and power = 330 W

$$L3 = 82 \mu H$$

If L is set to a larger value, THD will be lowered, but the part size will be larger.

3 Input voltage detection

The Brownout voltage is set so that switching begins when the voltage divider ratio is 1:100 and the input voltage exceed approximately 80 V_{AC}.

If the voltage divider resistor is too small, the voltage divider loss increases, worsening the no-load loss.

The recommended values are as follows:

$$1:100 = R3:(R2 + R3) = R5:(R4 + R5) = 100 k\Omega : 9.9 M\Omega$$

It is recommended to attach a filter capacitor to the LVSNS1 and the LVSNS2 to remove noise.

4 Compensator

Reference when power = 330 W, $L3 = 82 \mu H$ and $C3 = 300 \mu F$

$$C5 = 2.2 \mu F, C6 = 0.047 \mu F, R17 = 68 k\Omega$$

These parameters must be adjusted according to the inductance of L3 and capacitance of C3.

I/O Equivalence Circuit

1	SLEEP	2	FAULT	3	SRH	4	SRL
5	PWMH	6	PWML	7	ZCD	8	GND
9	AUX	10	CS	11	LVSNS2	12	LVSNS1
13	COMP	14	FB	15	VREG	16	TEST
17	VCC	18	NC	19	NC	20	HV
		No Connection		No Connection			

Figure 59. I/O Equivalence Circuits

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

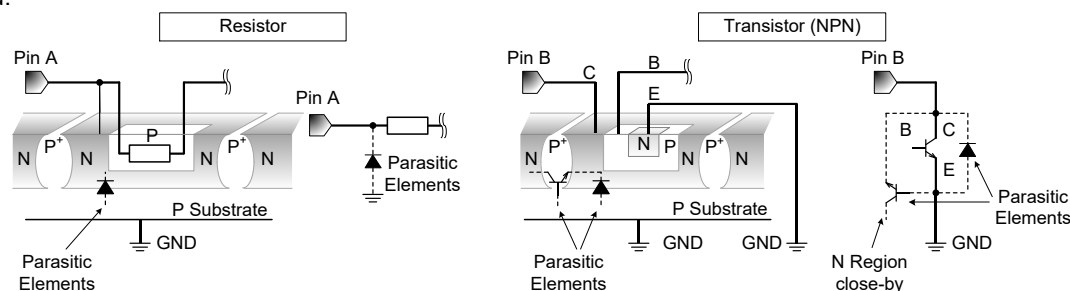


Figure 60. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

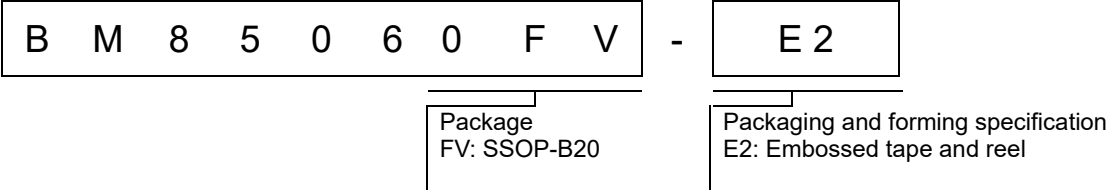
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

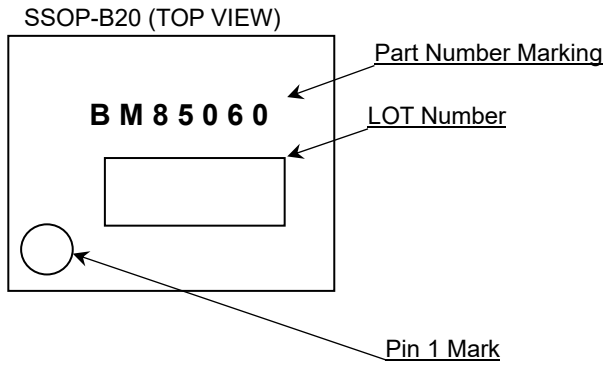
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

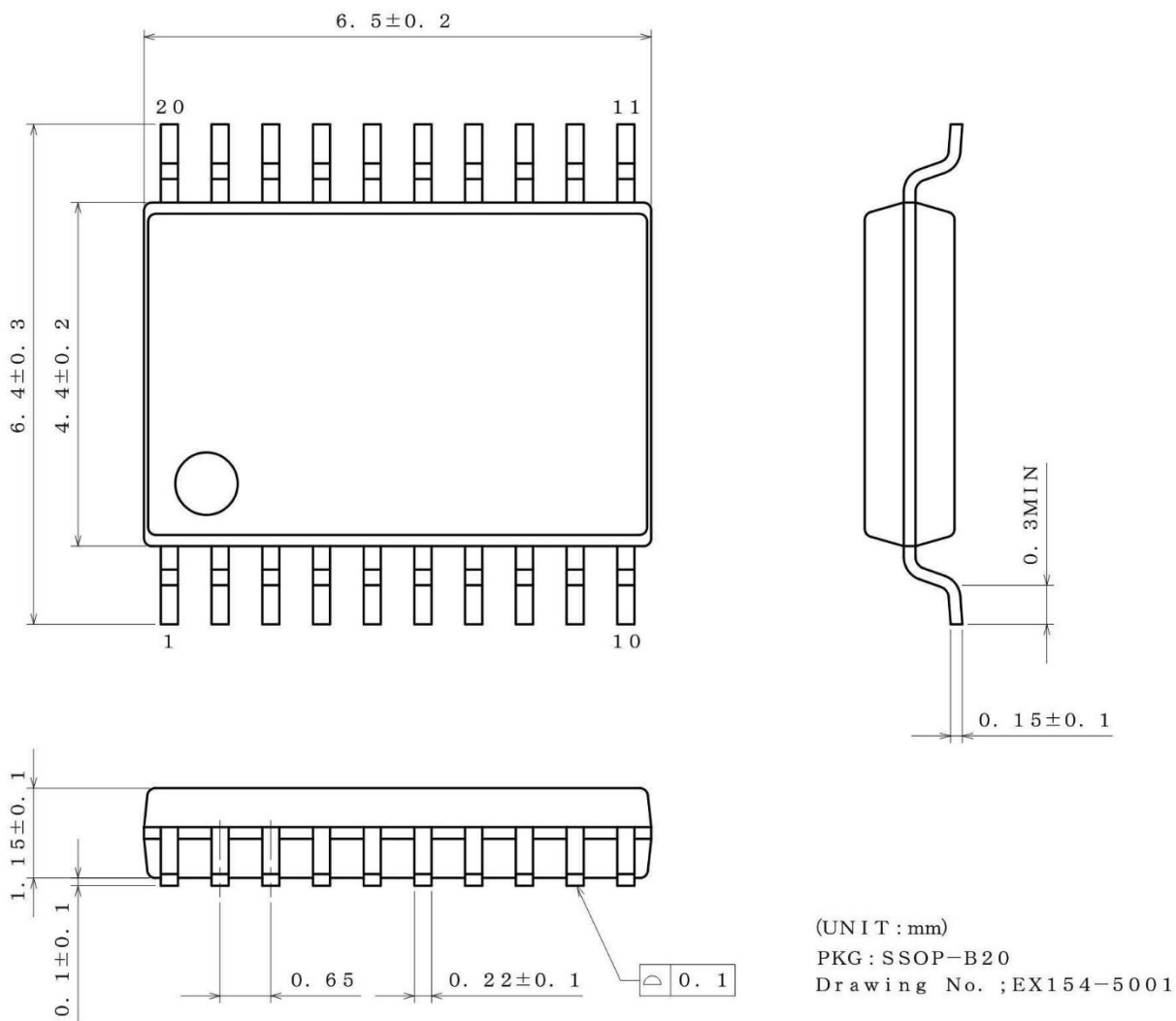


Marking Diagram



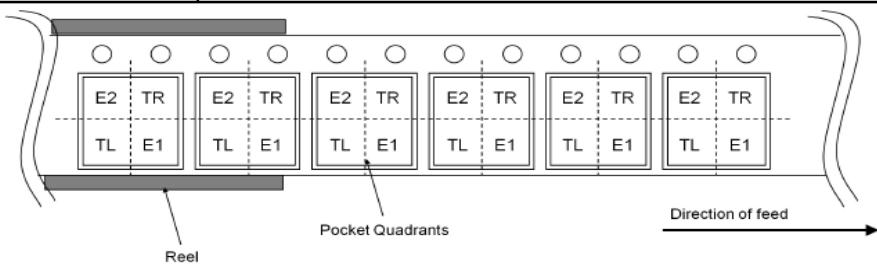
Physical Dimension and Packing Information

Package Name	SSOP-B20
--------------	----------



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
09.Feb.2026	001	New release

Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - Installation of protection circuits or other protective devices to improve system safety
 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application examples, their constants, software, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.
2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).
3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.
2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.
3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.
4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.
2. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.
2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.
3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.