NEX40400

4.5 V to 40 V, 600 mA, synchronous step-down converter

Rev. 1 — 6 December 2024 Product data sheet

1. General description

The NEX40400 is a high efficiency step-down converter with low operating quiescent current of typically 60 µA. It provides up to 600 mA output with current mode control for fast loop response.

The wide 4.5 V to 40 V input range is suitable for variety of the power step-down applications in industrial and automotive environments. 0.3 µA ultra-low shutdown supply current allows use in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by folding down the switching frequency at light load condition reducing the switching losses.

Frequency foldback helps to prevent inductor current runaway during start-up and to allow operation in both high conversion ratio and low drop-out cases. Thermal shutdown provides reliable and robust operation.

The NEX40400 comes in a cost-effective 6 leads SOT8061-1 (TSOT23-6) plastic, surface-mounted package with 2.9 mm x 1.6 mm body dimensions.

2. Features and benefits

- 4.5 V to 40 V wide input voltage range
- 600 mA continuous output current
- 60 µA standby, 0.3 µA shutdown current
- 1% output voltage accuracy
- 1.05 MHz and 2.1 MHz fixed switching frequency
- Pulse Frequency Modulation (PFM) option for light load efficiency
- Frequency foldback for high conversion ratio and low drop-out applications
- Force PWM (FPWM) option for small output ripple
- Spread spectrum for better EMI
- Start-up with pre-biased output
- Precision enable
- Internal compensation
- Short circuit protection with Hiccup mode
- SOT8061-1 (TSOT23-6) 6 leads, plastic surface-mounted package

3. Target applications

- Industrial distributed power systems
- Grid infrastructure: Smart E-meter
- Battery powered home appliances
- White goods

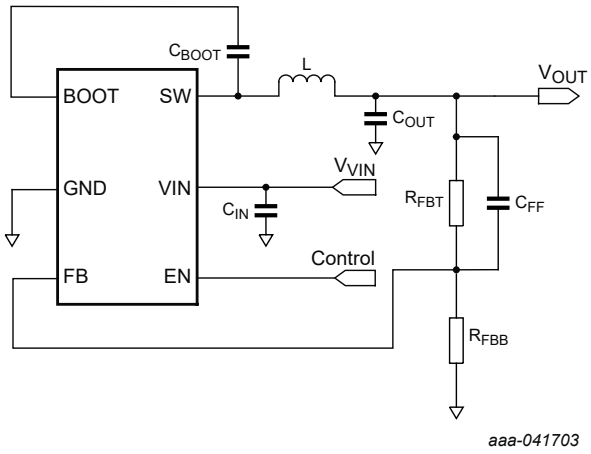
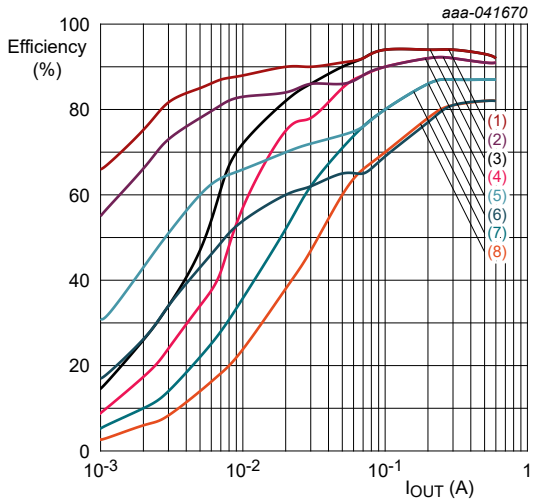


Fig. 1. Typical application circuit



V_{OUT} = 5 V, f_{SW} = 1.05 MHz

(1) PFM, V_{VIN} = 8 V
(2) PFM, V_{VIN} = 12 V
(3) FPWM, V_{VIN} = 8 V
(4) FPWM, V_{VIN} = 12 V
(5) PFM, V_{VIN} = 24 V
(6) FPM, V_{VIN} = 40 V
(7) FPWM, V_{VIN} = 24 V
(8) FPWM, V_{VIN} = 40 V

Fig. 2. Efficiency versus load current

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX40400ADA	-40 °C to +150 °C	TSOT23-6	Plastic, surface-mounted package (TSOT23-6); 6 leads	SOT8061-1
NEX40400BDA				
NEX40400CDA				
NEX40400DDA				
NEX40400EDA				
NEX40400FDA				

5. Marking

Table 2. Marking

Type number	Marking code
NEX40400ADAZ	N4A
NEX40400BDAZ	N4B
NEX40400CDAZ	N4C
NEX40400DDAZ	N4D
NEX40400EDAZ	N4E
NEX40400FDAZ	N4F

6. Pinout

6.1. Pinout

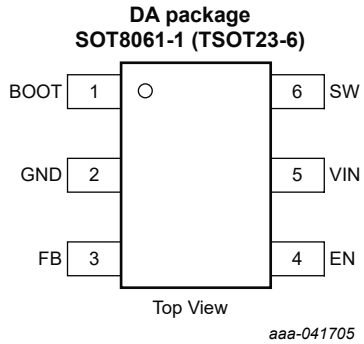


Fig. 3. Pin configuration SOT8061-1 (TSOT23-6)

6.2. Pin description

Table 3. Pin description

Pin		I/O	Description
Number	Name		
1	BOOT	PWR	Bootstrap capacitor connection for high-side FET drive. Connect 100 nF or larger capacitor between the BOOT pin and SW pin.
2	GND	PWR	Power ground pin, internally connected to the source of low-side FET. Connect to system ground. Path to the input decoupling capacitor must be short.
3	FB	IN	Inverting input of the error amplifier. Connect FB pin to the middle of a resistor divider of the converter output to set the target output voltage.
4	EN	IN	Precision enable input of the converter. High level enables converter. Can be tied to VIN. Adjustable UVLO can be achieved by connecting EN to the middle of a resistor divider between VIN and ground.
5	VIN	PWR	Power supply input for internal bias LDO and high-side FET. Place 2.2 µF or larger decoupling capacitor between VIN and ground close to this pin.
6	SW	OUT	The switch pin is connected to the internal power MOSFET switches. Connect SW pin to the inductor of the output LC filter.

7. Device Comparison

Table 4. Device Comparison

Type number	Operation Mode	Spread Spectrum	Switching Frequency
NEX40400ADAZ	PFM	Off	2.1 MHz
NEX40400BDAZ	FPWM	Off	2.1 MHz
NEX40400CDAZ	FPWM	On	2.1 MHz
NEX40400DDAZ	PFM	Off	1.05 MHz
NEX40400EDAZ	FPWM	Off	1.05 MHz
NEX40400FDAZ	FPWM	On	1.05 MHz

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{VIN}	supply voltage		-0.3	+42	V
V_{SW}	switch node voltage	DC	-0.3	V_{VIN} + 0.3	V
		AC, less than 20 ns	-3.5	V_{VIN} + 0.3	V
V_{EN}	EN pin voltage		-0.3	V_{VIN} + 0.3	V
V_{FB}	FB pin voltage		-0.3	+6	V
$V_{BOOT-SW}$	BOOT pin voltage	Referenced to SW node	-0.3	+6	V
T_j	junction temperature		-40	+150	°C
T_{stg}	storage temperature		-65	+150	°C

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{CCA}	supply voltage	4.5		40	V
I_{OUT}	output current	0		0.6	A
V_{EN}	enable input	0		V_{VIN}	V
V_{FB}	feedback input		0.8		V
T_j	junction temperature	-40		150	°C

10. ESD ratings

Table 7. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	± 2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	± 500	V

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Condition	SOT402-1	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	90	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case (top) of package	in free air; JEDEC test board	32	°C/W

12. Characteristics

12.1. Electrical characteristics

Table 9. Electrical characteristics

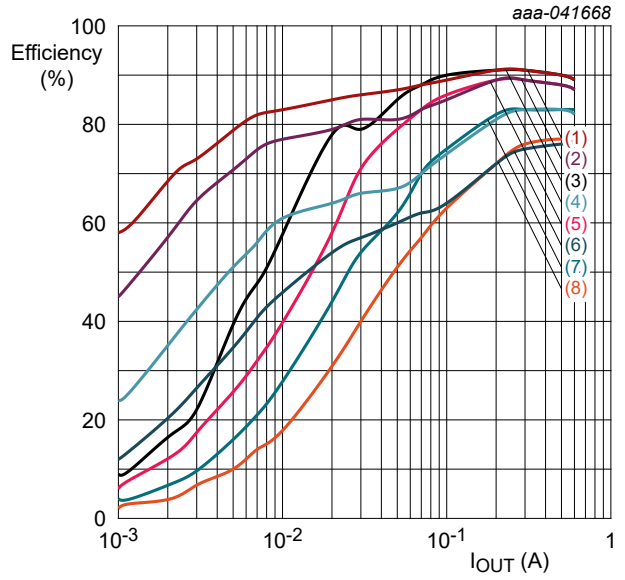
V_{VIN} = 4.5 V to 40 V, typical values are at T_j = 25 °C (unless otherwise noted)

Symbol	Parameter	Test Conditions	T_j = -40 °C to 150 °C			Unit
			Min	Typ	Max	
Supply (VIN pin)						
I_Q	operating quiescent current (non-switching)	PFM variants, V_{VIN} = 12 V, V_{EN} = V_{VIN}, V_{FB} = 0.9 V	-	60	100	µA
I_{SD}	shutdown current	V_{VIN} = 12 V, EN = GND	-	0.3	1.5	µA
V_{IN_UVLO+}	undervoltage lockout threshold	rising V_{VIN}	-	4.3	4.4	V
V_{IN_UVLO-}		falling V_{VIN}	3.8	3.9	-	V
Enable (EN pin)						
V_{EN_H}	enable rising threshold		-	1.23	1.30	V
V_{EN_L}	enable falling threshold		1.0	1.1	-	V
V_{EN_HYS}	enable hysteresis voltage		-	0.13	-	V
I_{EN}	leakage current at EN	V_{VIN} = 12 V, V_{EN} = 3.3 V	-	10	100	nA
Power switches						
R_{ON_HS}	high side MOSFET on-resistance	V_{VIN} = 12 V, V_{BOOT} - V_{SW} = 5 V, I = 200 mA	-	440	800	mΩ
R_{ON_LS}	low side MOSFET on-resistance	V_{VIN} = 12 V, I = 200 mA	-	240	450	mΩ
t_{ON_MIN}	minimum ON time		-	45	-	ns
t_{OFF_MIN}	minimum OFF time	1.05 MHz FPWM variant	-	100	-	ns
t_{ON_MAX}	maximum ON time		-	10	-	µs
I_{HS_LIMIT}	peak inductor current limit		0.8	1.0	1.4	A
I_{LS_LIMIT}	valley inductor current limit		0.5	0.65	0.8	A
I_{LS_ZC}	zero cross threshold	PFM variants	-	30		mA
Voltage reference (FB pin)						
V_{REF}	reference voltage	T_j = 25 °C	792	800	808	mV
		T_j = -40 °C to 150 °C	788	800	812	mV
I_{FB}	leakage current at FB pin	V_{FB} = 0.85 V	-	5	50	nA
Oscillator						
f_{SW}	oscillator frequency	1.05 MHz variants	0.94	1.05	1.16	MHz
		2.1 MHz variants	1.88	2.1	2.32	MHz
f_{SW_SS}	spread spectrum switching frequency variation		-	+/-5	-	%
Hiccup and soft start						
t_{HIC_WAIT}	waiting time before hiccup shutdown	$V_{FB} \leq 0.4 \times V_{REF}$	-	256	-	clock cycles
t_{HICCUP}	hiccup shutdown time before restart	PFM variants	-	120	-	ms

Symbol	Parameter	Test Conditions	T_j = -40 °C to 150 °C			Unit
			Min	Typ	Max	
t_{SS}	internal soft-start time	the time for internal reference to ramp up from 10% to 90% of V_{REF}, V_{VIN} = 12 V	-	1.8	-	ms
Overvoltage protection						
V_{FB_OVP+}	overvoltage threshold	V_{FB} is rising, % of V_{REF}	-	109	-	%
V_{FB_OVP-}		V_{FB} is falling, % of V_{REF}	-	104	-	%
Thermal shutdown						
T_{SHDN}	thermal shutdown threshold	rising junction temperature	-	170	-	°C
T_{HYS}	hysteresis		-	15	-	°C

12.2. Typical characteristics

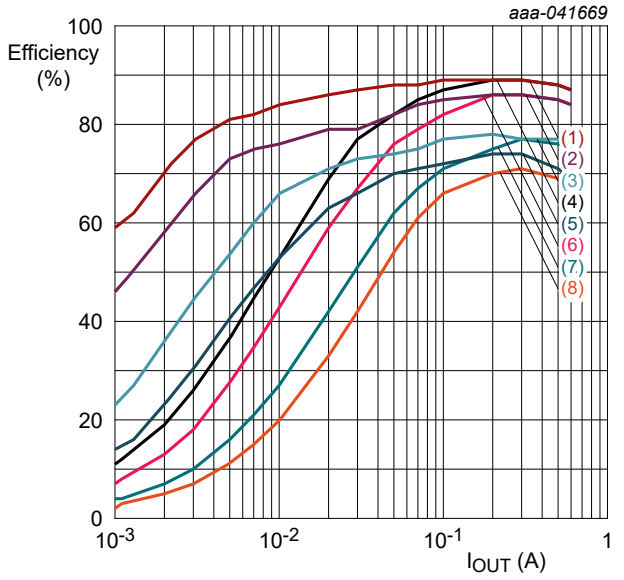
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); typical values are at 25 °C (unless otherwise noted).



V_{OUT} = 3.3 V, f_{SW} = 1.05 MHz

(1) PFM, V_{VIN} = 8 V
(2) PFM, V_{VIN} = 12 V
(3) FPWM, V_{VIN} = 8 V
(4) PFM, V_{VIN} = 24 V
(5) FPWM, V_{VIN} = 12 V
(6) FPM, V_{VIN} = 40 V
(7) FPWM, V_{VIN} = 24 V
(8) FPWM, V_{VIN} = 40 V

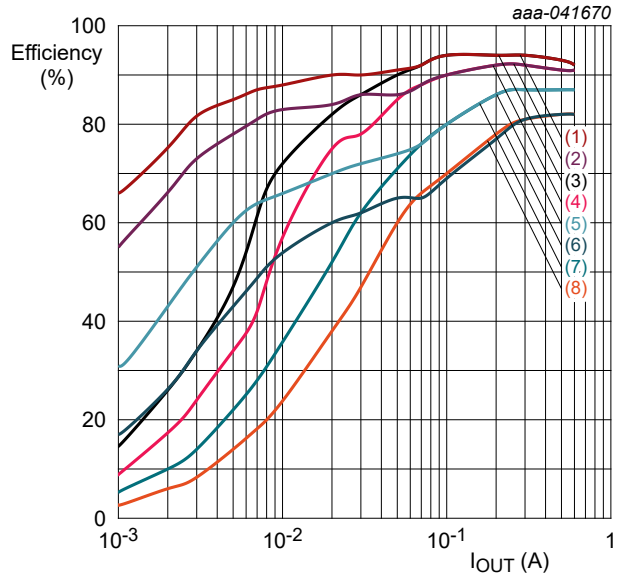
Fig. 4. Efficiency versus load current



V_{OUT} = 3.3 V, f_{SW} = 2.1 MHz

(1) PFM, V_{VIN} = 8 V
(2) PFM, V_{VIN} = 12 V
(3) PFM, V_{VIN} = 24 V
(4) FPWM, V_{VIN} = 8 V
(5) FPM, V_{VIN} = 36 V
(6) FPWM, V_{VIN} = 12 V
(7) FPWM, V_{VIN} = 24 V
(8) FPWM, V_{VIN} = 36 V

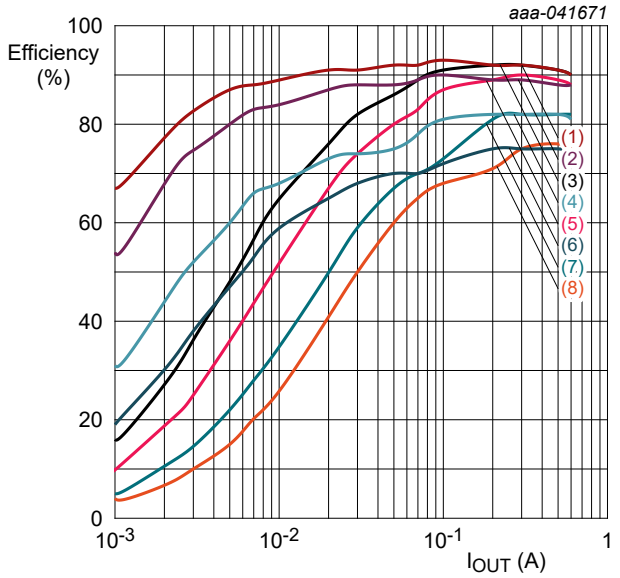
Fig. 5. Efficiency versus load current



V_{OUT} = 5 V, f_{SW} = 1.05 MHz

(1) PFM, V_{VIN} = 8 V
(2) PFM, V_{VIN} = 12 V
(3) FPWM, V_{VIN} = 8 V
(4) FPWM, V_{VIN} = 12 V
(5) PFM, V_{VIN} = 24 V
(6) FPM, V_{VIN} = 40 V
(7) FPWM, V_{VIN} = 24 V
(8) FPWM, V_{VIN} = 40 V

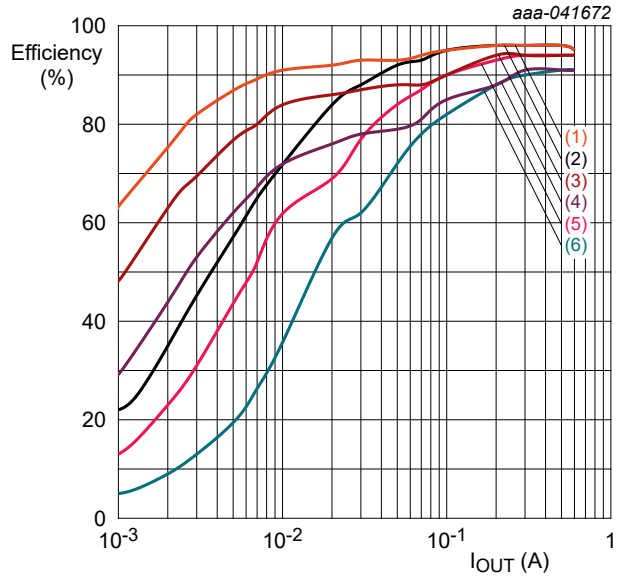
Fig. 6. Efficiency versus load current



V_{OUT} = 5 V, f_{SW} = 2.1 MHz

(1) PFM, V_{VIN} = 8 V
(2) PFM, V_{VIN} = 12 V
(3) FPWM, V_{VIN} = 8 V
(4) PFM, V_{VIN} = 24 V
(5) FPWM, V_{VIN} = 12 V
(6 PFM, V_{VIN} = 36 V
(7) FPWM, V_{VIN} = 24 V
(8) FPWM, V_{VIN} = 36 V

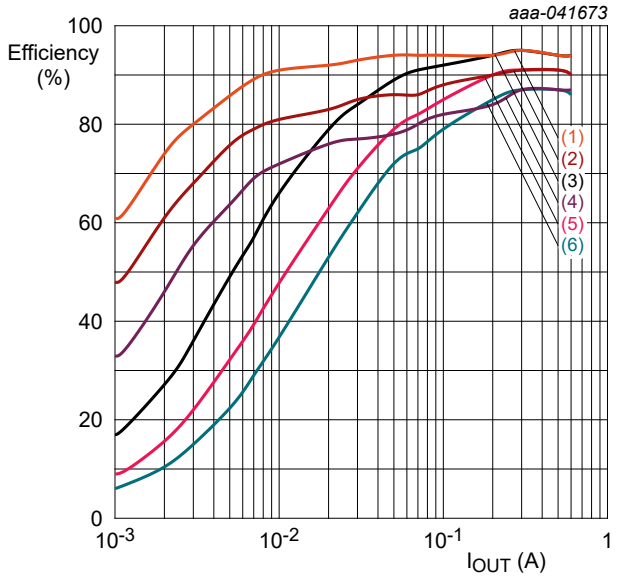
Fig. 7. Efficiency versus load current



V_{OUT} = 12 V, f_{SW} = 1.05 MHz

(1) PFM, V_{VIN} = 15 V
(2) FPWM, V_{VIN} = 15 V
(3) PFM, V_{VIN} = 24 V
(4) PFM, V_{VIN} = 40 V
(5) FPWM, V_{VIN} = 24 V
(6) FPWM, V_{VIN} = 40 V

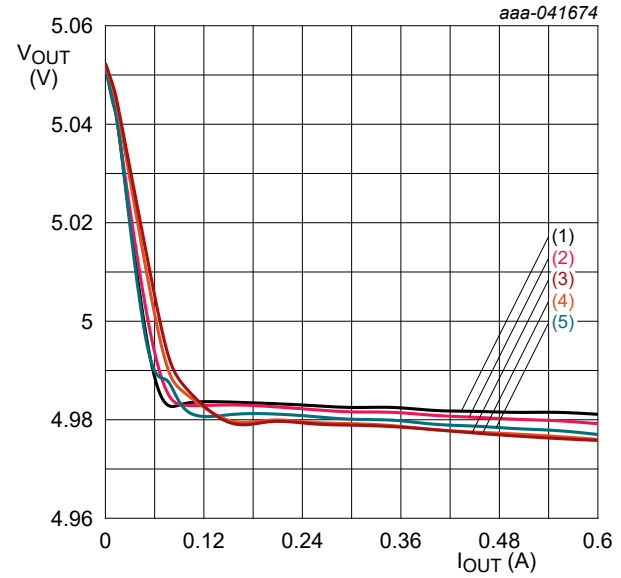
Fig. 8. Efficiency versus load current



V_{OUT} = 12 V, f_{SW} = 2.1 MHz

(1) PFM, V_{VIN} = 15 V
(2) PFM, V_{VIN} = 24 V
(3) FPWM, V_{VIN} = 15 V
(4) PFM, V_{VIN} = 36 V
(5) FPWM, V_{VIN} = 24 V
(6) FPWM, V_{VIN} = 36 V

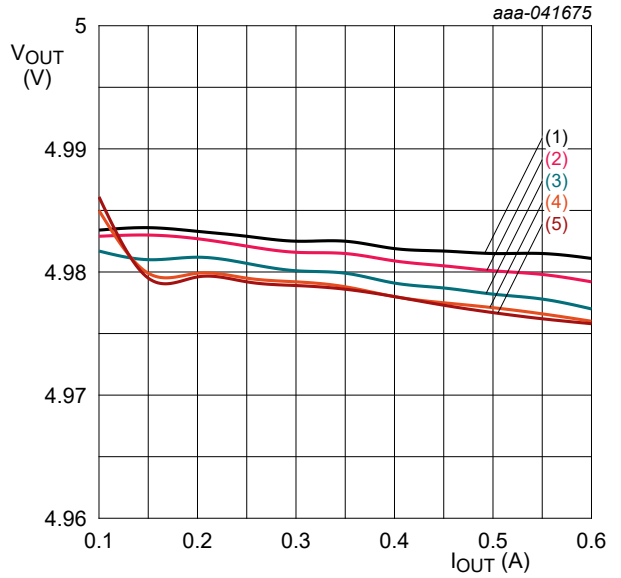
Fig. 9. Efficiency versus load current



PFM, V_{OUT} = 5 V, f_{SW} = 1.05 MHz

(1) V_{VIN} = 8 V
(2) V_{VIN} = 12 V
(3) V_{VIN} = 40 V
(4) V_{VIN} = 36 V
(5) V_{VIN} = 24 V

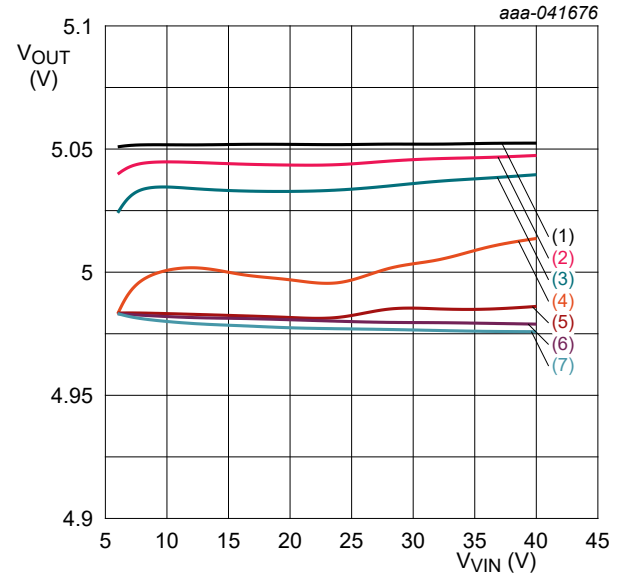
Fig. 10. Load regulation



PFM, V_{OUT} = 5 V, f_{SW} = 1.05 MHz, I_{OUT} = 0.1 A to 0.6 A

(1) V_{VIN} = 8 V
(2) V_{VIN} = 12 V
(3) V_{VIN} = 24 V
(4) V_{VIN} = 36 V
(5) V_{VIN} = 40 V

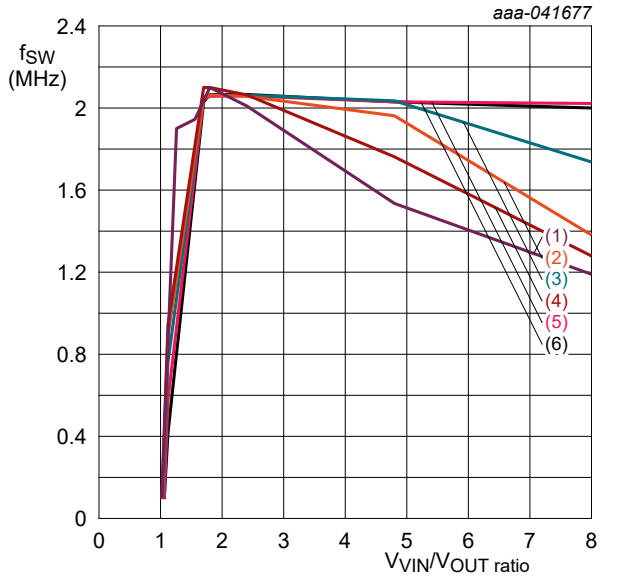
Fig. 11. Load regulation



PFM, V_{OUT} = 5 V, f_{SW} = 1.05 MHz

(1) I_{OUT} = 0 mA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 20 mA
(4) I_{OUT} = 50 mA
(5) I_{OUT} = 100 mA
(6) I_{OUT} = 300 mA
(7) I_{OUT} = 600 mA

Fig. 12. Line regulation



FPWM, V_{OUT} = 5 V, f_{SW} = 2.1 MHz

(1) I_{OUT} = no load
(2) I_{OUT} = 60 mA
(3) I_{OUT} = 150 mA
(4) I_{OUT} = 30 mA
(5) I_{OUT} = 300 mA
(6) I_{OUT} = 600 mA

Fig. 13. Switching frequency foldback

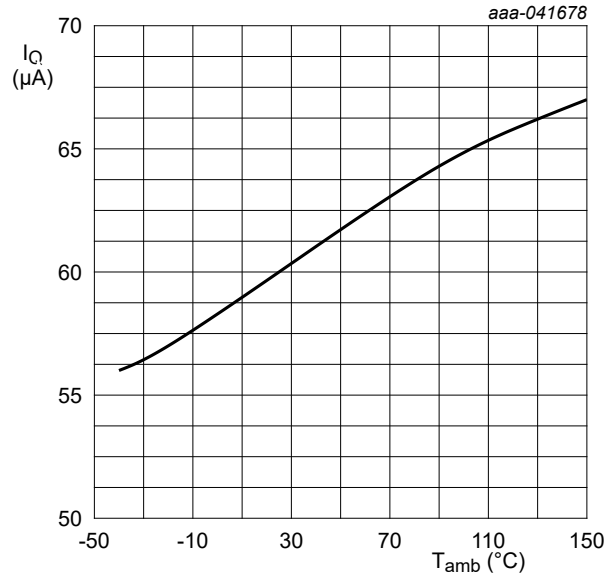
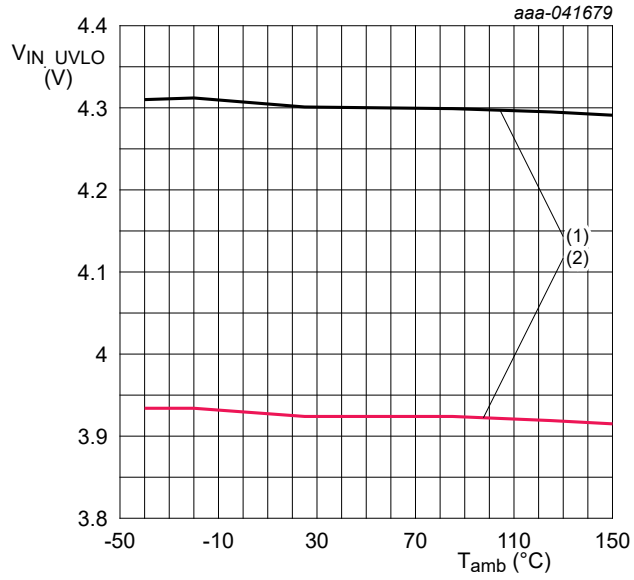


Fig. 14. Quiescent current versus ambient temperature



(1) V_{IN_UVLO+} (rising V_{VIN})
(2) V_{IN_UVLO-} (falling V_{VIN})

Fig. 15. V_{IN_UVLO} versus ambient temperature

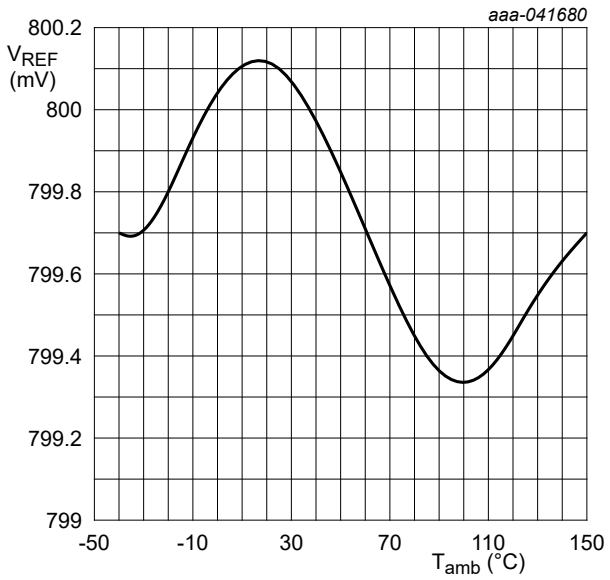
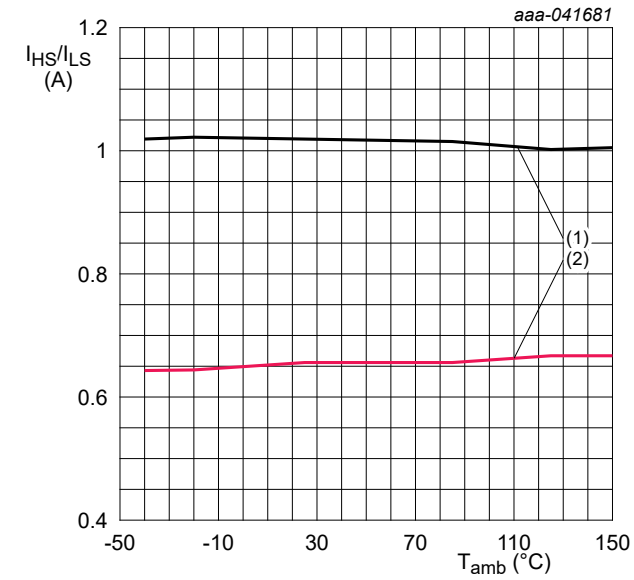


Fig. 16. Reference voltage versus ambient temperature



(1) I_{HS_LIMIT}
(2) I_{LS_LIMIT}

Fig. 17. HS and LS limits versus ambient temperature

13. Functional description

13.1. Overview

The NEX40400 is a fixed-frequency, synchronous step-down converter with low quiescent current consumption. It operates from 4.5 V to 40 V supply voltage, and capable of delivering up to 600 mA DC load current in a small solution size. There are six variants available that are suitable to various applications; refer to Section 7 for detailed information.

The NEX40400 employs fixed-frequency peak-current mode control. The device enters PFM (Pulse Frequency Modulation) mode at light load to achieve high efficiency with PFM version. The FPWM (Forced Pulse Width Modulation) version is provided to achieve low output voltage ripple. The device is internally compensated, which reduces design time, and requires few external components. Frequency foldback helps prevent inductor current runaway during start-up and output short circuit fault condition. It also helps achieving high conversion ratio and low drop-out. Frequency spread spectrum function is implemented to improve EMI performance of converters.

Additional features such as precision enable and internal soft start provide a flexible and easy to use solution for a wide range of applications. Protection features include thermal shutdown, V_{VIN} under-voltage lockout, output over-voltage protection, cycle-by-cycle current limit, and hiccup mode for short-circuit protection.

13.2. Functional Block Diagram

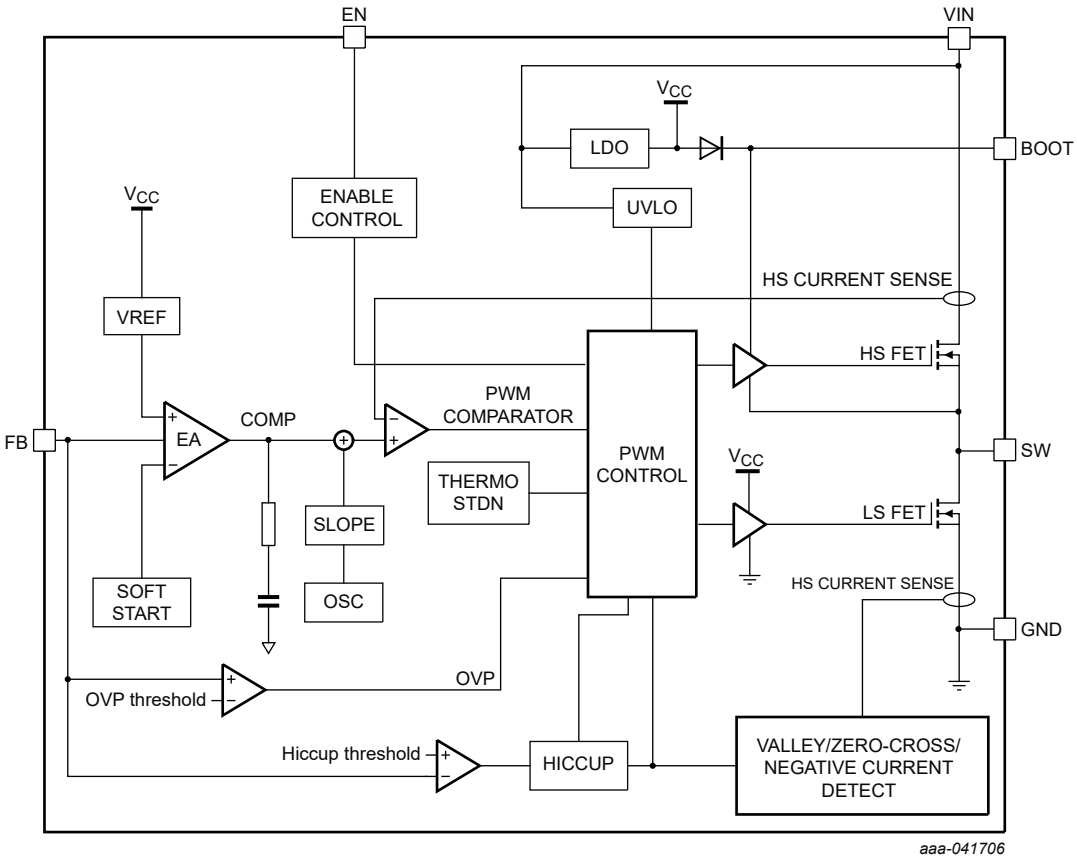


Fig. 18. Functional block diagram

13.3. Features

13.3.1. Pulse-Width Modulation (PWM) Operation

At mid-to-high output currents, the NEX40400 operates in a fixed-frequency, peak-current control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage – the output of the Error Amplifier (AE). After the HS-FET is off, the low-side MOSFET (LS-FET) turns on, and the inductor current flows through the LS-FET. To avoid a shoot-through, a dead time prevents the HS-FET and LS-FET from turning on at the same time. LS-FET turns off at the end of the switching cycle, and then a new PWM cycle begins with the next clock. Under light load conditions, depending on the variant, the NEX40400 operates in different mode.

13.3.2. Pulse Frequency Modulation (PFM) Operation

For Pulse Frequency Modulation (PFM) version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the NEX40400 operates in Discontinuous Conduction Mode (DCM). In DCM operation, the LS switch is turned off when the inductor current drops to I_{LS_ZC} threshold (30 mA typical) to reduce conduction loss and improve efficiency.

At lower load, PFM mode is activated to maintain high efficiency operation the minimum peak inductor current I_{PEAK_MIN} (150 mA typical) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching.

13.3.3. Forced PWM Operation

For FPWM variant, the NEX40400 operates in Continuous Conduction Mode (CCM) in the whole load range. This operation is maintained even at no-load condition, by allowing the negative inductor current as low as minus 0.5 A to slightly discharge the output and keep it in regulation. In FPWM mode, the light load efficiency will be lower than in PFM mode.

13.3.4. Adjustable output voltage

The output voltage is set by a resistor divider from the output voltage to the FB pin. 1% tolerance resistors are recommended. Select the bottom-side resistor R_{FBB} for the desired divider current and use below equation to calculate top-side resistor R_{FBT}. R_{FBB} in the range from 10 kΩ to 100 kΩ is recommended for most applications.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB}$$

13.3.5. V_{IN_UVLO} and enable control (EN)

The NEX40400 implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The converter shuts down when the VIN pin voltage falls below the internal threshold V_{IN_UVLO}. The internal VIN UVLO threshold has a hysteresis of 400 mV.

The NEX40400 has a dedicated enable control pin (EN) to control ON or OFF operation of device. A voltage less than 1 V disables the converter, while a voltage higher than 1.30 V enables the regulator. The EN pin may not be left open or floating; if not used, to be connected to VIN.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown on Fig. 19 to program the required V_{IN_UVLO} threshold.

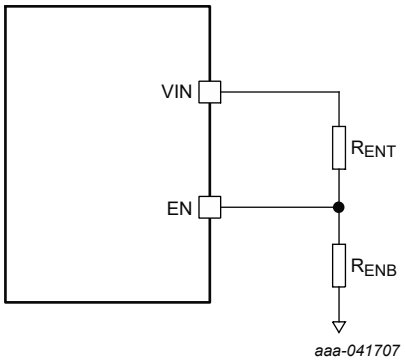


Fig. 19. External UVLO by enable divider

13.3.6. Frequency foldback

The NEX40400 has a minimum on-time and off-time limitation for HS-FET, which is t_{ON_MIN} and t_{OFF_MIN} respectively. Given a fixed switching frequency and target output voltage, t_{ON_MIN} and t_{OFF_MIN} determine the allowed maximum and minimum input voltage to keep the output voltage in regulation. This relationship is described in equations below.

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}}$$

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}}$$

To extend the input voltage range for the regulated output voltage, a frequency foldback scheme is implemented in NEX40400.

The on-time decreases while VIN voltage increases. Once the on-time decreases to t_{ON_MIN}, the switching frequency starts to decrease while VIN continues to go up, thus the actual duty cycle is lower, and higher input voltage is allowed for a regulated output voltage. This feature is important to prevent inductor current and output voltage runaway during start-up or output short circuit fault condition.

On the other hand, as VIN voltage decreases, duty cycle increases, and the off-time decreases. Once the off-time decreases to t_{OFF_MIN} and VIN continue to decrease, the inductor flux balance can't be maintained in a normal cycle. The current in the HS-FET can't reach the COMP-set current value within one nominal PWM cycle, the HS-FET remains on until its current hit the COMP-set current value, then HS-FET will turn off for t_{OFF_MIN} (100 ns typical) before next turn-on. In this condition, the switching frequency is lower than nominal frequency, and the maximum duty cycle is extended, the output voltage can be kept in regulation with a lower input voltage. To effectively refresh the bootstrap capacitor, the maximum on-time of HS-FET is limited at 10 µs, corresponding to a minimum 100 kHz switching frequency.

13.3.7. Over current and Hiccup protections

The NEX40400 has cycle-by-cycle current limit on both the peak and valley of the inductor current. High-side MOSFET over-current protection is implemented by the Peak Current Mode control. The HS switch current is sensed when the HS-FET is turned on after a set blanking time. The HS-FET will be turned off once its current intersects the current command from COMP minus slope compensation every switching cycle. In an over current or short circuit fault condition, COMP voltage is pushed to and clamped at V_{COMP_MAX}, correspondingly the peak current of HS-FET is limited by the maximum peak current threshold I_{HS_LIMIT}.

Sometimes the inductor current may run away due to the t_{ON_MIN} limitation of HS-FET. For example, during start-up period, or during output short-to-ground fault condition, the output voltage is too low, may not have enough time to reset the inductor flux properly, inductor current may be higher and higher by cycles, which is called current run away. To address this problem, the current going through LS-FET is also sensed and monitored in the NEX40400. When the LS-FET turns on, the inductor current begins to ramp down. The LS switch will not be turned off at the end of a switching cycle if its current is above the LS current limit set by COMP voltage. The LS switch is kept on so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit. Then the LS switch will be turned off and the HS switch will be turned on to start a new cycle. In this way, the valley of inductor current is controlled by COMP voltage. In short circuit fault condition, as COMP voltage is clamped at V_{COMP_MAX}, the corresponding LS current limit is clamped at its maximum value I_{LS_LIMIT}.

If the feedback voltage is lower than 40% of the VREF and the current of the LS switch triggers I_{LS_LIMIT} for 256 consecutive cycles, hiccup current protection mode is activated. In hiccup mode, the regulator shuts down and keeps off for a period of hiccup, t_{HICCUP} (120 ms typical for PFM variants; 15 ms for FPWM), before the NEX40400 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe over-current conditions, prevents over-heating and potential damage to the device.

For FPWM variants, the inductor current is allowed to go negative. If the negative inductor reaches minus 0.5 A the LS switch is turned off immediately. This protects the LS switch from excessive negative current.

13.3.8. Internal soft start

A reference-type soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0 V during the soft start time. When V_{SS} is lower than V_{REF}, V_{SS} overrides V_{REF} as the error amplifier reference. The typical soft start time (t_{SS}) is 1.8 ms.

There is over-current protection blanking time t_{OCP_BLK} (20 ms typical) at the beginning of power-up to prevent start-up failure for some application with high output voltage and large output capacitance. In those application, due to current limit, the time to charge up output cap will be much longer than 1.8 ms.

13.3.9. Safe start-up into pre-biased output

The NEX40400 has been designed to prevent the LS FET from discharging a pre-biased output. During monotonic pre-biased start-up, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage, except of the need to re-fresh the boot capacitor.

13.3.10. Spread spectrum

The NEX40400 implements frequency spread spectrum to improve EMI performance in FPWM version. The jittering span is ±5 % of the switching frequency with pseudo-random swing frequency.

13.3.11. Bootstrap voltage

The NEX40400 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the bootstrap capacitor is 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 16 V or higher is recommended for stable performance over temperature and voltage.

13.3.12. Output Overvoltage Protection (OVP)

The NEX40400 incorporates an overvoltage transient protection (OVP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 109% × V_{REF}, the high-side MOSFET will be forced off. When the FB pin voltage falls below 104% × V_{REF}, the high-side MOSFET will be enabled again.

13.3.13. Thermal shutdown

The junction temperature (T_j) of the device is monitored by an internal temperature sensor. Once the T_j exceeds the thermal shutdown threshold T_{SHDN} of 170 °C, the device enters thermal shutdown. Both the high side and low side power FETs are turned off. When T_J falls below 155 °C, the device re-initiates the power up sequence controlled by the internal soft-start circuitry.

14. Application information

The following session discusses the external components to complete the power supply design for several input and output voltage options by using the typical applications as a reference.

14.1. Typical application

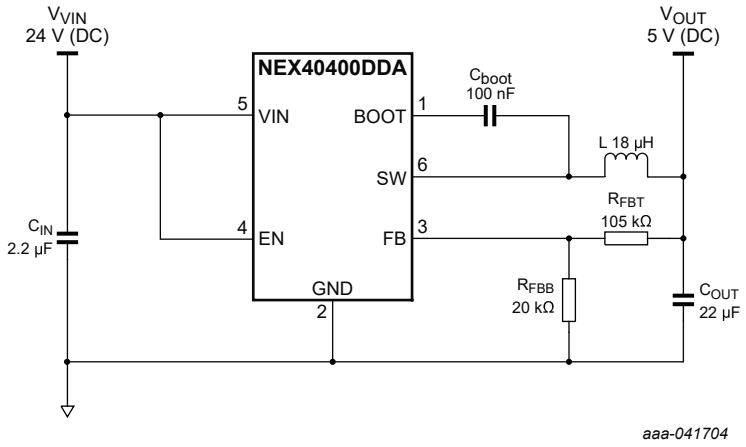


Fig. 20. NEX40400 typical application circuit

14.2. Design requirements

Table 10. Typical recommended values of inductor, output capacitor, and the feedback resistive divider

f_{SW} (MHz)	V_{OUT} (V)	L (µH)	C_{OUT}(µF) / (V)	R_{FBB} (kΩ)	R_{FBT} (kΩ)
1.05	3.3	12	22 µF / 10 V	20	61.9
	5.0	18	22 µF / 10 V	20	105
	12	33	10 µF / 25 V	20	280
2.1	3.3	6.2	10 µF / 10 V	20	61.9
	5.0	10	10 µF / 10 V	20	105
	12	18	10 µF / 25 V	20	280

14.3. Inductor selection

The inductor value affects the peak-to-peak ripple current, the PWM to PFM transition point, the output voltage ripple and the efficiency. To optimize the efficiency and solution size, allow the peak-to-peak ripple current in the inductor to be around 30% of the maximum load current is suggested. The inductance value can be calculated with below equation:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{VIN}}\right)$$

Where V_{OUT} is the output voltage, V_{VIN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Once the inductance is chosen, the peak-to-peak inductor ripple current can be calculated. The maximum peak inductor current can be calculated with below equation:

$$I_{LP} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Where I_{LOAD} is the maximum load current.

Choose an inductor that will not saturate under the maximum inductor peak current calculated above.

A more conservative way is to select the inductor saturation current according to the high side MOSFET switch current limit, because during a heavy load transient the inductor current may rise above the calculated maximum peak inductor current value.

14.4. Input capacitor selection

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (e.g.: 0.1 µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by the capacitance can be estimated with equation:

$$\Delta V_{VIN} = \frac{I_{LOAD} \times V_{OUT}}{f_{SW} \times C_{IN} \times V_{VIN}} \times \left(1 - \frac{V_{OUT}}{V_{VIN}}\right)$$

Where I_{LOAD} is the maximum load current, and C_{IN} is the input capacitance.

14.5. Output capacitor selection

Output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{VIN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor, and C_{OUT} is output capacitance.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{VIN}}\right)$$

14.6. Typical operation

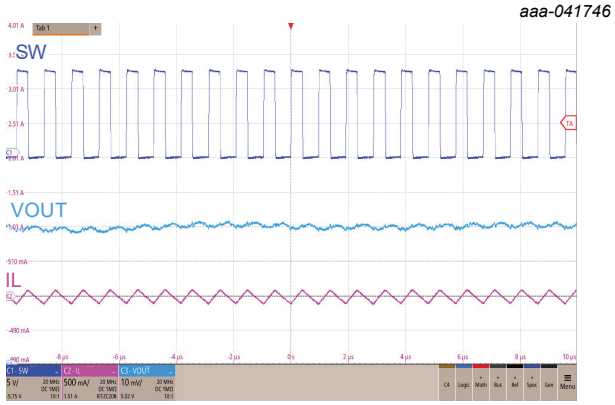


Fig. 21. V_{OUT} ripple (no load)

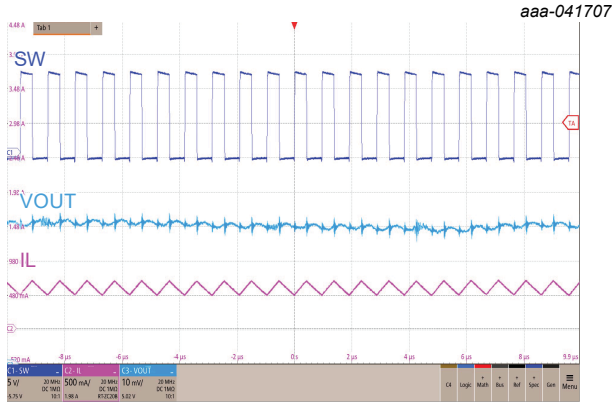


Fig. 22. V_{OUT} ripple (full load)

aaa-041748

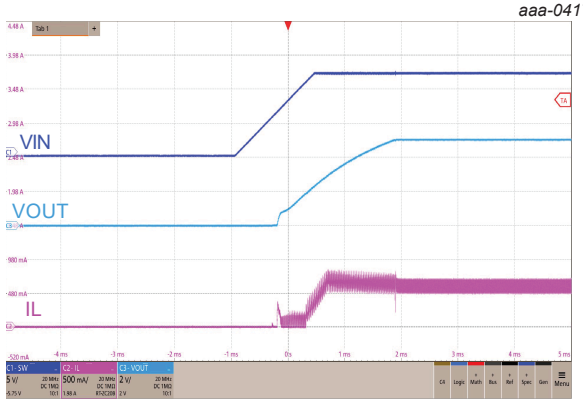


Fig. 23. Start-up by V_{VIN}

aaa-041749

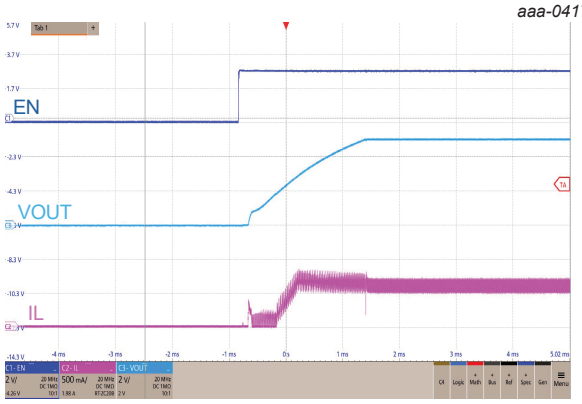


Fig. 24. Start-up by EN

aaa-041750

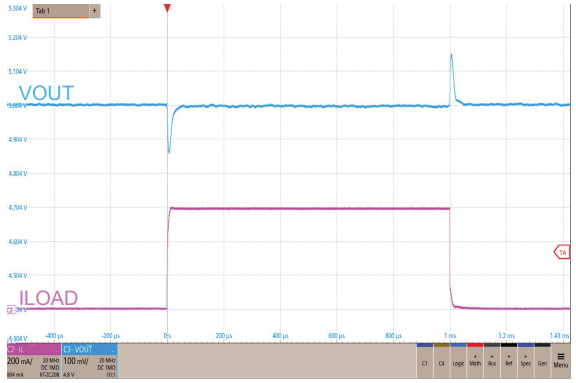


Fig. 25. Load transient response

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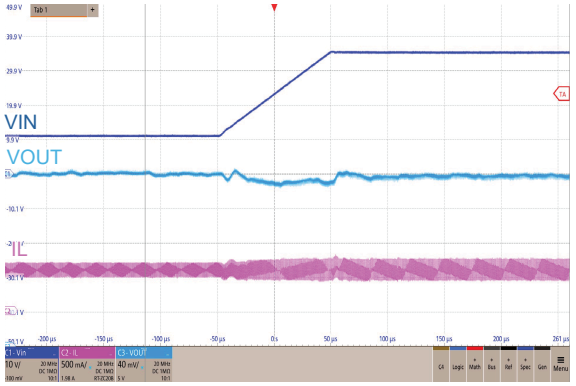

Fig. 26. Line transient response

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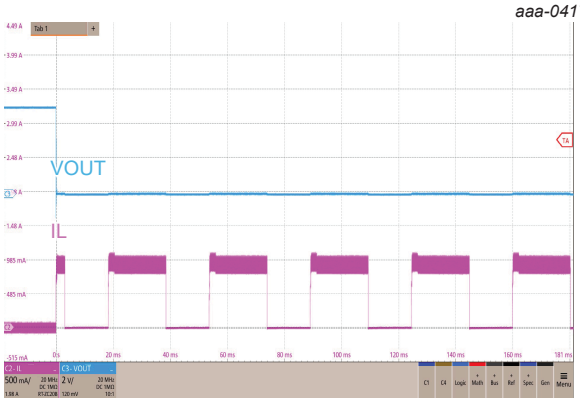

Fig. 27. Short protection

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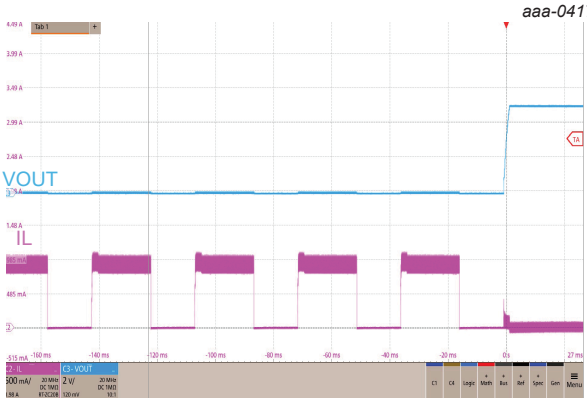


Fig. 28. Short recovery

14.7. PCB layout

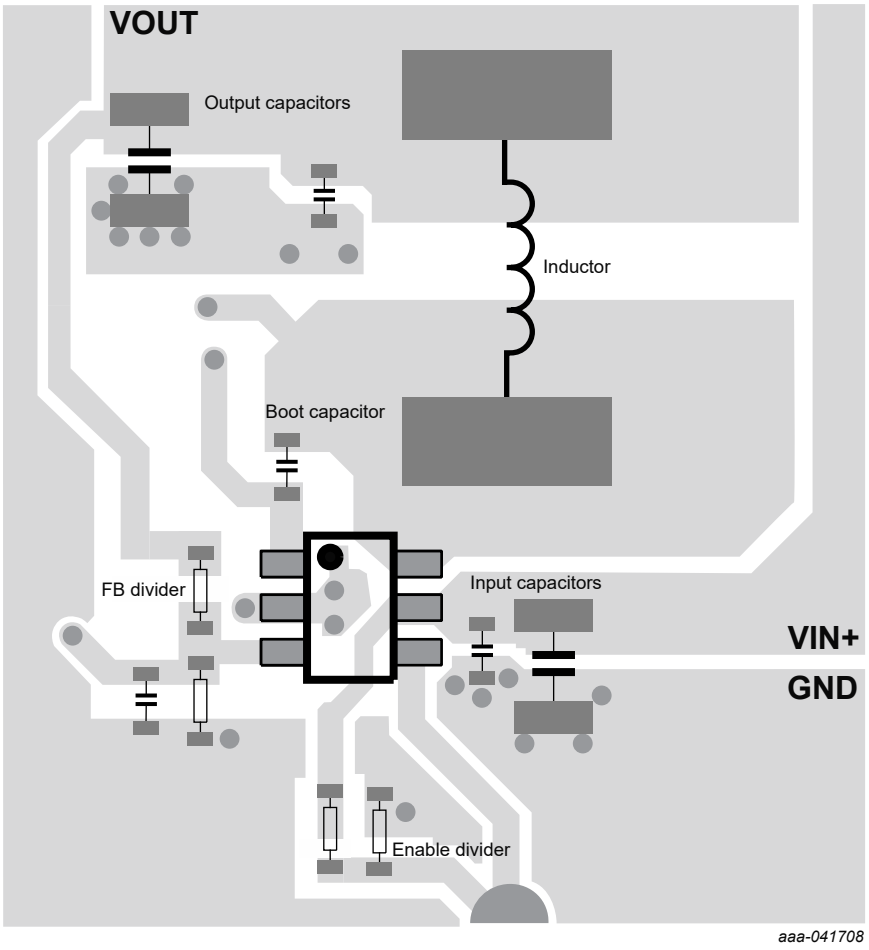
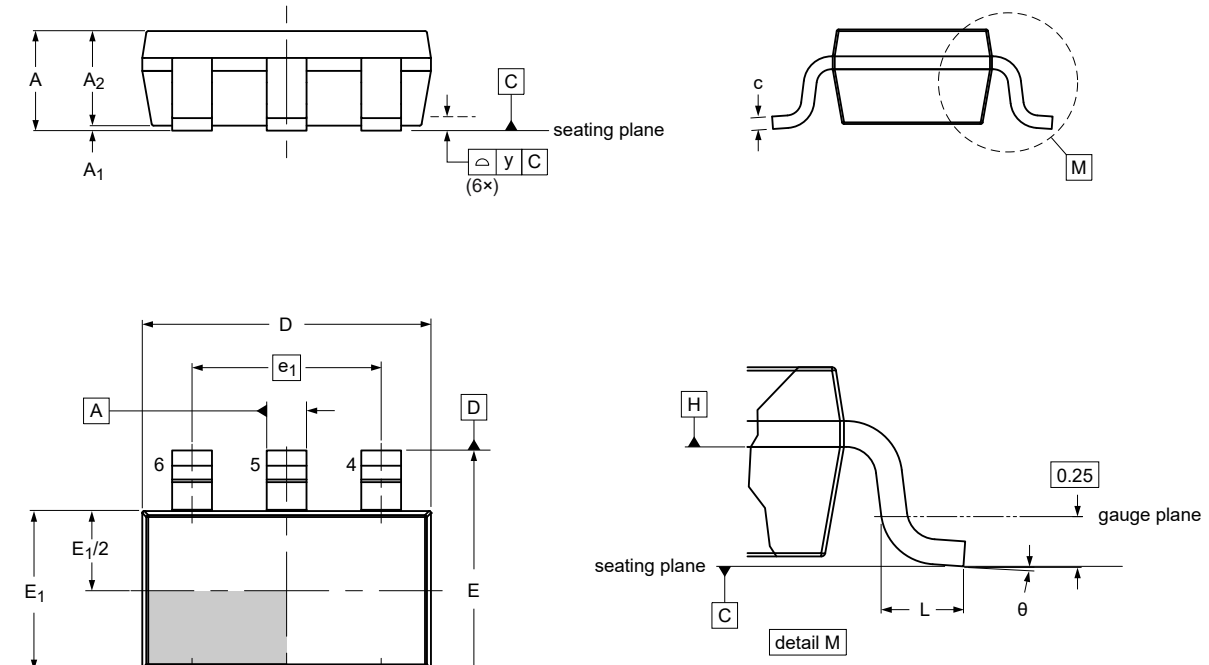


Fig. 29. Example of NEX40400 PCB Layout

15. Package information

Plastic, surface-mounted package (TSOT23-6); 6 leads **SOT8061-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	e_1	L	y	w	θ
mm	max	1.10	0.10	1.00	0.50	0.20	3.05	3.00	1.75	0.95 BSC	1.90 BSC	0.60	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min		0.00	0.70	0.30	0.08	2.75	2.60	1.45			0.30			0°

Note
Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per end.
Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0. 25 mm per side.
D and E_1 dimensions are determined at datum H.

sot8061-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8061-1		MO-193				~~24-09-04~~ 24-09-16

Fig. 30. Package outline SOT8061-1 (TSOT23-6)

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX40400 v.1	20241206	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 6 December 2024

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