ACPL-333J/332J/331J/330J

Managing Very Narrow Input Pulse Width Signals to Highly Integrated Gate Drive Optocouplers with a Simple RC Circuit

Application Note 5430

Introduction

The ACPL-333J/332J/331J/330J are advanced 1.5 A to 2.5 A output current, easy to use, intelligent gate drivers which make IGBT VCE fault protection compact, affordable, and easy to implement. Features such as integrated VCE detection, under voltage lockout (UVLO), "soft" IGBT turn-off, isolated open-collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

The ACPL-333J/332J/331J/330J are also designed with V_{out} sensing when V_{out} goes from high to low. This is to prevent the top and bottom output stage drivers from turning on at the same time and causing a short circuit. This has become critical as the speed of motor control and inverter applications has increased. During a output high state, the sense circuit will require the Vcg output to reach 3.5 V for 20 ns before allowing any input logic to turn on the bottom driver. With a very narrow input pulse width, there may not be sufficient time for the output voltage to be charged up to the desired level and duration. This can be made worse if the output loading is large as the non-overlapping effect will get longer in such operating conditions.

The Non-overlapping Effect

The non-overlapping effect is a normal phenomenon in which both the top and bottom of the output stage drivers are turned off at same time during switching. This causes the voltage at the output to hold for a few tens of nanoseconds, as shown in Figure 1, but will not pose a problem during applications.

Figure 2 shows an undesirable long non-overlapping effect as a result of a large output load (Rg and Cg) and a very narrow input pulse width. The output voltage, V_{cg}, does not have sufficient time to be charged to 3.5 V for 20 ns. The bottom driver cannot sense effectively and hence when V_{out} goes low, the bottom driver cannot be turned on as desired. When the voltage drops below 2 V, the bottom driver will turn on and it returns back to normal operation. This holding voltage ranges from 2 V to 3.5 V.

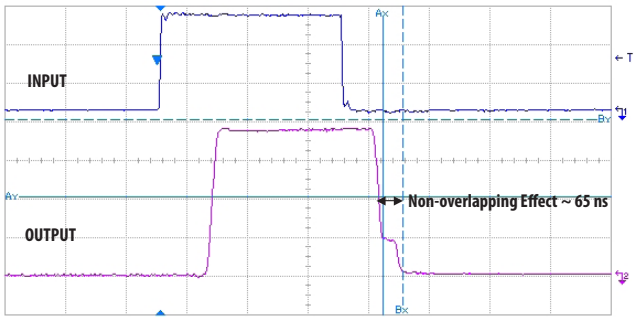

Figure 1. Normal non-overlapping effect

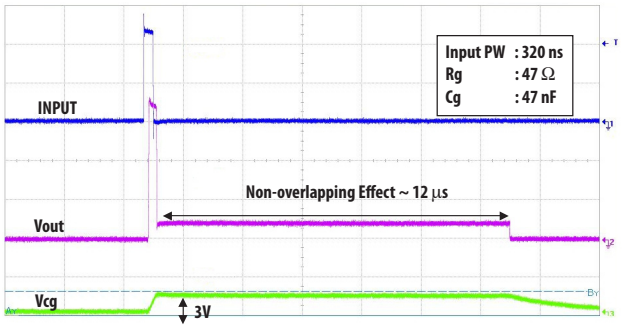

Figure 2. Long non-overlapping effect due to narrow input pulse width and large output load

Recommended Solution

The long non-overlapping effect can be solved by connecting R_f and C_f in parallel with R_g and C_g which simulate the load of the IGBT or Power MOSFET as shown in Figure 3.

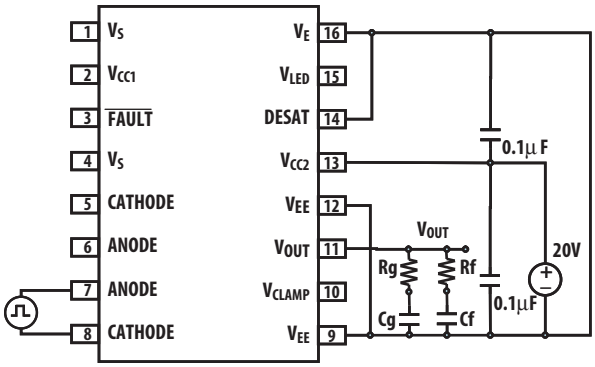

Figure 3. Additional Rf and Cf to solve the non-overlapping problem

The value of R_f and C_f must meet the following conditions:

Condition 1:

$$V_{out(init)} = V_{cg} \cdot \frac{R_f}{R_f + R_g} + V_{cf} \cdot \frac{R_g}{R_f + R_g} > 3.5\ V$$

Condition 2:

$$T_{(duration)} = -\ln \left| \frac{V_{cf(final)} - V_{cg}}{(V_{cf} - V_{cg})} \right| \cdot C_f \cdot (R_f + R_g) > 20\ ns$$

V_{cg} is the voltage across C_g at the instant V_{out} goes from high to low. V_{cf} is the voltage across C_f at the instant V_{out} goes from high to low. $V_{cf(final)}$ is the voltage across C_f at the time the output voltage drops to 3.5 V.

With the correct values of R_f and C_f that meet the above conditions, the undesired long non-overlapping effect will not be observed for different values of R_g and C_g.

Determining the Input Pulse Width that Causes the Non-overlapping Effect

Using the charging voltage across Cg,

$$V_{cg} = V_{out} \cdot \left(1 - e^{\frac{-t_{pw}}{R_g \cdot C_g}} \right)$$

the V_{out} pulse width range $t_{pw(min)}$ to $t_{pw(max)}$ that will cause V_{out} to reach 2 V to 3.5 V can be calculated. This will approximate the input pulse width range that will cause the long non-overlapping effect.

Table 1 shows the V_{out} pulse width range for V_{out}=18 V, V_{CC}=20 V for different loading conditions.

Table 1. Input pulse width that will cause the non-overlapping effect

		V_{out} Pulse Width	
R_g, Ω	C_g, nF	$t_{pw(min)}$, ns	$t_{pw(max)}$, ns
47	47	260	447
25	47	138	254
15	47	83	152
47	25	138	254
25	25	73	135
10	10	12	22

Hence, for Figure 2 conditions, the non-overlapping effect will be long since the input pulse width of 320 ns falls inside the range of $t_{pw(min)}$=260 ns and $t_{pw(max)}$=447 ns.

Choosing R_f and C_f

The value of C_f has to be at least 10 times smaller than C_g so that the charged voltage across V_{cf} does charge up C_g when V_{out} goes from high to low. The gate voltage of IGBT, V_{cg}, needs to be independent of V_{cf}.

The value of R_f has to be small enough to allow V_{cf} to charge up to a certain value. This value has to be high enough to bring V_{out} higher than 3.5 V for at least 20 ns when the top driver is turning off. This is because an internal comparator needs at least 3.5 V for 20 ns to be able to sense the high to low transition of V_{out}. If these conditions are met, then the long non-overlapping problem will not be observed.

Charging of C_g and C_f during the gate driver on time

Let t_{pw} be the pulse width time of V_{out} during the high state. The charging voltage of C_g, V_{cg} during t_{pw} is:

$$V_{cg} = V_{out} \cdot \left(1 - e^{\frac{-t_{pw}}{R_g \cdot C_g}}\right) \quad (1)$$

The charging voltage of C_f, V_{cf} during t_{pw} is:

$$V_{cf} = V_{out} \cdot \left(1 - e^{\frac{-t_{pw}}{R_f \cdot C_f}}\right) \quad (2)$$

The V_{out} pin is in a high impedance state at the instant the output switches from high to low, because the top driver is turned off and the bottom driver has not turned on yet. The voltage V_{out} at that instant can be calculated based on voltage superposition:

$$V_{out(init)} = V_{cg} \cdot \frac{R_f}{R_f + R_g} + V_{cf} \cdot \frac{R_g}{R_f + R_g} \quad (3)$$

This equation has to be higher than 3.5 V.

Discharging time when top driver turn off

As $C_g >> C_f$, it is assumed that voltage across C_g, V_{cg}, is constant during the first few tens of microseconds. The discharge voltage of C_f, $V_{cf(discharge)}$, will start from V_{cf} to V_{cg}. The equation is:

$$V_{cf(discharge)} = (V_{cf} - V_{cg}) \cdot e^{\frac{-t}{C_f \cdot (R_f + R_g)}} + V_{cg} \quad (4)$$

Based on superposition, the voltage of $V_{cf(discharge)}$ when V_{out} drops to 3.5 V is:

$$V_{cf(final)} = 3.5 \cdot \frac{R_f + R_g}{R_g} + V_{cg} \cdot \frac{R_f}{R_g} \quad (5)$$

Hence the time taken for $V_{cf(discharge)}$ to drop from V_{cf} to $V_{cf(final)}$ is also the time when V_{out} drops to 3.5 V. Substituting $V_{cf(final)}$ into equation (4) gives:

$$T_{(duration)} = -\ln\left|\frac{V_{cf(final)} - V_{cg}}{(V_{cf} - V_{cg})}\right| \cdot C_f \cdot (R_f + R_g) \quad (6)$$

This equation has to be longer than 20 ns.

Hence, to avoid the non-overlapping problem, the values selected for R_f and C_f must meet the following conditions based on equation (3) and (6):

Condition 1:

$$V_{out(init)} = V_{cg} \cdot \frac{R_f}{R_f + R_g} + V_{cf} \cdot \frac{R_g}{R_f + R_g} > 3.5\ V$$

Condition 2:

$$T_{(duration)} = -\ln\left|\frac{V_{cf(final)} - V_{cg}}{(V_{cf} - V_{cg})}\right| \cdot C_f \cdot (R_f + R_g) > 20\ ns$$

Example for verifying the choice of R_f and C_f

Table 2 shows an example of how to verify the non-overlapping effect based on an R_f=34 Ω and C_f=560 pF.

Table 2. Verifying the choice of R_f and C_f

R_g, Ω	C_g, nF	V_{out} Pulse Width, ns	V_{cg}, V	$V_{out(init)}$, V	$T_{(duration)}$, ns
47	47	$t_{pw(min)}$=260	2	11.28	82
		$t_{pw(max)}$=477	3.5	11.91	345
25	47	$t_{pw(min)}$=138	2	8.77	49
		$t_{pw(max)}$=254	3.5	9.64	297
15	47	$t_{pw(min)}$=83	2	6.83	32
		$t_{pw(max)}$=152	3.5	7.93	170
47	25	$t_{pw(min)}$=138	2	11.27	82
		$t_{pw(max)}$=254	3.5	11.91	422
25	25	$t_{pw(min)}$=73	2	8.61	48
		$t_{pw(max)}$=135	3.5	9.64	249
20	20	$t_{pw(min)}$=47	2	7.36	38
		tpw(max)=86	3.5	8.79	172

The choice of R_f=34 Ω and C_f=560 pF has met the two specified conditions and hence the long non-overlapping problem will not be observed for the various loading conditions.

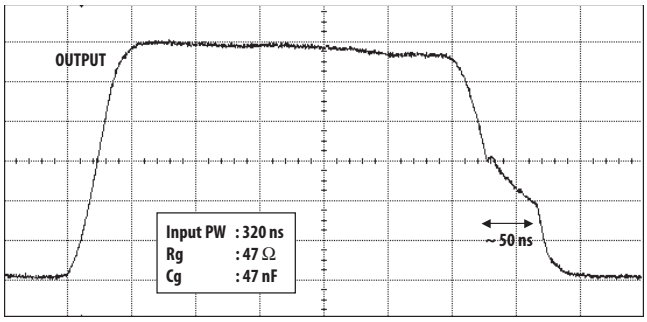

Figure 4. Undesired long non-overlapping effect is not observed with the additional R_f = 34Ω and C_f = 560 pF

Conclusion

A simple R_f and C_f solution has been presented for the ACPL-33XJ gate driver optocoupler series to be used in very narrow input pulse width applications. The mathematical analysis of the Non-overlapping effect and the derivation of the values of R_f and C_f have been discussed. The proposed solution has been successfully simulated and tested to work under different loading conditions.

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