Introduction

This application note provides an overview of the isolation barrier requirements for Power over Ethernet (PoE) systems as defined by IEEE 802.3 standards, including IEEE802.3bt. It examines how these standards drive isolation requirements in equipment design, including the relationship to relevant safety standards such as IEC 62368-1.

In addition, this document outlines key design considerations for implementing compliant PoE interfaces. Particular focus is given to the selection of suitable isolation components and the implications for printed circuit board (PCB) layout.

Specification Requirements

The current IEEE802.3 specification requires electrical isolation between the powered interface (PI) and all externally accessible circuitry. This includes the Ethernet interface, any unused MDI pairs, and any accessible non-MDI connections. The IEEE802.3 specification aligns with the safety principles of IEC 62368-1.

To comply with IEEE 802.3, the required isolation must be maintained between all PoE primary side connected circuitry and all externally accessible conductors. Components that span this boundary, such as transformers, optocouplers, and isolated power supplies, should be selected to meet the applicable insulation and dielectric withstand requirements.

The electrical isolation means that the PoE applications should shall withstand at least one of the following electrical strength tests with no signs of insulation breakdown, as defined in subclause 6.2.2.3 of IEC 60950-1:2001:

a) 1500 Vrms steady-state at 50-60 Hz for 60 seconds, applied as specified in subclause 6.2 of IEC 60950-1:2001.

b) An impulse test consisting of a 1500 V, 10/700µs waveform, applied 10 times, with a 60 second interval between pulses, applied as specified in subclause 6.2 of IEC 60950-1:2001.

Origin of Isolation Requirements

It is important to note that the requirement for an isolation barrier in PoE systems was driven primarily by the IEEE 802.3 specifications, with IEC safety standards defining the underlying insulation and safety framework.
The IEEE standards mandated isolation at the Ethernet interface to account for installations where cabling could be exposed to external environments and transient overvoltage’s, such as lightning surges.
Under IEC 60950-1, PoE circuits typically fell within the SELV classification (≤60 Vdc), and exemptions existed for interconnections between IT equipment. As a result, IEC 60950-1 did not explicitly require an isolation barrier for these circuits. Instead, the isolation implemented in PoE designs exceeded basic safety requirements and was defined by IEEE system-level considerations.
With the transition to IEC 62368-1, SELV concepts were replaced by a hazard-based approach, but PoE interfaces generally remained within ES1 limits. Consequently, while safety standards set baseline requirements, the need for isolation in PoE systems continued to be determined primarily by IEEE specifications.

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Isolated PD Modules

All Silvertel isolated PD modules comply with the 1500 V impulse test requirement outlined above. However, the PD module is only one of the components that interfaces across the isolation barrier; the Ethernet magnetics and layout must also provide the required isolation.

Figure 1 illustrates a simplified block diagram showing the location of the isolation barrier and the components that cross it. The connections on the left-hand side of the barrier interface to the Powered Interface (PI), while those on the right-hand side may connect directly or indirectly to accessible external conductors.

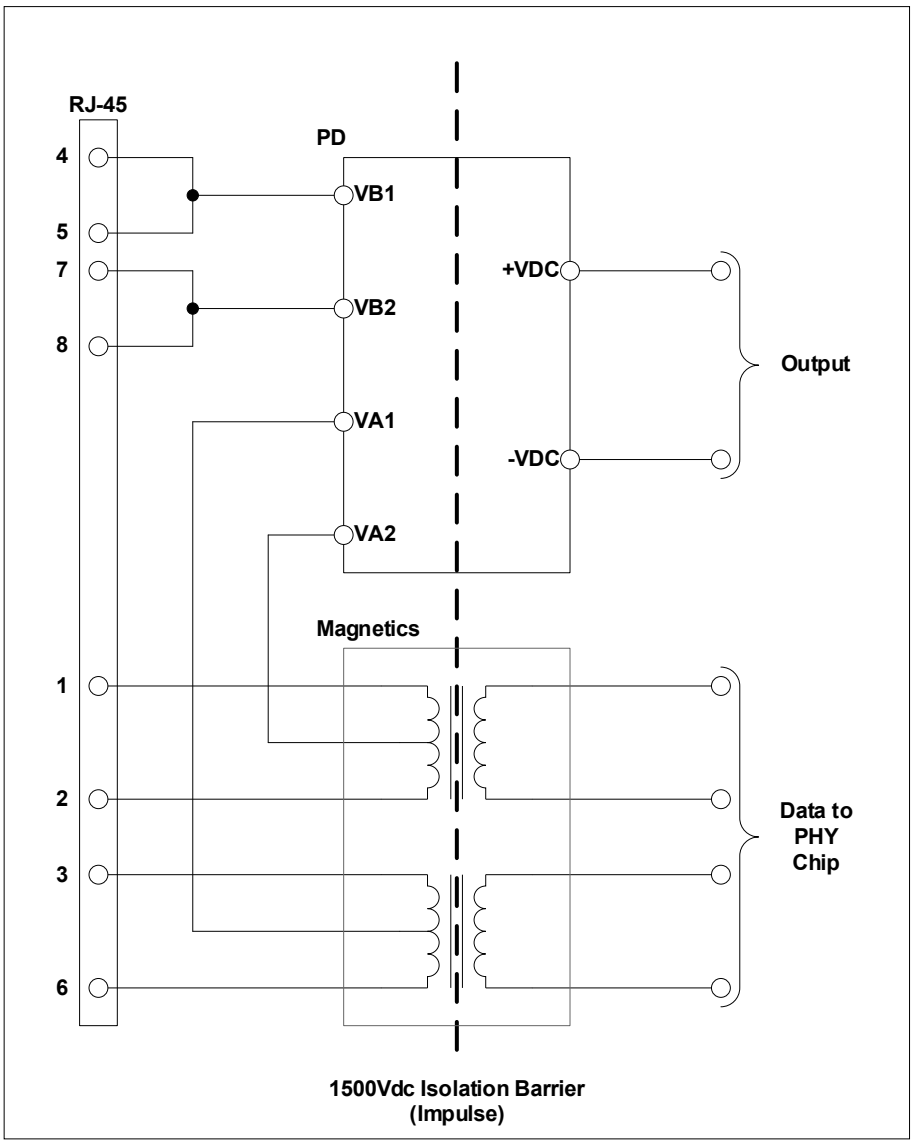


Figure 1: Isolation Barrier

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Integrated Magnetics

To optimise PCB area and simplify layout, a number of manufacturers offer RJ45 connectors with integrated magnetics. These devices combine the Ethernet connector and the required isolation transformer(s) within a single package. The integrated magnetics typically include the isolation transformers, common-mode chokes, and termination components required for Ethernet operation, effectively implementing the isolation barrier within the connector itself.

Using RJ45 connectors with integrated magnetics can reduce component count, minimise routing complexity, and optimise board space, as the magnetics and connector are combined into a single module. While discrete LAN transformers are widely available as off-the-shelf components, integrated solutions simplify layout. However, this integration typically comes at a higher cost compared to discrete implementations.

Figure 2 shows an example PCB layout using an integrated RJ45 connector in conjunction with an Ag97000-FL PD module. The tracks are colour-coded to indicate their relationship to the isolation barrier: those shown in red are on the PI (cable) side, while those in blue are on the system side, which may be connected to accessible external conductors. The hatched region represents the isolation barrier.

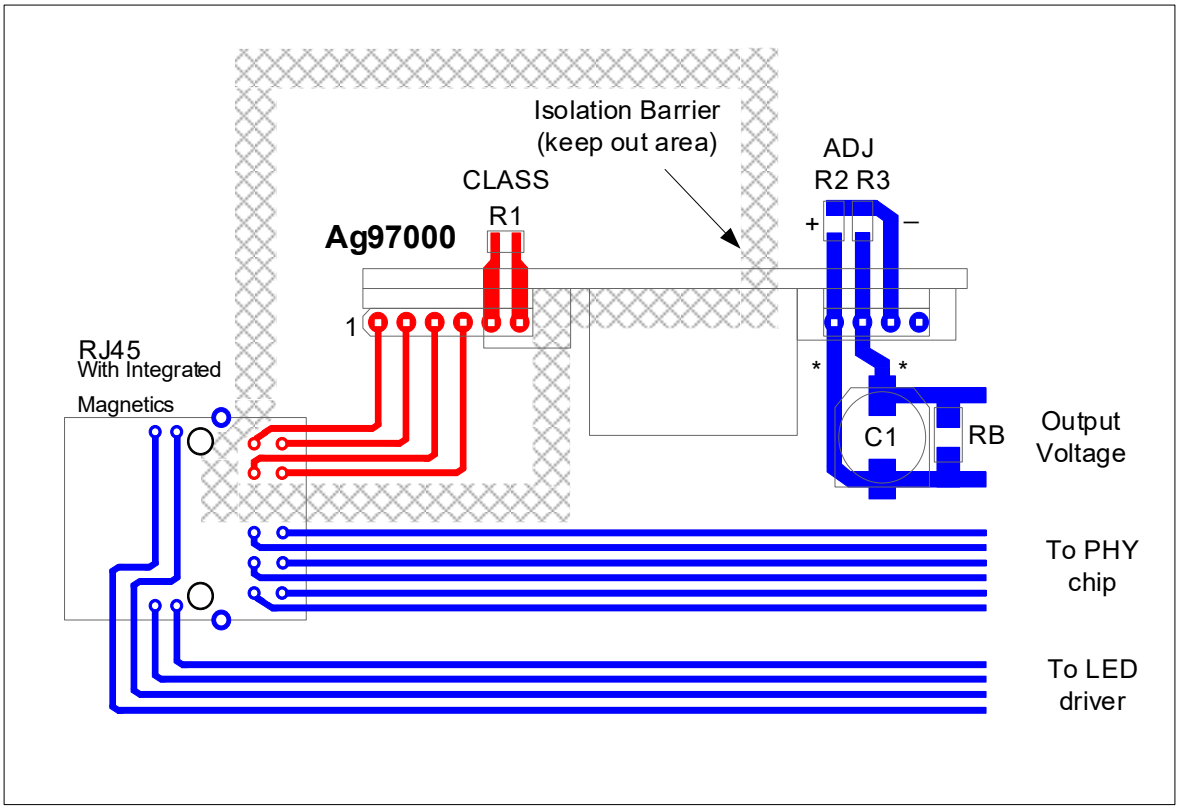


Figure 2: Example Layout

As a general guideline, the clearance between conductors on either side of the isolation barrier should be no less than 3 mm where possible to account for variability in environmental conditions. Clearances below this may increase the risk of flashover.

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Non-Isolated PD Module

The use of a non-isolated PD module can be a practical solution in applications where system-level design provides the required isolation barrier. Figure 3 illustrates an example of this approach using a self-contained product housed within a non-conductive enclosure. Silvertel offer only a select few non-isolated modules, such as the Ag210 and Ag59FE; however, the design principles described in this section are generally applicable to any non-isolated PoE PD implementation.

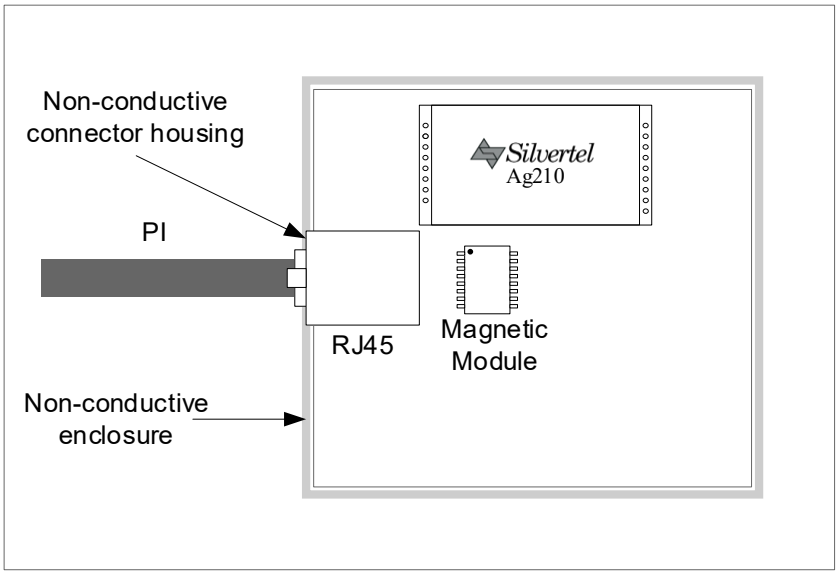


Figure 3: Non-conductive enclosure

In this implementation, the enclosure forms the primary isolation barrier between the PI and any user-accessible surfaces. The PD module and associated circuitry are fully enclosed, ensuring that no conductive parts are exposed to the user.

The Ethernet magnetics (shown as a separate magnetic module) continue to provide the required isolation between the network and the PD circuitry. This architecture is most suitable for fully self-contained equipment with no additional user accessible I/O connections. If external data or output ports are introduced, additional isolation measures may be required, as these interfaces can bypass the enclosure-based isolation barrier and compromise compliance.

In both isolated and non-isolated implementations, correct PCB layout is essential to ensure that the isolation barrier is preserved throughout the design.

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PCB Layout Considerations

Correct PCB layout is critical to ensure that the isolation barrier is maintained throughout the design. While components such as PD modules and Ethernet magnetics establish the functional isolation, the PCB layout should ensure that the isolation remains in practice. Poor layout can introduce unintended conductive paths or reduce clearance distances, compromising both safety and compliance.

Maintaining the Isolation Barrier on the PCB

The isolation barrier shown conceptually in Figure 1 must be clearly defined and maintained within the PCB layout. This barrier separates the Powered Interface (PI), connected to the Ethernet cable, from the system-side circuitry, which may be referenced to accessible external conductors.

All conductive elements associated with the PI side (including RJ45 pins, transformer primary windings, and associated routing) must be physically separated from system-side circuitry. As a general guideline, a minimum clearance of 3 mm or outer layers and 1,7mm for inner layers should be maintained between conductors on either side of the isolation barrier. This spacing helps to prevent dielectric breakdown and reduces the risk of flashover under transient overvoltage conditions.

The isolation barrier should be clearly identifiable within the PCB layout, often implemented as a keep-out region or gap between copper features.

Isolation Across PCB Layers

The isolation barrier must be maintained throughout the PCB structure, including all internal copper layers. While FR4 typically provides sufficient insulation between layers allowing for variation in the barrier's location on each PCB layer. However, any transitions between layers, such as plated through-holes and vias, should be carefully reviewed to ensure that the required creepage and clearance distances are maintained.

In some designs, the isolation boundary may be routed through different PCB layers to optimise the layout or improve thermal performance. For example, heat can be transferred across the barrier through the PCB structure while still maintaining the required electrical isolation.

Design considerations include:

- Maintaining the required clearance across all PCB layers.
- Carefully reviewing vias, plated through-holes, and component transitions where the isolation boundary changes layers.
- Partitioning ground and power planes between PI and system domains to maintain the required electrical separation.
- Reviewing the PCB stack-up and copper placement to ensure the required insulation performance is maintained.

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Routing and Vias

All signal routing must be implemented with careful consideration of the isolation barrier. Trace from the PI side should not come into close proximity to system side traces and planes, and vice versa.

Practical routing guidelines include:

- Keep signal traces between the PHY and the Ethernet connector or discrete magnetics as short as possible
- If trace lengths exceed approximately 75–100 mm (3–4 inches), increased attention should be given to impedance control and maintaining symmetry to avoid line imbalance
- Avoid routing signals parallel to the isolation boundary on opposite sides, as this can increase capacitive coupling

Special care must also be taken with routing transitions across PCB layers. Where vias or traces pass close to conductors on the opposite side of the isolation barrier, the required creepage and clearance distances must be maintained. As a guide, this may require a minimum separation of approximately 1.7 mm on internal layers and 3 mm on external layers, depending on the applicable insulation requirements.

Design considerations include:

- Ensuring vias remain within their intended isolation domain.
- Restricting stitching vias to ground and power planes within the same isolation domain.
- Verifying that routing transitions between layers maintain the required separation from conductors in the adjacent domain.

Power and ground routing should also be carefully managed to maintain the required electrical separation and minimise unintended coupling across the isolation barrier.

Components Crossing the Isolation Barrier

Some components are intentionally connected across the isolation barrier as part of the system design. These components must be specifically selected and rated for operation across the isolation boundary to ensure that the required insulation performance is maintained.

Common examples include:

- Ethernet transformers (magnetics), which provide the primary galvanic isolation between the MDI and the application circuitry.
- Optocouplers, which transfer control or feedback signals while maintaining electrical isolation.
- ‘V’ or ‘Y’ capacitors, which may be used to reduce common-mode noise and improve EMC performance. These capacitors provide a controlled AC coupling path across the isolation barrier and must be safety-rated for the intended application.
- Bob Smith termination networks, which are commonly connected to the cable side of the Ethernet interface for EMI reduction. Where these networks reference circuitry on the isolated side of the system via a capacitor, the connection must be made using an appropriately rated component.

When components cross the isolation barrier, their voltage ratings, insulation characteristics, creepage distances, and clearance distances should be reviewed as part of the overall isolation assessment. The use of standard components that do not provide the required insulation performance can compromise compliance, even if PCB spacing requirements have been met.

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EMI Considerations

Proper termination of the Ethernet interface plays an important role in both EMI performance and overall system stability. The use of Bob Smith Termination (BST), typically implemented using 75 Ω resistors and 10nF DC blocking capacitors connected to the cable-side centre taps, is recommended to improve common-mode noise performance.

In many applications, the BST network is connected to chassis or system ground through a barrier capacitor. These capacitors provide a low-impedance path for high-frequency common-mode noise while preventing the flow of DC current, helping to maintain both EMC performance and Ethernet signalling integrity.

Many RJ45 connectors with integrated magnetics incorporate the Bob Smith termination network and associated DC-blocking capacitors internally. Where these functions are not integrated, they can be implemented externally in accordance with the connector manufacturer's recommendations.

Example Using Integrated Magnetics

RJ45 connectors with integrated magnetics, such as the example shown in Figure 2, can simplify PCB layout by defining the isolation barrier within a single component. The internal transformer provides the required galvanic isolation, effectively separating the cable-side (PI) connections from the system-side interface.

However, careful PCB layout is still required to maintain this separation:

- Pins connected to the PI side must be routed only within the PI domain
- System-side pins must connect exclusively to system circuitry
- The isolation barrier should be preserved beneath the connector footprint by ensuring that no internal copper layers create unintended coupling paths
- Adequate clearance must be maintained between PI and system pins, including across all PCB layers

Figure 2 demonstrates this clearly, with colour-coded routing distinguishing the two domains and the hatched region indicating the isolation barrier.

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Example Using Non-Integrated Magnetics

RJ45 connectors without integrated magnetics require the isolation barrier to be implemented using external Ethernet magnetics placed between the connector and the Ethernet PHY. In this arrangement, the galvanic isolation is provided by the discrete transformer, with the cable-side (PI) connections separated from the system-side circuitry at the magnetics rather than within the connector itself.

However, careful PCB layout is still required to maintain this separation:

- Connector pins and traces between the RJ45 and the cable-side of the magnetics must remain entirely within the PI domain
- Traces connected to the system-side of the magnetics must route exclusively within the system domain
- The isolation barrier created by the external magnetics should be maintained across all PCB layers, ensuring that no copper planes or signal traces create unintended coupling paths between the two domains
- Adequate clearance and creepage distances must be maintained between the PI-side and system-side circuitry, particularly around the magnetics and any associated components

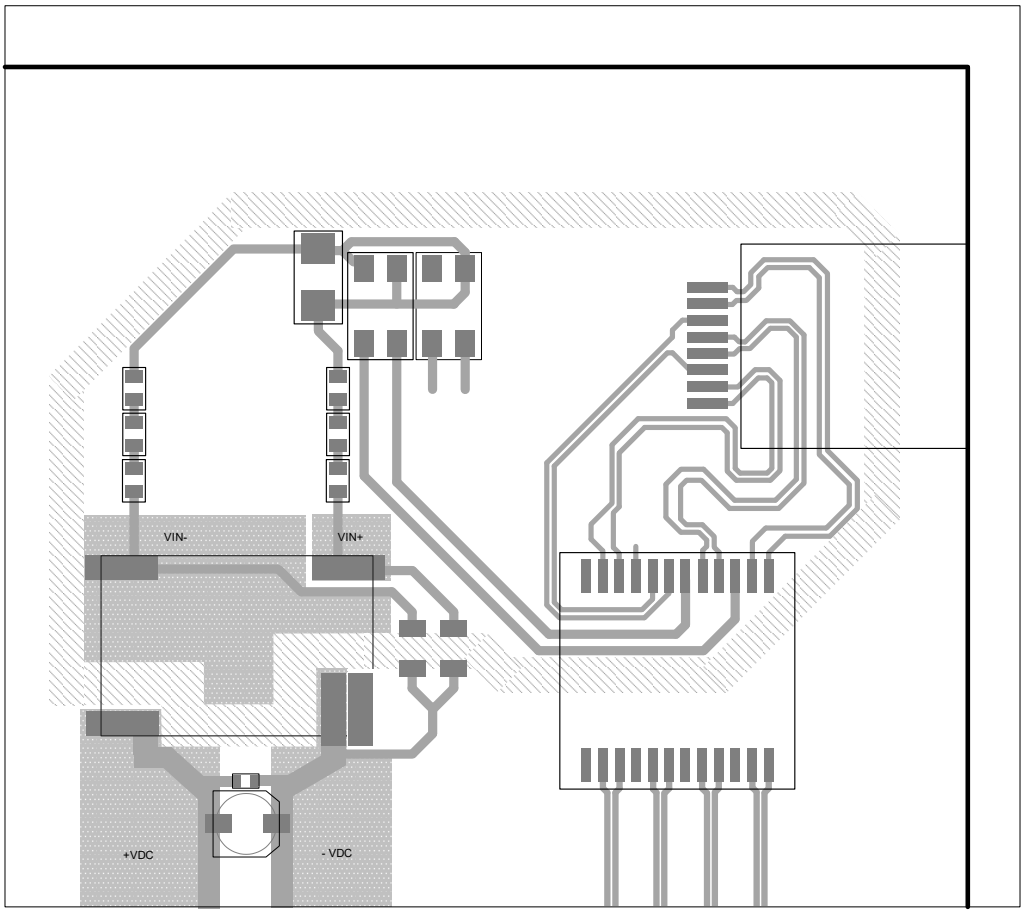


Figure 4 demonstrates this arrangement, with the RJ45 connectors located within the PI domain and the data transformer (Wurth 749052050) providing the galvanic isolation. The Bob Smith Termination (BST) capacitors remain on the PI/Cable side of the isolation barrier but do not themselves provide any isolation. The hatched area indicates the isolation barrier.

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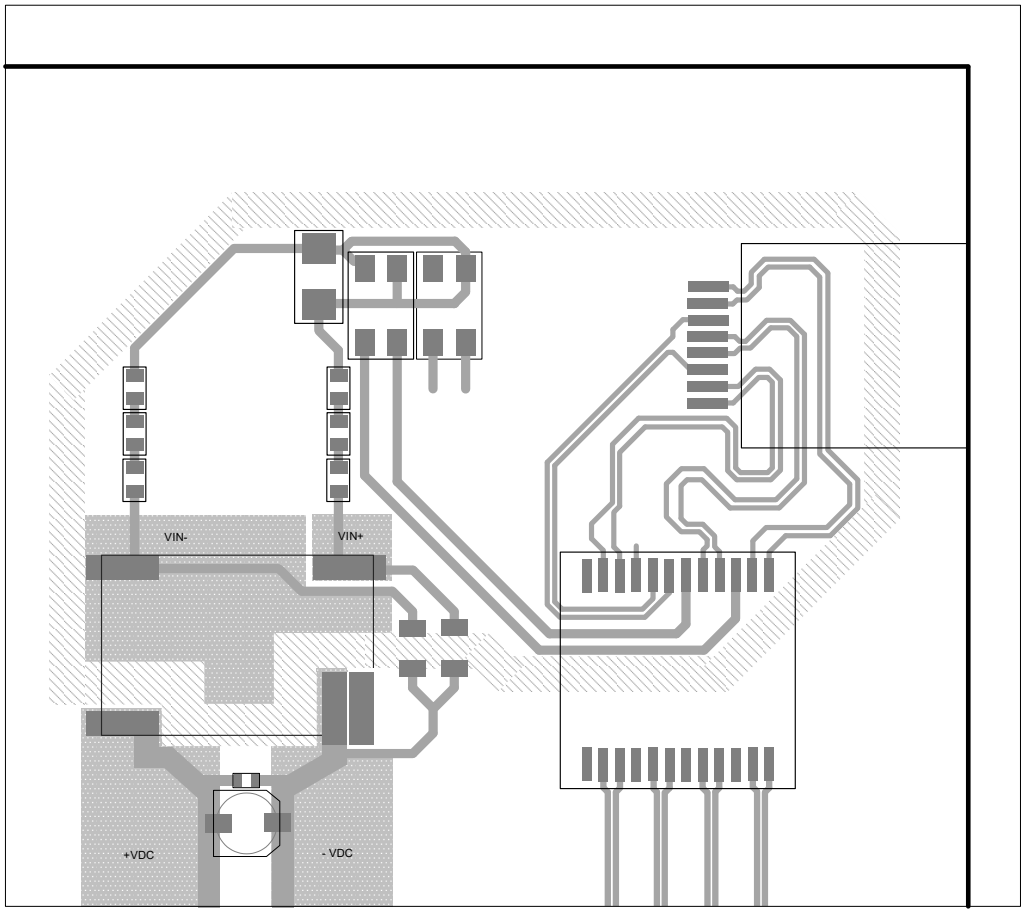


Figure 4: EvalAg9900 Non-Integrated Magnetics Layout

Conclusion

The IEEE 802.3 standards define the isolation requirements for PoE systems at the Ethernet interface. Compliance depends on both appropriate component selection and correct system implementation.

Whether using isolated or non-isolated PD modules, the isolation barrier must be clearly defined and maintained. Careful PCB layout and system design are essential to preserve this barrier and ensure reliable operation.

In summary, effective isolation in PoE designs relies on a combination of correct component choice, appropriate system architecture, and disciplined PCB layout.

We hope you have found the information detailed in this document useful. We would be happy to discuss anything included, or any other technical related questions at any time. Please contact apps.support@silvertel.com.

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