STPMIC2L application hints

Introduction

How to connect unused pins

In some STPMIC2L + STM32MP2x family MPU applications, not all the peripherals and functions may be required, and to minimize any possible issues and unnecessary power consumption, the relevant pins must be connected correctly.

The following tables provide guidance on how to connect unused pins of the STPMIC2L, and they are valid for all pins except VIN, VIO, and all GNDs.

Note 1: To avoid any damage to the STPMIC2L, VIN must be the first and highest input supply.

Note 2: The DC-DC converter input pins (pins #15, #04, and #14) cannot be separated from the main input pin (pin #30).

Figure 1. Pin configuration, VFQFPN 40L (top view)

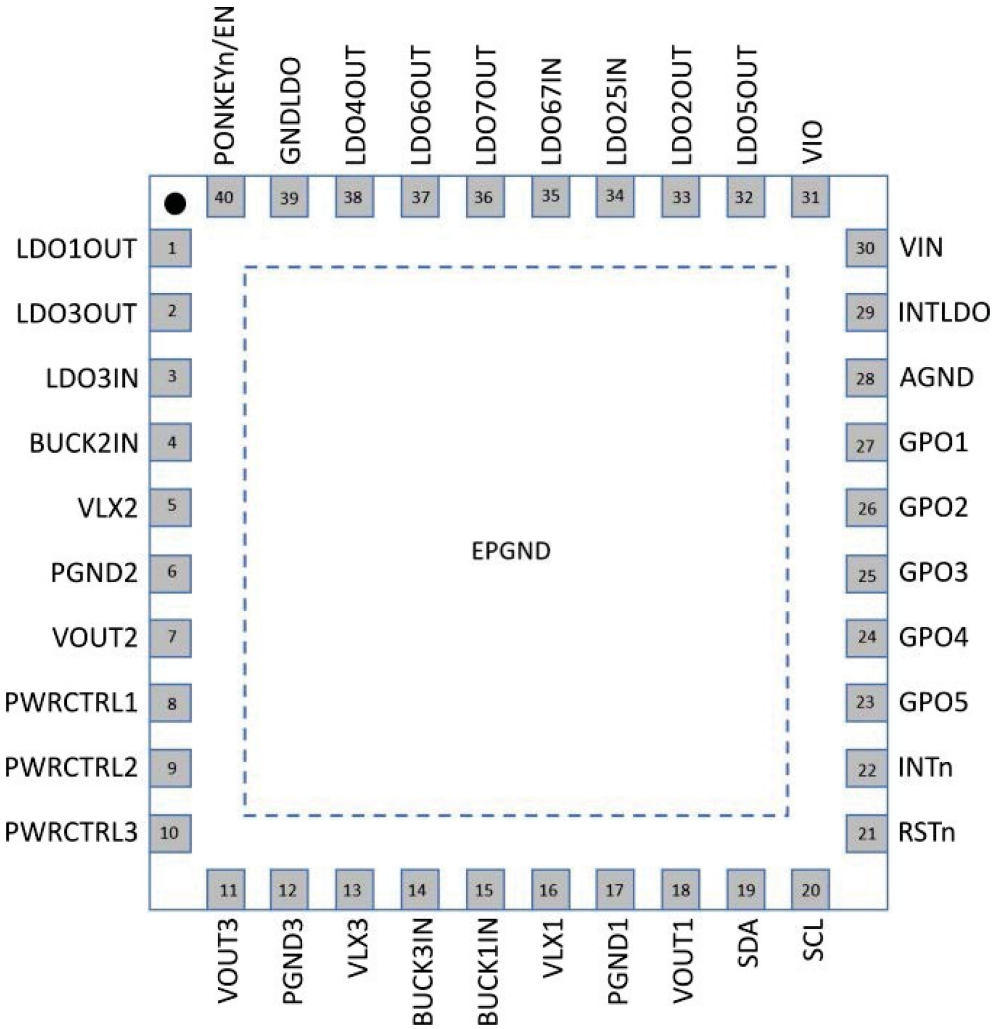

Table 1 shows the possible configuration of STPMIC2L digital input/output pins if they are not used in the final application:

Table 1. STPMIC2L digital pin configuration

Pin Number	Pin Name	Type	If not used
08	PWRCTRL1	I	Floating
09	PWRCTRL2	I	Floating
10	PWRCTRL3	I	Floating
19	SDA	I/O	VIO
20	SCL	I	VIO
21	RSTn	I/O	Floating
22	INTn	O	Floating
40	PONKEYn/En	I	Floating

Table 2 shows the possible configuration of STPMIC2L analog input/output pins if they are not used in the final application:

Table 2. STPMIC2L power analog I/O pin configuration

Pin Number	Pin Name	Type	If not used
01	LDO1OUT	O	Floating
02	LDO3OUT	O	Floating
03	LDO3IN	I	VIN
04	BUCK2IN	I	VIN
05	VLX2	O	Floating
07	VOUT2	I	Floating
11	VOUT3	I	Floating
13	VLX3	O	Floating
14	BUCK3IN	I	VIN
15	BUCK1IN	I	VIN
16	VLX1	O	Floating
18	VOUT1	I	Floating
23	GPO5	O	Floating
24	GPO4	O	Floating
25	GPO3	O	Floating
26	GPO2	O	Floating
27	GPO1	O	Floating
29	INTLDO	O	4.7 µF capacitor
30	VIN	I	VIN
31	VIO	I	VIO
32	LDO5OUT	O	Floating
33	LDO2OUT	O	Floating
34	LDO25IN	I	VIN
35	LDO67IN	I	VIN
36	LDO7OUT	O	Floating
37	LDO6OUT	O	Floating
38	LDO4OUT	O	Floating

If the passive components (inductors, capacitors) of the unused LDOs and buck converters are not mounted (for cost constraints, to reduce the occupied area around the STPMIC2L etc.), it is mandatory to disable these IPs by setting their respective ranks to 0 in the NVM. This avoids any possible oscillation or saturation of the internal circuitry and ensures that, at each power-on cycle, the unused IPs will not be automatically turned on.

1 STPMIC2L default NVM content shadow register map

The table below shows the default NVM content shadow register map of the STPMIC2LA and STPMIC2LB versions.

Table 3. STPMIC2LA/B default NVM shadow register map

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map							
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURNON
			A: 0xF1	1	1	1	1	0	0	0	1
			B: 0xD1	1	1	0	1	0	0	0	1
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CONFIG	NVM_PKEY_LKP_FSLS	NVM_PKEY_LKP_TMR[1:0	
			A: 0x0A	0	0	0	0	1	0	1	0
			B: 0x0A	0	0	0	0	1	0	1	0
0x92	NVM_RANK_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
			A: 0x02	0	0	0	0	0	0	1	0
			B: 0x02	0	0	0	0	0	0	1	0
0x93	NVM_RANK_SHR2	R/W		-	-	-			BUCK3_RANK[2:0]		
			A: 0x04	0	0	0	0	0	1	0	0
			B: 0x04	0	0	0	0	0	1	0	0
0x96	NVM_RANK_SHR5	R/W		-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
			A: 0x09	0	0	0	0	1	0	0	1
			B: 0x09	0	0	0	0	1	0	0	1
0x97	NVM_RANK_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
			A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0x98	NVM_RANK_SHR7	R/W		-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
			A: 0x1D	0	0	0	1	1	1	0	1
			B: 0x1D	0	0	0	1	1	1	0	1
0x99	NVM_RANK_SHR8	R/W		-	-	-			LDO7_RANK[2:0]		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9A	NVM_BUCK_MODE_SHR1	R/W		-		BUCK3_PREG_MODE[1:0]		BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9C	NVM_BUCK1_VOUT_SHR	R/W		BUCK1 voltage range	NVM_VOUT[6:0]						
			A: 0x20	0	0	1	0	0	0	0	0
			B: 0x20	0	0	1	0	0	0	0	0

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x9D	NVM_BUCK2_VOUT_SHR	R/W		Reserved	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9E	NVM_BUCK3_VOUT_SHR	R/W		Reserved	NVM_VOUT[6:0]						
			A: 0x9E	1	0	0	1	1	1	1	0
			B: 0x9E	1	0	0	1	1	1	1	0
0x9F	NVM_GPO_CONFG_S	R/W		-			GPO5 polarity config.	GPO4 polarity config.	GPO3 polarity config.	GPO2 polarity config.	GPO1 polarity config.
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA0	NVM_BUCGPO_RANK_SHR1	R/W		-	-	GPO2_RANK			GPO1_RANK		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA1	NVM_BUCGPO_RANK_SHR2	R/W		-	-	GPO4_RANK			GPO3_RANK		
			A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0xA2	NVM_BUCGPO_RANK_SHR3	R/W		-		-			GPO5_RANK		
			A: 0x05	0	0	0	0	0	1	0	1
			B: 0x05	0	0	0	0	0	1	0	1
0xA3	NVM_LDO2_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x12	0	0	0	1	0	0	1	0
0xA4	NVM_LDO3_SHR	R/W		SNK-SRC	-	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0xA6	NVM_LDO6_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x12	0	0	0	1	0	0	1	0
			B: 0x12	0	0	0	1	0	0	1	0
0xA7	NVM_LDO7_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA9	NVM_PD_SHR1	R/W		-		NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x19	0	0	0	1	1	0	0	1
			B: 0x19	0	0	0	1	1	0	0	1
0xAB	NVM_PD_SHR3	R/W		-	NVM_LDO7_PD	NVM_LDO6_PD	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	NVM_LDO1_PD

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xAB	NVM_PD_SHR3	R/W	A: 0x7F	0	1	1	1	1	1	1	1
			B: 0x7F	0	1	1	1	1	1	1	1
0xAC	NVM_BUCKS_IOUT_SHR1	R/W		-		BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0x3A	0	0	1	1	1	0	1	0
			B: 0x3A	0	0	1	1	1	0	1	0
0xAD	NVM_BUCKS_IOUT_SHR2	R/W		HICCUP_DLY[1:0]		-		-		-	
			A: 0x40	0	1	0	0	0	0	0	0
			B: 0x40	0	1	0	0	0	0	0	0
0xAE	NVM_LDOS_IOUT_SHR	R/W		LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xAF	NVM_FS_OCP_SHR1	R/W		-	-	-	-	-	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
			A: 0x07	0	0	0	0	0	1	1	1
			B: 0x07	0	0	0	0	0	1	1	1
0xB0	NVM_FS_OCP_SHR2	R/W		-	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_FS_OCP_LDO1
			A: 0x67	0	1	1	0	0	1	1	1
			B: 0x67	0	1	1	0	0	1	1	1
0xB1	NVM_FS_SHR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xB2	NVM_FS_SHR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xB3	NVM_FS_SHR3	R/W		-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
			A: 0x4F	0	1	0	0	1	1	1	1
			B: 0x4F	0	1	0	0	1	1	1	1
0xB4	NVM_BUCK_AUTOCAL_SHR	R/W		BUCKS_AUTOCAL_PD	IP_SAFE_MRST	-	-	-	-	-	NVM_BUCK_AUTOCAL_CFG
			A: 0x80	1	0	0	0	0	0	0	0
			B: 0x80	1	0	0	0	0	0	0	0
0xB5	NVM_I²C_ADDR_SHR	R/W		LOCK_NVM	I2C_ADDR[6:0]						
			A: 0x33	0	0	1	1	0	0	1	1
			B: 0x33	0	0	1	1	0	0	1	1
0xB6	NVM_USER_SHR1	R/W		NVM_USER1[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0xB6	NVM_USER_SHR1	R/W	B: 0x00	0	0	0	0	0	0	0	0
0xB7	NVM_USER_SHR2	R/W		NVM_USER2[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xB9	NVM_MAIN_CTRL_SHR3	R/W		NVM "VIN" delay		-	-	NVM PONKEYn/ ENABLE pull		NVM PONKEYn /ENABLE polarity	NVM "PONKEY n" functionality active
			A: 0x46	0	1	0	0	0	1	1	0
			B: 0x46	0	1	0	0	0	1	1	0

1. *This column contains the STPMIC2L default values of the NVM content shadow register for STPMIC2LA/B versions in hexadecimal format.*

Revision history

Table 4. **Document revision history**

Date	Version	Changes
03-Dec-2025	1	Initial release.

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