STPMIC2L NVM configuration

Introduction

The STPMIC2L is a fully integrated power management IC designed for STM32MP2x MPU family applications requiring low power and high efficiency.

The device integrates advanced low-power features controlled by a host processor via I²C and I/O interfaces.

The STPMIC2L features a large input voltage range from 2.8 V to 5.5 V to supply:

- 5 V DC wall-adaptor applications
- 1-cell 3.6 V Li-ion / Li-Po battery applications

The STPMIC2L provides all the regulators needed to power supply a complete application:

- 4 adjustable general-purpose LDOs
- 1 LDO for DDR3L/DDR4 termination (sink-source) or as a general-purpose LDO
- 2 LDOs with a fixed output voltage
- 3 step-down (buck) converters with 2 MHz switching frequency in PWM mode
- 5 GPO output controls for external command

The STPMIC2L regulators are designed to supply power to the application processor as well as to the external system peripherals, such as DDR, flash memories, and other system devices.

1 STPMIC2L NVM configuration

The STPMIC2L has a non-volatile memory (NVM) that can be (re)programmed via I²C directly in target applications to facilitate mass production, enabling scalability to support a wide range of applications. The main settings of the STPMIC2L are stored in the NVM memory:

- V_{IN} voltage threshold
- Auto turn-on feature
- Default I²C slave device address
- Regulator default output voltages at startup
- Regulator power-up sequence at startup (rank)
- Safety management (behavior in case of failure), overcurrent protection, overtemperature protection, VIN_low, watchdog and PONKEY fault counters
- Possibility to lock the NVM content to prevent further re-programming by writing the LOCK_NVM bit
- Other features (see the STPMIC2L datasheet for further details)

The STPMIC2LA and STPMIC2LB are the two standard NVM configurations that support the STM32MP2xx family of MPU application versions with a minimum set of regulators enabled by default:

- STPMIC2LA version:
  - Typical use case: 5 V continuous input voltage (wall adapter) applications
  - VDDIO @ 3.3 V (LDO2 output)
- STPMIC2LB version:
  - Typical use case: Li-ion/Li-Po single-cell battery applications
  - VDDIO @ 1.8 V (LDO2 output)

The main settings of the STPMIC2LA and STPMIC2LB versions are listed in the table below:

Table 1. Main settings of STPMIC2LA and STPMIC2LB

IP	STPMIC2LA			STPMIC2LB		
	Voltage	Pull	Rank	Voltage	Pull	Rank
LDO1 (VDDA18AON)	1.8V	Pull DOWN	1	1.8V	Pull DOWN	1
LDO2 (VDDIO)	3.3V	Pull DOWN	1	1.8V	Pull DOWN	1
LDO3 (VTT/VDD1_DDR)	OFF	Pull DOWN	0	OFF	Pull DOWN	0
LDO4 (VDD33USB)	3.3V	Pull DOWN	5	3.3V	Pull DOWN	5
LDO5 (VDD_FLASH)	3.3V	Pull DOWN	5	2.9	Pull DOWN	5
LDO6 (VDDA)	1.8V	Pull DOWN	3	1.8	Pull DOWN	3
LDO7 (VPP_DDR4)	OFF	Pull DOWN	0	OFF	Pull DOWN	0
BUCK1 (VDDCORE)	0.82V	SLOW	2	0.82V	SLOW	2
BUCK2 (VDDDDR)	OFF	FAST	0	OFF	FAST	0
BUCK3 (VDDCPU/VDDGPU)	0.8V	SLOW	4	0.8V	SLOW	4
GPIO1	OFF	Pull HIGH	0	OFF	Pull HIGH	0
GPIO2	OFF	Pull HIGH	0	OFF	Pull HIGH	0
GPIO3	OFF	Pull HIGH	0	OFF	Pull HIGH	0
GPIO4	VIN	Pull HIGH	5	VIN	Pull HIGH	5
GPIO5	VIN	Pull HIGH	5	VIN	Pull HIGH	5

The startup sequence of STPMIC2L is divided into four steps (Rank0 to Rank5).

Each buck converter, LDO regulator and/or GPO can be programmed to be turned ON automatically in one of these ranks. Each rank phase is separated by a delay, which is 1.5 ms by default.

This rank delay can be programmed in the NVM (Reg0x91[7:6]) at 1.5 ms, 3 ms, 4.5 ms or 6 ms (RANK_DLY[1:0]).

- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence
- Rank = 1: rail automatically turned ON after 7 ms (which is the fixed delay from VIN > VINOK_Rise to the start of IPs with rank1), following a Turn_ON condition
- Rank = 2: rail automatically turned ON after a further 1.5 ms compared to Rank1 output rails
- Rank = 3: rail automatically turned ON after a further 1.5 ms compared to Rank2 output rails
- Rank = 4: rail automatically turned ON after a further 1.5 ms compared to Rank3 output rails
- Rank = 5: rail automatically turned ON after a further 1.5 ms compared to Rank4 output rails

Regardless of the STPMIC2L version:

- AUTO_TURN_ON option is set

Table 2 shows the miscellaneous settings at startup of STPMIC2LA and STPMIC2LB version:

Table 2. Miscellaneous settings of STPMIC2LA and STPMIC2LB at startup

Parameter	STPMIC2LA	STPMIC2LB	Comments
VIN_OK_Rise	4.0 V	3.3 V	VIN threshold enabling PMIC to turn ON
VIN_OK_hysteresis	0.5 V	0.5 V	-
Auto_Turn_ON	ON	ON	Automatic PMIC turn-ON when VIN exceeds VIN_OK_Rise
Rank duration	1.5 ms	1.5 ms	Duration of delay between two ranks
NRST delay	0	0	Delay after last rank before PMIC releases NRST
I²C address	0x33	0x33	-
USER NVM byte	0	0	2 free NVM bytes for the user

Table 3 shows the complete NVM shadow register map of STPMIC2LA and STPMIC2LB versions:

Table 3. Safety management settings of STPMIC2LA and STPMIC2LB at startup

Parameter	STPMIC2LA	STPMIC2LB	Comments
NVM_WDG_EN	OFF	OFF	Watchdog can be enabled at runtime
PKEY_LKP_OFF	ON	ON	A long PONKEY key press does not switch OFF STPMIC2L
PKEY_LKP_EN_FSLS	OFF	OFF	A long PONKEY press allows the STPMIC2L to skip the fail-safe lock state
PKEY_LKP_TMR	10 s	10 s	Long PONKEY press timer duration settings
HICCUP_DLY	100 ms	100 ms	
VIN_FLT_CNT_MAX	∞ restart	∞ restart	
TSHDN_FLT_CNT_MAX	∞ restart	∞ restart	
OCP_FLT_CNT_MAX	∞ restart	∞ restart	If regulator OCP management set in fail-safe (FS) mode
WDG_FLT_CNT_MAX	∞ restart	∞ restart	
PKEY_FLT_CNT_MAX	∞ restart	∞ restart	
RST_FLT_CNT_TMR	Disabled	Disabled	
FAIL_SAFE_LOCK_DIS	Disabled	Disabled	PMIC will never be locked in FS mode state (will go to OFF mode)
VIN_DLY	10 ms	10 ms	Additional VIN delay
PKEY_EN_CFG	PONKEY	PONKEY	PONKEYn/EN feature configuration
NVM_PKEY_EN_PULL	Pull-up active	Pull-up active	PONKEYn/EN pad pull resistor selection

Table 4 shows the fail-safe OCP settings at startup of STPMIC2LA and STPMIC2LB versions:

Table 4. Fail-safe OCP settings of STPMIC2LA, and STPMIC2LB at startup

Parameter	STPMIC2LA OCPmgt / OCP lim	STPMIC2LB OCPmgt / OCP lim	Comments
BUCK1 (VDDCORE)	FS/ 1.5 A / SPD	FS/ 1.5 A / SPD	SPD: Slow pull-down when BUCK1 disabled
BUCK2(VDDDDR)	FS/ 1.5 A / FPD	FS/ 1.5 A / FPD	FPD: Fast pull-down when BUCK2 disabled
BUCK3 (VDDCPU/GPU)	FS/ 2 A / SPD	FS/ 2 A / SPD	SPD: Slow pull-down when BUCK1 disabled
LDO1 (VDDA18AON)	FS	FS	-
LDO2 (VDDIO)	FS/400 mA	FS/400 mA	-
LDO3 (VTT/VDD1_DDR)	FS	FS	-
LDO4 (VDD33USB)	Hiccup	Hiccup	-
LDO5 (VDD_FLASH)	Hiccup/ 400 mA	Hiccup/ 400 mA	-
LDO6 (VDDA)	FS / 400 mA	FS / 400 mA	-
LDO7 (VPP_DDR4)	FS / 400 mA	FS / 400 mA	-
GPO1/2/3/4/5	NA	NA	-

Table 5 shows the complete NVM shadow register map of the STPMIC2LA and STPMIC2LB versions:

Table 5. STPMIC2LA/B NVM shadow register map

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURNON
			A: 0xF1	1	1	1	1	0	0	0	1
			B: 0xD1	1	1	0	1	0	0	0	1
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CONFIG	NVM_PKEY_LKP_FSLS	NVM_PKEY_LKP_TMR[1:0]	
			A: 0x0A	0	0	0	0	1	0	1	0
			B: 0x0A	0	0	0	0	1	0	1	0
0x92	NVM_RANK_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
			A: 0x02	0	0	0	0	0	0	1	0
			B: 0x02	0	0	0	0	0	0	1	0
0x93	NVM_RANK_SHR2	R/W		-	-	-			BUCK3_RANK[2:0]		
			A: 0x04	0	0	0	0	0	1	0	0
			B: 0x04	0	0	0	0	0	1	0	0
0x96	NVM_RANK_SHR5	R/W		-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
			A: 0x09	0	0	0	0	1	0	0	1
			B: 0x09	0	0	0	0	1	0	0	1
0x97	NVM_RANK_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x97	NVM_RANK_SHR6	R/W	A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0x98	NVM_RANK_SHR7	R/W		-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
			A: 0x1D	0	0	0	1	1	1	0	1
			B: 0x1D	0	0	0	1	1	1	0	1
0x99	NVM_RANK_SHR8	R/W		-	-	-			LDO7_RANK[2:0]		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9A	NVM_BUCK_MODE_SHR1	R/W		-		BUCK3_PREG_MODE[1:0]		BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9C	NVM_BUCK1_VOUT_SHR	R/W		BUCK1 voltage range	NVM_VOUT[6:0]						
			A: 0x20	0	0	1	0	0	0	0	0
			B: 0x20	0	0	1	0	0	0	0	0
0x9D	NVM_BUCK2_VOUT_SHR	R/W		Reserved	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0x9E	NVM_BUCK3_VOUT_SHR	R/W		Reserved	NVM_VOUT[6:0]						
			A: 0x9E	1	0	0	1	1	1	1	0
			B: 0x9E	1	0	0	1	1	1	1	0
0x9F	NVM_GPO_CONFG_S	R/W		-			GPO5 Polarity Config.	GPO4 Polarity Config.	GPO3 Polarity Config.	GPO2 Polarity Config.	GPO1 Polarity Config.
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA0	NVM_BUCGPO_RANK_SHR1	R/W		-	-	GPO2_RANK			GPO1_RANK		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA1	NVM_BUCGPO_RANK_SHR2	R/W		-	-	GPO4_RANK			GPO3_RANK		
			A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0xA2	NVM_BUCGPO_RANK_SHR3	R/W		-		-			GPO5_RANK		
			A: 0x05	0	0	0	0	0	1	0	1
			B: 0x05	0	0	0	0	0	1	0	1
0xA3	NVM_LDO2_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x12	0	0	0	1	0	0	1	0
0xA4	NVM_LDO3_SHR	R/W		SNK-SRC	-	NVM_VOUT[4:0]					-

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xA4	NVM_LDO3_SHR	R/W	A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
0xA6	NVM_LDO6_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x12	0	0	0	1	0	0	1	0
			B: 0x12	0	0	0	1	0	0	1	0
0xA7	NVM_LDO7_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xA9	NVM_PD_SHR1	R/W		-		NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x19	0	0	0	1	1	0	0	1
			B: 0x19	0	0	0	1	1	0	0	1
0xAB	NVM_PD_SHR3	R/W		-	NVM_LDO7_PD	NVM_LDO6_PD	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	NVM_LDO1_PD
			A: 0x7F	0	1	1	1	1	1	1	1
			B: 0x7F	0	1	1	1	1	1	1	1
0xAC	NVM_BUCKS_IOUT_SHR1	R/W		-		BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0x3A	0	0	1	1	1	0	1	0
			B: 0x3A	0	0	1	1	1	0	1	0
0xAD	NVM_BUCKS_IOUT_SHR2	R/W		HICCUP_DLY[1:0]		-		-		-	
			A: 0x40	0	1	0	0	0	0	0	0
			B: 0x40	0	1	0	0	0	0	0	0
0xAE	NVM_LDOS_IOUT_SHR	R/W		LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xAF	NVM_FS_OCP_SHR1	R/W		-	-	-	-	-	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
			A: 0x07	0	0	0	0	0	1	1	1
			B: 0x07	0	0	0	0	0	1	1	1
0xB0	NVM_FS_OCP_SHR2	R/W		-	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_FS_OCP_LDO1
			A: 0x67	0	1	1	0	0	1	1	1
			B: 0x67	0	1	1	0	0	1	1	1
0xB1	NVM_FS_SHR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xB2	NVM_FS_SHR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			

Reg (Hex)	Register Name	R/W	STPMIC2LA/B default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xB2	NVM_FS_SHR2	R/W	A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
0xB3	NVM_FS_SHR3	R/W		-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
			A: 0x4F	0	1	0	0	1	1	1	1
			B: 0x4F	0	1	0	0	1	1	1	1
0xB4	NVM_BUCK_AUTOCAL_SHR	R/W		BUCKS_AUTOCAL_PD	IP_SAFE_MRST	-	-	-	-	-	NVM_BUCK_AUTOCAL_CFG
			A: 0x80	1	0	0	0	0	0	0	0
			B: 0x80	1	0	0	0	0	0	0	0
0xB5	NVM_I²C_ADDR_SHR	R/W		LOCK_NVM	I2C_ADDR[6:0]						
			A: 0x33	0	0	1	1	0	0	1	1
			B: 0x33	0	0	1	1	0	0	1	1
0xB6	NVM_USER_SHR1	R/W		NVM_USER1[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xB7	NVM_USER_SHR2	R/W		NVM_USER2[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
0xB9	NVM_MAIN_CTRL_SHR3	R/W		NVM "VIN" delay		-	-	NVM PONKEYn/ ENABLE pull		NVM PONKEYn /ENABLE polarity	NVM "PONKEYn" functionality active
			A: 0x46	0	1	0	0	0	1	1	0
			B: 0x46	0	1	0	0	0	1	1	0

1. This column contains the STPMIC2L default values of the NVM content shadow register for STPMIC2LA/B versions in hexadecimal format.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
24-Nov-2025	1	Initial release.

Contents

List of tables