Application note

ST60A3H1 PCB design guidelines

Introduction

The aim of this document is to help users integrate the ST60A3H1 into their boards by providing guidelines for both the schematic design and PCB layout, based on the X-NUCLEO-60K1A1 kit.

These guidelines are applicable to products with a single ST60A3H1 pair as additional constraints apply to multi-lane applications involving more than one ST60A3H1 pair.

The X-NUCLEO-60K1A1 is a kit composed of two expansion boards, an X-NUCLEO-60L1A1 expansion board, and an X-NUCLEO-60R1A1 expansion board, working as a pair, which can be plugged onto most STM32 Nucleo boards equipped with the Arduino® R3 connectors. It provides a complete evaluation kit that allows you to learn, evaluate, and develop applications based on the ST60A3H1 transceiver, for contactless connectivity up to 480 Mbit/s.

The ST60A3H1 is a full RF transceiver with a dual-linear-polarization integrated antenna, operating in half-duplex mode. It provides an optimized solution for a high-speed, low-power, short-range point-to-point 60 GHz RF link.

1 Layout recommendations

The ST60A3H1 combines a high data rate digital interface, millimeter wave RF, and an antenna in package. Besides the IC and antenna design, the end-to-end link's performance depends on the way the IC is implemented and used in the application: the IC integration on the application board and the operating conditions (temperature, RF gap, casing, 3D environment, etc.). Careful consideration is therefore needed during the application board design to achieve the desired performance.

The following PCB guidelines are provided to help users integrate the ST60A3H1 on the board, optimizing the radiation properties of the antenna and the IC's end-to-end performance (link budget and ripple).

1.1 General ST60A3H1 antenna integration principles

To preserve the ST60A3H1 antenna's radiation properties and end-to-end performance, STMicroelectronics' general recommendations are:

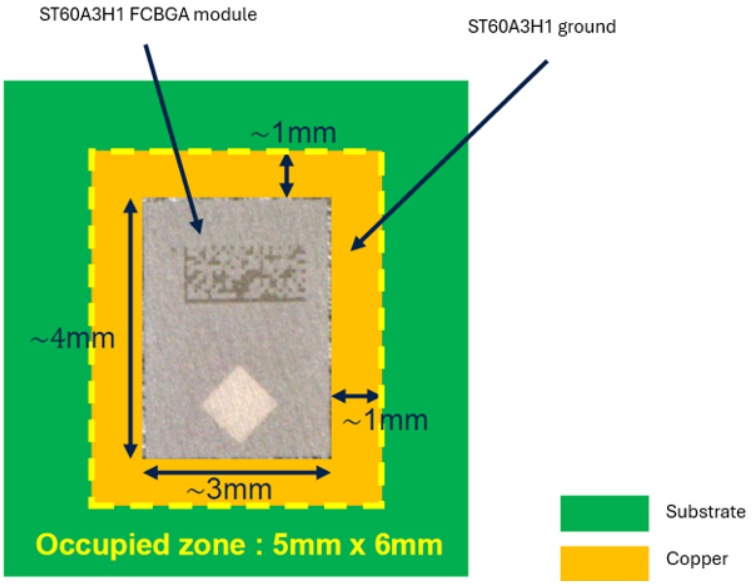
- To minimize the metal plates around the ST60A3H1's ground and/or add ground openings to isolate it from the rest of the board.
- To shield the interconnects (power supply, high-speed IOs, low-speed data, and control signals) using a dedicated inner layer ground plane.
- To route the ST60A3H1 signals using stacked and buried vias and not directly on the ST60A3H1 component layer.
- To integrate the ST60A3H1 as a standalone component and separated from other board components (isolated on a rectangular part that emerges from the rest of the PCB). This helps avoid extra coupling and rippling on the radiation due to substrate waves and edges.

The guidelines presented in this section are an application of the above principles with more details. Strictly following them is not mandatory for the system to be functional and it is possible to find different configurations that are good enough, but it is strongly recommended to follow STMicroelectronics guidelines to preserve the system's performances. Any deviation from these guidelines can have an impact on the ST60A3H1's performance that would need to be evaluated in an EM (ElectroMagnetic) simulation. Under NDA conditions, STMicroelectronics can provide an encrypted Ansys HFSS model of the ST60A3H1 so that users can run these EM (ElectroMagnetic) simulations.

1.1.1 ST60A3H1 grounding, reflector, and radiation properties

The ST60A3H1 grounding is crucial for its antenna performance. The ground plane under the ST60A3H1 is at the right distance to play the role of a reflector, which is why this ground plane pattern can induce radiated performance variations. The objective being to improve the radiated performances of the board compared to the ST60A3H1 module alone. This ground is considered as a part of the radiated system and needs to be well controlled and isolated from the rest. This ground plane is also necessary for proper IC grounding. The external size of the ground plane can affect the radiated gain (value and ripple vs. angle, beam angle). The 1 mm value shown in ST60A3H1 grounding is optimized for gain and beam centering.

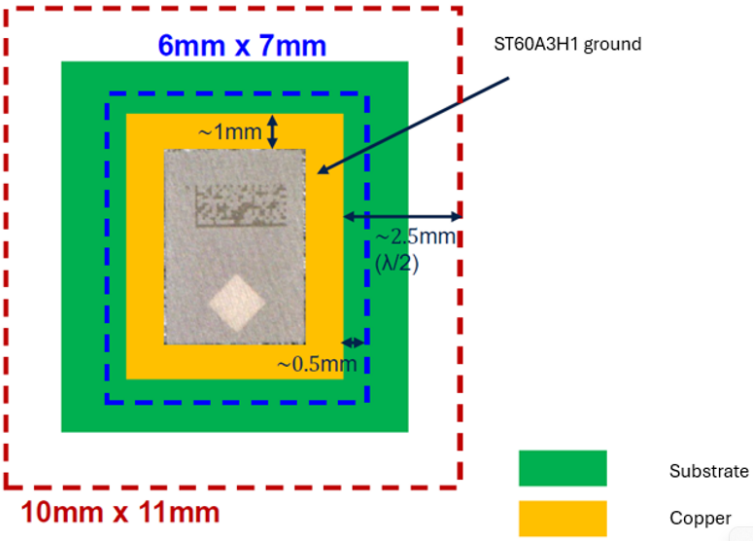
Figure 1. **ST60A3H1 grounding**



Provided the previous definition of the ST60A3H1's ground plane, a minimum isolation guard distance of 0.5 mm is needed (see Figure 2. ST60A3H1 various implementation zones), especially on this component layer. This isolation guard distance helps preserve the radiated performances, especially in terms of radiated gain and optimized angular beam, thus no copper should be present in this zone. If the ST60A3H1's ground is not cut from the rest of the board's ground, at least on the component layer, surface currents propagation can be different and can induce a different radiation pattern with a tilted beam and a reduced gain value, considering a far-field use. This rule (ground cut) should also be applied on the layer next to the component layer.

The 0.5 mm guard distance (blue zone in Figure 2) is mandatory even in cases where the application constraints prevent the integrator from removing the ground plane on the whole component layer and close to the ST60A3H1.

Figure 2. **ST60A3H1 various implementation zones**



The red zone is a recommended keep-out zone for SMD/packages to eliminate their influence on the IC. It is a second order recommendation to follow if enough space is available. A dedicated EM simulation would be required if one or more packages were inside the red zone. An alternative would be to place these packages on the opposite side of the board.

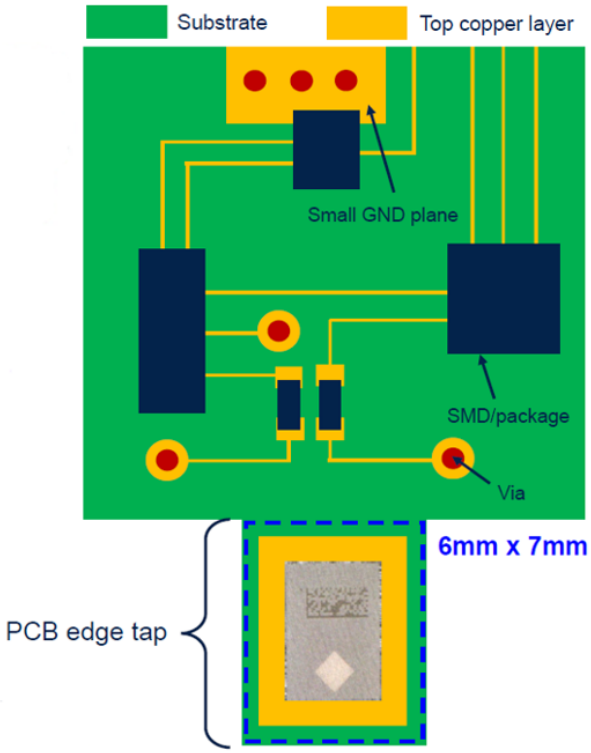
1.1.2 Recommended board form factor

Figure 3 presents an example of the recommended board form factor to isolate the ST60A3H1 on a PCB edge tap in order to control its close environment. This minimizes:

- The interference between the space waves of the antenna and the parasitic radiation from substrate-guided modes (surface waves) inside the PCB, leading to radiation pattern ripple signature.
- The rippling on the end-to-end link loss due to metal reflection, refraction, and diffraction mechanisms. It is recommended to remove all ground surface on the rest of the top copper layer (if possible or reduce at maximum their size) to limit as much as possible metal surfaces facing in the end-to-end configuration.

The isolation guard distance zone (in blue) is also the recommended substrate cut zone in this case.

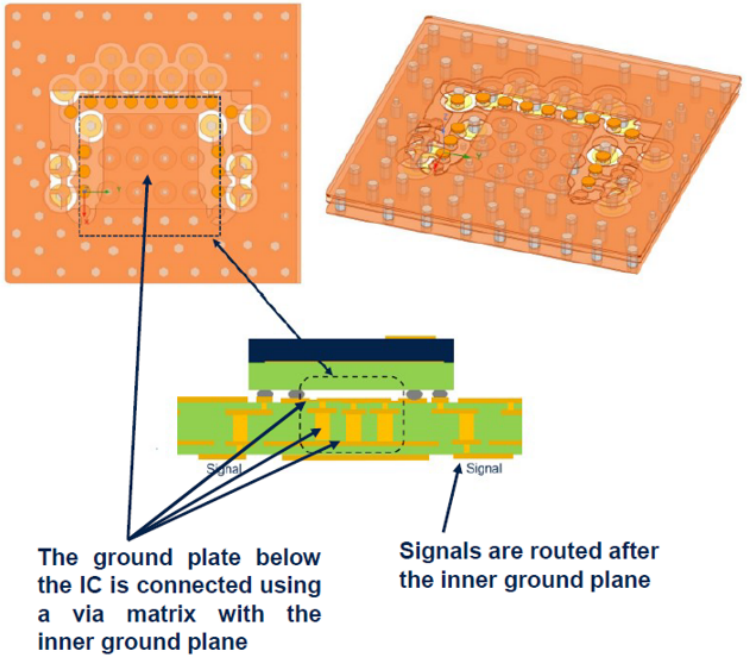
Figure 3. Board form factor



1.1.3 Local control of the injected E-field density inside the PCB

A ground plate below the ST60A3H1 package connected through a via matrix to an inner layer (full) ground plane helps minimize the waves propagation underneath the ST60A3H1 (see Figure 4. Ground plane below the ST60A3H1).

Figure 4. Ground plane below the ST60A3H1

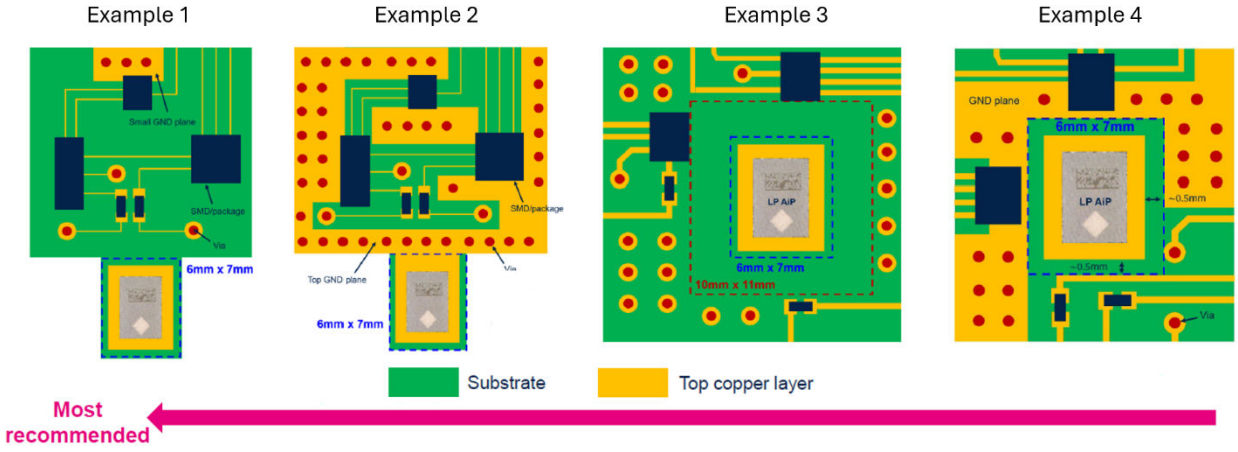


In other words, the goal is to reduce as much as possible the injected E-field inside the PCB to avoid exciting substrate wave propagation modes. No routing is allowed between the ST60A3H1's layer and this inner ground layer.

1.1.4 Other possible PCB implementations

STMicroelectronics has performed multiple EM simulations with the ST60A3H1 which led to the recommended implementation described in the previous sections. Other PCB implementations are possible depending on the application and its constraints, but they require a validation with EM simulations. Four different implementation examples (not necessarily simulated by STMicroelectronics) are shown in Figure 5. ST60A3H1 implementation examples.

Figure 5. ST60A3H1 implementation examples



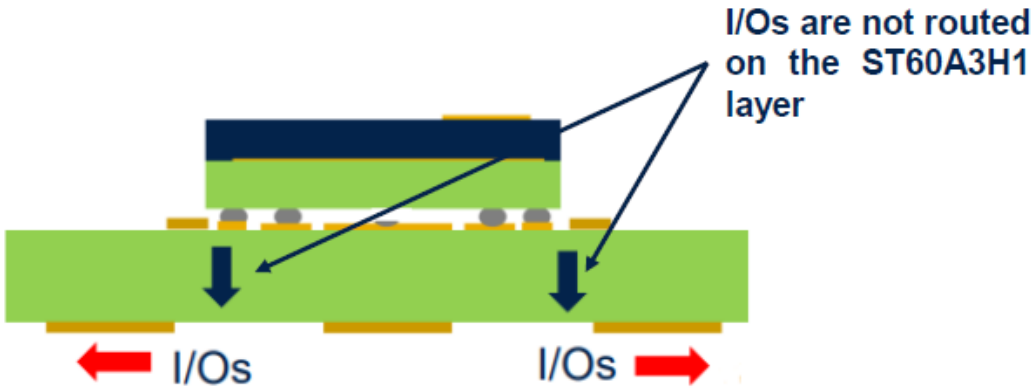
As can be seen in Section 1.2, the X-NUCLEO-60K1A1 was designed and optimized to be close to typical application boards and does therefore not follow all the general recommendations. This is to show that the ST60A3H1 can work with classical/common PCB implementations even if we know from experience that implementations following our recommendations could lead to even better performances.

1.1.5 I/Os routing

The I/Os must be routed from the ST60A3H1's balls on layers other than the ST60A3H1 layer. In-pad vias must therefore be used (see Figure 6. ST60A3H1 I/Os routing). This minimizes:

- 60 GHz noise on the traces, especially the high-speed I/Os.
- Broadside parasitic radiation which is relative to the E-field density injected inside the PCB.

Figure 6. ST60A3H1 I/Os routing



1.2 X-NUCLEO-60K1A1 implementation

The previous section described the generally recommended rules for an optimal integration of the ST60A3H1. There may however be additional constraints (cost, manufacturing, mechanical, etc.) which would prevent the board designer from following all these rules. In such cases, EM simulations would be needed to evaluate the impact on the ST60A3H1 performance of any deviation.

The X-NUCLEO-60K1A1 is an implementation example with a common PCB which follows some of the rules listed previously and discards some others. EM simulations have been done on this board and the impact compared to the optimal implementation has been quantified and deemed acceptable.

Therefore, users can and are advised to copy the X-NUCLEO-60K1A1 PCB board (the ST60A3H1 zone) and be assured that their boards can obtain similar RF performances.

Users who would deviate from the X-NUCLEO-60K1A1, including a change in the board stack-up, layers number (even down to 2), etc. would need to evaluate the impact of such deviation through EM simulations (standalone and end-to-end in the targeted RF channel) and are invited to contact STMicroelectronics for support.

Captures from the X-NUCLEO-60K1A1 PCB are used to illustrate the various rules that were followed in its design.

1.2.1 PCB specification and stack-up

The X-NUCLEO-60K1A1 is a 4-layer 1.6 mm thick FR4 board. The core, prepreg, and solder mask characteristics are indicated in Figure 7. X-NUCLEO-60K1A1 stack-up. PTH vias are the only type of vias used. The various layers are described later in this document.

Figure 7. X-NUCLEO-60K1A1 stack-up

Name	Material	Type	Weight	Thickness	Dk	Df
Top Overlay		Overlay				
Top Solder	SM-003	Solder Mask		0.0254mm	4	0.03
Top Layer 1 Sign...	Cu EXT	Signal	1oz	0.035mm		
Dielectric 1	2 x 7628	Prepreg		0.36mm	4.6	0.02
Layer 2	CF-004	Signal	1/2oz	0.018mm		
Core	CORE- 6 X 7...	Core		0.71mm	4.4	0.02
Layer 3	CF-004	Signal	1/2oz	0.018mm		
Dielectric 2	2 x 7628	Prepreg		0.36mm	4.6	0.02
Bottom Layer 4...	Cu EXT	Signal	1oz	0.035mm		
Bottom Solder	SM-003	Solder Mask		0.0254mm	4	0.03
Bottom Overlay		Overlay				

Note: Dk and Df in this table are given at 1 MHz. Prepreg Dk is given by the manufacturer at 4.3 at 10 GHz.

1.2.2 Form factor and keep-out zone

The X-NUCLEO-60K1A1 board follows an implementation which mixes examples 3 and 4 in Figure 5. ST60A3H1 implementation examples. The ST60A3H1 is placed together with the rest of the board's components (instead of being on a separated edge tap) with the 10 mm x 11 mm keep-out zone.

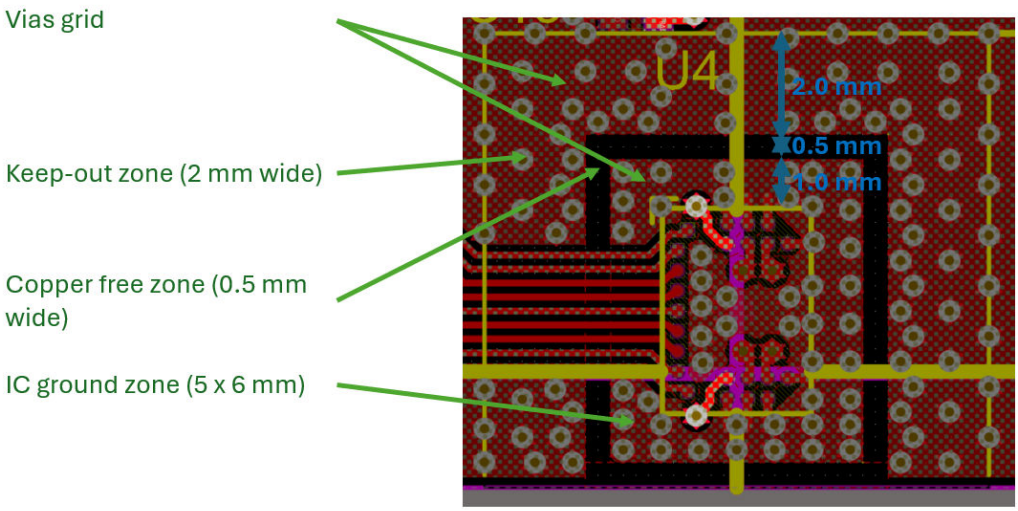
1.2.3 Board layers

Layer 1

This is the most important layer for the antenna behavior both in standalone and end-to-end configurations. Among the rules defined previously, two are fully followed on the X-NUCLEO-60K1A1 while the others have been discarded with minimum impact on the RF link performance quantified through EM simulations. The two rules that have been implemented are:

- Three specific zones around the ST60A3H1 (see Figure 8. X-NUCLEO-60K1A1 Layer 1)
  - The IC ground zone (5 mm x 6 mm) is filled with copper except for the PTH vias and routings.
  - A 0.5 mm wide rectangular ring with the copper removed and surrounding the first zone.
  - A 2 mm wide rectangular ring surrounding the second zone and free of any SMD but the ST60A3H1. This creates a 10 mm x 11 mm keep-out zone. This zone on the X-NUCLEO-60K1A1 is 10 mm x 9 mm only as it is stripped of the bottom 2 mm because the IC is placed on the border of the board.
- Ground vias grid over the first and third zone.

Figure 8. **X-NUCLEO-60K1A1 Layer 1**



Layer 2

This is a ground layer with a vias grid. No routing is done on this layer in the ST60A3H1 zone.

Layer 3

This is a ground layer with a vias grid. It is the reference ground plane for the eUSB2 differential lane that is routed on Layer 4.

Layer 4

This layer is used to route the 1.8 V power supply and the eUSB2 bus as can be seen in the next section.

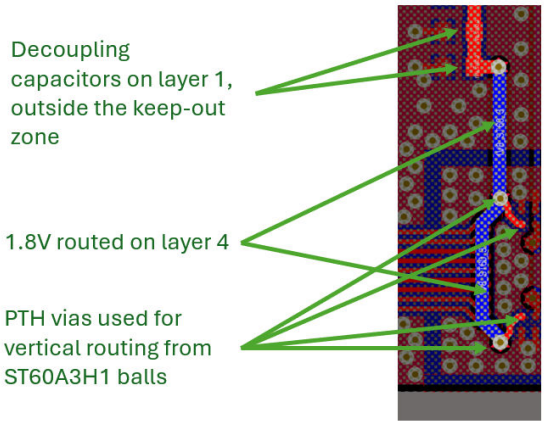
1.2.4 ST60A3H1 routing

Ground and power supply

The ground balls of the ST60A3H1 are connected to Layer 1's ground plane, as can be seen in Figure 8. X-NUCLEO-60K1A1 Layer 1.

The 1.8 V power supply is routed through a track on Layer 4. The decoupling capacitors are placed on Layer 1, outside the keep-out zone, but if the user is willing to place components on the bottom layer, then it is better to do so with the capacitors placed close to their respective balls on Layer 4. It is also better to use in-pad vias, micro-vias, and buried vias for vertical routing of the power signals from the ST60A3H1 balls but PTH vias can be used with minimum impact on the antenna performance as done on the X-NUCLEO-60K1A1. See Figure 9. Power supply routing, Layer 1 and Layer 4.

Figure 9. **Power supply routing, Layer 1 and Layer 4**



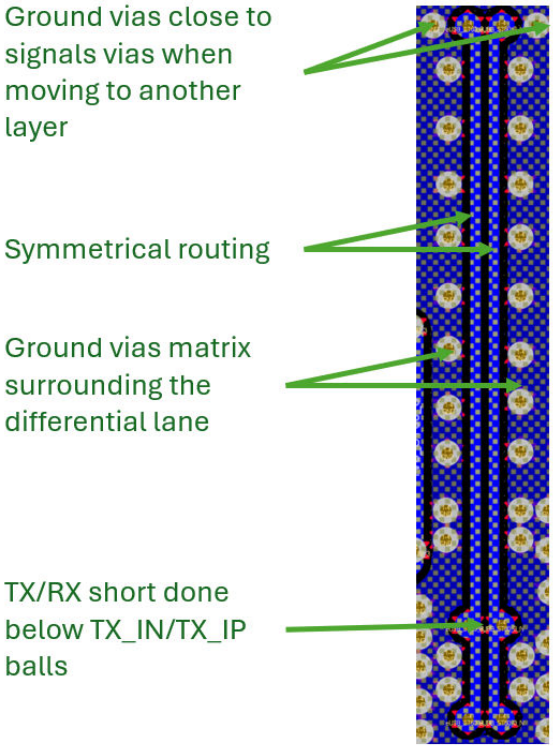
eUSB2 bus

This is a high-speed differential lane signal and the usual recommended practices to route such lanes must be followed. They include:

- Ensuring a good impedance control (85 Ω differential in our case) from end to end.
- Keeping the lane on the same layer as much as possible and in any case avoiding too many layer changes. If the lane routing changes layers, make sure the signal vias are closely surrounded by ground vias.
- Having a continuous reference ground plane (no cuts and no signal routing) placed on the layer above or below the differential lane's routing layer.
- Routing the P and N tracks symmetrically and ensuring the tracks have the same length (total and layer-per-layer individually if routed on more than one). The lane's total length must be kept short and, in all cases, compatible with the eUSB2 standard.
- Avoiding right angles and adding passives on the lane only when necessary.
- Isolating the differential lane for the rest of the signals by surrounding it by a ground vias matrix.

Some of these rules are illustrated in Figure 10. eUSB2 bus routing, Layer 4, showing the routing done on the X-NUCLEO-60K1A1.

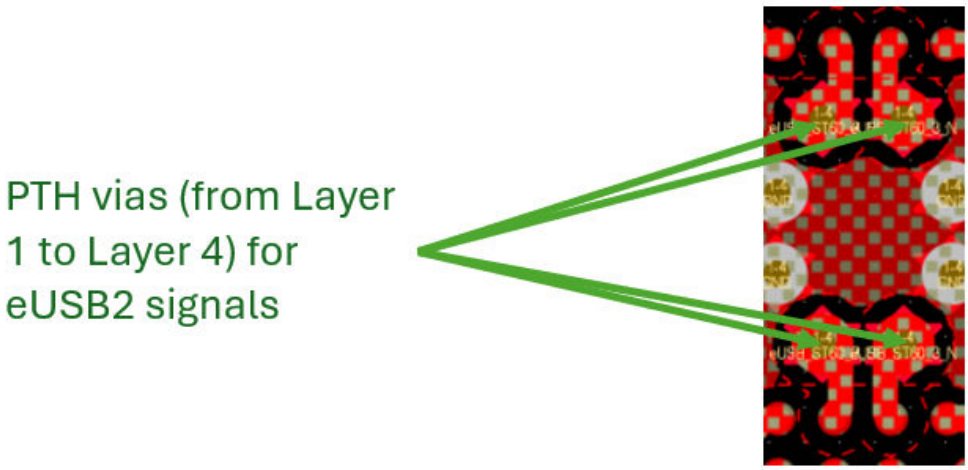
Figure 10. **eUSB2 bus routing, Layer 4**



Additionally, and specific to the ST60A3H1, it is necessary to short TX_IN with RX_ON and TX_IP with RX_OP. These shorts must be positioned below TX_IN/TX_IP balls for a minimized impedance matching break. If the suggested LC circuit is added (see Section 3.7: eUSB2 bus), place it symmetrically close to the short.

As much as possible, and to preserve the component's layer and therefore the ST60A3H1's antenna performances, it is advised to use in-pad, stacked micro-vias and buried vias for the vertical routing of the signals from the ST60A3H1's balls to the desired routing layer. It is however possible to use PTH vias with a minimum impact on the antenna's performance, as can be seen in Figure 11. eUSB2 routing from ST60A3H1 balls, Layer 1.

Figure 11. **eUSB2 routing from ST60A3H1 balls, Layer 1**

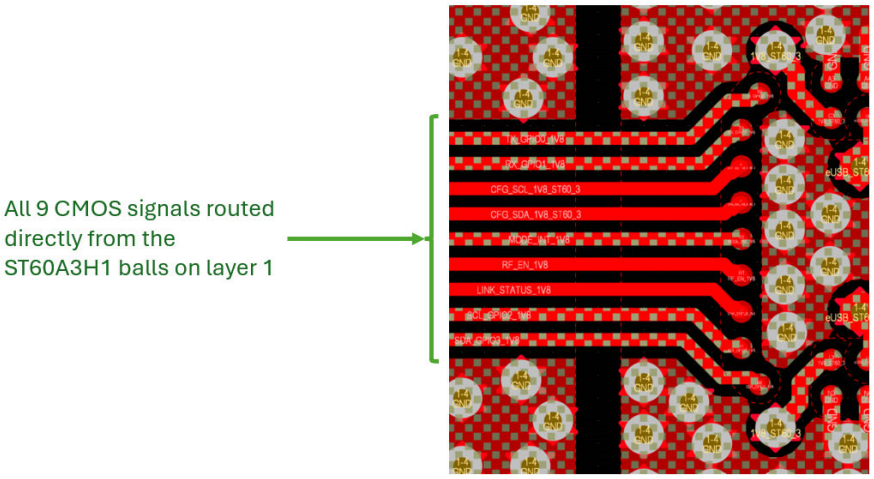


Single-ended signals

As much as possible, and to preserve the component's layer and therefore the ST60A3H1's antenna performances, it is advised to use in-pad, stacked micro-vias and buried vias for the vertical routing of the signals from the ST60A3H1's balls to the desired routing layer. It is however possible to route these signals directly on the ST60A3H1 component layer with a minimum impact on the antenna's performance, as can be seen in Figure 12. Single-ended signals routing from ST60A3H1 balls, Layer 1.

While these signals are low speed and some even static, their rise/fall time is very small and is a source of noise on the board. It is advised to route the active signals (I^2C for example) far from the sensitive signals/zones such as the eUSB2 lane.

Figure 12. Single-ended signals routing from ST60A3H1 balls, Layer 1



2 X-NUCLEO-60K1A1 RF performance

The X-NUCLEO-60K1A1 performance has been simulated and measured in both functional positions (0° and 180°) achieving very similar results. This section shows the results of the 0° position.

2.1 EM simulations

2.1.1 Standalone simulations

This section presents standalone simulation results or, in other words, only one side with one board and one LP AiP (linearly polarized antenna in package) module (ST60A3H1) as shown in Figure 13.

Figure 13. Standalone simulation 3D model view with the full X-NUCLEO board

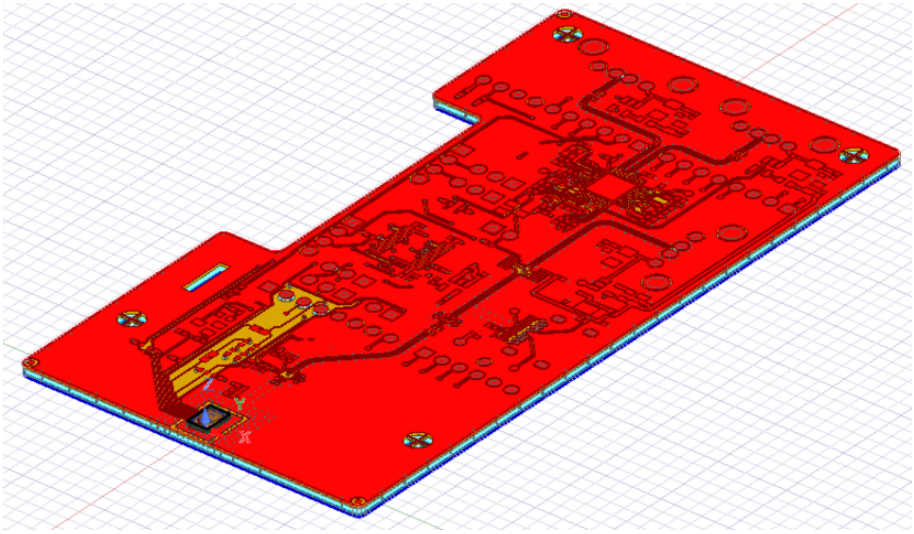


Figure 14. ST60A3H1 antenna matching to the die impedance presents the matching results of the LP AiP module, with defined excitation ports placed at ALUCAP PAD chip level with measured impedances set in the ports (probe measurements). The matching to the die impedance is acceptable for both TX and RX paths with limited mismatch losses. This matching is dependent on the PCB implementation.

Figure 14. ST60A3H1 antenna matching to the die impedance

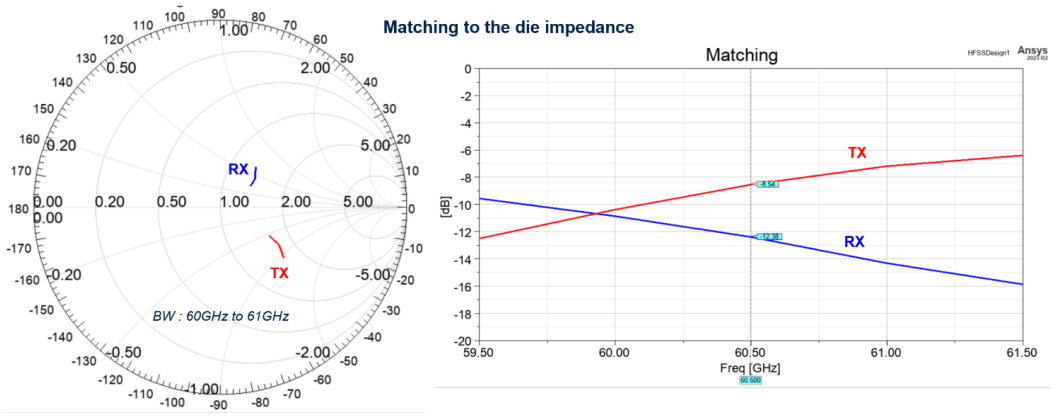
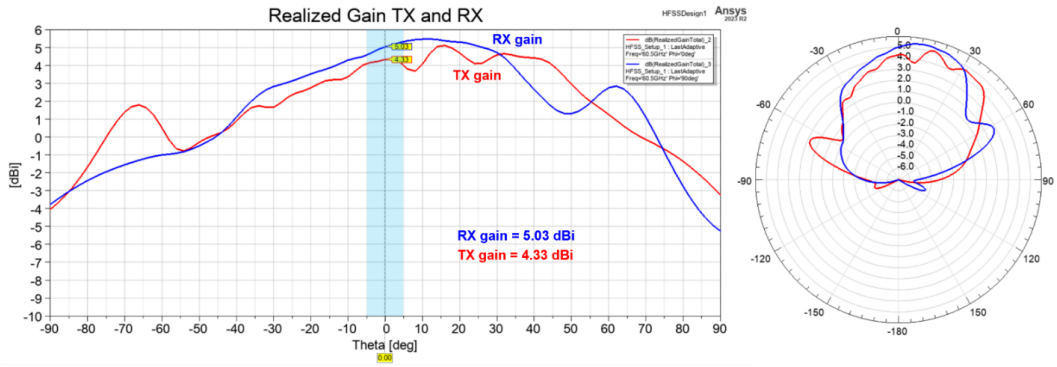


Figure 15. ST60A3H1 antenna TX and RX realized gain at 60.5 GHz below shows far-field realized gain results: θ = 0° is the targeted direction directly perpendicular to the center of the patch antenna of the LP AiP module. A good gain flatness from = θ -5° to θ = 5° is targeted along with a -3 dB gain bandwidth quite large to be able to tolerate some misalignment between both sides as well as manufacturing variations.

Figure 15. **ST60A3H1 antenna TX and RX realized gain at 60.5 GHz**



TX and RX realized gains are well balanced and no back lobe radiation is observed at θ = -180° (θ is the elevation and φ the azimuth).

2.1.2 End-to-end simulations

This section presents end-to-end simulation results with two boards facing each other, as shown in Figure 16. End-to-end simulation 3D model view with half boards.

This type of simulation allows us to predict the maximum achievable communication distance between these two boards and to see whether the RF communication channel is stable over distance (ripple vs. distance) or perturbed (reflections, refractions, etc.). It is mandatory to ensure that one board does not disturb the other and that they are functional together.

Figure 16. **End-to-end simulation 3D model view with half boards**

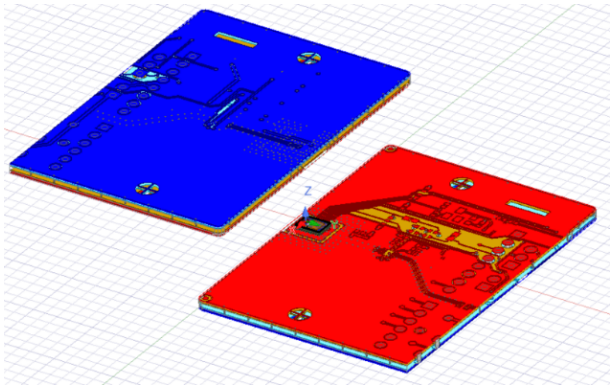
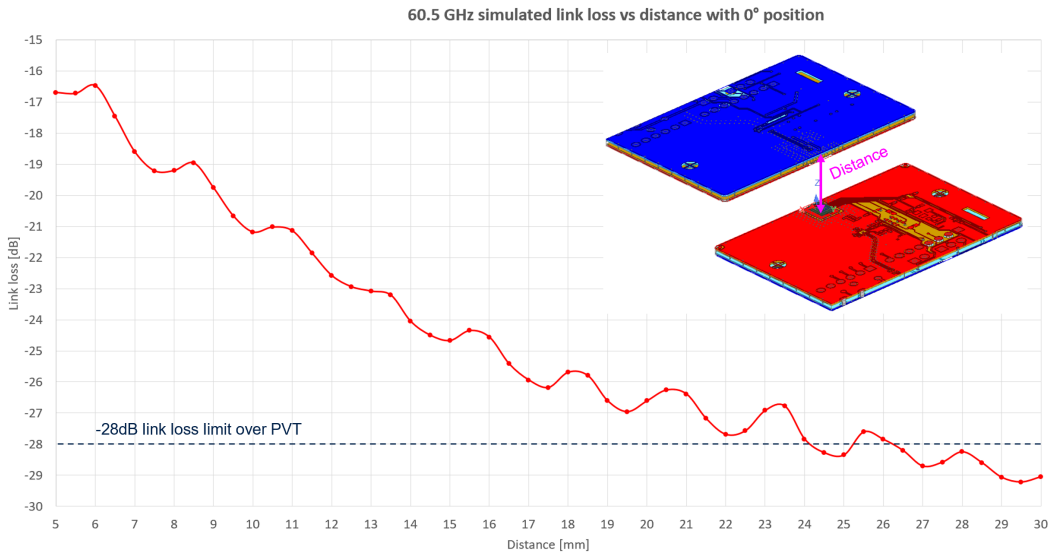


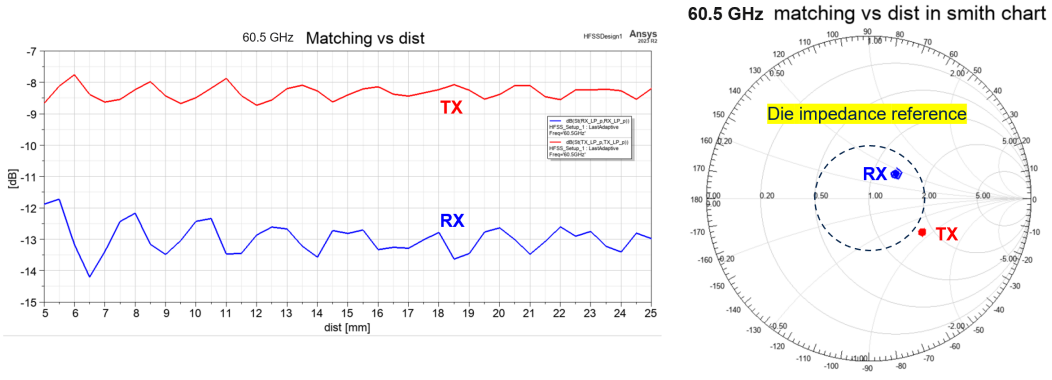
Figure 17. X-NUCLEO-60K1A1 60.5 GHz link loss vs. distance presents the 60.5 GHz link loss results vs. distance between the two LP AiP modules with 0.5 mm distance step with the two modules perfectly aligned. According to these results, the system should work up to 24 mm including PVT variations (see Section 2.2: Measurements for the measured value). Ripple vs. distance seems acceptable even if it is still visible (peak higher than 1 dB) due to the board shape and implementation with full ground planes around the LP AiP modules. This ripple vs. distance is expected to be higher in measurements due to this implementation and the half-board simplification in simulation.

Figure 17. **X-NUCLEO-60K1A1 60.5 GHz link loss vs. distance**



As shown in Figure 18. ST60A3H1 antenna matching to the die impedance in end-to-end configuration, the matching is stable vs. the distance between boards. The Smith chart also shows that TX and RX matching impedance is stable vs. the distance with the same positions.

Figure 18. **ST60A3H1 antenna matching to the die impedance in end-to-end configuration**



Thanks to other metrics, the far-field seems to be established from around 15 mm.

2.2 Measurements

2.2.1 Standalone measurements

The antenna radiation pattern is measured on an X-NUCLEO-60L1A1 board in nominal voltage and temperature conditions. The measurement is done using a 6-axes robot handling a horn test antenna which is connected to a spectrum analyzer. Facing this antenna is the X-NUCLEO-60L1A1 board which is positioned on a rotative platform. The robot combined with the rotative platform allows the measurement to cover the half sphere above the ST60A3H1 package. The distance between the ST60A3H1 package and the test antenna is kept constant at 10 cm for each measurement point to be in the far-field zone.

Some zones of the half sphere are excluded from the measurement because of mechanical constraints.

The ST60A3H1 is configured to output a CW (continuous wave) and the spectrum analyzer measures the received power. The reported values are EIRP (effective isotropic radiated power) de-embedded on the ST60A3H1 antenna plan.

The EIRP 3D pattern is shown in Figure 19. X-NUCLEO-60L1A1 EIRP 3D pattern. An ST60A3H1 die CW output power of 3.5 dBm is targeted during the trimming step but with a limited accuracy EIRP (Effective Isotropic Radiated Power) of at least ±1 dB and even more considering the impedance variation in this specific configuration. Given the previous elements, the TX gain can be deduced from EIRP measurement to be between 1.6 and 3.6 dBi compared to 4.3 dBi in simulation, which is quite coherent especially for only one sample measured.

Figure 19. X-NUCLEO-60L1A1 EIRP 3D pattern

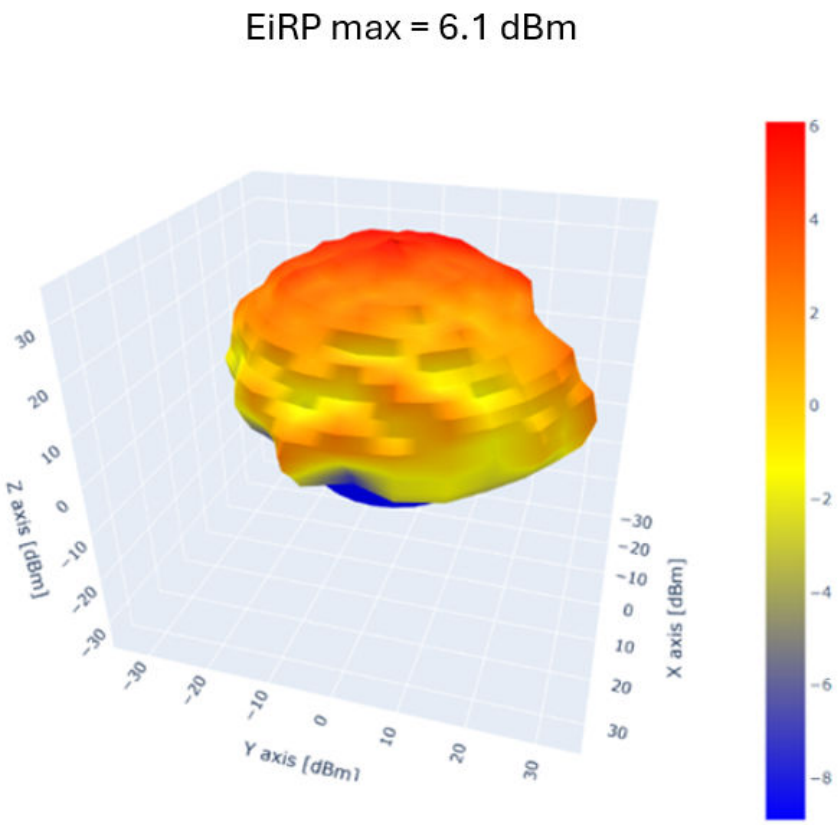
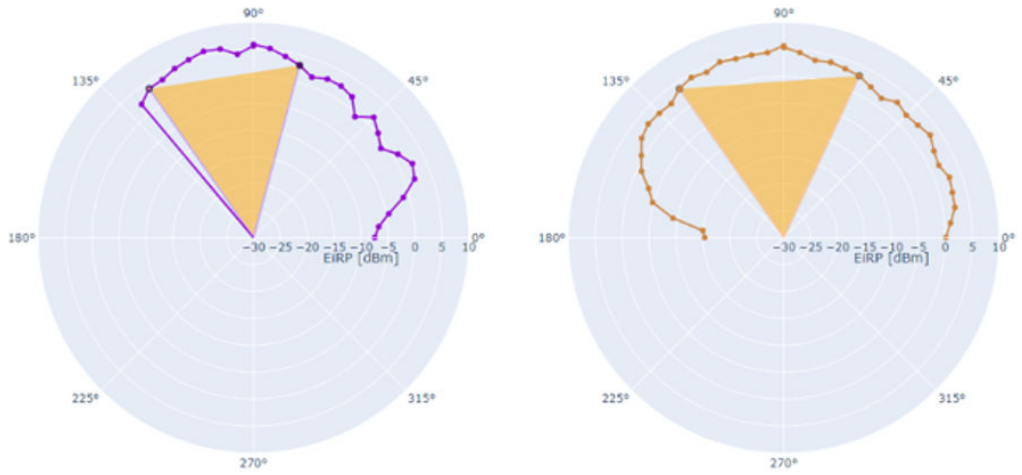


Figure 20. X-NUCLEO-60L1A1 EIRP 2D pattern shows two 2D cuts (EIRP vs. elevation) of the 3D pattern for azimuths of 0° and 90°.

Figure 20. **X-NUCLEO-60L1A1 EIRP 2D pattern**



Azimuth = 0° Azimuth = 90°

2.2.2 End-to-end measurements

RF performance of the X-NUCLEO-60K1A1 has been evaluated in free-space and typical operating conditions (room temperature, nominal supply voltage, etc.). CW RSSI has been recorded as a function of the RF gap between the two ST60A3H1 devices. Several kit samples have been tested.

Figure 21. **CW RSSI as a function of RF gap**

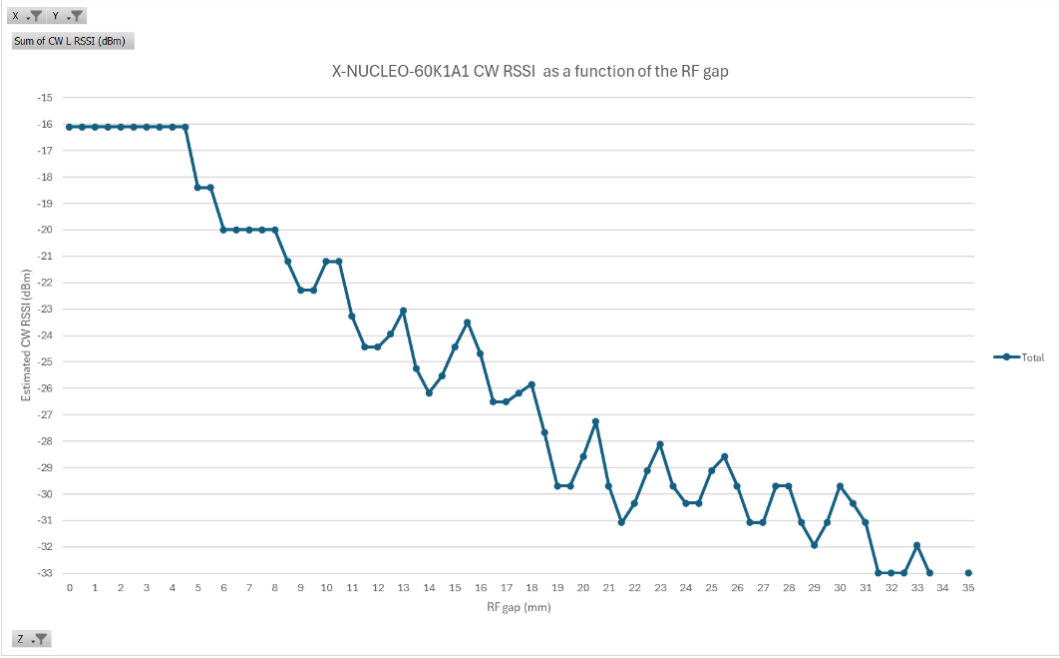


Figure 21. CW RSSI as a function of RF gap above shows the result of one sample. It can been seen that the RF link is established with the X-NUCLEO-60K1A1 in free space with an estimated CW RSSI higher than -32.5 dBm (ST60A3H1 typical sensitivity value for eUSB2 total jitter smaller than 212 ps) for RF gaps up to around 30 mm. An estimation of the free space performance over consumer temperature range, supply voltage range, and silicon process dispersion is given for a CW RSSI higher than -26.5 dBm which corresponds to a maximum RF gap of 16 mm.

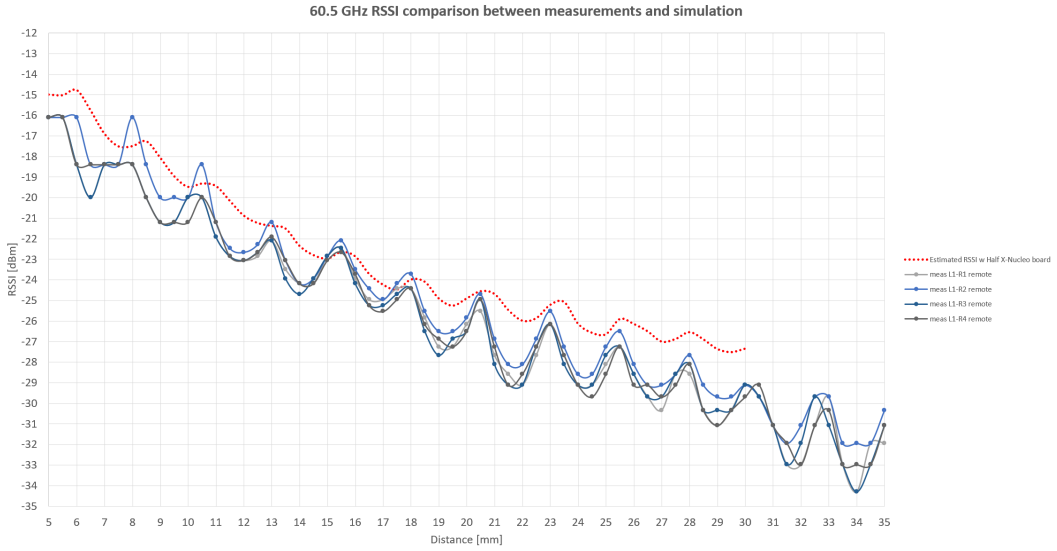
Note that all these distances are estimates based on a single kit sample's results obtained with the ST60A3H1's RSSI indicator which has a low accuracy, as can be seen in the ST60A3H1 datasheet. These various inaccuracy sources easily explain the difference between the simulation and measurement maximum RF gap estimations.

We can also note the high ripple on the RSSI vs. distance which is due to the "worst common PCB implementation" used (not respecting the guidelines) and is, as expected, higher than the one simulated. The consequence is a reduction of the maximum achievable communication distance.

Users must run dedicated qualification tests on the X-NUCLEO-60K1A1 kit or their own hardware (over targeted operating conditions and on several hardware samples) to ensure the product works well over their targeted RF channel. If users target a higher range than that achieved by the X-NUCLEO-60K1A1, then they must use a more recommended implementation with a specific board shape that reduces the link loss ripple.

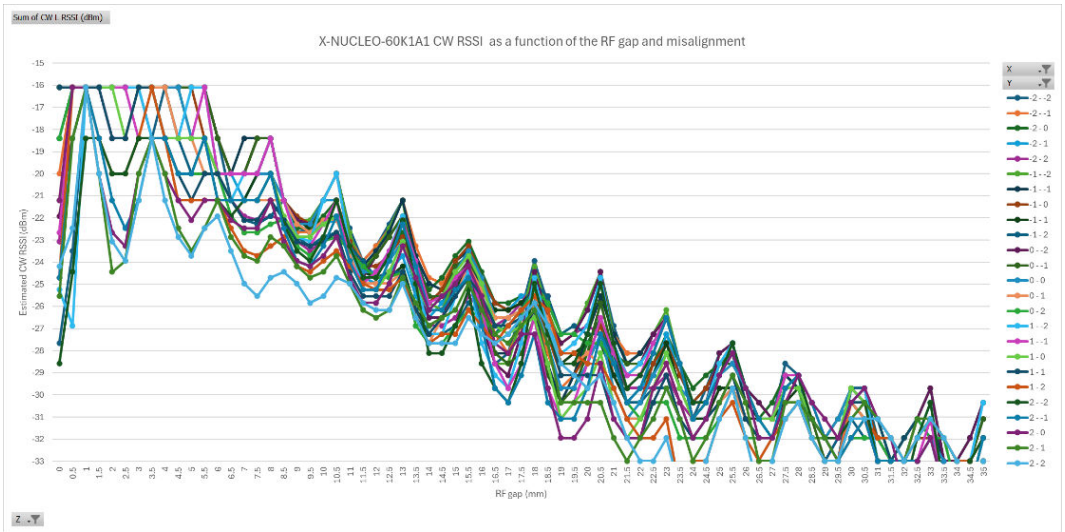
Figure 22. 60.5 GHz RSSI comparison between measurements and simulation shows the comparison between an estimated RSSI (using the link loss simulation and an estimation of the output power at die level) and RSSI measurements done on 4 different samples (R1, R2, R3, and R4). Using the previous EIRP measurement and the simulated gain, the die output power was estimated around 1.7 dBm (instead of the 3.5 dBm target).

Figure 22. 60.5 GHz RSSI comparison between measurements and simulation



An RSSI vs. RF gap test was also performed while adding some scalar misalignment between the two ST60A3H1 devices. Figure 23. CW RSSI as a function of RF gap and misalignment shows that with a ± 2 mm maximum misalignment in both axes, the CW RSSI remains above -32.5 dBm for an RF gap up to 21 mm in typical operating conditions. Considering -26.5 dBm as the PVT threshold, the estimated functional range over PVT would be between 1 mm and 13.5 mm, always with ± 2 mm maximum misalignment in both axes.

Figure 23. **CW RSSI as a function of RF gap and misalignment**



2.3 Additional considerations

The previous sections show the simulated and measured free-space RF performances of the X-NUCLEO-60K1A1 board in typical operation conditions. Such performances do vary according to the channel between the ST60A3H1 devices and the whole 3D environment as well as the operating conditions. Metrics such as link loss and antenna VSWR (voltage standing wave ratio) are heavily impacted by:

- Temperature and voltage which have an impact on the ST60A3H1's intrinsic performance.
- Board size and topology: Moving the antenna away from the board as advised is a plus.
- Linear and/or angular (tilt) misalignment between the two ST60A3H1 devices.
- Number of ST60A3H1 pairs in the application.
- Air gap distance (near-field or far-field zone).
- Casing:
  - Number (1 or 2).
  - Thickness: Consider the thickness compared to the RF signal wavelength inside the casing.
  - Material (dielectric constant value [Dk] and loss tangent value [Df]).
  - When two casings are present, whether both have the same Dk or not could make a significant difference.
  - If a metal casing is used, then a hole must be created in it to allow the 60 GHz radiation, and this hole's size has an impact on the radiation and end-to-end performance.
  - Distance between the casings (air gap).
  - Distance between each ST60A3H1 and its casing.

Users are invited to use the X-NUCLEO-60K1A1 to evaluate the range they could expect in their targeted operating conditions (RF channel, casing, alignment tolerances, operating temperature).

2.3.1 Performance examples with casings

Depending on their EM properties, dimensions, and distance to the ST60A3H1 devices, the casings affect the way the EM waves propagate creating an impact on the minimum and maximum supported range as well as on the maximum supported misalignment.

As explained above, users must perform their own evaluation considering their casing specification (material, dimensions, etc.) constraints.

The examples in this section show the impact of inserting two PLA casings in the RF channel between the Local and Remote X-NUCLEO boards, with variable casing thicknesses and distances to the ST60A3H1 device package.

Figure 24. Impact of casing-to-package distance on CW RSSI (PLA casing with 0.5 mm thickness)

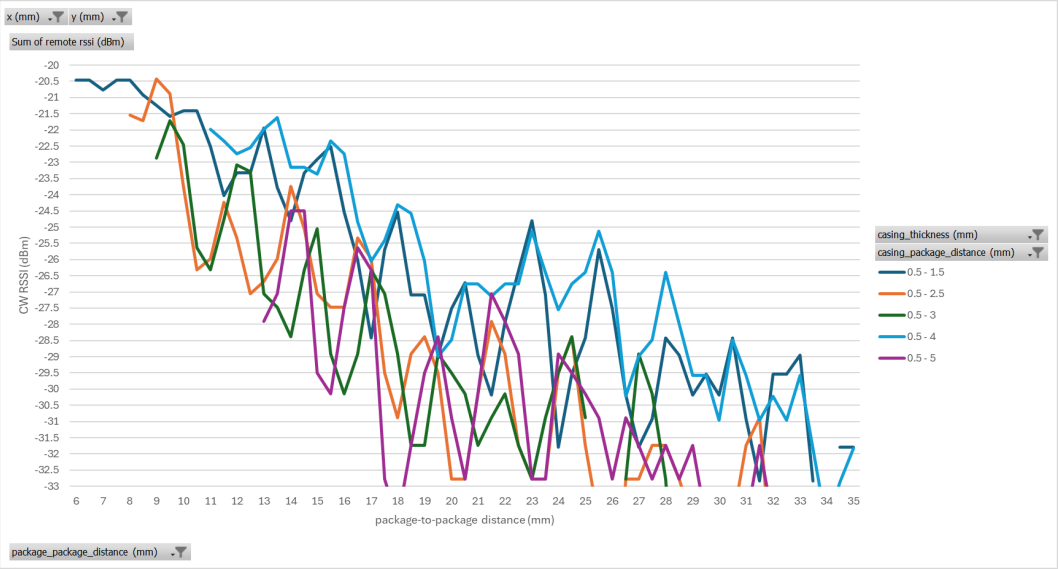


Figure 25. Impact of casing-to-package distance on CW RSSI (PLA casing with 1.5 mm thickness)

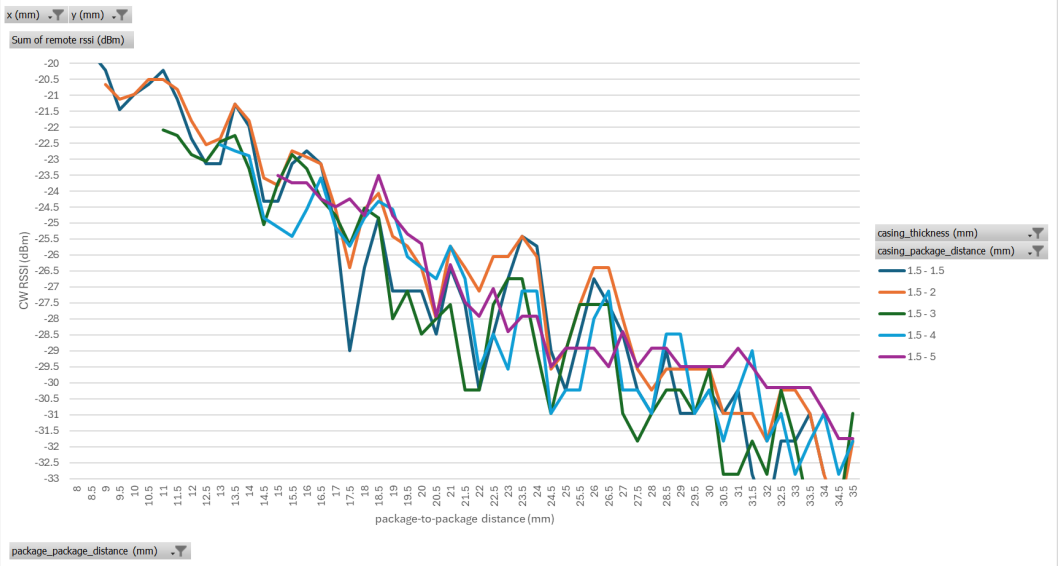


Figure 26. Impact of casing thickness on CW RSSI (PLA casing with 1.5 mm casing-to-package distance)

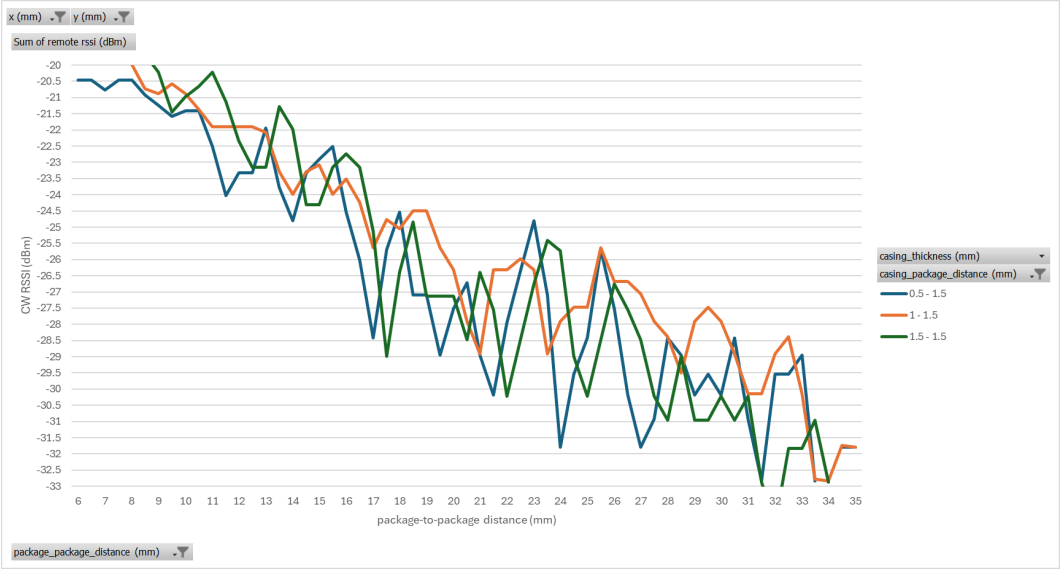
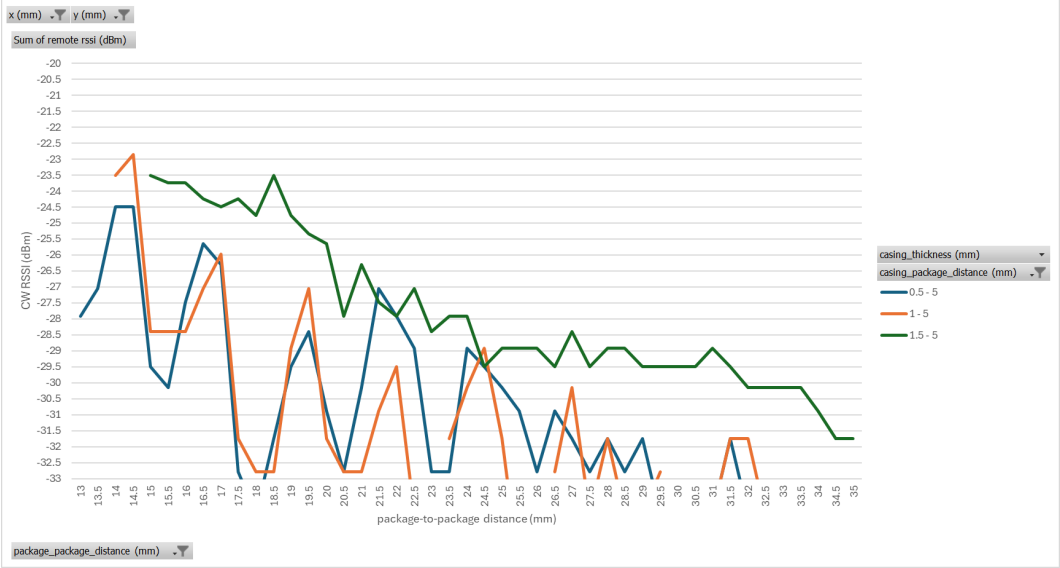


Figure 27. Impact of casing thickness on CW RSSI (PLA casing with 5 mm casing-to-package distance)



3 Schematics recommendation

The recommendations below must be read in conjunction with Section 3.1: Schematic diagrams and all the related documentation.

3.1 Schematic diagrams

Figure 28. **X-NUCLEO-60L1A1 circuit schematic (1 of 4) - ST60A3H1**

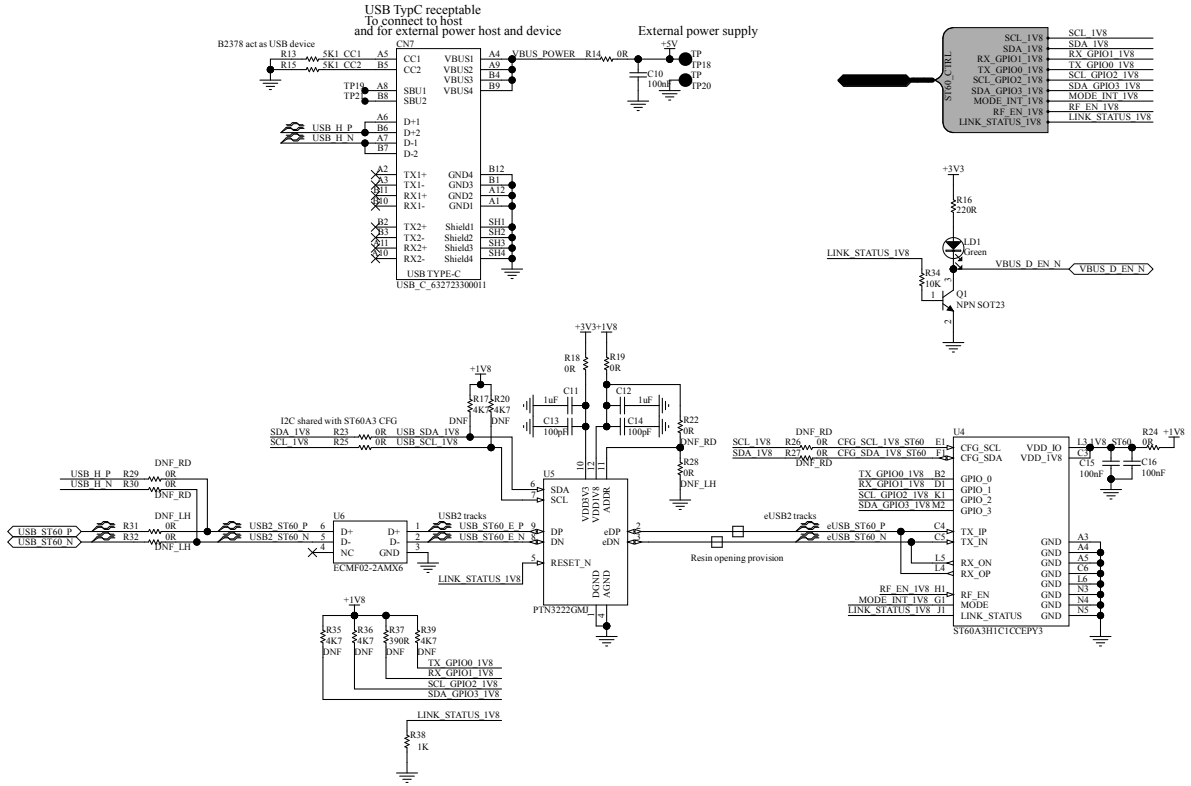


Figure 29. X-NUCLEO-60L1A1 circuit schematic (2 of 4) - Nucleo

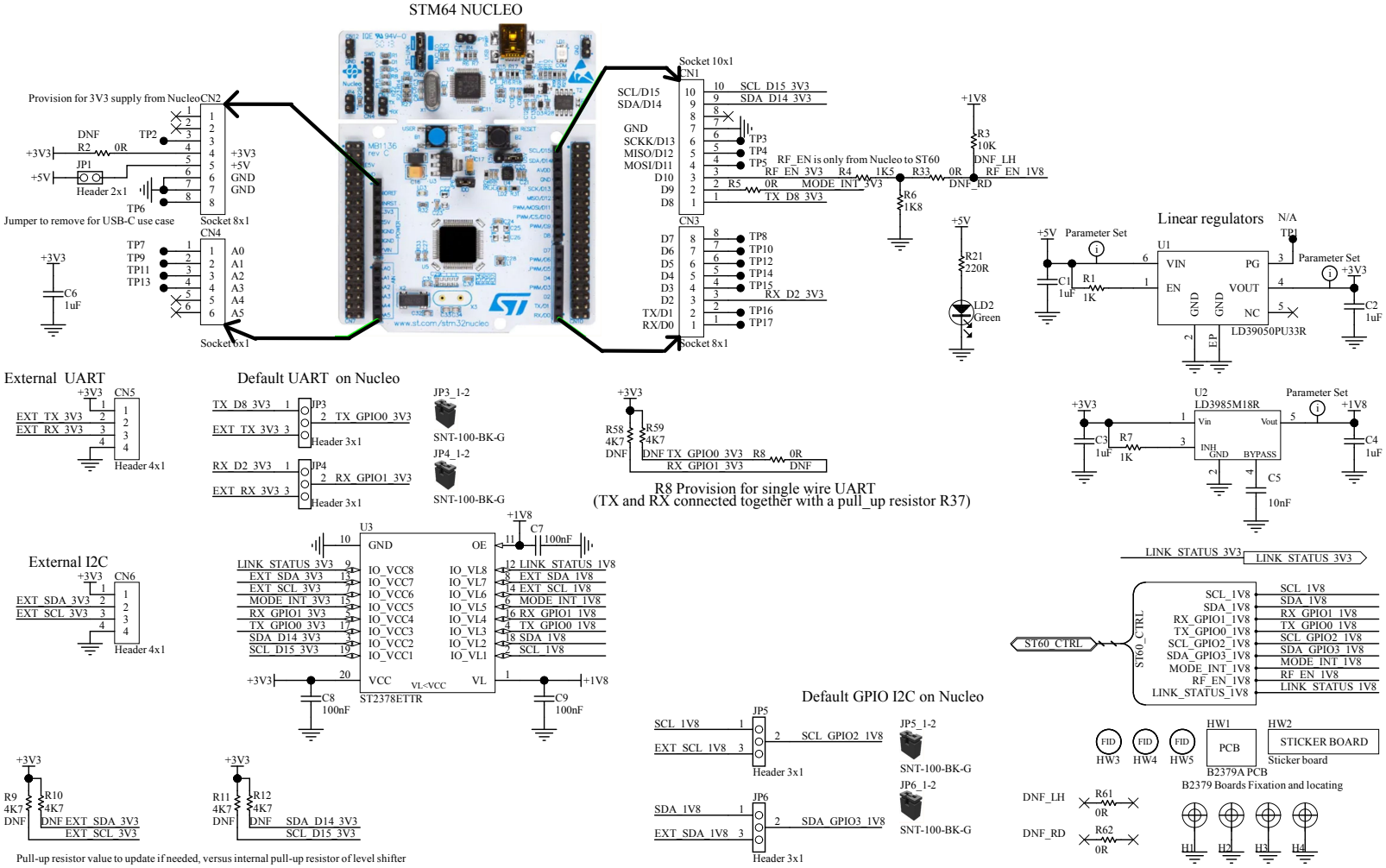


Figure 30. X-NUCLEO-60L1A1 circuit schematic (3 of 4) - Switch

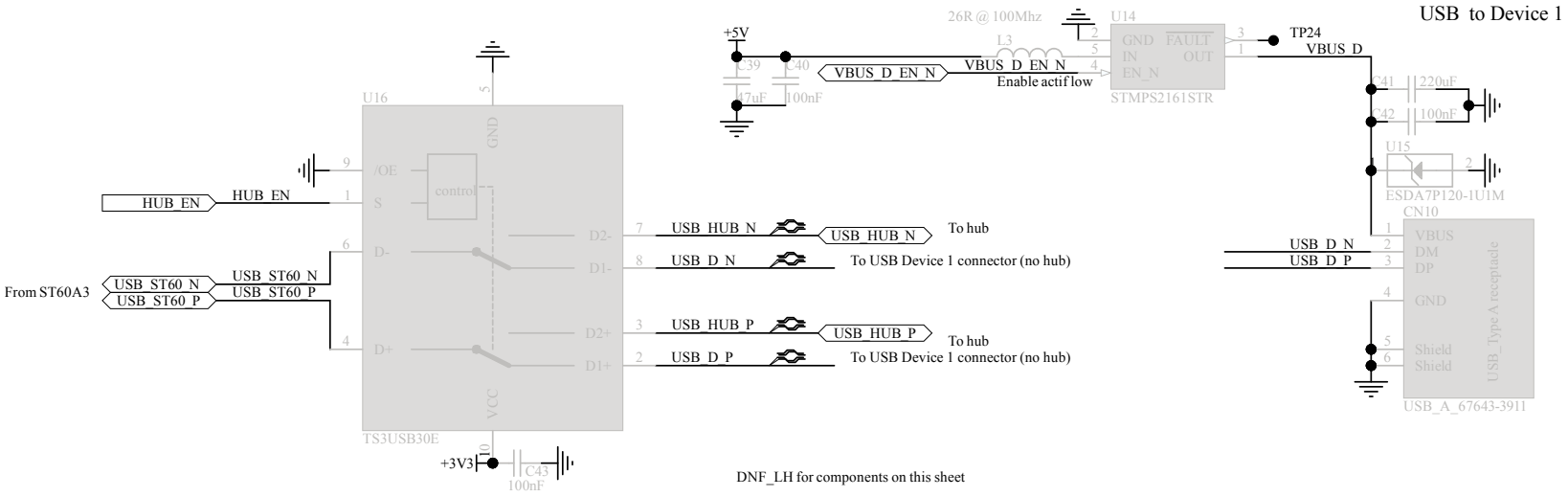


Figure 31. X-NUCLEO-60L1A1 circuit schematic (4 of 4) - Hub

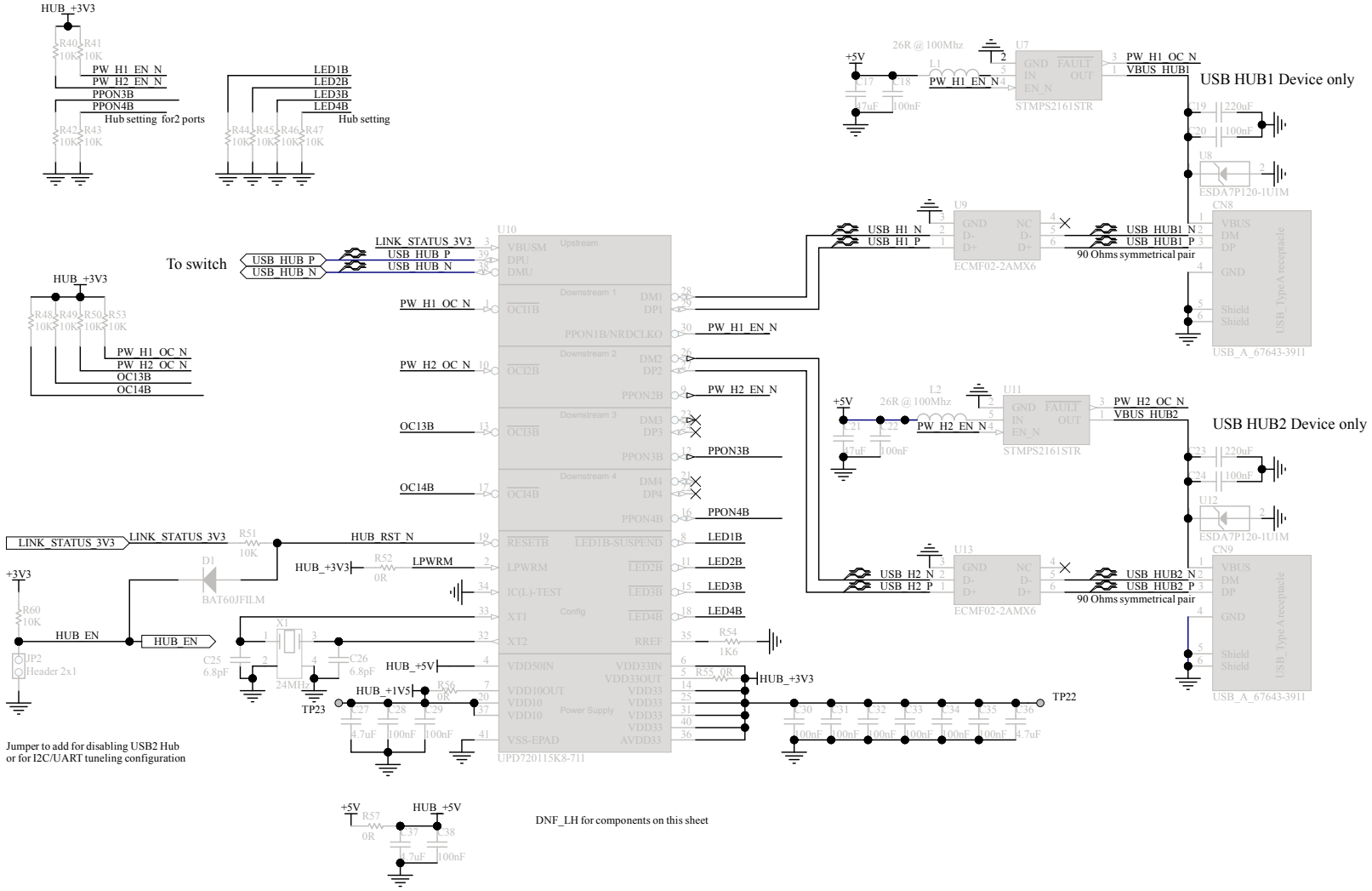


Figure 32. X-NUCLEO-60R1A1 circuit schematic (1 of 4) - ST60A3H1

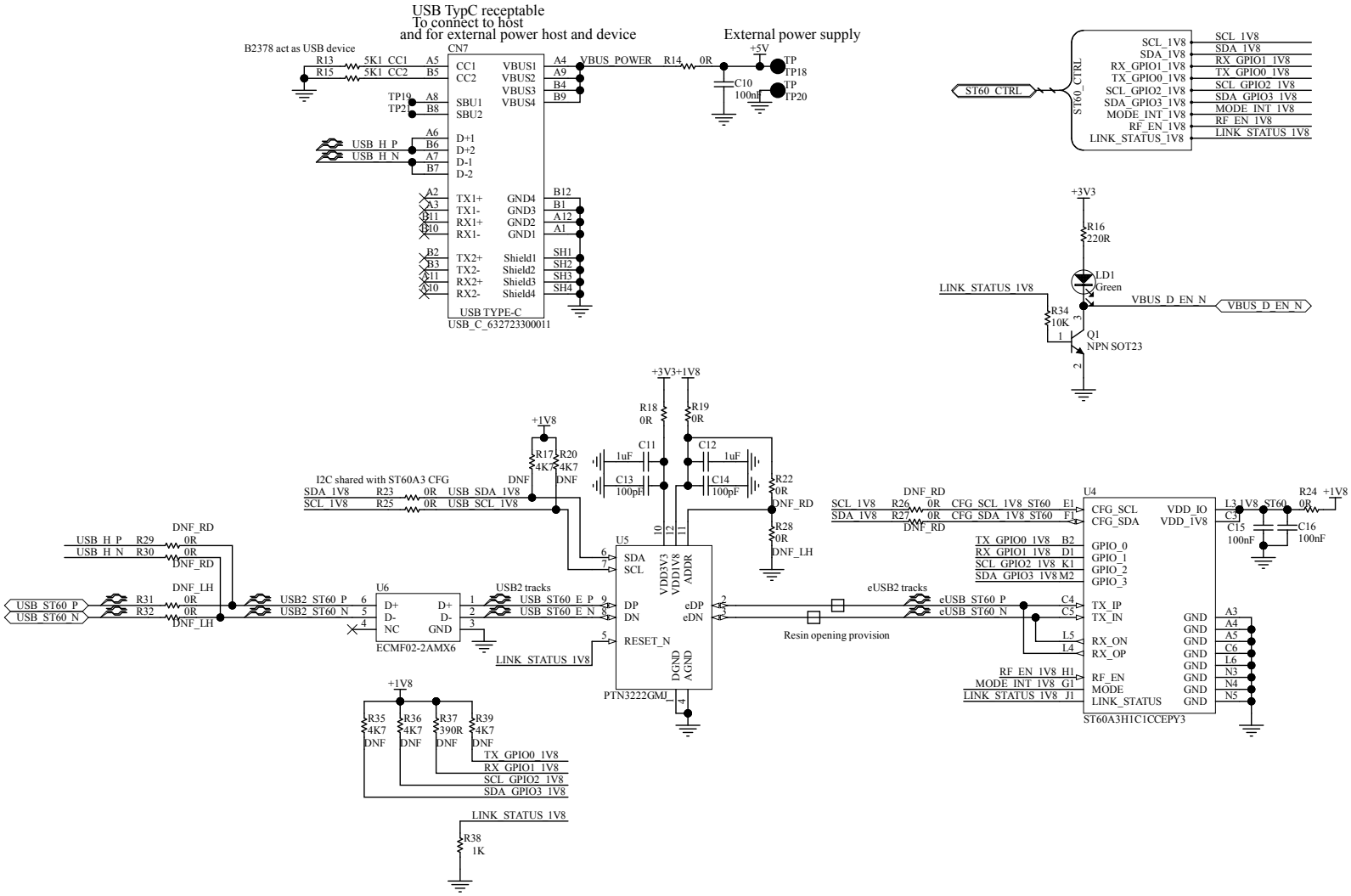


Figure 33. **X-NUCLEO-60R1A1 circuit schematic (2 of 4) - Nucleo**

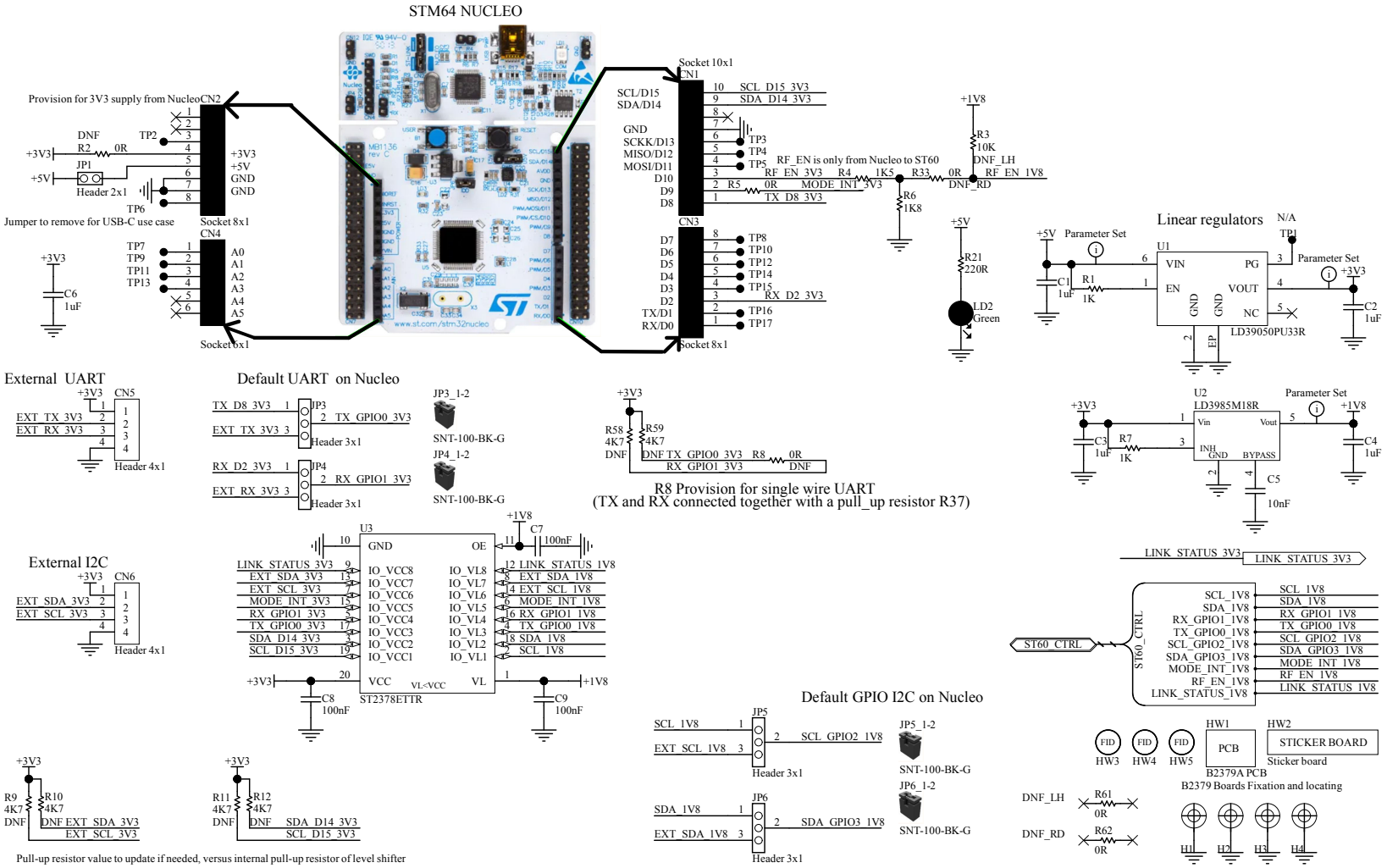
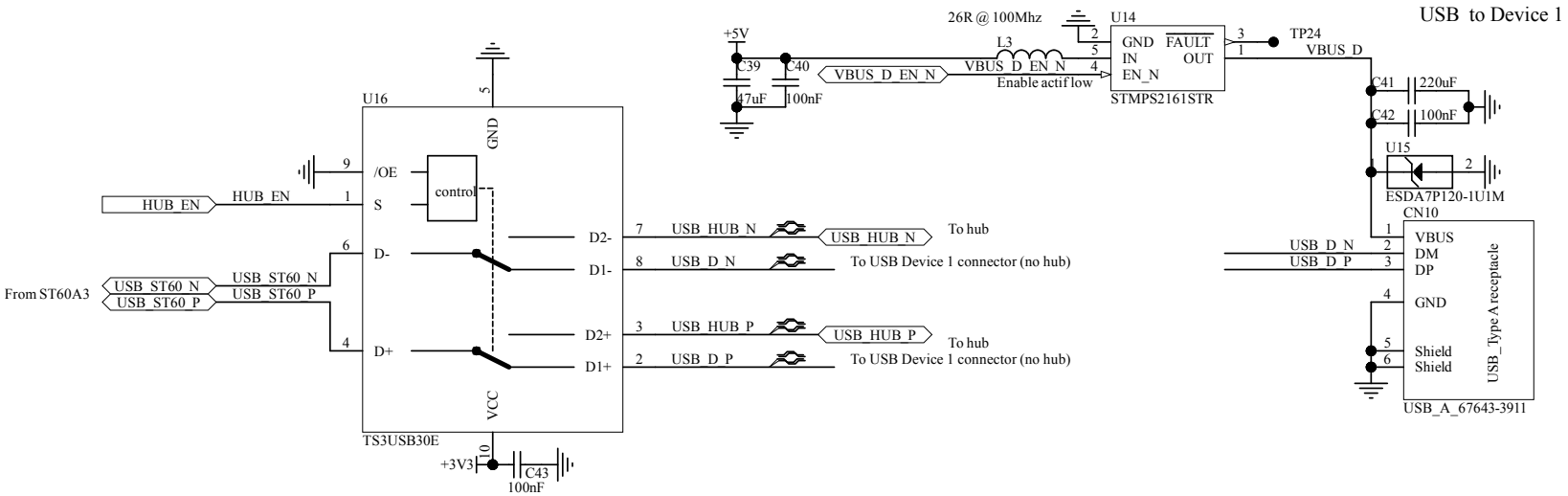
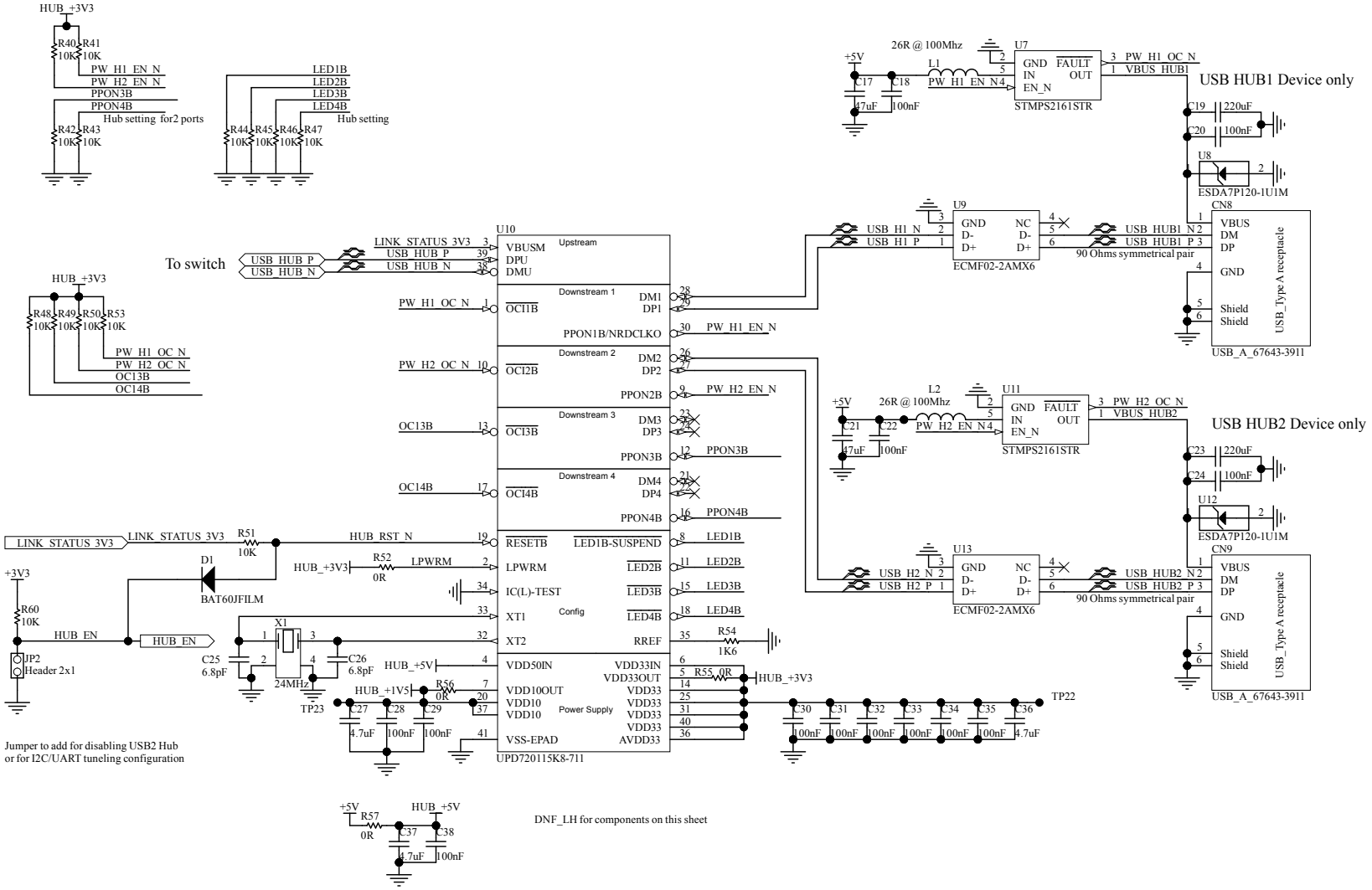


Figure 34. X-NUCLEO-60R1A1 circuit schematic (3 of 4) - Switch



DNF_LH for components on this sheet

Figure 35. X-NUCLEO-60R1A1 circuit schematic (4 of 4) - Hub



3.2 Power supplies

3.2.1 GND (A3, A4, A5, C6, L6, N3, N4, and N5)

They must be connected to the board ground.

3.2.2 VDD_IO (L3) and VDD_1V8 (C3)

They must be shorted together and connected to the 1.8 V power supply. A minimum of two 100 nF bypass capacitors must be used.

An LDO or a buck can be used to generate this 1.8 V, ensuring a clean voltage with less than 120 mVpp ripple. The 1.8 V supply voltage must be within the 1.65 V to 1.95 V range. It is advised to select an LDO/buck with a current output that is ~30% higher than the total of maximum currents of all the devices supplied by this LDO/buck.

3.3 Configuration I^2C bus

A single I^2C controller is generally needed to control the pair of ST60A3H1 devices. It is placed on the Local ST60A3H1's side with a direct connection to its I^2C pins. The Remote ST60A3H1 is controlled by the same I^2C controller using Over-the-air programming through the Local ST60A3H1.

3.3.1 Local CFG_SCL (E1) and CFG_SDA (F1)

They must be pulled-up to 1.8 V and connected to the I^2C controller controlling the Local ST60A3H1. If the controller's I^2C IOs are not 1.8 V, bidirectional level shifters must be used.

It is possible to have other devices, including devices addressed through I^2C tunneling, on the same I^2C bus so long as none of the devices is at the Local ST60A3H1's I^2C address (0xC0) and the total load capacitance remains within the I^2C specification. The I^2C specification limits the bus capacitance to 400 pF in Standard mode, Fast mode, and Fast mode plus. For an only resistive pull-up, the maximum bus capacitance is limited to 200 pF.

The pull-up resistances must be tuned by the integrator depending on the maximum I^2C speed that is targeted and the bus topology. The pull-up resistor value (Rp) depends on the I/O supply voltage (1.8 V on the ST60A3H1 side) and the I^2C bus capacitance (Cb). It must be in a range defined by the following two equations from the I^2C specification:

- $Rp(max) = t_r / (0.8473 \times Cb)$
- $Rp(min) = (1.8\ V - V_{OL}\ (max)) / I_{OL}$

Where t_r is the rise time of SDA and SCL signals, and V_{OL} and I_{OL} are the output low voltage and output current, respectively, defined in the ST60A3H1 documentation.

3.3.1.1 eUSB2 tunneling use-case

The I^2C controller must be connected to the eUSB2/USB2 repeater which must be configured in I^2C mode. This is needed for RF regulation tests.

3.3.2 Remote CFG_SCL (E1) and CFG_SDA (F1)

They can be left unconnected.

In rare cases where a customer application necessitates having a direct I^2C connection to the Remote ST60A3H1, the Local side rule must be applied to the Remote side too.

3.4 RF enable

3.4.1 Local RF_EN (H1)

It must be directly connected to the MCU or the AP controlling it. If this MCU/AP's IO is not 1.8 V then a level shifter or divider bridge must be used. It is important for the application to be able to enable or disable the RF of the Local ST60A3H1 to save power consumption and to be ready for RF regulation tests.

3.4.2 Remote RF_EN (H1)

It can be connected to 1.8 V or connected to a controlling MCU/AP in the same way as the Local.

3.5 Interrupt signal

3.5.1 Local MODE_INT (G1)

It must be connected to an interrupt input pin of the MCU/AP controlling the Local ST60A3H1. This interruption signal is then used by the ST60A3H1 driver. A level shifter may be needed if the interfaces are not all 1.8 V.

3.5.2 Remote MODE_INT (G1)

It can be left open or connected to wherever it may be needed by the user application. A level shifter may be needed if the interfaces are not all 1.8 V.

3.6 LINK_STATUS (J1)

LINK_STATUS (J1) indicates the status of the RF link. It can be left open, connected to an LED, or to the MCU/AP if the RF link status is supposed to trigger some action. A level shifter may be needed if the interfaces are not all 1.8 V.

3.6.1 eUSB2 tunneling use-case

It is necessary to notify the system application of any RF link loss to ensure a reliable USB2 link recovery. This is done using the LINK_STATUS (J1) signal which must be connected in a way to perform the following:

- Reset the eUSB/USB2 repeaters on both Host and Device sides before re-establishing the USB2 link after the RF link is enabled.
- Disable the VBUS of the USB2 Device if it has one.
- Reset the USB2 Device (PHY and controller by software means) if it does not use a VBUS.
- Disable the VBUS and reset any hub IC that would be on the board.

Doing the above also helps reduce the overall system power consumption when the RF link is disabled.

On the Local ST60A3H1's side, it is preferred for the sake of flexibility to have the LINK_STATUS signal routed to the MCU where dedicated signals are created to control the USB2 features.

3.7 eUSB2 bus

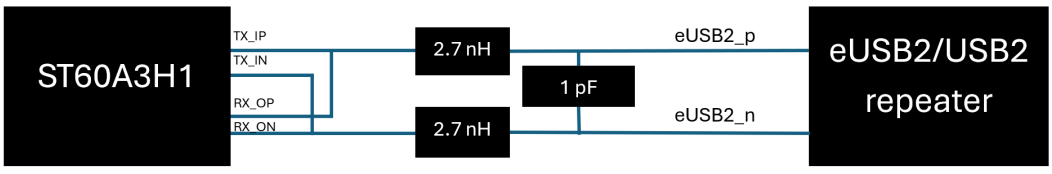
eUSB2 lanes (C4, C5, L4, and L5) can be left unconnected or tied to ground when not used.

If eUSB2 tunneling is desired, these lanes must be shorted together (C4 with L4, and C5 with L5) and connected to their corresponding eUSB2/USB2 repeater (see Section 1.2.4).

Shorting C4/C5 with L4/L5 respectively creates a stub on these lines which degrades their signal integrity (SI). The impact of this stub is sufficiently reduced due to a proper layout (see **eUSB2 bus** in Section 1.2.4), leading to a performing design.

Users who want to further improve SI (and slightly reduce the link jitter) could insert an LC circuit between the ST60A3 and the eUSB2/USB2 repeater as shown in Figure 36. LC circuit on eUSB2 lanes. In this case, ST recommends using 2.7 nH inductors and a1 pF capacitor with an estimated improvement of ~1 ps in random jitter (RJ). ST also advises users to run SI simulations to find the optimized values for their design.

Figure 36. LC circuit on eUSB2 lanes



3.8 GPIOs

If any of the GPIOs (B2, D1, K1, and M2) are unused, then they can be left unconnected, otherwise, their connection depends on the targeted application (tunneling protocol).

Besides being used in a tunneling protocol, the four GPIOs can be alternatively used as general-purpose I/O pins, the value of which can be written or read by an I^2C register access or through RRA (in LOW_POWER state).

3.8.1 Single-wire half-duplex UART tunneling

GPIO_0 (B2) and GPIO_1 (D1) must be shorted together, pulled-up to 1.8 V, and connected to the TXD pin of the UART source or sink. The pull-up value (Rp) must be tuned vs. the targeted data rate keeping in mind the items below:

- It must be such that the input pin of the UART reads a high state when not driven by the ST60A3H1. The rise time of the signal depends on the RC circuit made of the pull-up resistor and the capacitive load of the UART line. The value of the resistor is a trade-off between the targeted data rate and the current driven at a low level. It can be fine-tuned to optimize the amount of current flowing from 1.8 V when the pin is driven low.
- As GPIO_0 and GPIO_1 are connected together, when the ST60A3H1 receives a transition to perform on its GPIO_1 output line, it masks its GPIO_0 input line so that it does not retransfer this received transition. This masking period is around 50 ns and the signal must reach its new level within this period. This implies having a steep edge or, in other words, decreasing Rp value. As the longest transition is from low level to high level, the masking period begins at the start of the rising edge of the GPIO_1 RX signal and ends when the signal level on GPIO_0 TX reaches V_{IH} (input high voltage defined in the ST60A3H1 documentation).

Level shifters may be needed if the interfaces are not all 1.8 V and, in such cases, the short between GPIO_0 and GPIO_1 must be done on the ST60A3H1 side. This avoids any additional delay between the RX and the TX signals, with respect to the above masking period.

3.8.2 Dual-wire half-duplex UART, full-duplex UART or bidirectional GPIO tunneling

GPIO_0 (B2) must be connected to the TXD pin of the UART source or sink or to the GPIO's source. This signal is an input to the ST60A3H1. A pull-up to 1.8 V must be added in case the source or sink's TXD is configured in open-drain mode.

GPIO_1 (D1) must be connected to the RXD pin of the UART source or sink or to the GPIO's sink. This signal is an output from the ST60A3H1.

Level shifters may be needed if the interfaces are not all 1.8 V.

3.8.3 Single-direction GPIO tunneling

GPIO_0 (B2) must be connected to the GPIO source's first TXD line or GPIO sink's first RXD line.

GPIO_1 (D1) must be connected to the GPIO source's second TXD line or GPIO sink's second RXD line.

Level shifters may be needed if the interfaces are not all 1.8 V.

3.8.4 I²C tunneling on GPIO_0/1

GPIO_0 (B2) must be pulled up to 1.8 V and connected to the I^2C controller or target(s)' SCL. GPIO_1 (D1) must be pulled up to 1.8 V and connected to the I^2C controller or target(s)' SDA. Refer to Section 3.3.1: Local CFG_SCL (E1) and CFG_SDA (F1) for more details on the pull-ups value selection and on multi-target operation.

Level shifters may be needed if the interfaces are not all 1.8 V. The pull-up resistors must be tuned by the integrator depending on the maximum I^2C speed that is targeted.

3.8.5 I²C tunneling on GPIO_2/3

GPIO_2 (K1) must be pulled up to 1.8 V and connected to the I^2C controller or target(s)' SCL. GPIO_3 (M2) must be pulled up to 1.8 V and connected to the I^2C controller or target SDA. Refer to Section 3.3.1: Local CFG_SCL (E1) and CFG_SDA (F1) for more details on the pull-ups value selection and on multi-target operation.

Level shifters may be needed if the interfaces are not all 1.8 V. The pull-up resistors must be tuned by the integrator depending on the maximum I^2C speed that is targeted.

3.9 Forbidden boot configuration

In all the cases described above, users must ensure that CFG_SCL, CFG_SDA, LINK_STATUS, MODE_INT, and the four GPIOs are not all set to 1 L (1.8 V) at IC power-up as this is a forbidden configuration. There are many possible solutions to do so:

- Keep MODE_INT and/or LINK_STATUS unconnected. The internal pull-downs on these two pins ensure that it is set to 0L (0 V) during power-up.
- Connect MODE_INT and LINK_STATUS as constrained by the application but make sure one of them bears 0 V during the ST60A3H1 power-up.
- Pull down any one of the GPIOs, preferably GPIO_2 or GPIO_3.

4 Typical application schematics

In this chapter, typical schematics with the minimum required components are shown for each tunneling protocol.

Figure 37. eUSB2 tunneling (USB2 Host on Local ST60A3 side)

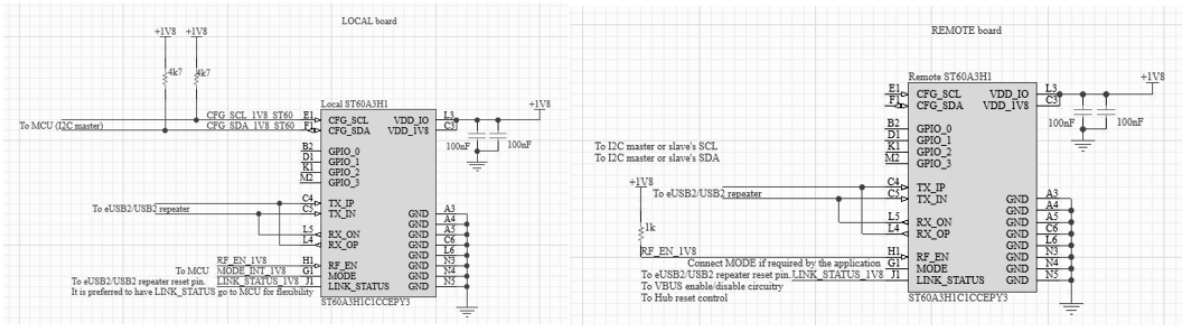


Figure 38. eUSB2 tunneling (USB2 Host on Remote ST60A3 side)

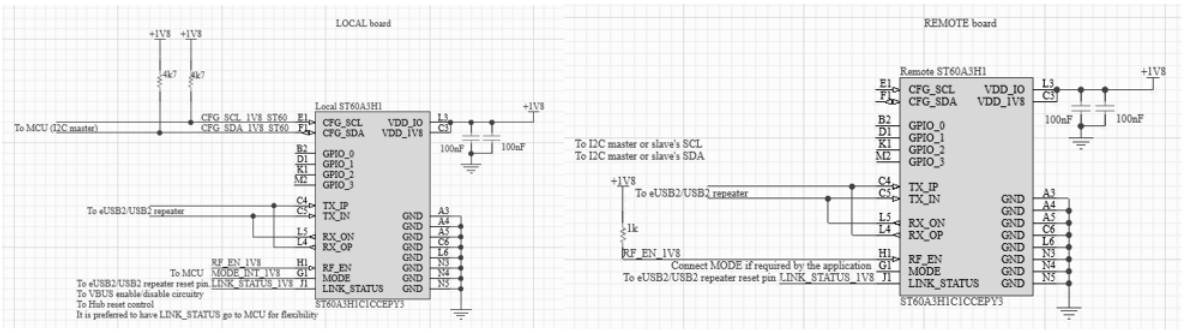


Figure 39. Single-wire half-duplex UART tunneling

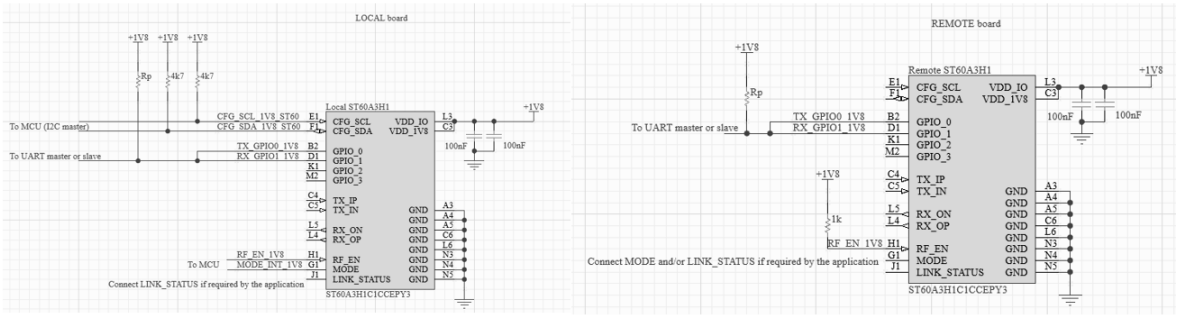


Figure 40. **Dual-wire half-duplex UART or full-duplex UART tunneling**

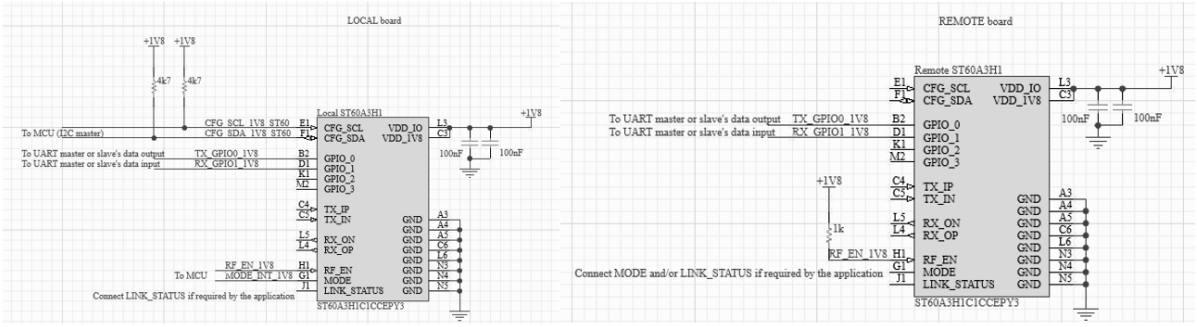


Figure 41. **Bidirectional GPIO tunneling**

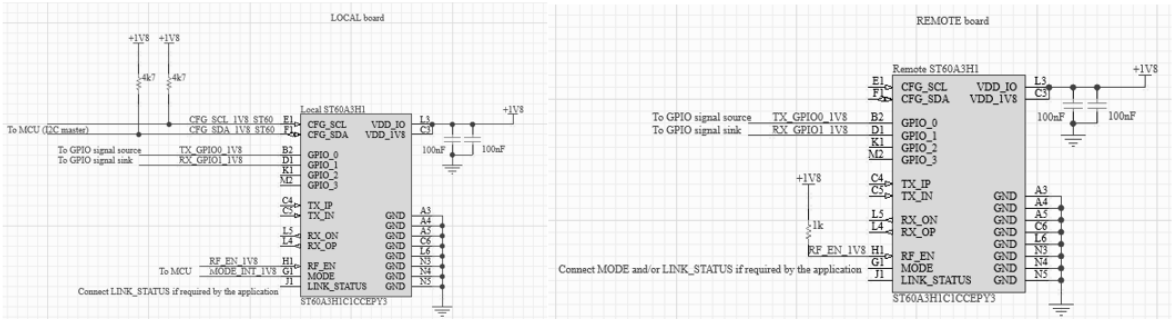


Figure 42. **Single-direction GPIO tunneling**

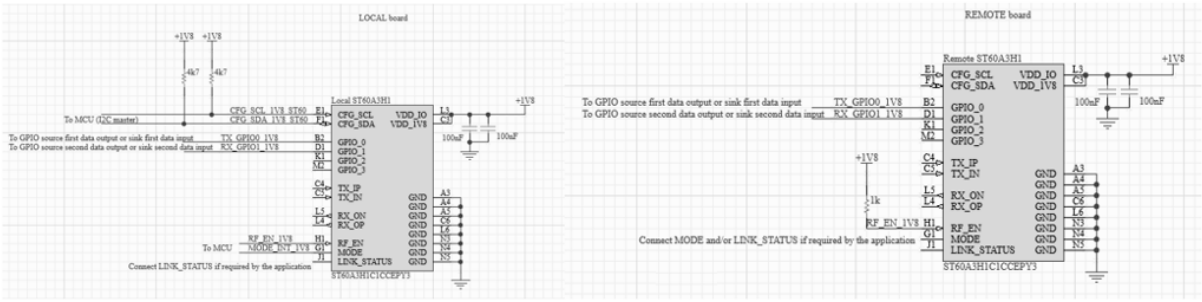
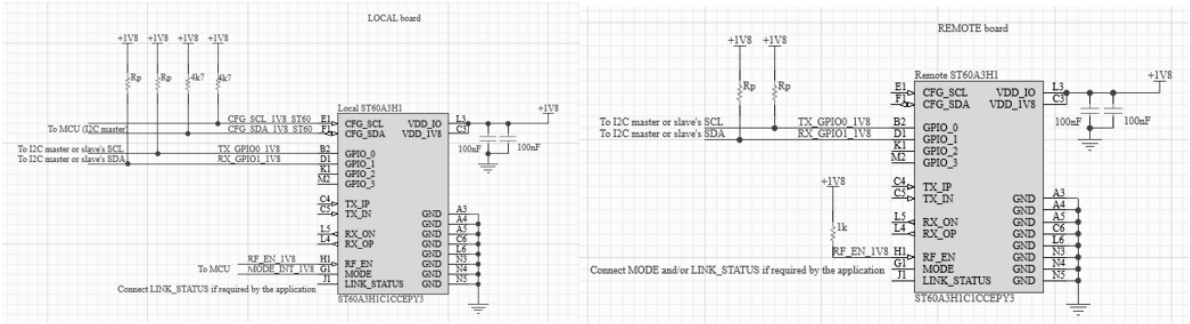
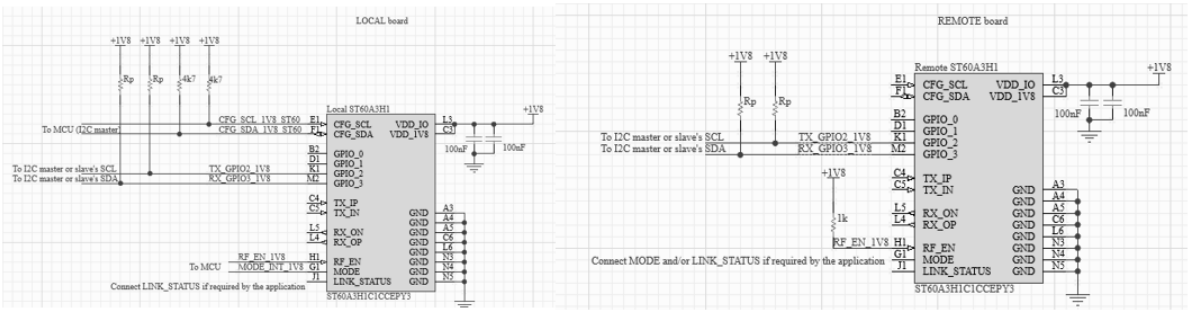


Figure 43. **I²C tunneling on GPIO_0 and GPIO_1**



Note: It is possible to have the tunneled I²C signal on GPIO0/1 on the Local side and on GPIO2/3 on the Remote side, and vice versa.

Figure 44. I²C tunneling on GPIO_2 and GPIO_3



Note: It is possible to have the tunneled I²C signal on GPIO0/1 on the Local side and on GPIO2/3 on the Remote side, and vice versa.

Revision history

Table 1. **Document revision history**

Date	Revision	Changes
06-Apr-2025	1	Initial release.
16-Oct-2025	2	Updated Section 1.2.4: ST60A3H1 routing and Section 3.7: eUSB2 bus. Added Section 2.3.1: Performance examples with casings and Section 4: Typical application schematics. Minor text changes.

Contents

List of figures