STPMIC25: how to connect unused PINs

1. How to connect unused PINs

In some STPMIC25 + Panther applications, not all the peripherals and functions may be required, and to minimize any possible issues and useless power consumption, the relative pins must be connected correctly.

The following tables provide guidance on how to connect unused pins of the STPMIC25, and they are valid for all pins except V_{IN}, V_{IO}, and all GNDs.

Note 1: To avoid any damage to the STPMIC25, the V_{IN} must be the first and the highest input supply. VBUS input voltage can be applied before the V_{IN}.

Note 2: The DC-DC converter input pins (pins #20, #24, #25, #38, #39, #49, and #50) cannot be separated from the main input pin (pin #11).

Figure 1. Pin configuration WFQFN 56L top view

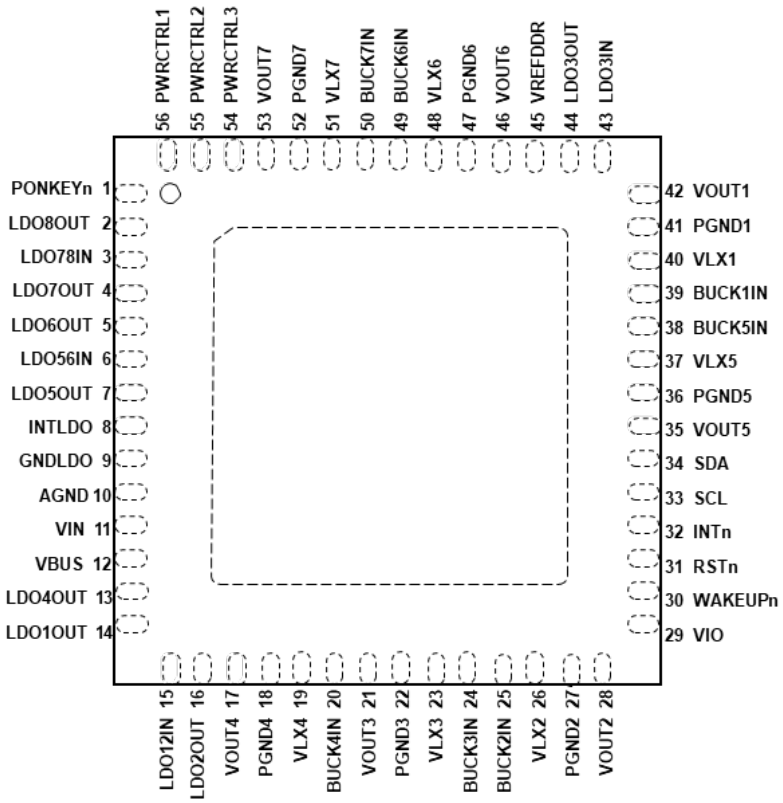

Table 1 shows the possible configuration of the STPMIC25 input/output digital pins if they are not used in the final application:

Table 1. STPMIC25 digital pin configuration

Pin number	Pin name	Type	If not used
1	PONKEYn	I	Floating
30	WAKEUPn	I	Floating
31	RSTn	I/O	Floating
32	INTn	O	Floating
33	SCL	I	VIO
34	SDA	I/O	VIO
54	PWRCTRL3	I	Floating
55	PWRCTRL2	I	Floating
56	PWRCTRL1	I	Floating

Table 1 shows the possible configuration of the STPMIC25 input/output analog pins if they are not used in the final application:

Table 2. STPMIC25 power analog I/O pin configuration

Pin number	Pin name	Type	If not used
2	LDO8OUT	O	Floating
3	LDO78IN	I	VIN
4	LDO7OUT	O	Floating
5	LDO6OUT	O	Floating
6	LDO56IN	I	VIN
7	LDO5OUT	O	Floating
12	VBUS	I	Floating
13	LDO4OUT	O	Floating
14	LDO1OUT	O	Floating
15	LDO12IN	I	VIN
16	LDO2OUT	O	Floating
17	VOUT4	I	Floating
19	VLX4	O	Floating
20	BUCK4IN	I	VIN
21	VOUT3	I	Floating
23	VLX3	O	Floating
24	BUCK3IN	I	VIN
25	BUCK2IN	I	VIN
26	VLX2	O	Floating
28	VOUT2	I	Floating
35	VOUT5	I	Floating
37	VLX5	O	Floating
38	BUCK5IN	I	VIN
39	BUCK1IN	I	VIN

Pin number	Pin name	Type	If not used
40	VLX1	O	Floating
42	VOUT1	I	Floating
43	LDO3IN	I	VIN
44	LDO3OUT	O	Floating
45	VREFDDR	O	Floating
46	VOUT6	I	Floating
48	VLX6	O	Floating
49	BUCK6IN	I	VIN
50	BUCK7IN	I	VIN
51	VLX7	O	Floating
53	VOUT7	I	Floating

If the passive components (inductors, capacitors) of the unused LDOs and BUCK converters are not mounted (for cost constraints, to reduce the occupied area around the STPMIC25, etc.), it is mandatory to disable these IPs, setting their respective ranks to 0 in the NVM memory of STPMIC25. This avoids the risk of any possible oscillation or other saturation of the internal circuitry, and at each power ON cycle the unused IPs are not automatically turned ON.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
14-May-2024	1	Initial release.

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