AN4191
Application note

Power MOSFET: R_g impact on applications

By Giuseppe Longo, Filadelfo Fusillo, Filippo Scrimizzi

Introduction

This report shows the analysis performed on Power MOSFET devices, in which the goal is the evaluation of the intrinsic R_g parameter while it works in real applications. Generally, the R_g parameter is an intrinsic resistance value of the device itself, which cannot be changed because it's linked to the manufacturing process. The R_g parameter, according to the external driving circuit, allows the switching operation mode to be defined in terms of turn-on/off period and also coupling power dissipation of the external driver itself.

Starting from this statement, the analysis focused on devices having different intrinsic internal R_g and these were tested in a simple testing board with a fixed driver. The various tests performed allow us to understand the electro-thermal behavior of the device better and to find new conclusions on this parameter, which are often not known.

Contents

List of figures

1 Brief introduction to Power MOSFET intrinsic gate resistance

Power MOSFETs are 3-pin voltage-controlled devices: with a suitable voltage applied between gate and source, higher than the Power MOSFET threshold voltage, a current flows through the device channel between drain and source.

Figure 1. Power MOSFET symbol, typical circuit and device structure

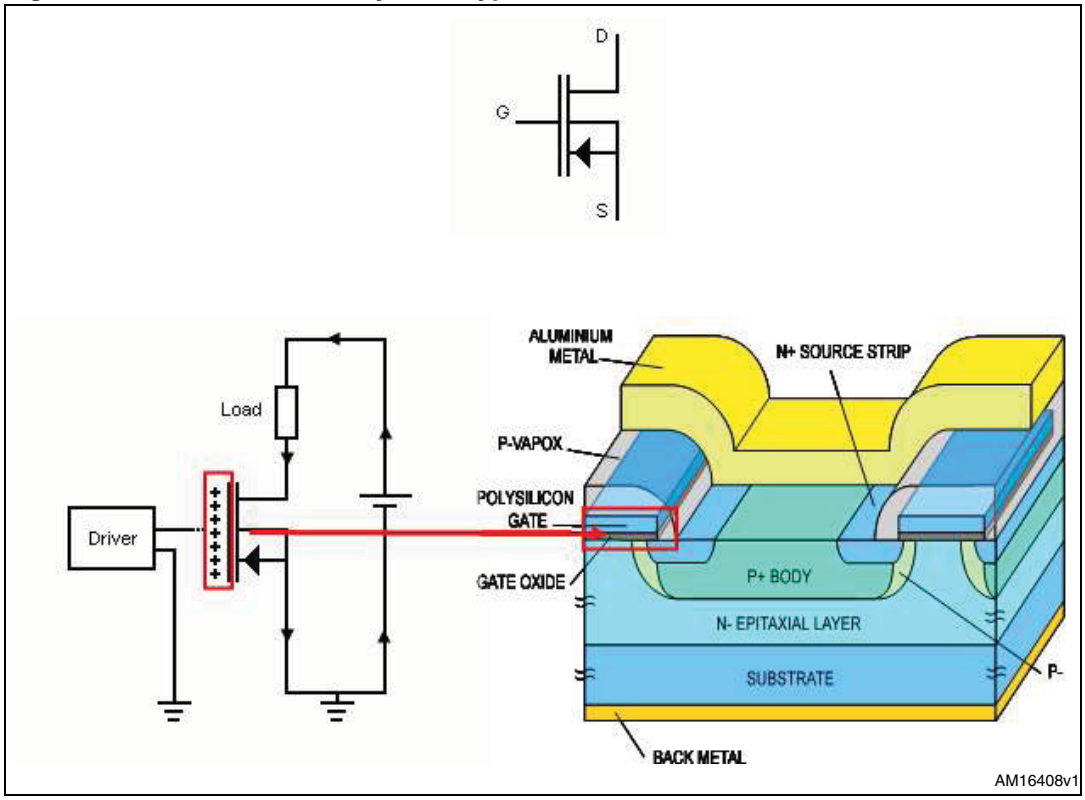
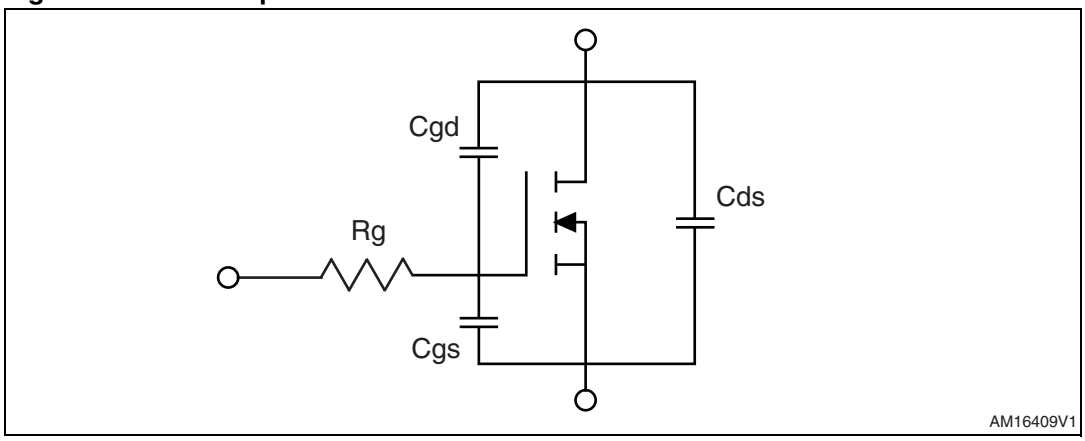


Figure 1 represents the Power MOSFET symbol, a typical circuit used for characterization tests and the device structure. The gate-source junction in the silicon is isolated by the oxide layer (gate oxide) and the drain-source current Id flows only if $V_{gs} > V_{th}$ is applied. Generally, even though the oxide layer is present in the gate-source structure, a leakage current flows through it. In other words, the gate-source structure can be represented for simplicity as a highly capacitive impedance; the real part of the impedance is the intrinsic R_g of the MOSFET.

The intrinsic gate resistance is an equivalent electrical resistance due to many device structure contributions (oxide, P-body, gate finger distributions…). The R_g value is a critical parameter that deeply impacts the device's switching performance, together with the power conversion efficiency and device thermal management. The higher the R_g, the larger the device's switching and gate drive losses, and consequently, the higher the working temperature of the MOSFET. In this case, there is the need for additional cooling components (i.e. heatsinks). *Figure 2* shows a simple representation of the internal parameters of a device.

Figure 2. Internal parameters of the device



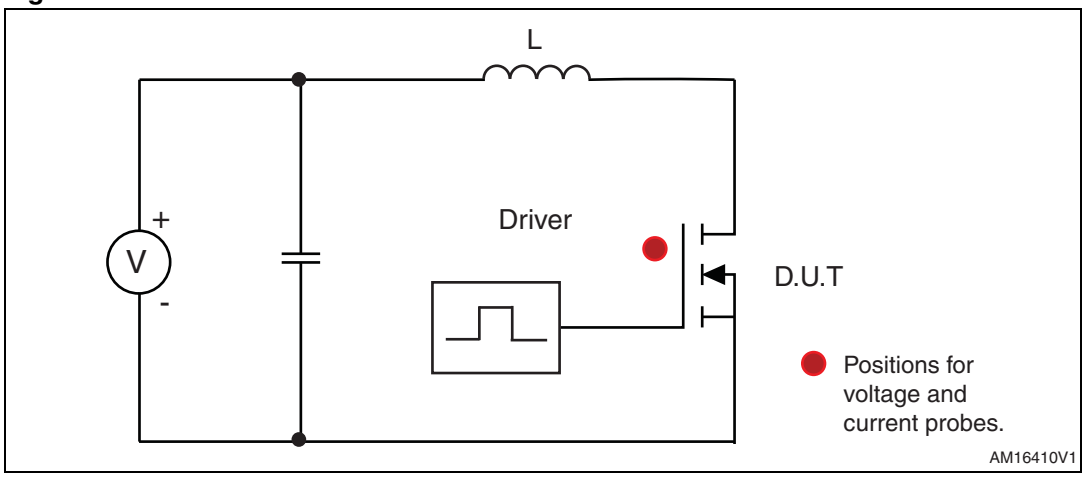
In order to better understand the impact of R_g on the device's switching performance, two different analyses are performed:

1. "Unclamped inductive switching" test on a characterization board; the device under test is a 120 A / 40 V LL V_{th} device selected with different intrinsic R_g values.
2. Application analysis on a 2.5" HDD board, where "good" parts (with correct R_g value) are compared with "bad" devices (with high R_g) in terms of switching behavior and device temperature.

2 R_g impact evaluation by UIS test

The electrical schematic used is shown in *Figure 3*:

Figure 3. Electrical schematic for UIS test



First of all, the dynamic MOSFET parameters (C_{iss}, C_{rss}, C_{oss}, R_g) are measured and the relevant values are reported in *Table 1*. Then, the UIS test is performed (V_{dd} = 12/18 V, L = 10 µH, t_{on} = 8 µs, T = 100 µs) on the low and high R_g parts. In this way, it is possible to make a first evaluation of the R_g impact.

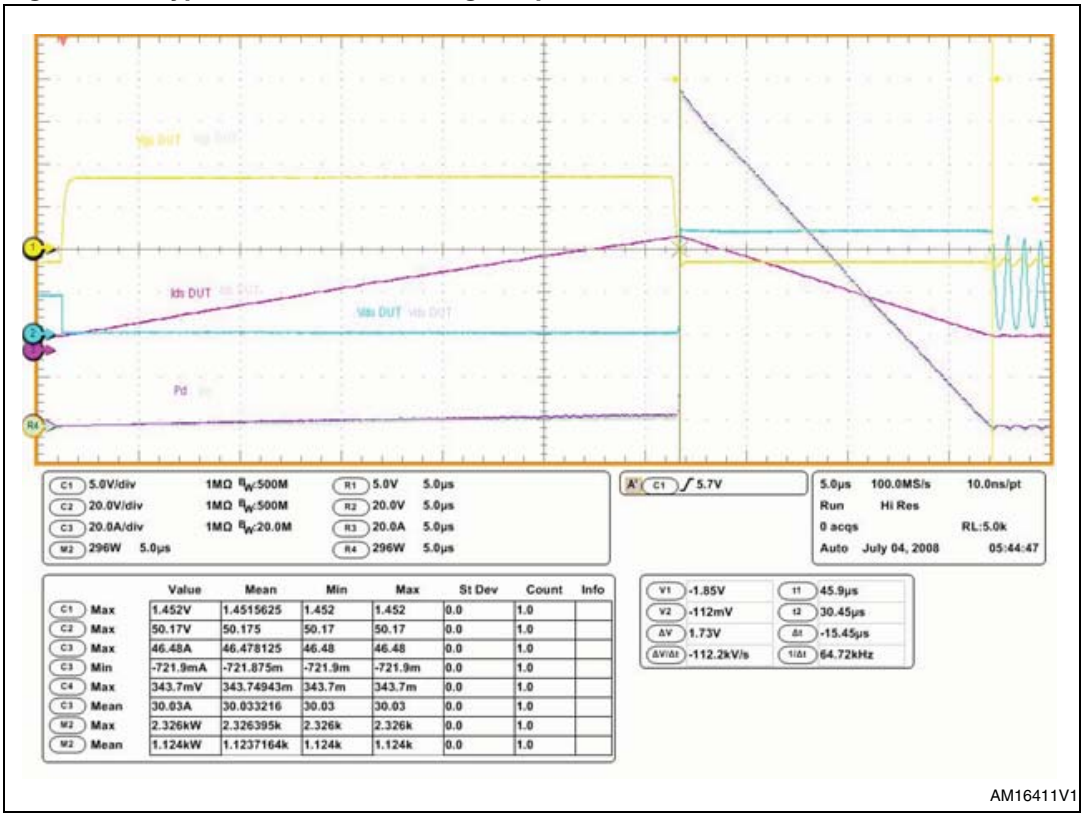
The UIS test is also performed on standard devices, varying the external gate resistance and monitoring the case temperature at steady-state. Additional tests are performed with resistive and capacitive load at various external $R_{g,ext}$. Based on the results obtained, we try to carry out the correlation between case temperature and R_g and the possible suggestions for a specific R_g limit for final test screening.

Table 1. Dynamic parameters of devices under test

n.	C_{iss} [pF]	C_{oss} [pF]	C_{rss} [pF]	R_g [Ω]
1	5909	1208	210	1.80
2	5909	1289	220	1.83
3	5885	1296	220	1.80
4	3720	1289	114	54.00
5	5907	1079	214	1.81
6	5867	1295	218	1.95
7	5883	1296	220	1.87
8	2902	1288	83	84.00

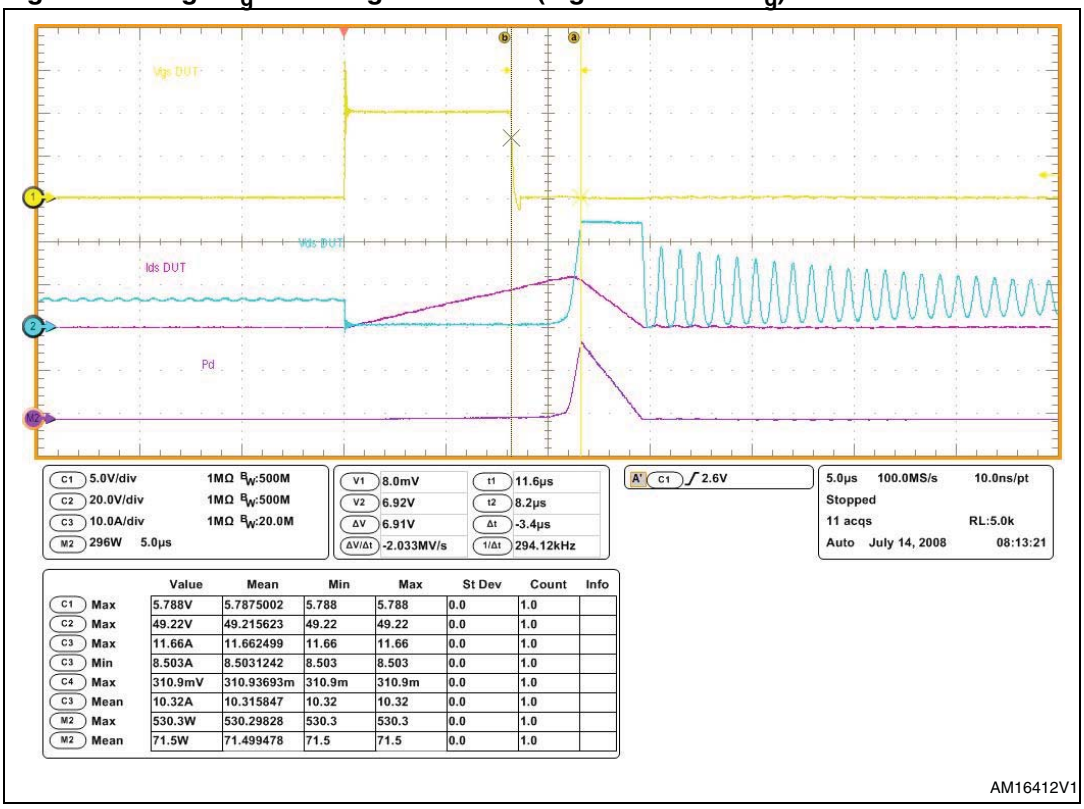
In *Figure 4* the typical waveforms for a good part (device #5) during an entire switching cycle are reported.

Figure 4. Typical waveforms for a good part



It's important to highlight that when the V_{GS} value goes down, the current begins to decrease and the V_{DS} increases its value, achieving the avalanche condition. During the discharge the device must dissipate a power represented by the P_d curve (violet and with a triangular shape). If a high R_g device is tested, the relevant waveform is reported in *Figure 5*:

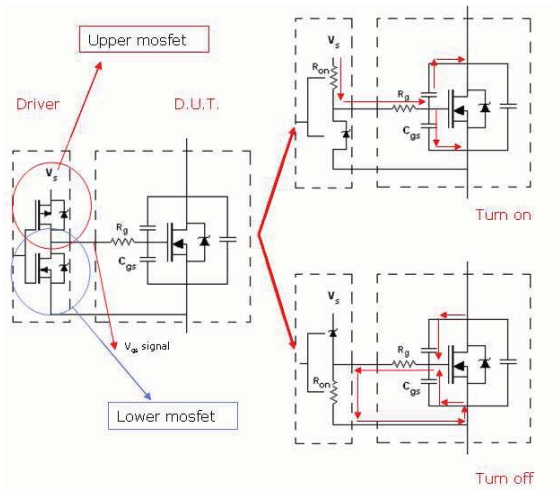
Figure 5. High R_g switching waveforms (higher intrinsic R_g)



In this image, the D.U.T. is the sample #4 that has an intrinsic R_g around 54 Ω Comparing *Figure 4* and *Figure 5*, it is easy to see that the device behavior and the relevant waveforms are very different. In fact, when the V_{gs} (yellow trace) goes down, the drain current (purple trace) continues to increase.

To better understand this phenomenon, a simple image is used:

Figure 6. MOSFET gate driving circuits with turn-on/off current paths



AM16413V1

The image shows the electrical connection between the driver and D.U.T. and the current flowing during switching-on and off.

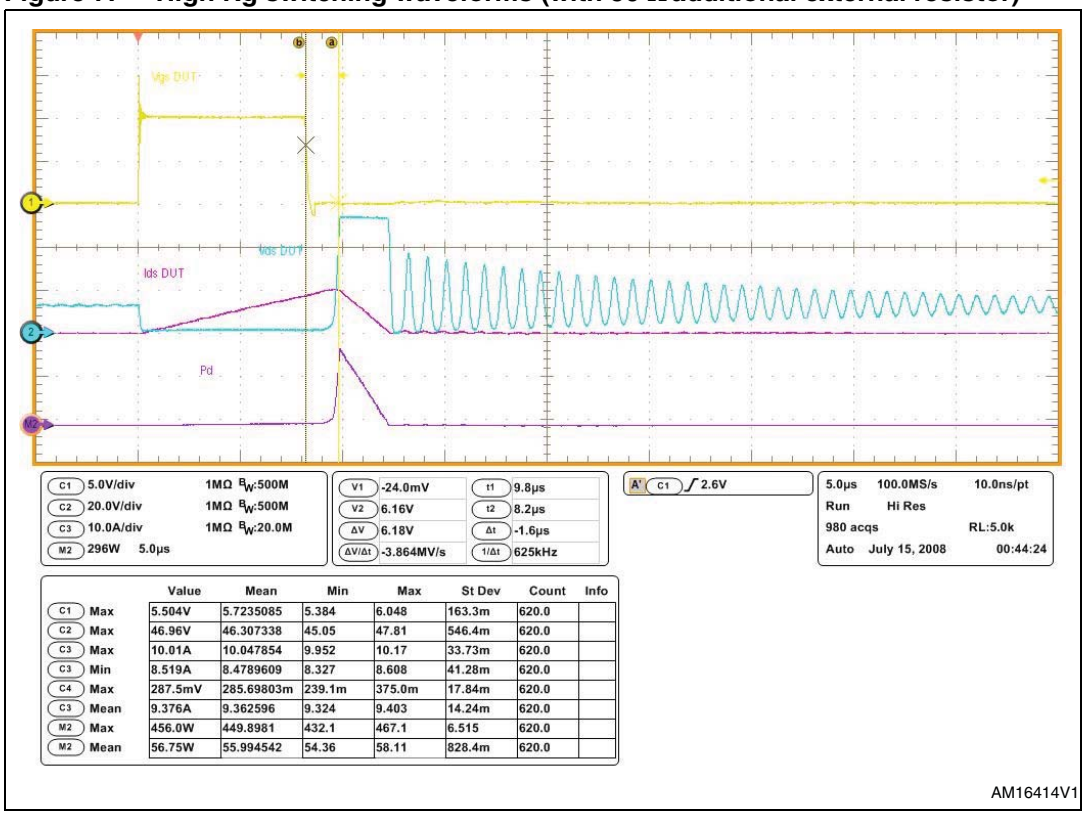
The “Driver” is composed of two Power MOSFETs in push-pull configuration. The D.U.T. turn-on is achieved when a positive gate-source voltage ($V_{GS} = V_S$) is applied to the gate, switching on the upper MOSFET; and vice-versa, the D.U.T. turns off when the lower MOSFET of the driver is in ON state, pulling down the D.U.T. gate to GND.

The red arrows show the current path charging internal capacitances when D.U.T. is turned on, and discharging capacitances when it is turned off. The image points out the internal R_g resistance and C_{gs} capacitance, since T_{on} and T_{off} are affected by those values. T_{on} and T_{off} represent times to complete the D.U.T. turn-on and turn-off.

The combination of R_g and C_{gs} is a simple RC circuit whose constant time $\tau = RC$ affects charge and discharge time. There are also other parameters that contribute to the turn-on/off of D.U.T. but it is important to underline that R_g is a key factor. In this case, with inductive load, the power dissipated by the device with higher R_g is bigger than the standard R_g device one because the switching slowdown, especially at turn-off, produces an additional current increase, due to the fact that the device remains on slightly longer, even if the gate-source voltage is already low.

A similar behavior may be obtained adding an external R_g resistor to a standard device. By inserting an external resistor of 50 Ω, we have the following waveform:

Figure 7. High Rg switching waveforms (with 50 Ω additional external resistor)



	Value	Mean	Min	Max	St Dev	Count	Info
C1 Max	5.504V	5.7235085	5.384	6.048	163.3m	620.0	
C2 Max	46.96V	46.307338	45.05	47.81	546.4m	620.0	
C3 Max	10.01A	10.047854	9.952	10.17	33.73m	620.0	
C3 Min	8.519A	8.4789609	8.327	8.608	41.28m	620.0	
C4 Max	287.5mV	285.69803m	239.1m	375.0m	17.84m	620.0	
C3 Mean	9.376A	9.362596	9.324	9.403	14.24m	620.0	
M2 Max	456.0W	449.8981	432.1	467.1	6.515	620.0	
M2 Mean	56.75W	55.994542	54.36	58.11	828.4m	620.0	

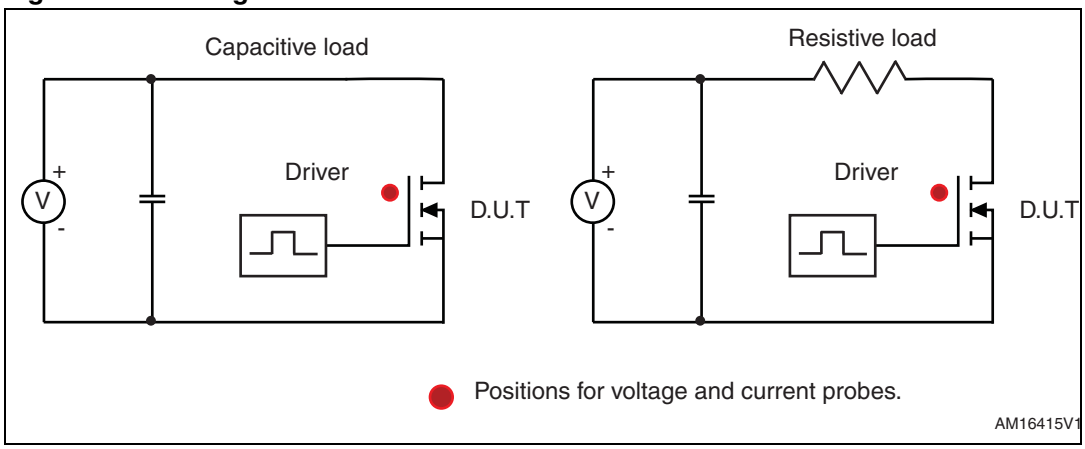
The curve shows that the external R_g enlarges switching times and the main effect appears at turn-off. In fact, the V_{gs} is down and the current increases itself for an additional 1.6 µs.

In order to measure the impact of R_g, we performed many tests at the same electrical conditions on an R_g standard device inserting an external R_g driver and catching the case temperature at steady-state.

At bench, we performed many trials at various resistances using the same electrical circuit board at different loads, which are the following:

- inductor load
- capacitive load (see *Figure 8*)
- resistor load (see *Figure 8*).

Figure 8. Testing circuit schematics



The results show that the device with high inner R_g has a higher temperature than the device with equivalent external R_g. The values obtained were plotted for each load configuration, obtaining the following curves:

Figure 9. Inductive load

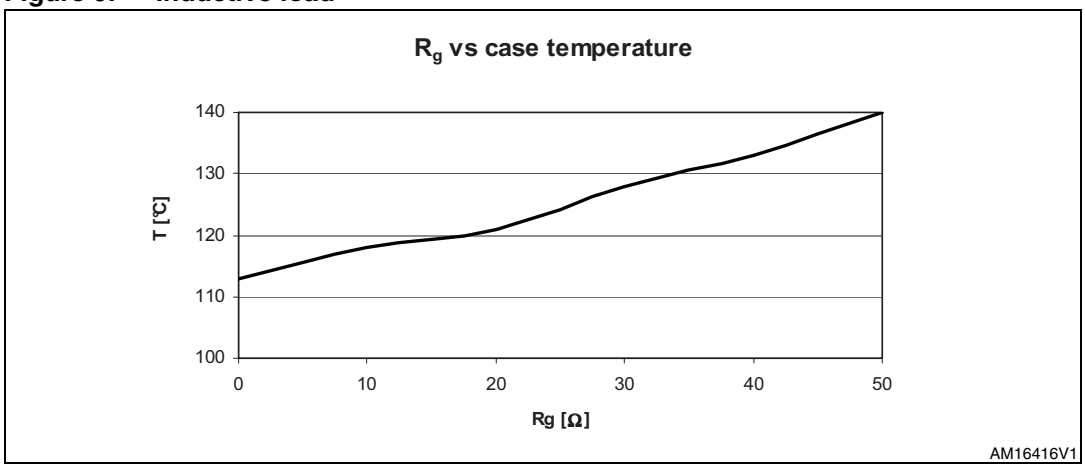


Figure 10. Capacitive load

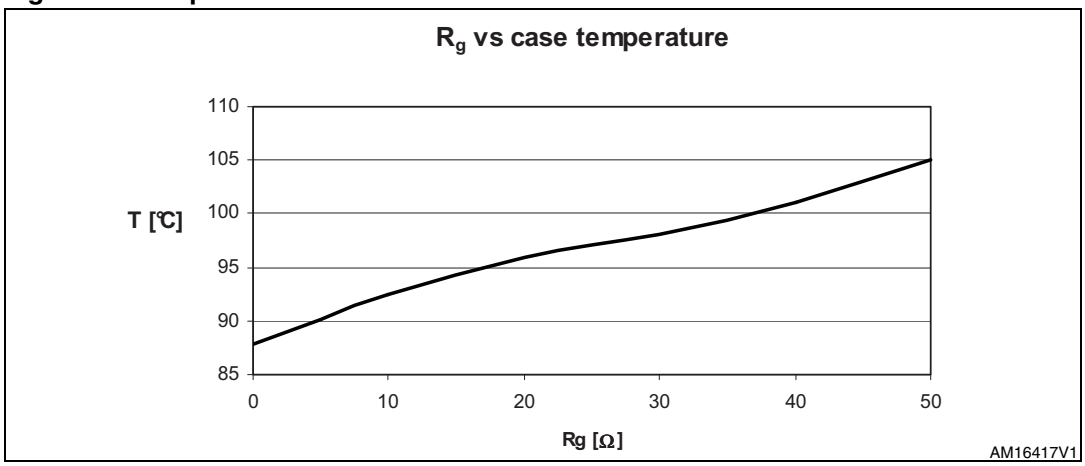
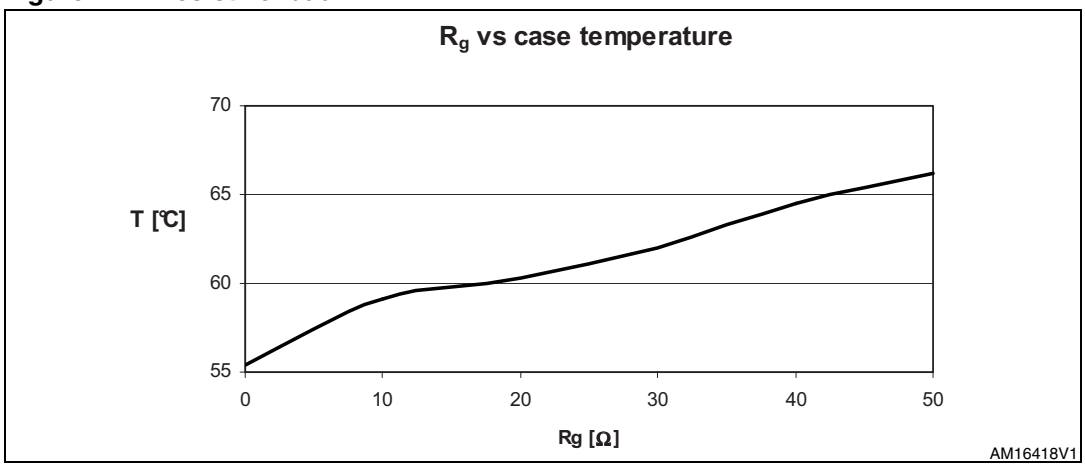


Figure 11. Resistive load



3 R_g impact for MOSFETs in buck/buck-boost configurations

Let's consider now the R_g impact on MOSFET switching behavior and thermal management in a real customer application. In particular, the MOSFET is used as a control or synchronous switch in a single-phase synchronous buck or buck-boost converter. These topologies are widely used in the computer and peripherals sector, when a fixed output voltage is generated from a regulated input voltage by adjusting properly the device turn-on time and therefore the converter duty cycle ($D = V_{OUT} / V_{IN}$). The output voltage feeds various system blocks (i.e. CPU, DDR, etc.…).

Too high R_g values can affect the MOSFET performance in the application, particularly:

a) Rising/falling edges slowing down.

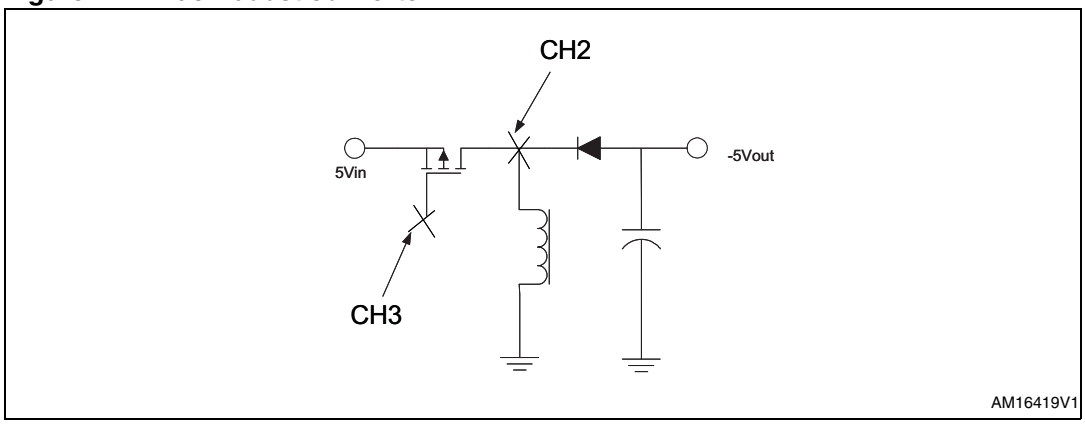
b) LS false turn-on risk enhancement.

c) Driver/MOSFET temperature increase.

3.1 Rising/falling edges slowing down

Initially, let's consider a buck-boost converter (*Figure 12*), that lowers the input voltage (5 V) generating - 5 V as V_{OUT}. Ch2 (drain voltage) and Ch3 (gate voltage) indicate the probe placement. Two equal FETs, with different R_g values, are compared as the control switch.

Figure 12. Buck-boost converter



In *Figure 13* and *Figure 14* respectively, the waveforms for a “good” part (standard R_g value) and “bad” part (high R_g value) are illustrated.

Figure 13. Standard R_g value

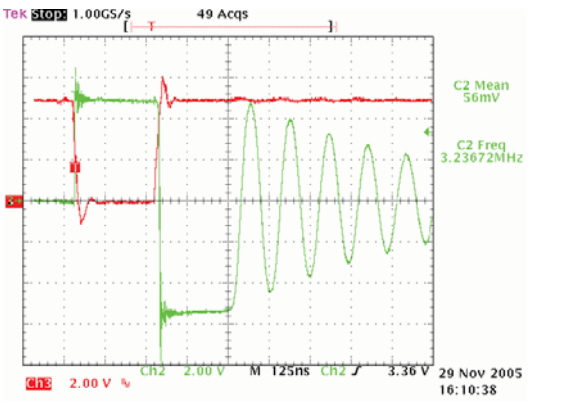
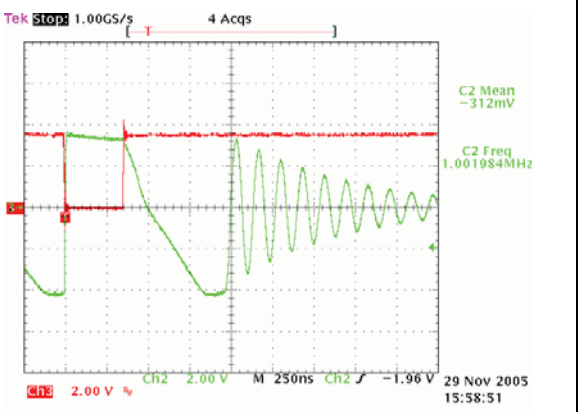
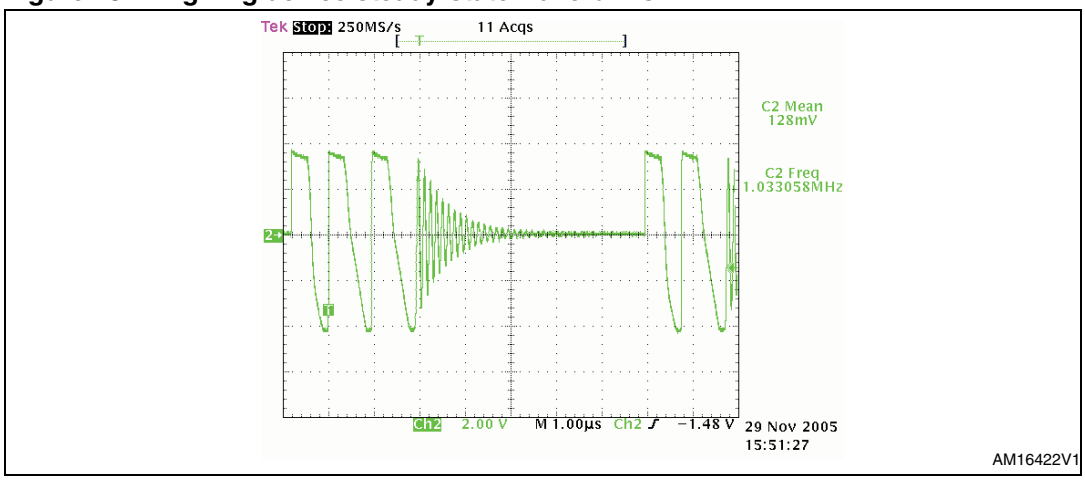


Figure 14. High R_g value



Looking at the green trace (Ch2, drain voltage) in *Figure 13*, the input voltage (5 V) and the output voltage (- 5 V) are clearly evident, together with the oscillations due to the converter DCM. On the other hand, in *Figure 14* the "high R_g" device shows an incorrect behavior. In fact, the converter works in "overcurrent protection mode" when the 5 V is pulled down to 3.5 V and the output voltage has an incorrect value. In *Figure 15*, more switching cycles for the "bad" part are shown.

Figure 15. High Rg device steady-state waveforms

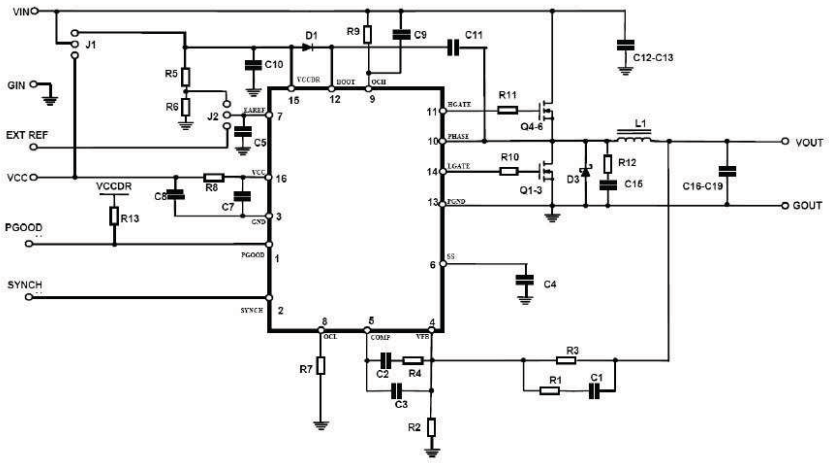


Analyzing the drain voltage waveform, the slow drain falling edge indicates that the FET is not turned off although the gate voltage is high (P-channel device). It is evident that the slow falling-down of the FET drain voltage becomes more dangerous during steady-state conditions, when the device turns on and off with a certain fsw. In fact, the device cannot be turned-off effectively at each switching cycle. So, this slow MOSFET turn-off causes an undesired switching loss increase, and therefore, a power dissipation and temperature rise, finally producing the device failure.

3.2 Synchronous buck converter for motherboard: LS false turn-on risk enhancement

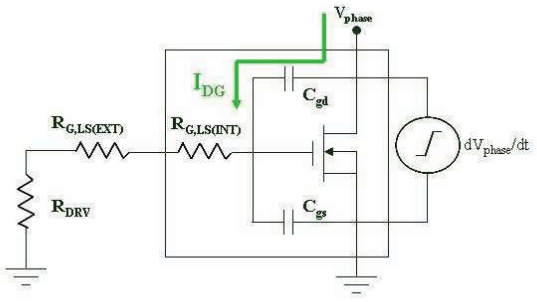
In *Figure 16*, the schematic of a single-phase synchronous buck converter is shown (V_{IN} = 12 V, V_{OUT} = 1.5 V, f_{SW} = 500 kHz, $I_{OUT,MAX}$ = 30 A); Q4-6 is the high-side device, while Q1-3 is the low-side FET.

Figure 16. Schematic of a single-phase synchronous buck converter



The LS device can be affected by the so-called “LS false turn-on,” which can be potentially dangerous for the MOSFET itself and the reliability of the entire converter. When the high-side turns on, a high dV/dt appears across the low-side device (*Figure 17*). Through the Miller capacitance, a capacitive current flows ($i_c = C_{gd} * dV/dt$), coupling to the LS gate pin. If the total resistance formed by the intrinsic, external, and driver resistances is much lower than the equivalent MOSFET impedance between gate and source, this current flows through the above mentioned resistive path. This causes a spurious bouncing across gate and source MOSFET pins; if this induced voltage is higher than minimum threshold voltage, the LS can be partially turned on, creating a low-resistance path between supply voltage and GND. In other words, undesired power dissipation is present in each switching cycle, worsening the converter efficiency, thermal management, and reliability.

Figure 17. Cdv/dt false turn-on event



In order to evaluate the R_g impact on the LS false turn-on, two identical FETs (same silicon) but different R_g values (1.5 Ω vs. 4 Ω) are mounted in the converter shown in *Figure 16*. *Figure 18* and *19* illustrate the LS gate-source waveforms for the two LS FETs.

Figure 18. High R_g (4 Ω) LS turn-off

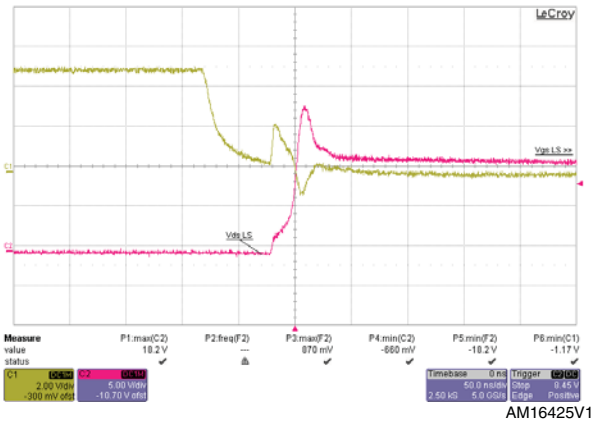
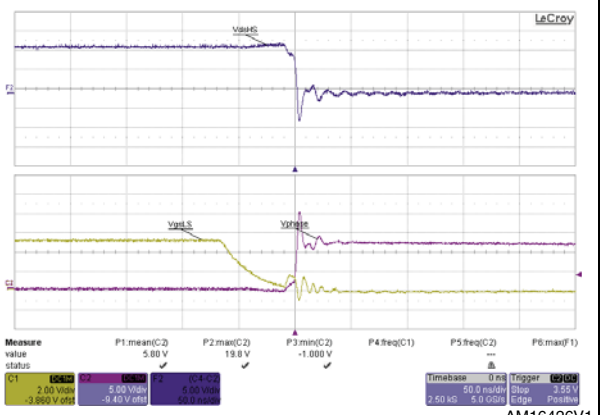


Figure 19. Low R_g (1.5 Ω) LS turn-off



Comparing the two images, the “high R_g” MOSFET has a higher and larger (over the minimum threshold voltage) spurious bouncing than the standard device. This causes a “shoot-through” event (for each switching cycle), that increases the converter power losses. So, higher device (MOSFETs and driver) temperatures are measured when “high R_g” samples are mounted on the board in the low-side position, as shown in the thermal captures of *Figure 20* (standard part) and *Figure 21* (high R_g).

Figure 20. Thermal capture for standard part

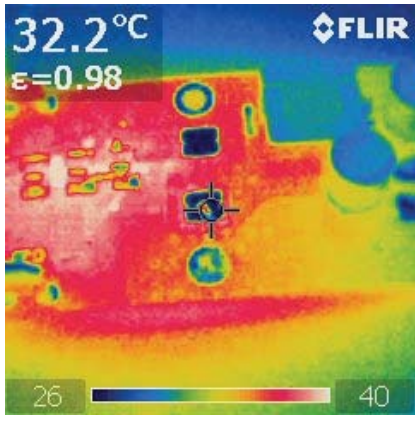
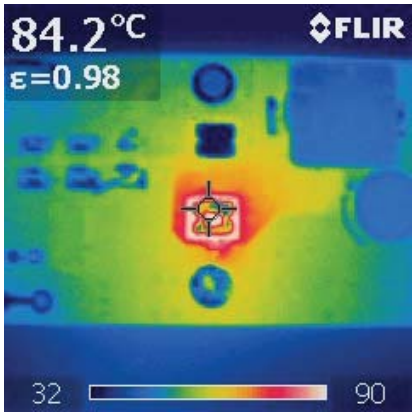


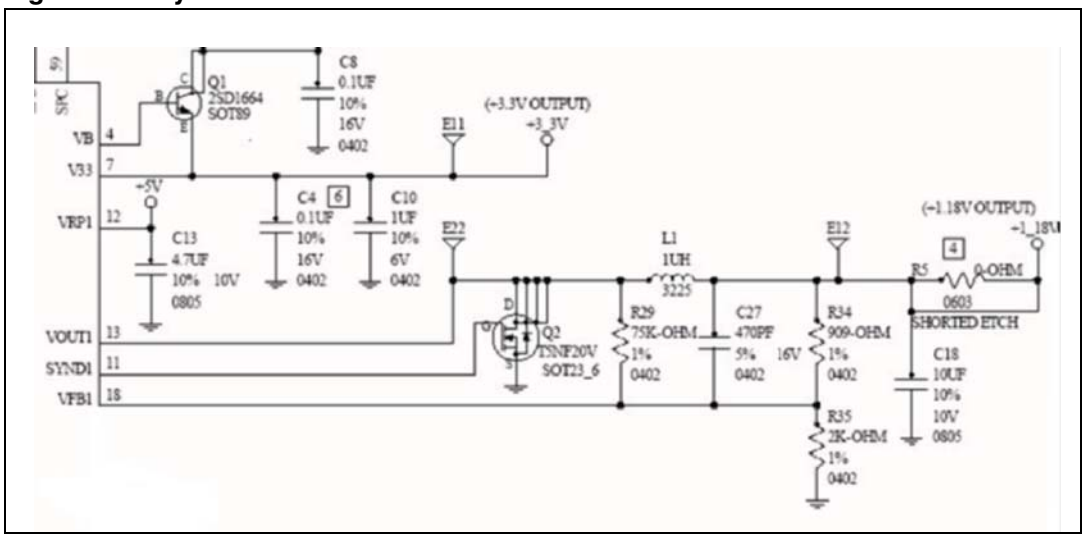
Figure 21. Thermal capture for high R_g



3.3 Synchronous buck converter for HDD: LS false turn-on risk enhancement

Figure 22 shows (inside the light blue rectangle) a single phase synchronous buck converter, which provides 1.18 V as output voltage, with 1.1 MHz as switching frequency.

Figure 22. Synchronous buck converter schematic



In this board two different sample categories of the same device (20 V / 5A SLL V_{th}) are compared: the “good” parts, with standard R_g (aligned to datasheet values) and the “bad” parts, with high R_g values. The dynamic parameters are reported in *Table 2* and *3*.

Table 2. Dynamic parameters for “good” part

C_{iss} [pF]	C_{oss} [pF]	C_{rss} [pF]	R_g [Ω]
375.14	173.54	46.08	2.98

Table 3. Dynamic parameters for “bad” part

C_{iss} [pF]	C_{oss} [pF]	C_{rss} [pF]	R_g [Ω]
335.14	172.48	41.99	125.02

The main analysis key points are:

- Switching behavior evaluation and waveform capture
- Driver/MOSFET thermal measurements at board startup.

In *Figure 23* and *Figure 24*, the V_{DS} and V_{OUT} waveforms for “good” and “bad” parts, respectively, are illustrated.

Figure 23. "Good" part steady-state waveforms

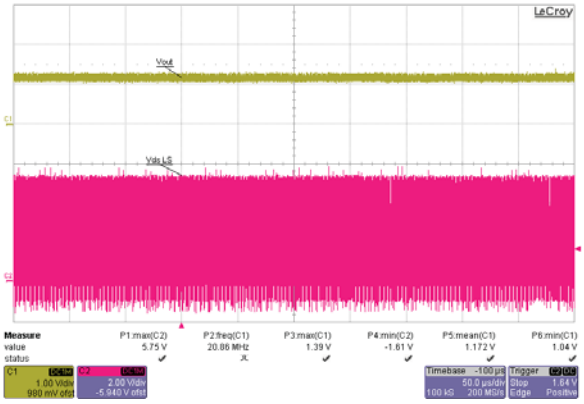
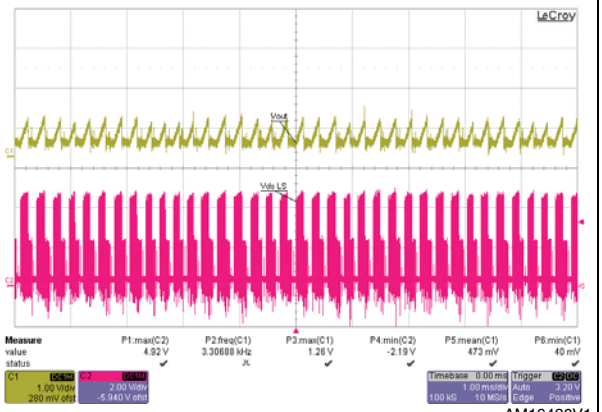


Figure 24. "Bad" part steady-state waveforms



As shown in the previous images, the "bad" part shows an incorrect output voltage value (0.473 V vs. 1.18 V), due to the different MOSFET switching speed and switching times. The thermal measurements are made at the board startup and no load conditions, using a thermal camera to detect MOSFET and driver temperatures. *Figure 25* and *Figure 24* show, respectively, the images for "good" and "bad" parts.

Figure 25. "Good" part thermal image

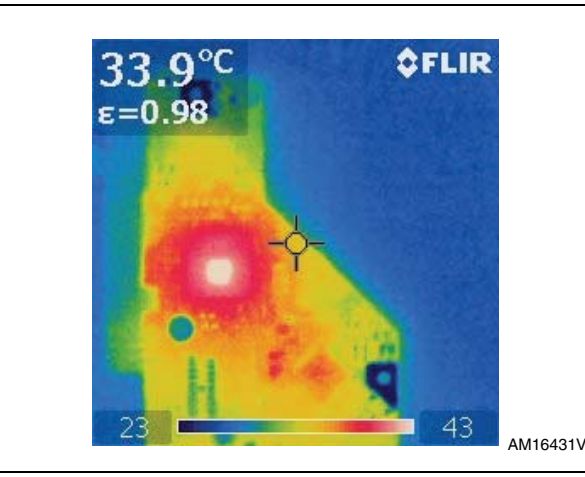
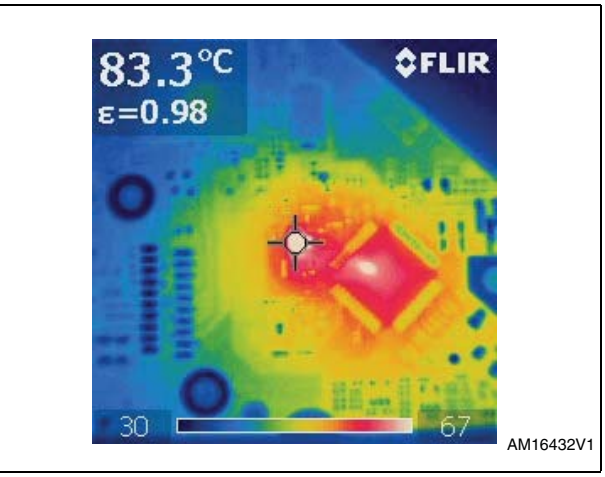


Figure 26. "Bad" part thermal image



For the "good" sample, the MOSFET temperature is 35.4 °C, while for the "bad" device its 87.4 °C. A similar temperature increase is detected for the driver: 37.8 °C for the first configuration and 73.4 °C for the second one. It is obvious that such high R_g values cause:

- MOSFET temperatures to rise due to switching loss enlargements (the higher the R_g, the longer the MOSFET switching times)
- Driver temperature increases because of gate drive losses rising.

Unfortunately, full load conditions haven't been reached due to the quick device temperature increase till maximum rating.

4 Conclusions

From the experimental results, we can summarize that a higher R_g value not only worsens the MOSFET's working conditions, by increasing the temperature and switching losses, it also worsens application efficiency and working conditions by fully modifying the device's switching behavior and doesn't achieve the converter values set by design. Moreover, a higher R_g heavily affects the driver/PWM controller safety working condition, forcing it to sustain a higher temperature, as well as dissipating a larger power to charge up the MOSFET input capacitance. It is also dangerous for producing the cross conduction that may cause system disruption by the static dV/dt.

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
09-Nov-2012	1	Initial release.