AN1179: Si34071 802.3bt PD PoE Interface

This document provides guidelines for designing an IEEE 802.3bt Power over Ethernet (PoE) Powered Device (PD) interface by using the Silicon Labs Si34071 device.

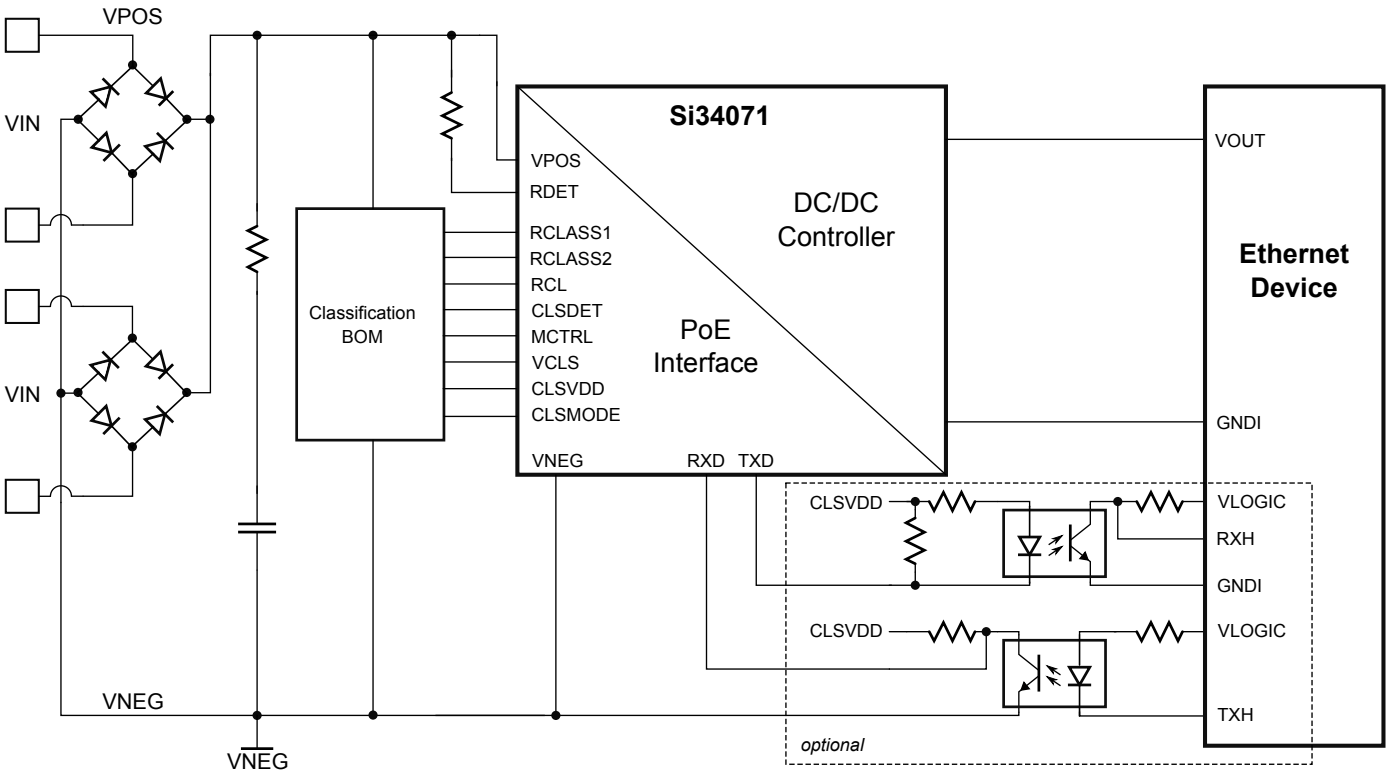
Si34071 device with the surrounding BOM provides the necessary detection, up to 5-event classification and mark, and operating current levels compliant with IEEE 802.3bt Type 3 and Type 4 PoE standard.

The Si34071 is a Type 3 or Type 4 device recommended for applications needing up to 90 W input power with high conversion efficiency.

The tiny 5x5 QFN package makes it ideal for systems needing low cost and compact PCB sizes. Beside the PoE interface, the Si34071 includes a dc-dc controller along with drivers for external switches, a UART interface for optional diagnostic messages, IEEE 802.3at and IEEE 802.3bt compliant MPS funcionality as well as optional integrated sleep/wake functions. A simplified application diagram of the Si34071 is shown below.

KEY FEATURES

- IEEE 802.3bt PoE compliant interface
- Various diagnostic messages through UART
- Integrated dc/dc controller
- Autoclass signaling and short MPS



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1. Introduction to the Si34071 PoE Powered Device

PoE makes use of the massive install base of UTP cabling for wired Ethernet networks – with multiple-billion ports worldwide. PoE (Power over Ethernet) is part of the IEEE's 802.3 Ethernet standard, which specifies the technical requirements for the safe and reliable distribution of power over the same Category-5 (CAT-5) unshielded twisted pair (UTP) cabling used for carrying data.

Designers face numerous challenges designing PoE powered applications, including maximizing efficiency, controlling EMI and minimizing cost while still delivering the necessary output power. This application note focuses on the features and configuration of the Si34071's 802.3bt compliant interface. The table below shows the available input power for different PD classes. For DC/DC conversion related information such as architecture, cost, efficiency, EMI performance, thermal performance and output power please visit https://www.silabs.com/power-over-ethernet.

Table 1.1. Available Input Power for Different PD Classes

PD Type	PD Class	PSE Output Power (W)	Cable Loss (W)[1]	PD Input Power (W)
3	1	4.0	0.16	3.84
	2	6.7	0.21	6.49
	3	14.0	1.0	13.0
	4	30.0	4.5	25.5
	5	45.0	5.0	40.0
	6	60.0	9.0	51.0
4	7	75.0	13.0	62.0
	8	90.0	18.7	71.3

Note:
1. At maximum cable length = 100 m.

1.1 Si34071 PoE-PD Product Features

The following list highlights the features of Si34071 devices.

- Type 3, Class 4-6 Signaling Support (.bt PoE)
- Type 4, Class 7-8 Signaling Support (.bt PoE)
- Integrated TVS Surge Protection, IEC 61000-4-5: 10/700µs common mode
- Integrated DC/DC Controller
- Tunable Switching Frequency
- Standard MPS and IEEE 802.3bt compliant short MPS
- Bias Winding Support
- Secondary FET Driver
- External Switching and Hotswap FET Support
- Optional Sleep Mode with Wake Control
- 5x5 mm 32 pin QFN package
- Available dc-dc Architectures:
  - Flyback
  - Forward

2. Si34071 PoE Interface Functional Description

2.1 Detection

During the detection phase, the Power Sourcing Equipment (PSE) applies two voltages between 2.7 V and 10.1 V and measures the current draw of the connected PD. When the input voltage is in the valid detection range, the Si34071 will present a detection resistance in the range of 23.7 kΩ to 26.3 kΩ to indicate to the PSE that a valid PD is connected.

The detection resistance signature presented by the Si34071 is determined by the external resistor R_{DET} connected between R_{DET} and V_{POS} pins. The type of rectifying bridge has an impact on the detection as well.

When using an external Schottky diode bridge, the high reverse leakage current of the diodes at high temperatures could result in the signature resistance violating the IEEE 802.3 specification, so to compensate this effect a slightly larger external R_{DET} resistor is recommended in this case. If FETs are used as a rectifier bridge and the PD device is utilized in sub-zero temperature, it is recommended to install low-leakage Schottky diodes such as BAT46ZFILM in parallel with the FET bridges. The table below summarizes the recommended R_{DET} values for various input bridge types.

Note: The detection phase is identical for both Type 3 and Type 4 PDs.

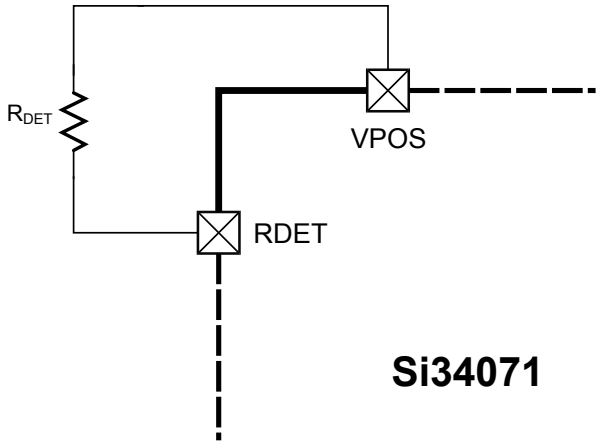


Figure 2.1. Detection Resistor R_{DET}

Table 2.1. Si34071 R_{DET} Selection

Rectifier Bridge	Detection Resistance	Precision	Minimum Package Size	Power Rating
Silicon diode	24.3 kΩ	1%	0201	1/20 W
Schottky diode	24.9 kΩ	1%	0201	1/20 W
FET	24.3 kΩ	1%	0201	1/20 W
FET||Schottky diode	25.5 kΩ	1%	0201	1/20 W

In addition to presenting a valid resistance during detection, the PD must also present a capacitance between 50 nF and 120 nF. This is established on the Si34071 by populating a ceramic C_{DET} of 100 nF between V_{POS} and V_{NEG}. To make the system more robust against non-standard PoE injectors it is necessary to include a resistor R_{INJ} with a value of 3 Ω in series with C_{DET} capacitance.

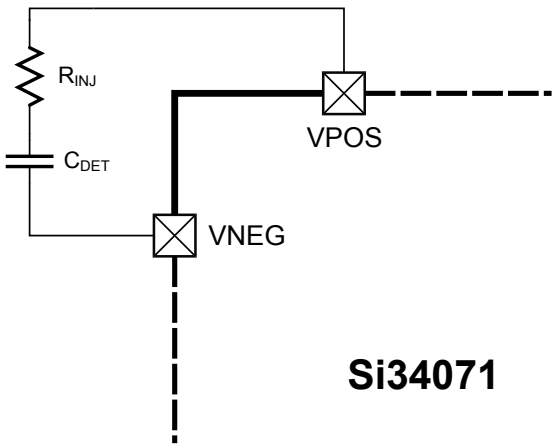


Figure 2.2. Detection Capacitance C_{DET} and Injector Resistance R_{INJ}

2.2 Classification

After a successful detection, the PSE transitions to the classification stage and raises the voltage between 14.5 V and 20.5 V. An IEEE 802.3bt compliant PSE produces 3 to 5 class pulses based on the signature presented by the PD. Every class pulse is followed by a mark and the PSE measures the current draw in each pulse and determines the requested Class. A Class 4 PD will draw the same current in all class events, while Class 5-8 PDs will present two different signatures during classification.

The Classification BOM in the figure below produces a 3.3 V rail to power the Si34071 and generate the correct classification signatures. These components are critical to the Si34071 operation and should not be modified. Only the highlighted resistors may be altered as described in Table 2.2 PD Class Signatures for Different Requested Classes on page 6 and Table 2.5 Configuration Resistors for Requested Class and Autoclass on page 7. These resistors are used to set up the requested power level, the class signature, and the Autoclass configuration of the device.

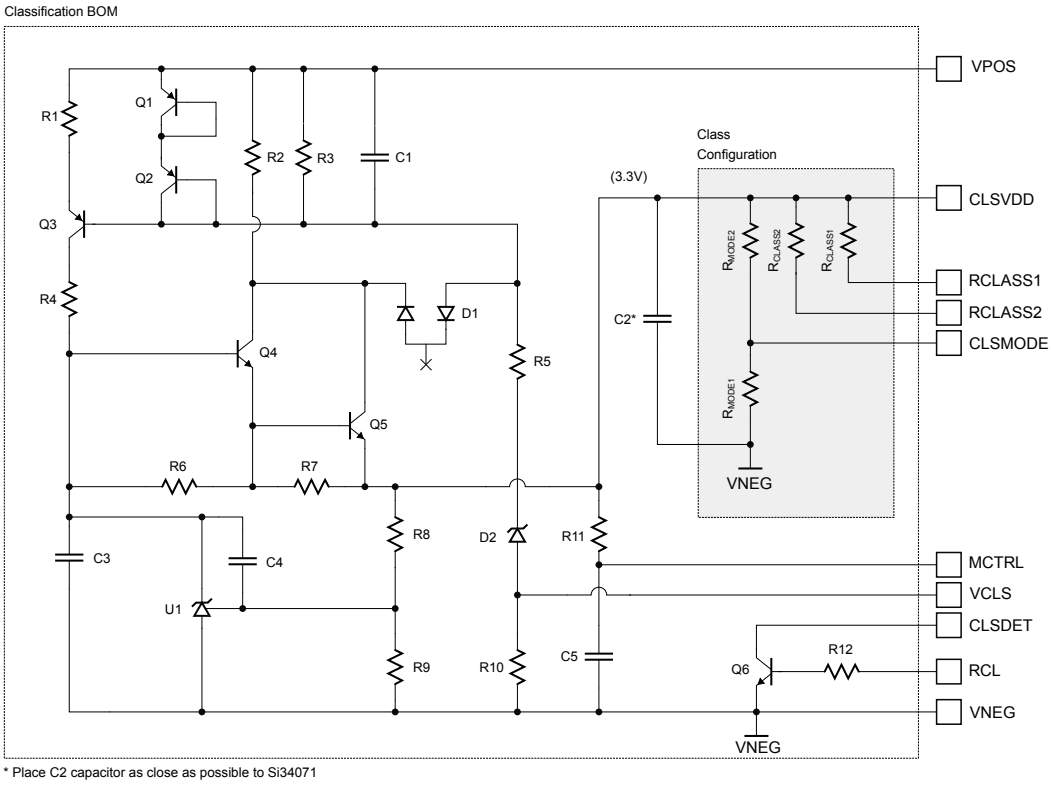


Figure 2.3. Classification BOM

An overview of the signatures produced by an IEEE 802.3bt compliant PD can be seen in the table below. The numbers represent the class signature that should be presented for each event. The relation between the classification signatures and the actual current consumption is summarized in Table 2.3 PD Consumption during Class Signatures on page 6. For Class 4–8, the first two classification events are always identical and should be class signature 4, this is indicated as SigA in the table. The subsequent events are different for each Class, this is denoted as SigB. The numbers in brackets shall not happen during an IEEE 802.3bt compliant classification, but will be presented by the PD if they are attached to a non-compliant PSE (see note). The Si34071 shall be used only for Class 4-8 designs; for lower power applications, the use of Si3406x is recommended.

Note: A non-compliant PSE produces more class events than the maximal number of class events defined by the standard.

Table 2.2. PD Class Signatures for Different Requested Classes

Requested Class	SigA		SigB		
	Event 1	Event 2	Event 3	Event 4	Event 5
Class 4	4	4	4	(4)	(4)
Class 5	4	4	0	0	(0)
Class 6	4	4	1	1	(1)
Class 7	4	4	2	2	2
Class 8	4	4	3	3	3

Table 2.3. PD Consumption during Class Signatures

Class Signature	Consumption (mA)
Class Signature 0	1-4
Class Signature 1	9-12
Class Signature 2	17-20
Class Signature 3	26-30
Class Signature 4	36-44

The Si34071 sets the classification current with the aid of two resistors R_{CLASS1} and R_{CLASS2}. The following table details the recommended resistor values for each power Class.

Table 2.4. Si34071 R_{CLASS1} and R_{CLASS2} Selection

Requested Class	R_{CLASS1}	R_{CLASS2}	Precision	Minimum Package Size	Minimum Power Rating (W)
Class 4	169 Ω	169 Ω	1%	0603	1/8
Class 5	169 Ω	169 Ω	1%	0603	1/8
Class 6	98 Ω	492 Ω	1%	0603	1/8
Class 7	138 Ω	215 Ω	1%	0603	1/8
Class 8	258 Ω	125 Ω	1%	0603	1/8

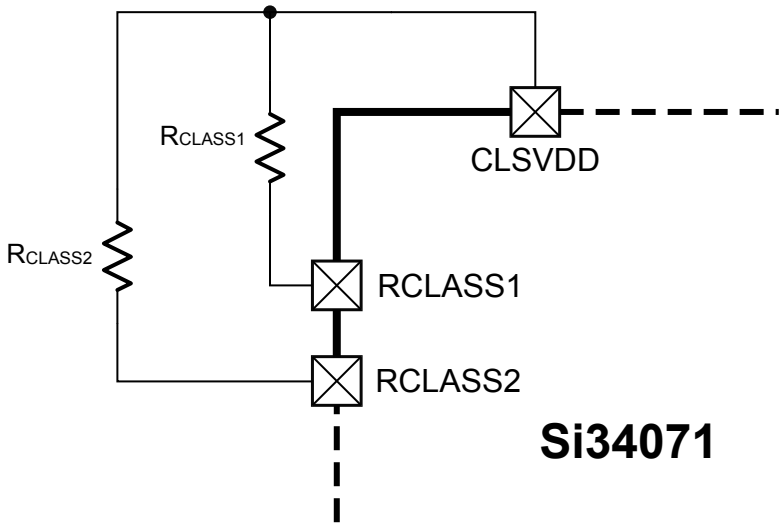


Figure 2.4. Classification Resistors R_{CLASS1} and R_{CLASS2}

To set up the desired Requested Class, the voltage on the CLSMODE pin must be in the [V_{MODE_MIN}, V_{MODE_MAX}] range. R_{MODE1} and R_{MODE2} are used as a resistor divider to control the voltage on the pin and also utilized to enable Autoclass (AC) configuration. See 2.6 Autoclass for more details.

The table below summarizes the voltage which must be present on the CLSMODE pin and gives suggestions for the resistor values. The relationship between R_{MODE1}, R_{MODE2} and the voltage on the CLSMODE pin, is as follows:

$$CLSMODE\ \left(V\right) = CLSVDD\frac{R_{MODE2}}{R_{MODE1} + R_{MODE2}}$$

where CLSVDD is 3.3 V and produced by the Classification BOM

Table 2.5. Configuration Resistors for Requested Class and Autoclass

Requested Class	V_{MODE_MIN} (V)	V_{MODE_TYP} (V)	V_{MODE_MAX} (V)	R_{MODE1}	R_{MODE2}	Precision
Class 4	0.00	0.16	0.32	6.8 kΩ	130 kΩ	5%
Class 5	0.34	0.49	0.65	16 kΩ	91 kΩ	5%
Class 6	0.66	0.82	0.98	30 kΩ	91 kΩ	5%
Class 7	1.00	1.15	1.30	33 kΩ	62 kΩ	5%
Class 8	1.32	1.48	1.64	39 kΩ	47 kΩ	5%
Class 4 + AC	1.66	1.82	1.98	47 kΩ	39 kΩ	5%
Class 5 + AC	1.99	2.15	2.30	82 kΩ	43 kΩ	5%
Class 6 + AC	2.32	2.48	2.64	91 kΩ	30 kΩ	5%
Class 7 + AC	2.65	2.80	2.96	130 kΩ	22 kΩ	5%
Class 8 + AC	2.98	3.14	3.30	200 kΩ	10 kΩ	5%

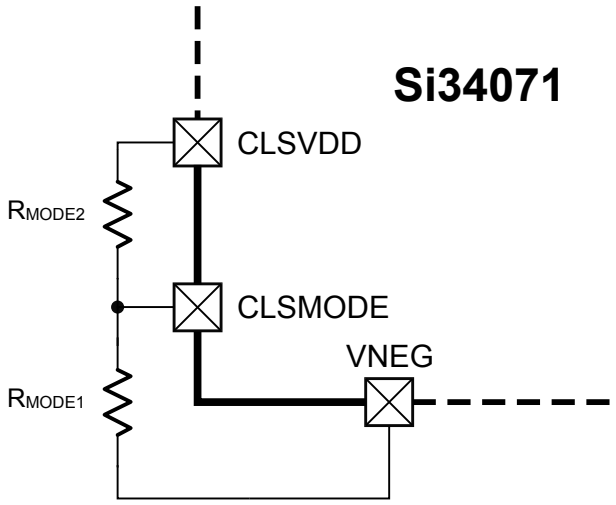


Figure 2.5. Resistor Divider to Set Up the Mode Configuration

2.3 Type 3 and Type 4 Classification

During Type 3 (Class 1–6 for 802.3bt) and Type 4 (Class 7–8 for 802.3bt) classification the PSE will always provide at least three classification events. The first class pulse for a Type 3 and Type 4 PSE will always be a long first class pulse. Class pulses are separated with a Mark Event where the PSE drops the voltage between 6.9 V and 10.1 V.

2.3.1 Type 3 – Class 4 – Input Power of 30.0 W

The detection and classification sequence can be observed in the figure below. The PSE forces the voltage toward the PD which can be seen in the upper figure where CE and ME indicates Class Event and Mark Event respectively. The lower chart represents the current consumption of the PD as a response to these events. Si34071 configured as a Class 4 PD will give a Class 4 (40 mA) signature in all three pulses. Non-compliant PSEs might provide more than three pulses where the PD will continue to provide the same signature as in the third Classification Event.

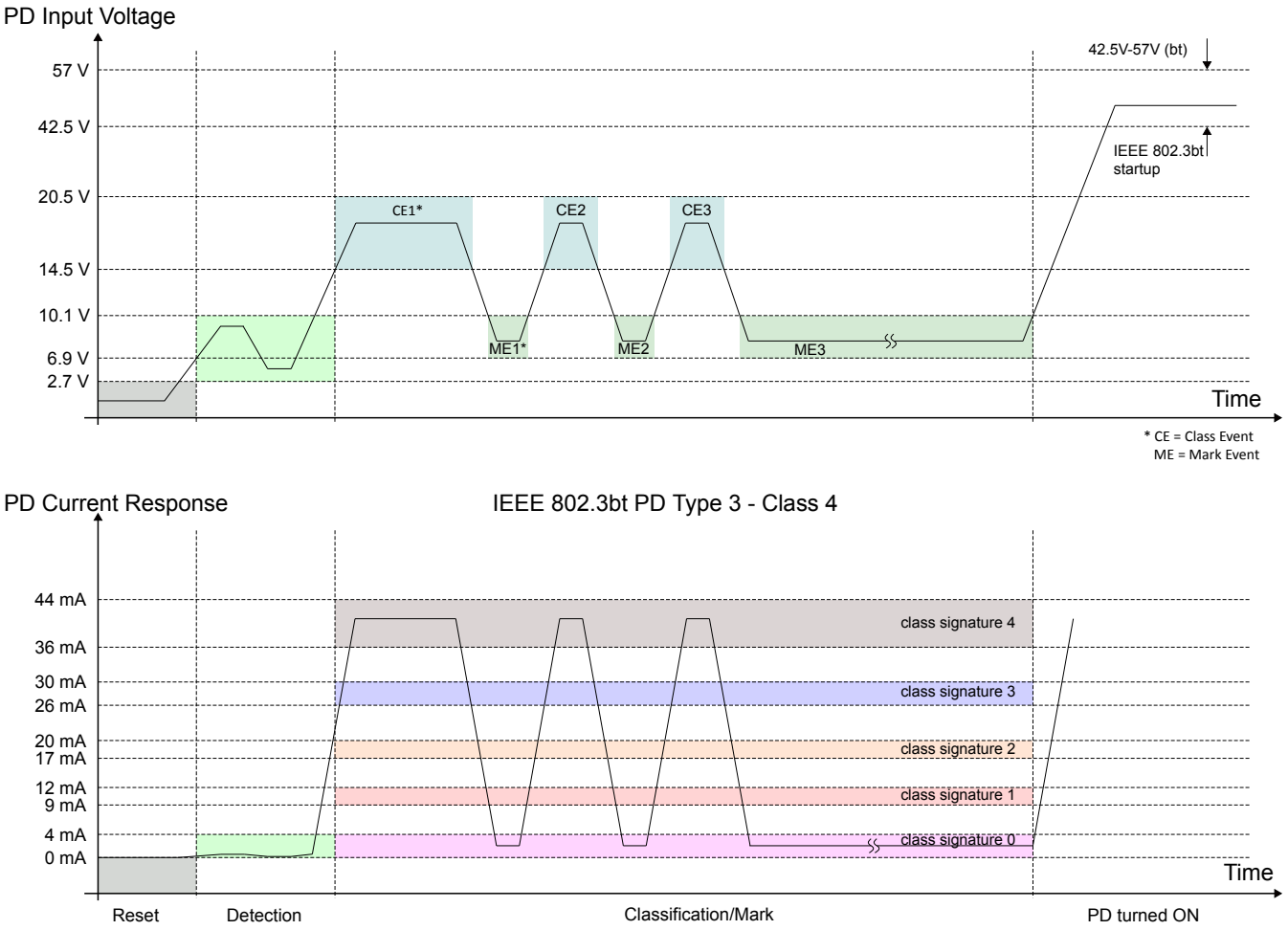


Figure 2.6. Classification Signature of Si34071 Configured as a Class 4 PD – 25.5 W

2.3.2 Type 3 – Class 5 and Class 6 – Input Power of 40.0 W and 51.0 W

The Si34071 configured as a Class 5 or Class 6 PD will give Class 4 (40 mA) signature in the first two pulses, and a lower classification signature in the subsequent two pulses; see the figures below. Third and fourth classification signatures are Class 0 (2.5 mA) for Class 5 and Class 1 (10 mA) for Class 6. Non-compliant PSEs might provide more than four pulses where the PD will continue to provide the same signature as in the third Classification Event.

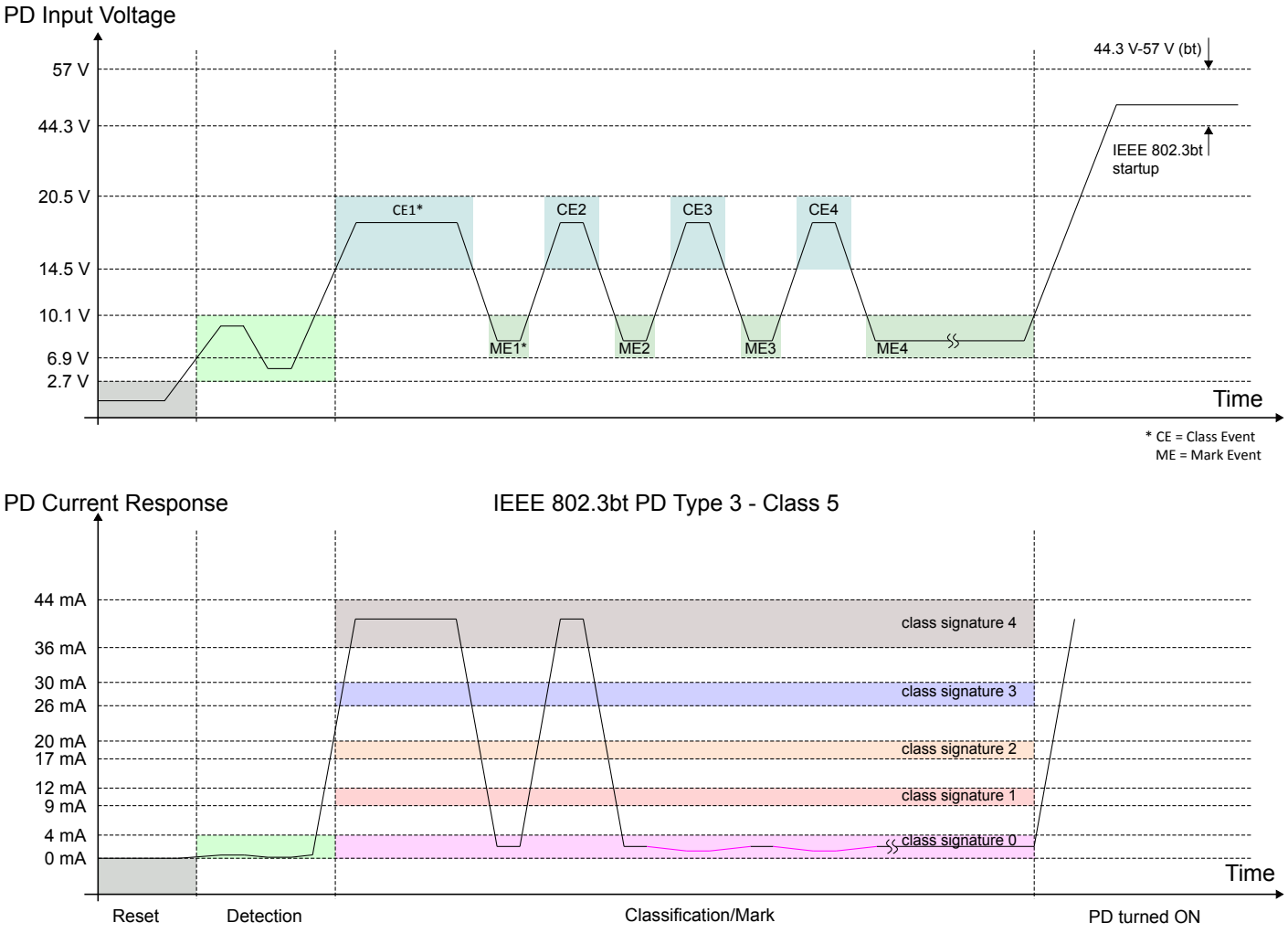


Figure 2.7. Classification Signature of Si34071 Configured as a Class 5 PD – 40 W

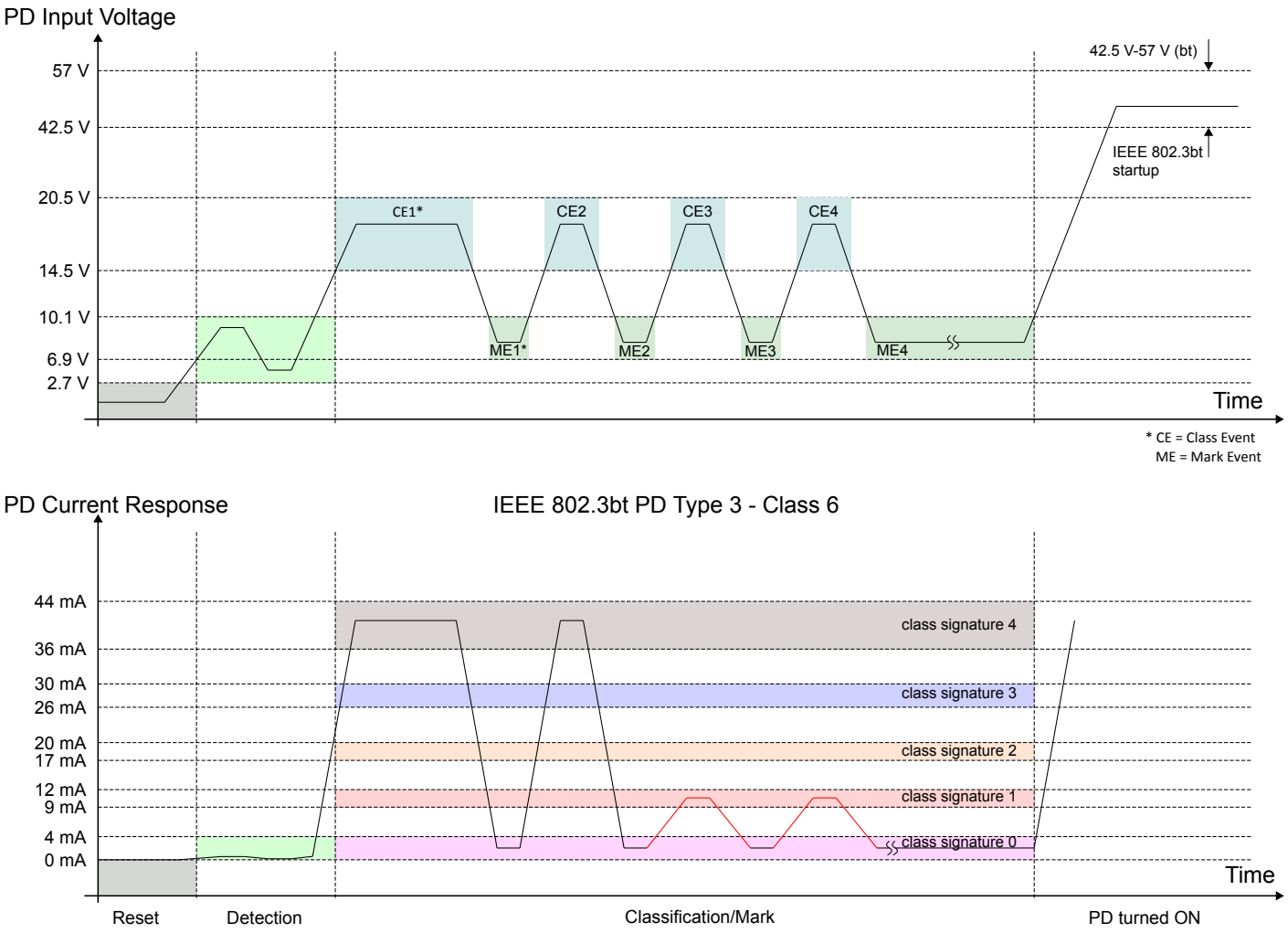


Figure 2.8. Classification Signature of Si34071 configured as a Class 6 PD – 51 W

2.3.3 Type 4 – Class 7 and Class 8 – Input Power of 62.0 W and 71.3 W

The Si34071 configured as a Class 7 or Class 8 PD will give Class 4 (40 mA) signature in the first two pulses, and a lower classification signature in the subsequent three pulses; see the figures below. Third, fourth and fifth classification signatures are Class 2 (18.5 mA) for Class 7 and Class 3 (28 mA) for Class 8. Non-compliant PSEs might provide more than five pulses where the PD will continue to provide the same signature as in the third Classification Event.

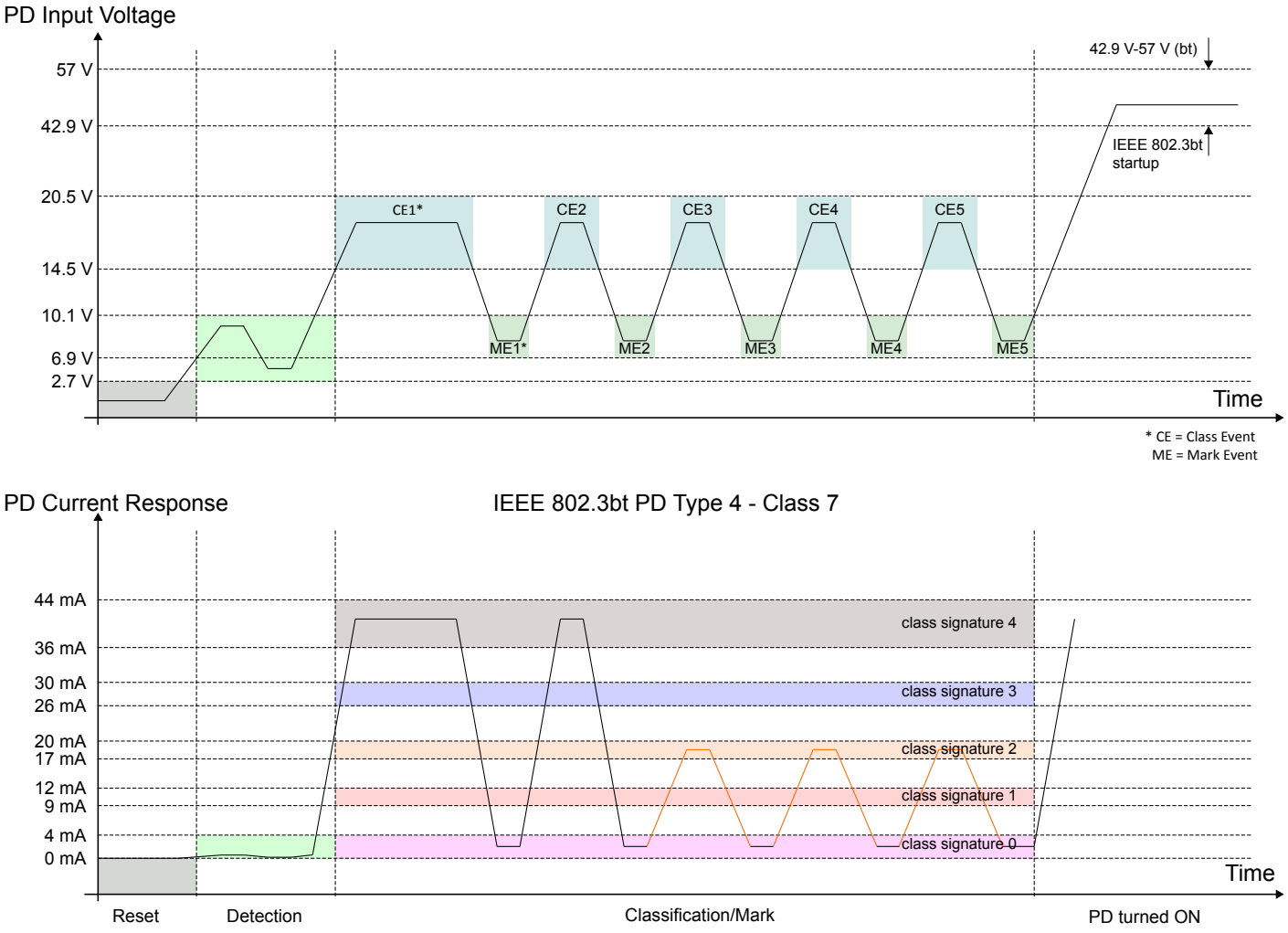


Figure 2.9. Classification Signature of Si34071 Configured as a Class 7 PD – 62W

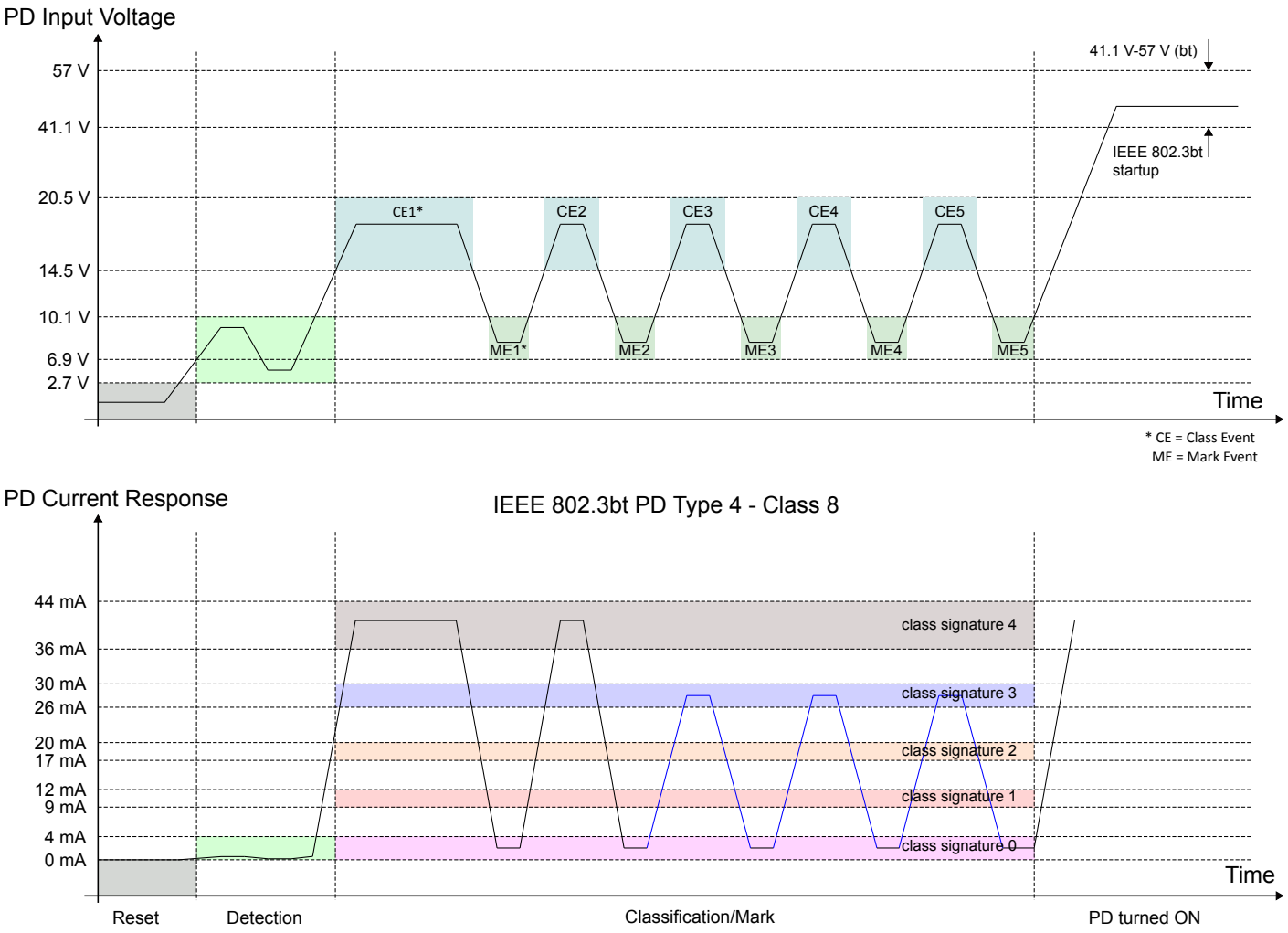


Figure 2.10. Classification Signature of Si34071 Configured as a Class 8 PD – 71.3W

2.4 PD Behavior During Mark Event

Since the voltage range forced by the PSE during a Mark event (7 V to 10 V) overlaps with the voltage range forced during the detection phase (2.7 V to 10.1 V), the PD must present an invalid detection signature during the Mark event. The Si34071 will present a high impedance (<12 kΩ) during Mark.

2.5 Type 3,4 PD Assigned Class

The Si34071 device is able to provide information to the host about the Assigned Class through UART. This information can be useful if the PD is connected to an 802.3.af or 802.3.at compliant PSE or if the PSE cannot grant power for the requested class. See 2.10 UART Configuration for details on UART setup and communication.

2.6 Autoclass

Autoclass is an optional power management technique introduced in the 802.3bt standard. If Si34071 is connected to a Type 3 or Type 4 PSE, the Autoclass feature can be utilized. A PD configured as an Autoclass device shall change its signature to class signature 0 level during the first, long classification pulse between 75.5 ms and 87.5 ms. It indicates to the Type 3 or Type 4 PSE that an Autoclass PD is connected, and it allows the PSE to measure the device's exact consumption when the PSE operates with a limited power budget. For that reason, the PD application has 1.35 seconds after start-up to switch into its maximum power state and shall maintain its maximum power consumption for at least 3.65 seconds after inrush up. While Si34071 might provide the Autoclass signature for the PSE if it has been enabled previously, the turn-on of the system's maximum power is the responsibility of the host controller. The following figure shows the classification signature of the Si34071 configured as an Autoclass PD and the time window when maximum power draw needs to be guaranteed by the host controller.

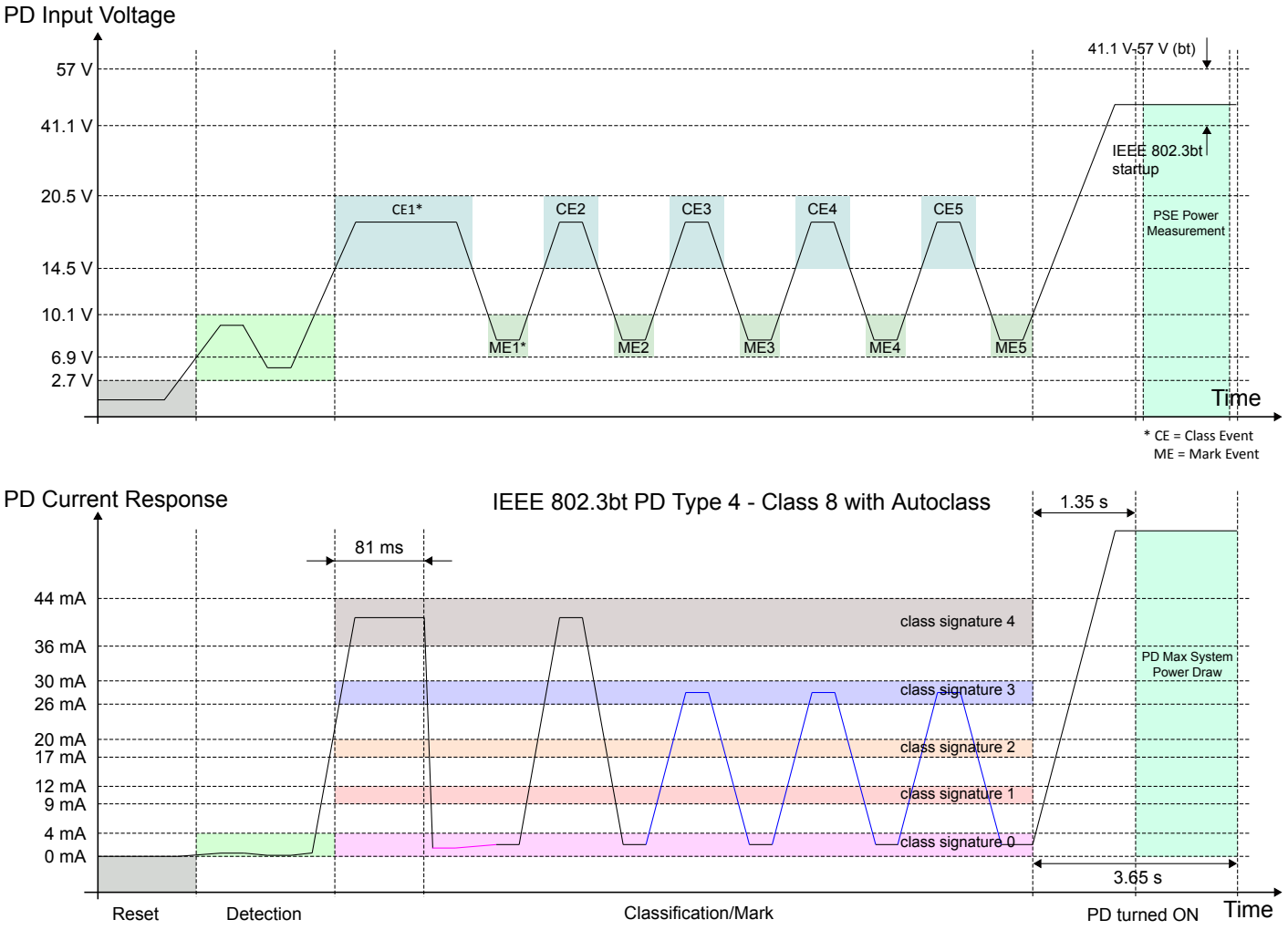


Figure 2.11. Autoclass Signature of Si34071 Configured as a Class 8 PD + AC

Autoclass is particularly beneficial in the following scenarios, presented in the following figures. In the first case, when requested power is much less than the allocated maximum power for the corresponding class, using Autoclass is a good indication that the PD does not require all that power, and allows the Autoclass-capable PSE to allocate the remaining power to other PDs. In the second scenario, when the PD is connected to the PSE with a short cable, the voltage drop on the cable will be much less than the expected maximum which requires less power to be provided by the PSE and results in significant power increase on the input side. Autoclass-capable PDs can utilize the advantages of both cases at the same time.

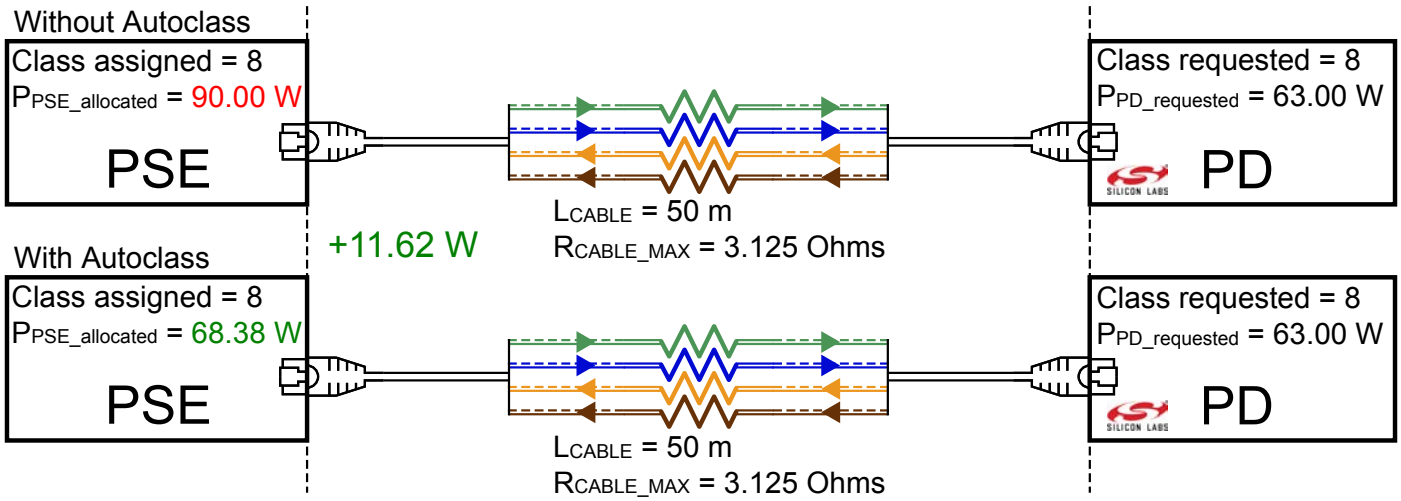


Figure 2.12. Power Difference Using Autoclass when Requested Power is Less than the Allocated

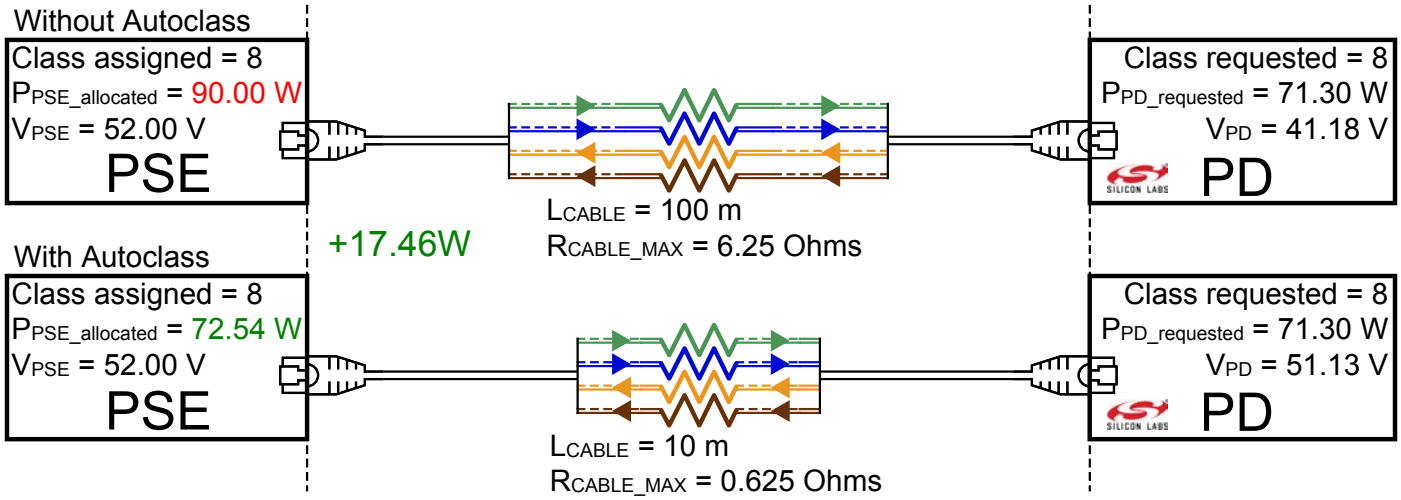


Figure 2.13. Power Difference Using Autoclass when Cable Length is Less than the Allowed Maximum

2.7 Thermal Protection During Classification

To protect the external components from overheating and damage, classification signatures are presented only until the maximum length of the classification pulses defined in the 802.3bt standard. It means 110 ms for the first, long Class Event (except when Auto-class is configured then this time is reduced to 81 ms) and 40 ms for any subsequent events.

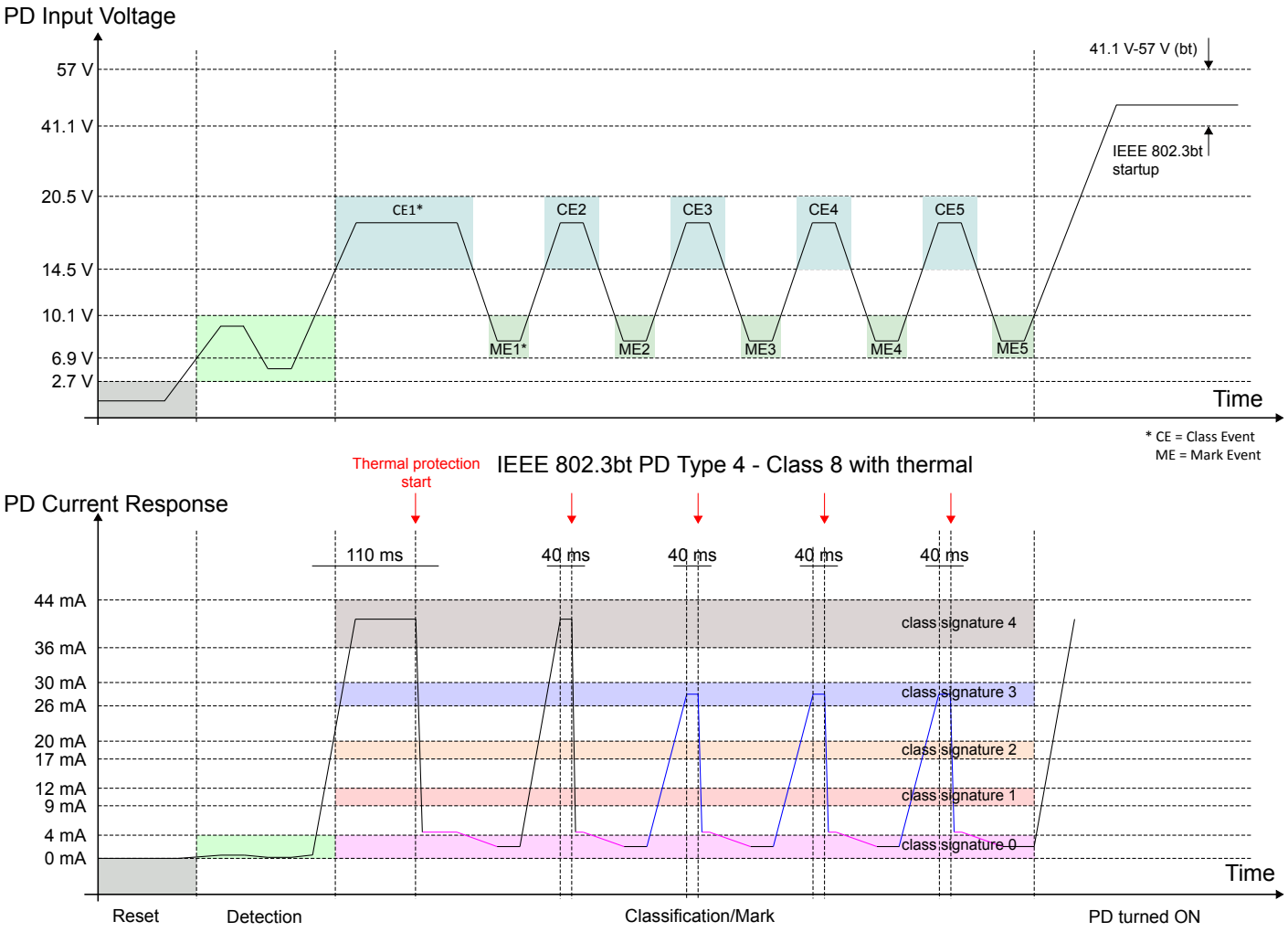


Figure 2.14. Thermal Protection of Si34071 Configured as a Class 8 PD

2.8 Apply Power

After successful detection and classifications sequences, the PSE will grant power to the PD by ramping up the voltage at the PD power interface (PI). Once the voltage at the PI exceeds 37 V (the Si34071's UVLO limit), the Si34071 hotswap switch (HSSW) enters into a current limit state to charge up dc-dc converter input capacitance. Once the capacitor is fully charged, the HSSW fully turns ON. The Si34071 has multiple resources to manage current consumption to ensure compliance: inrush control, soft-start, overload protection, and thermal shut-down.

2.9 Maintain Power Signature

The PSE is required to continuously monitor for the presence of the PD once it has been powered on by either looking for the ac impedance signature of the PD's input filter or by verifying that it is drawing current. For this reason, the Si34071's dc-dc input capacitance is required to be > 5 µF. In addition, a Type 1 or Type 2 PSE must detect minimum 75 ms continuous current draw of > 10 mA and maximum 250 ms off-time. This mandatory current draw is called Maintain Power Signature or MPS and is represented in Figures 2.15, 2.16, and 2.17 for the various standards. MPS timings and current levels of the Si34071 are shown in Figures 2.18 and 2.19.

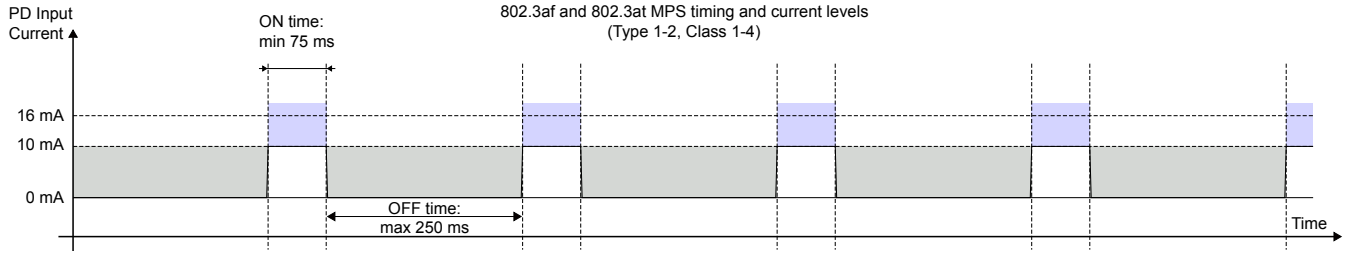


Figure 2.15. MPS Timings and Current Levels Defined in the IEEE 802.3af and IEEE 802.3at Standard

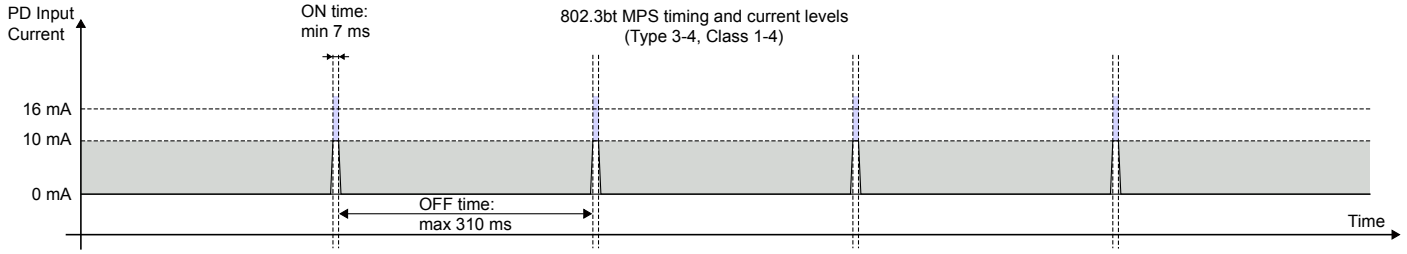


Figure 2.16. MPS Timings and Current Levels Defined in the IEEE 802.3bt Standard (Class 1-4)

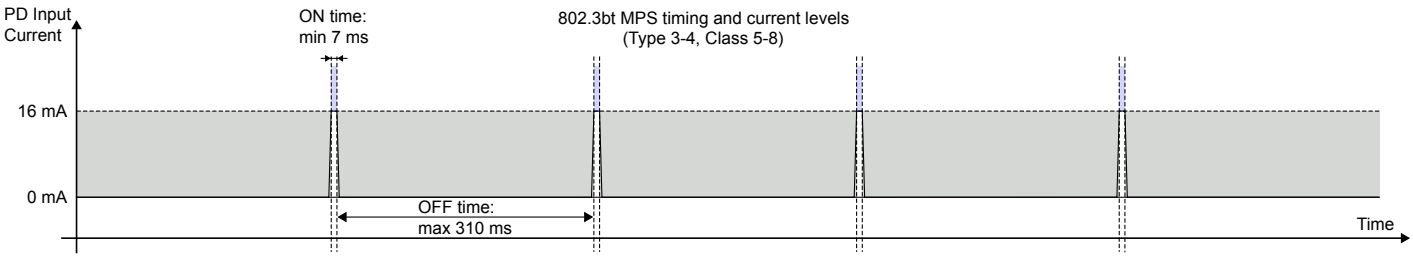


Figure 2.17. MPS Timings and Current Levels Defined in the IEEE 802.3bt Standard (Class 5-8)

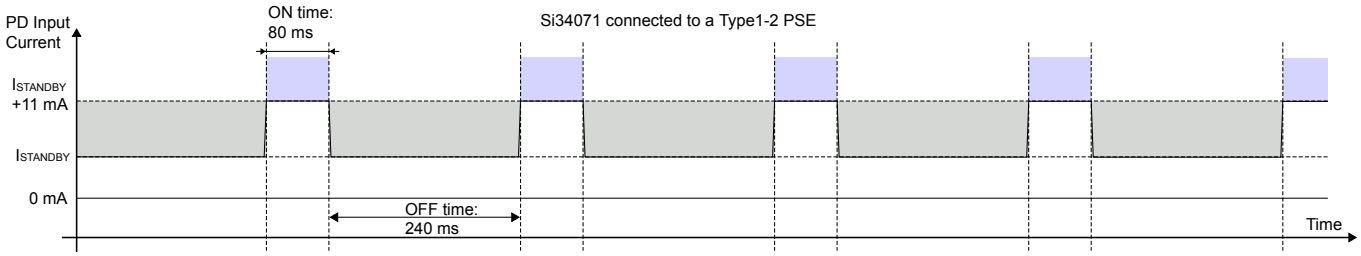


Figure 2.18. MPS Timings and Current Levels of the Si34071 Connected to a Type 1 or Type 2 PSE

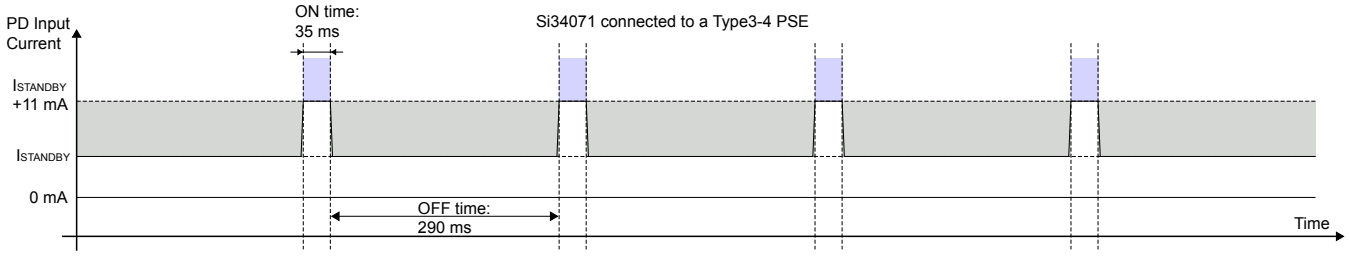


Figure 2.19. MPS Timings and Current Levels of the Si34071 Connected to a Type 3 or Type 4 PSE

2.9.1 Short MPS

With a Type 3 or Type 4 PSE connected the time length of the mandatory continuous current draw is reduced to the 1/10th of the value required by the 802.3at standard which means a minimum of 7 ms on-time and a maximum of 310 ms off-time, while the amplitude has been increased to 16 mA for Class 5–8 devices.

Si34071 offers both 802.3at and 802.3bt compliant MPS signature generation. The device automatically recognizes from the presence of a first, long Class Event if short MPS is allowed by the PSE and sets the length of the MPS pulses accordingly. To remain compliant with the newest standard a bit of extra margin has been added to the limits which has been summarized in the following table.

Table 2.6. MPS Turn-On and Drop-Off Time of Si34071

MPS Type	T_{ON}	T_{OFF}
Standard (802.3at and 802.3af) Type 1 or Type 2	80 ms	240 ms
Short (802.3bt) Type 3 or Type 4	35 ms	290 ms

To adjust the MPS current amplitude, RMPS should be modified. To achieve a current draw over the MPS limit when using the Si34071, connect R_{MPS} as shown in the figure below. The MPS feature is not automatic, it should be enabled or disabled by the host controller by sending a specific UART command to the PD. For further information about UART communication, please see the Si34071 Data Sheet.

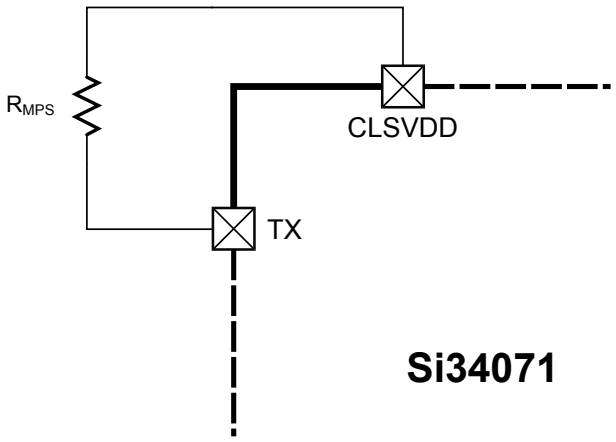


Figure 2.20. MPS Resistance R_{MPS}

The Si34071 has an optional, built-in Sleep mode for IP phone applications.

2.10 UART Configuration

UART communication is enabled when classification is done and PD is powered on. UART uses 9600 fixed baud rate and 8N1 (8 data bit, no parity bit, 1 stop bit). To ensure proper operation, check the data sheet of the chosen optocoupler for correct drive and pull-up resistor values. For connection details see the figure below.

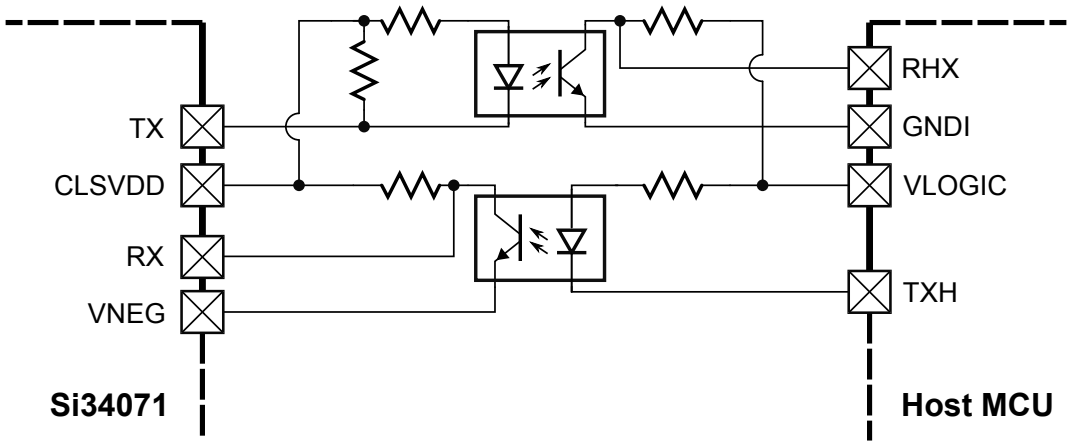


Figure 2.21. UART Connection for Isolated Designs

UART communication is based on commands. The host controller must send a 1-byte command (without any termination character), which will trigger various reactions dependent on the data that has been sent out. For detailed description of the UART commands and their responses, see the Si34071 Data Sheet.

As the RX of the host controller is also used for MPS generation, it may happen that disabling MPS and reenabling receive on the host controller happens exactly when RX line is low, causing a valid but meaningless UART transaction. It interferes with the next reply; therefore, after sending the disable MPS command (0x05), it is advisable to empty the UART data receive buffer before transmitting any commands to the Si34071 again. For details of correct UART implementation see the following figures.

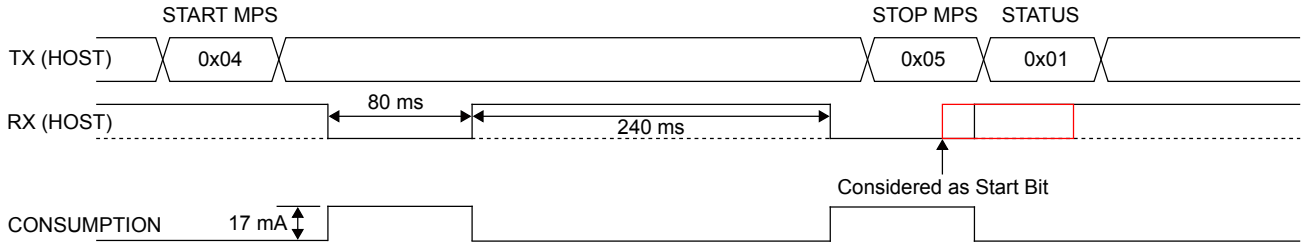


Figure 2.22. Incorrect UART Implementation

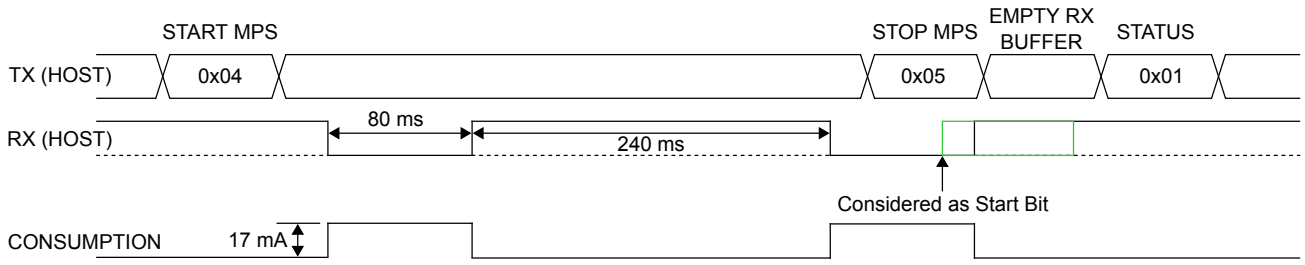


Figure 2.23. Correct UART Implementation

2.11 Sifos Compliance Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices. Si34071-5V-C8 EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies. The following table shows the test results of the Sifos Technologies 802.3bt Conformance Test Suite version 1.17.

Table 2.7. Si34071-5V-C8 EVB, 5V, Single Signature, Class 8 with Autocass PD SIFOS PoE Compliance Test Results

ALT A MDI ALT B MDI									
Detection								**Det_Cycles:**	**3**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		25.49	kΩ	25.49	25.49	25.49	23.50	26.60	P
Rdet_final_A		25.49	kΩ	25.49	25.49	25.49	23.50	26.60	P
Rdet_unpwr_A		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.49	kΩ	25.49	25.49	25.49	23.50	26.60	P
Rdet_at_Vmax_A		25.58	kΩ	25.58	25.58	25.58	23.50	26.60	P
Rdet_Voffset_A		0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		25.44	kΩ	25.44	25.44	25.44	23.50	26.60	P
Rdet_final_B		25.46	kΩ	25.46	25.46	25.46	23.50	26.60	P
Rdet_unpwr_B		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.55	kΩ	25.55	25.55	25.55	23.50	26.60	P
Rdet_at_Vmax_B		25.65	kΩ	25.65	25.65	25.65	23.50	26.60	P
Rdet_Voffset_B		0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Classification									
ClassNum		8		8	8	—	8	8	P
class_sig_EV1-2_min		39.6	mA	39.6	39.6	39.6	35.3	44.8	P
class_sig_EV1-2_max		41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min		28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max		29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI		2.41	mA	2.41	2.41	2.41	0.25	4.00	P
Tclass_max		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin		39.7	mA	39.7	39.7	39.7	35.5	44.7	P
Iclass_EV1_at_Vmax		39.9	mA	39.9	39.9	39.9	35.5	44.7	P
Class_Reset		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		83.8	ms	83.8	83.8	83.8	75.5	87.5	P

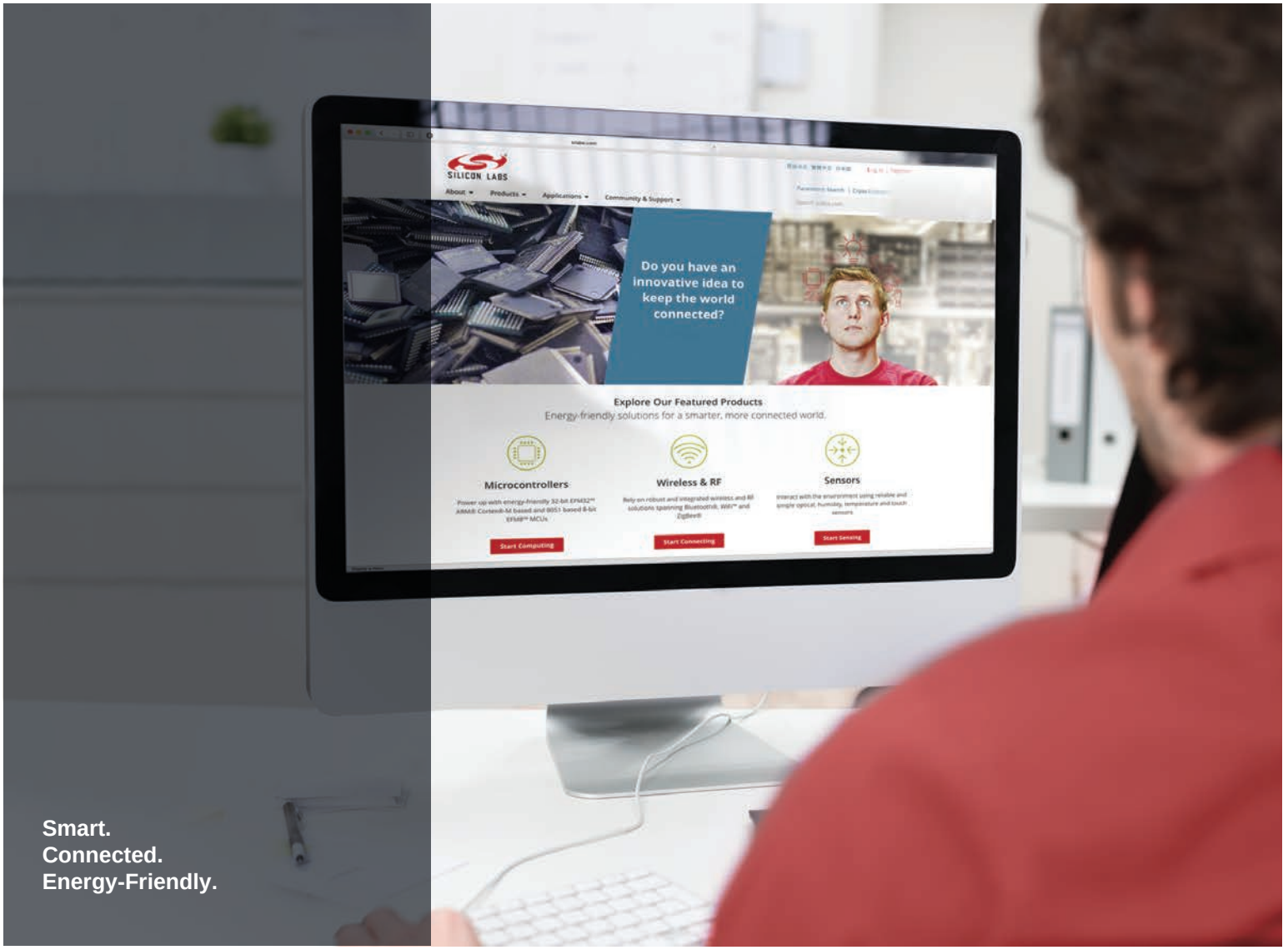
ALT A MDI-X ALT B MDI									
Detection								**Det_Cycles:**	**3**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		25.44	kΩ	25.44	25.44	25.44	23.50	26.60	P
Rdet_final_A		25.46	kΩ	25.46	25.46	25.46	23.50	26.60	P
Rdet_unpwr_A		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.67	kΩ	25.67	25.67	25.67	23.50	26.60	P
Rdet_at_Vmax_A		25.61	kΩ	25.61	25.61	25.61	23.50	26.60	P
Rdet_Voffset_A		0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		25.51	kΩ	25.51	25.51	25.51	23.50	26.60	P
Rdet_final_B		25.46	kΩ	25.46	25.46	25.46	23.50	26.60	P
Rdet_unpwr_B		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.69	kΩ	25.69	25.69	25.69	23.50	26.60	P
Rdet_at_Vmax_B		25.69	kΩ	25.69	25.69	25.69	23.50	26.60	P
Rdet_Voffset_B		0.3	VDC	0.3	0.3	0.3	0.0	1.9	P
Cdet_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Classification									
ClassNum		8		8	8	—	8	8	P
class_sig_EV1-2_min		39.2	mA	39.2	39.2	39.2	35.3	44.8	P
class_sig_EV1-2_max		41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min		28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max		29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI		2.41	mA	2.41	2.41	2.41	0.25	4.00	P
Tclass_max		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin		40.2	mA	40.2	40.2	40.2	35.5	44.7	P
Iclass_EV1_at_Vmax		40.2	mA	40.2	40.2	40.2	35.5	44.7	P
Class_Reset		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		83.8	ms	83.8	83.8	83.8	75.5	87.5	P

Power-Up / Down									
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
Iinrush		166.0	mA	166.0	166.0	166.0	0.0	800.0	P
Tinrush_energy		0.403	J	0.403	0.403	0.403	0.000	2.083	P
Iinrush_A		83.9	mA	83.9	83.9	83.9	0.0	600.0	P
Tinrush_energy_A		0.204	J	0.204	0.204	0.204	0.000	1.562	P
Imax_Tdelay_A		77.8	mA	77.8	77.8	77.8	0.0	600.0	P
Iinrush_B		82.4	mA	82.4	82.4	82.4	0.0	400.0	P
Tinrush_energy_B		0.200	J	0.200	0.200	0.200	0.000	1.040	P
Imax_Tdelay_B		76.3	mA	76.3	76.3	76.3	0.0	400.0	P
Vrefl		1.3	VDC	1.3	1.3	1.3	0.0	2.8	P
Von		36.4	VDC	36.4	36.4	36.4	30.0	42.0	P
Voff		32.9	VDC	32.9	32.9	32.9	30.0	42.0	P
Vhyst		3.5	VDC	3.5	3.5	3.5	0.0	12.0	P
2 Pair Powered Type-1 PHY		***PSE Emulation*:**		**On Time:**	**10 sec**	**Off Time:**	**10 sec**	**Vport:**	**48.0**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
MinI_1		56.2	mA	56.2	56.2	56.2	0.0	299.4	P
Vport_1		48.1	VDC	48.1	48.1	48.1	37.0	57.0	INFO
Ppeak_1		2.83	W	2.83	2.83	2.83	0.0	14.4	P
Pport_1		2.73	W	2.73	2.73	2.73	0.0	13.0	P
PeakViolation_1		0		0	0	—	0	0	P
MPSViolation_1		0		0	0	—	0	0	P
TcutWindowViolation_1		0		0	0	—	0	0	P
DutyCycleViolation_1		0		0	0	—	0	0	P
2 Pair Powered Type-2 PHY		***PSE Emulation*:**		**On Time:**	**10 sec**	**Off Time:**	**10 sec**	**Vport:**	**50.0**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
MinI_2		7.7	mA	7.7	7.7	7.7	0.0	565.0	P
Vport_2		50.2	VDC	50.2	50.2	50.2	42.5	57.0	INFO
Ppeak_2		3.28	W	3.28	3.28	3.28	0.0	28.3	P
Pport_2		2.82	W	2.82	2.82	2.82	0.0	25.5	P
PeakViolation_2		0		0	0	—	0	0	P
MPSViolation_2		0		0	0	—	0	0	P
TcutWindowViolation_2		0		0	0	—	0	0	P
DutyCycleViolation_2		0		0	0	—	0	0	P

4 Pair Powered Type-3 PHY		*PSE Emulation*:		On Time:	10 sec	Off Time:	10 sec	Vport:	50.0
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
MinI_3		9.4	mA	9.4	9.4	9.4	0.0	1070.0	P
Vport-2P_3_A		50.0	VDC	50.0	50.0	50.0	42.5	57.0	INFO
Vport-2P_3_B		50.0	VDC	50.0	50.0	50.0	42.5	57.0	INFO
Ppeak_3		3.29	W	3.29	3.29	3.29	0.0	53.5	P
Pport_3		2.89	W	2.89	2.89	2.89	0.0	3.0	P
PeakViolation_3		0		0	0	—	0	0	P
MPSViolation_3		0		0	0	—	0	0	P
TcutWindowViolation_3		0		0	0	—	0	0	P
DutyCycleViolation_3		0		0	0	—	0	0	P
4 Pair Powered Type-4 PHY		***PSE Emulation*:**		**On Time:**	**30 sec**	**Off Time:**	**10 sec**	**Vport:**	**52.0**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
MinI_4		9.8	mA	9.8	9.8	9.8	0.0	1440.4	P
Vport-2P_4_A		52.0	VDC	52.0	52.0	52.0	41.1	57.0	INFO
Vport-2P_4_B		52.0	VDC	52.0	52.0	52.0	41.1	57.0	INFO
Ppeak_4		3.23	W	3.23	3.23	3.23	0.0	74.9	P
Pport_4		3.01	W	3.01	3.01	3.01	0.0	3.1	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P
ALT A MDI ALT B MDI-X									
Detection								**Det_Cycles:**	**3**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		25.41	kΩ	25.41	25.41	25.41	23.50	26.60	P
Rdet_final_A		25.41	kΩ	25.41	25.41	25.41	23.50	26.60	P
Rdet_unpwr_A		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.54	kΩ	25.54	25.54	25.54	23.50	26.60	P
Rdet_at_Vmax_A		25.66	kΩ	25.66	25.66	25.66	23.50	26.60	P
Rdet_Voffset_A		0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		25.41	kΩ	25.41	25.41	25.41	23.50	26.60	P
Rdet_final_B		25.36	kΩ	25.36	25.36	25.36	23.50	26.60	P
Rdet_unpwr_B		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P

Rdet_at_Vmin_B	25.63	kΩ	25.63	25.63	25.63	23.50	26.60	P
Rdet_at_Vmax_B	25.64	kΩ	25.64	25.64	25.64	23.50	26.60	P
Rdet_Voffset_B	0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_B	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B	0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Classification								
ClassNum	8		8	8	—	8	8	P
class_sig_EV1-2_min	39.6	mA	39.6	39.6	39.6	35.3	44.8	P
class_sig_EV1-2_max	41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min	28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max	29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI	2.41	mA	2.41	2.41	2.41	0.25	4.00	P
Tclass_max	3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin	40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Iclass_EV1_at_Vmax	40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Class_Reset	1		1	1	—	1	1	P
Autoclass	1		1	1	—	1	1	P
Tacs	83.8	ms	83.8	83.8	83.8	75.5	87.5	P
ALT A MDI-X ALT B MDI-X								
Detection							**Det_Cycles:**	**3**
Parameter	**Cycle:**	**1**	**Units**	**Min.**	**Max.**	**Average**	**Low Lim.**	**High Lim.**	**P/F**
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		25.41	kΩ	25.41	25.41	25.41	23.50	26.60	P
Rdet_final_A		25.46	kΩ	25.46	25.46	25.46	23.50	26.60	P
Rdet_unpwr_A		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_A		25.51	kΩ	25.51	25.51	25.51	23.50	26.60	P
Rdet_at_Vmax_A		25.60	kΩ	25.60	25.60	25.60	23.50	26.60	P
Rdet_Voffset_A		0.4	VDC	0.4	0.4	0.4	0.0	1.9	P
Cdet_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_A		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Rdet_B		25.44	kΩ	25.44	25.44	25.44	23.50	26.60	P
Rdet_final_B		25.39	kΩ	25.39	25.39	25.39	23.50	26.60	P
Rdet_unpwr_B		–1.00	kΩ	–1.00	0.00	–1.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.61	kΩ	25.61	25.61	25.61	23.50	26.60	P
Rdet_at_Vmax_B		25.67	kΩ	25.67	25.67	25.67	23.50	26.60	P
Rdet_Voffset_B		0.3	VDC	0.3	0.3	0.3	0.0	1.9	P
Cdet_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P
Cdet_final_B		0.10	µF	0.10	0.10	0.10	0.04	0.13	P

Classification								
ClassNum	8		8	8	—	8	8	P
class_sig_EV1-2_min	39.6	mA	39.6	39.6	39.6	35.3	44.8	P
class_sig_EV1-2_max	41.3	mA	41.3	41.3	41.3	35.3	44.8	P
class_sig_EV3-5_min	28.0	mA	28.0	28.0	28.0	25.5	30.6	P
class_sig_EV3-5_max	29.2	mA	29.2	29.2	29.2	25.5	30.6	P
MarkI	2.41	mA	2.41	2.41	2.41	0.25	4.00	P
Tclass_max	3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin	40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Iclass_EV1_at_Vmax	40.0	mA	40.0	40.0	40.0	35.5	44.7	P
Class_Reset	1		1	1	—	1	1	P
Autoclass	1		1	1	—	1	1	P
Tacs	83.8	ms	83.8	83.8	83.8	75.5	87.5	P



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