AN1130: Si3404/06x PoE-PD Controller Design Guide

The following document provides guidelines for designing a PoE system Powered Device (PD) compliant with IEEE 802.3af Type 1 or 802.3at Type 2 standards by using the Silicon Labs Si3404 and Si3406x device families.

The Si3404 device provides the necessary detection, classification, and operating current levels compliant with IEEE 802.3af and 802.3at Type 1 PoE standards.

Si3406x devices provide the necessary detection, 2-event classification and mark for “at” flag, and operating current levels compliant with IEEE 802.3at Type 2 PoE standard.

This document provides a brief explanation of the whole PoE (Power over Ethernet) system and functionality with respect to the IEEE 802.3 standard. However, it is not to be considered as a substitute for the mentioned standard.

The Si3404 is a Type 1 device recommended for applications needing up to 15.4 W input power. The tiny 4x4 QFN package makes it ideal for systems needing low cost and compact PCB sizes.

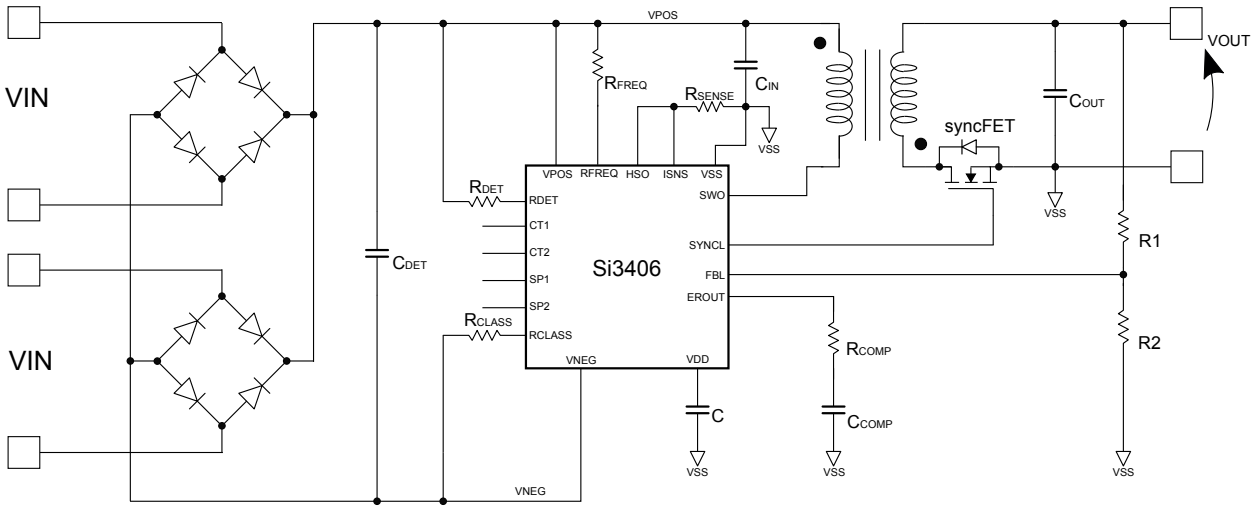
The Si3406 provides Type 2 signalization and up to 20 W of power. All the necessary components (TVS, HSSW, dc-dc Switch) for power conversion are integrated onto the device, reducing BOM costs and PCB component count.

The Si34061 is a Type 2 device capable of reaching high power (30 W) and up to 90% efficiency. It includes the same integrated components as the Si3406 with additional drivers for external switches.

The Si34062 provides Type 2 signalization and includes the same integrated high voltage components as the Si3406. The Si34062 device provides extra low standby mode, as well as integrated sleep/wake functions.

KEY FEATURES

- Small size
- High output power
- Low standby power
- Fully compliant with 802.3at



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1. Introduction to the Si340x PoE Powered Device Family

PoE makes use of the massive install base of UTP cabling for wired Ethernet networks – with multiple-billion ports worldwide. PoE (Power over Ethernet) is part of the IEEE's 802.3 Ethernet standard, which specifies the technical requirements for the safe and reliable distribution of power over the same Category-5 (CAT-5) unshielded twisted pair (UTP) cabling used for carrying data.

Designers face numerous challenges designing PoE powered applications, including maximizing efficiency, controlling EMI and minimizing cost while still delivering the necessary output power. This application note addresses these concerns by providing all of the information necessary for the user to select the proper Silicon Labs PoE Powered Device option to meet their requirements. Each product option is described in detail, along with design considerations regarding cost, efficiency, EMI performance, thermal performance and output power.

1.1 Si340x PoE-PD Product Features

The following table highlights the feature differences between the Si340x devices.

Table 1.1. PoE-PD Product Features

Feature	Si3404	Si3406	Si34061	Si34062
Type 1, Class 1-3 Signaling Support (PoE)	●	●	●	●
Type 2, Class 4 Signaling Support (PoE+)		●	●	●
Integrated TVS Surge Protection	●	●	●	●
Tunable Switching Frequency	●	●	●	●
Pulsed MPS		●	●	●
Auxiliary Bias Winding Support[1]	●		●	●
Integrated Diode Bridge[2]		●	●	●
Synchronous FET Driver		●	●	●
Integrated Switching and Hotswap FET	●	●	●	●
External Switching and Hotswap FET Support			●	
Low Voltage Auxiliary Input Supply Support			●	
Sleep Mode with Wake Control				●
LED Driver during dc-dc sleep				●
Maximum Output Power[3]	See Table 1.2 Si340x DC-DC Architecture Options on page 5.			
Package	4x4 QFN	5x5 QFN	5x5 QFN	5x5 QFN
Available dc-dc Architectures	Buck, Flyback, Non-Isolated Flyback	Buck, Flyback, Non-Isolated Flyback	Flyback, Non-Isolated Flyback	Buck, Flyback, Non-Isolated Flyback

Note:

1. Applies to Flyback architectures only.
2. Maximum input current supported by internal diode bridge is 176 mA.
3. Maximum output power depends on the dc-dc architecture. See Table 1.2 Si340x DC-DC Architecture Options on page 5 for details.

1.2 Si340x DC-DC Architectures

The Si340x devices support a variety of dc-dc architectures to meet the cost, power and efficiency targets of most designs. The following table highlights the available dc-dc architectures and their target power levels at common output voltages.

Table 1.2. Si340x DC-DC Architecture Options

Device	Output Voltage (V)	Buck		Non-Isolated Flyback		Isolated Flyback	
		Max Class	Max Output Power (W)	Max Class	Max Output Power (W)	Max Class	Max Output Power (W)
Si3404	3.3	2	7	3	15	3	15
	5	2	7	3	15	3	15
	12	3	15	3	15	3	15
Si3406	3.3	2	7	4	20	4	20
	5	2	7	4	20	4	20
	12	3	15	4	20	4	20
Si34061	3.3	—	—	4	30	4	30
	5	—	—	4	30	4	30
	12	—	—	4	30	4	30
Si34062	3.3	2	7	4	20	4	20
	5	2	7	4	20	4	20
	12	3	15	4	20	4	20

The **Buck** architecture is ideal for non-isolated Class 1 and Class 2 designs with low-cost and reasonable efficiency requirements.

The **Non-Isolated Flyback** architecture is ideal for Class 1-4 designs that do not require isolation and want to take advantage of the cost savings while still maintaining a high efficiency.

The **Isolated Flyback** architecture is ideal for Class 1-4 designs that require isolation and high-efficiency in exchange for a small increase in BOM cost.

When is Isolation Required?

Though the user should thoroughly understand the safety requirements of their design, isolation is required between all accessible external conductors, including frame ground (if any).

In addition to the safety benefits, isolated designs may achieve a higher level of noise immunity and conversion efficiency, particularly in situations where the cabling from the PSE is long. An isolated dc-dc converter uses a transformer to eliminate the dc path between its input and output thus minimizing ground loops and noise coupling from the PD input. A higher overall conversion efficiency is possible due to the turns ratio of the transformer. The turns ratio indirectly increases the efficiency, by lowering the primary current, that way reducing the power dissipation ($R*I^2$) on the switching device on the primary side.

For assistance in selecting the Si340x device and dc-dc architecture to meet your application's needs, please contact your local Silicon Labs field representative.

2. PoE Powered Devices

Power over Ethernet (PoE) is based on the IEEE standard (IEEE 802.3) for delivering power through Ethernet cables. The first PoE standard (IEEE 802.3af) was ratified in 2003 and defines a maximum PSE output power of 15.4 W. The standard evolved in 2009 (IEEE 802.3at) to extend the maximum PSE output power to 30 W.

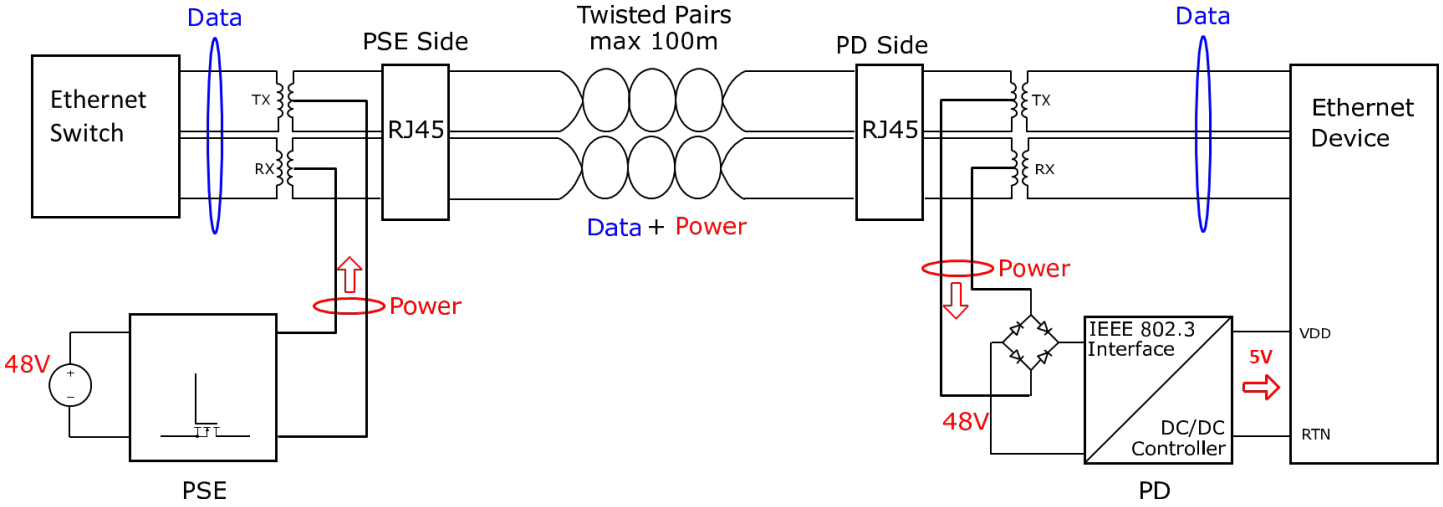


Figure 2.1. End-to-End PoE System

The following table provides a quick summary of the key differences between the IEEE 802.3 PoE standards.

Table 2.1. IEEE 802.3af/at PoE-PD Parameters

Standard	Maximum Current	Voltage Range @ PD	Name	Type	Maximum Cable Resistance	Power at PSE	Power at PD
IEEE 802.3af	350 mA	37 V – 57 V	PoE	Type 1	20 Ω (CAT3)	15.4 W	12.95 W
IEEE 802.3at	600 mA	42.5 V - 57 V	PoE+	Type 2	12.5 Ω (CAT5)	30 W	25.5 W

Attention must be paid on the losses in the system when calculating the maximum PD output power. For example, in the PoE+ (Type 2) case, if the cable length is 100m (12.5Ω), the power losses on the cable can reach 4.5W, resulting in only 25.5W on the PD input. Assuming a 90% conversion efficiency of the PD, the available power at the output of the PD is only 23W.

3. Si340x PD Controller Functional Description

The Si3404 and Si3406x PoE-PD devices integrate both the PD controller and a current mode dc-dc controller. This section will describe the operation of the PD controller portion, which includes detection, classification, inrush control and MPS (Maintain Power Signature).

3.1 PD Controller Functions

An IEEE 802.3af/at compliant PD requires a PD controller interface to communicate with the PoE-PSE source to allow it to establish and maintain a power connection. The following table summarizes the possible PSE states and the appropriate PD responses.

Table 3.1. PD Controller States

State	PSE	PD
Idle	PSE power is not connected or driving < 2.7 V	Powered off.
Detection	PSE sources two voltages between 2.7 V and 10.1V and evaluates impedance of PD	PD must present resistance between 23.7 kΩ and 26.3 kΩ and capacitance between 50 nF and 120 nF
Classification (Type 1)	PSE sources voltage between 15.5 V and 20.5 V and measures current draw of PD. Following valid Class 0–3 current measurement, PSE voltage increases to Power On voltage.	PD must present appropriate classification current (see Table 3.2 PoE Class Information on page 7)
Classification (Type 2)	PSE sources voltage between 15.5 V and 20.5 V and measures current draw of PD. Following valid Class 4 current measurement, PSE voltage drops to Mark voltage, then classification and Mark is repeated (2-event classification).	PD must present appropriate classification current (see Table 3.2 PoE Class Information on page 7). When PSE in Mark state, PD must present invalid detection impedance (<12 kΩ or >45 kΩ)
Apply Power (transition)	PSE sources voltage that exceeds turn-on voltage (UVLO limit on Si340x)	PD turns on hotswap switch (HSSW) and enforces appropriate current limiting scheme
Power On (steady state)	PSE maintains voltage above 37 V for Class 0–3 and above 42.5 V for Class 4.	PD maintains current consumption > MPS level (10 mA)
Dropout	PSE voltage falls below Si340x UVLO limit (32 V)	PD turns off and returns to idle state

Table 3.2. PoE Class Information

Class	Maximum PD Input Power (W)	Classification Type	PD Classification Current Min (mA)	PD Classification Current Max (mA)	PSE Mark Voltage Range (V)	Turn-On Voltage (V)	Turn-Off Voltage (V)
0	12.95	1	0	4	—	42	30
1	3.84	1	9	12	—	42	30
2	6.49	1	17	20	—	42	30
3	12.95	1	26	30	—	42	30
4	25.5	2	36	44	7–10	42	30

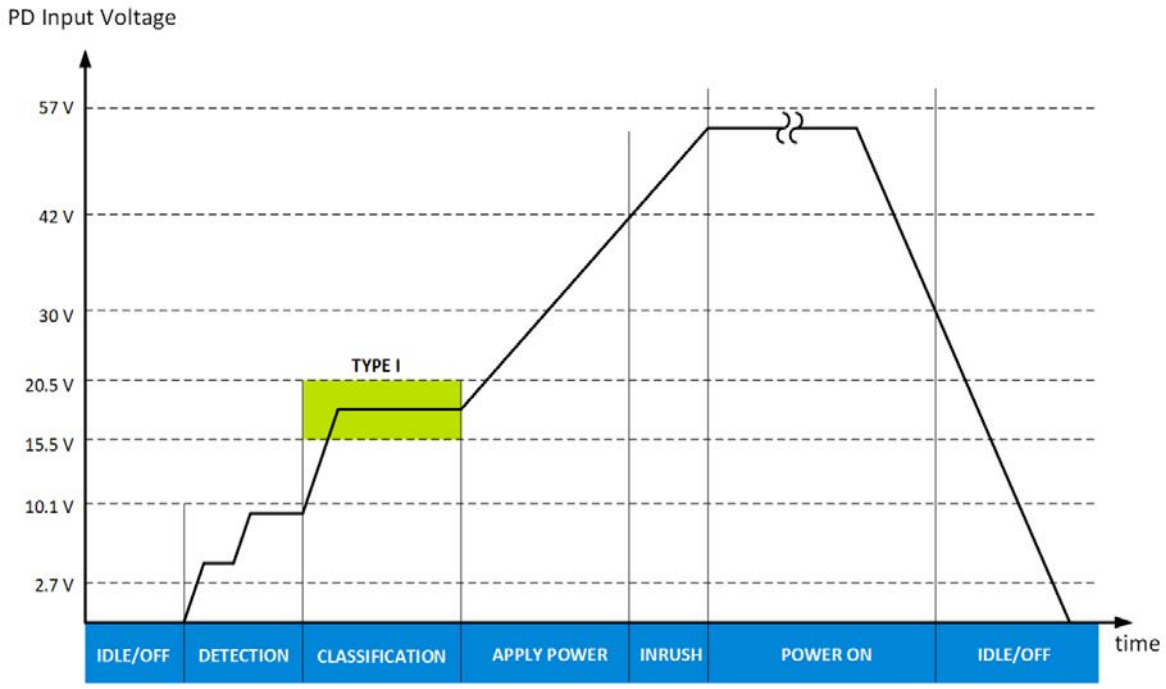


Figure 3.1. Si340x PoE States (Type 1)

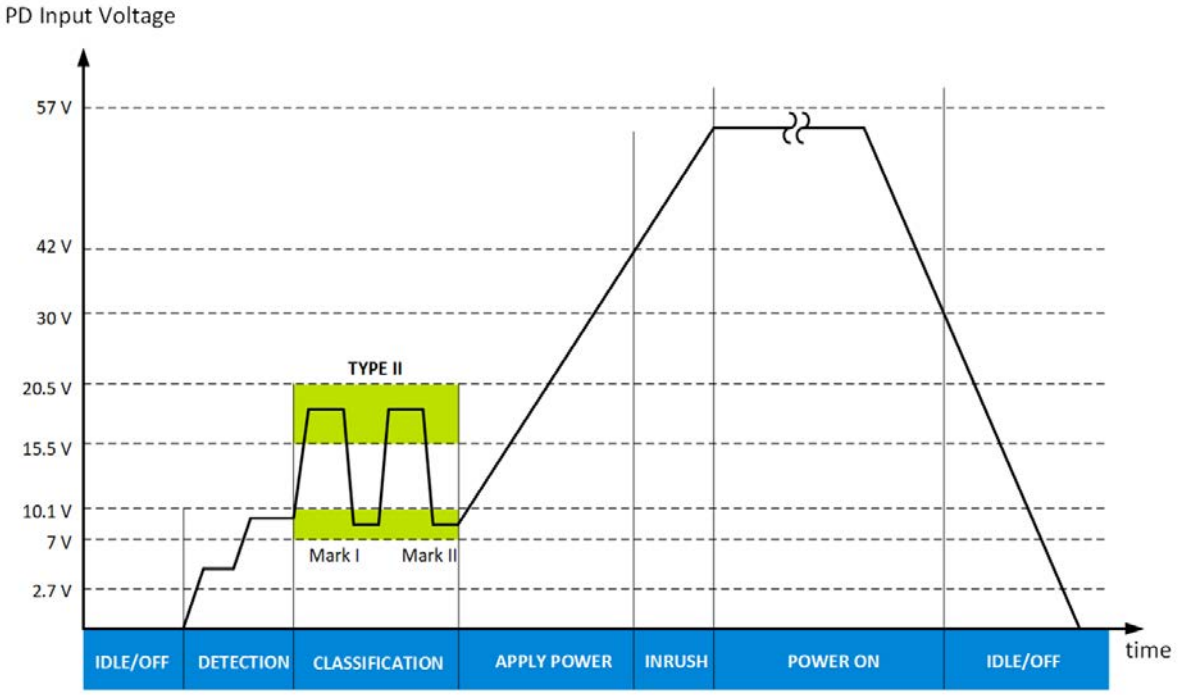


Figure 3.2. Si340x PoE States (Type 2)

3.2 Detection

During the detection phase, the PSE applies two voltages between 2.7 V and 10.1 V and measures the current draw of the connected PD. When the input voltage is in the valid detection range, the Si340x will present a detection resistance in the range of 23.7 kΩ to 26.3 kΩ to indicate to the PSE that a valid PD is connected.

The signature detection resistance presented by the Si340x is determined the external resistor R_{DET} connected to the R_{DET} pin and the type of diode bridge that is implemented. When using an external Schottky diode bridge, the high reverse leakage current of the diodes at high temperatures could result in the signature resistance violating the IEEE 802.3 specification, so a slightly larger external R_{DET} resistor is recommended in this case. The table below summarizes the recommended R_{DET} values.

The detection phase is identical for both Type 1 and Type 2 PDs.

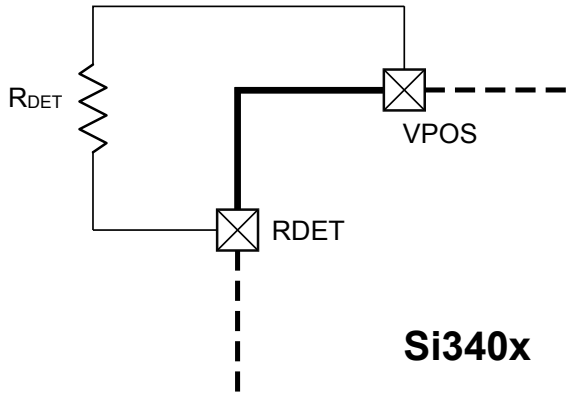


Figure 3.3. Detection Resistor R_{DET}

Table 3.3. Si340x R_{DET} Selection

Diode Bridge	Detection Resistance	Precision	Minimum Package Size	Power Rating
Internal	24.3 kΩ	1%	0201	1/20 W
Silicon	24.3 kΩ	1%	0201	1/20 W
Schottky	24.9 kΩ	1%	0201	1/20 W

In addition to presenting a valid resistance during detection, the PD must also present a capacitance between 50nF and 120nF. This is established on the Si340x by populating a ceramic, low ESR C_{DET} with 100 nF nominally.

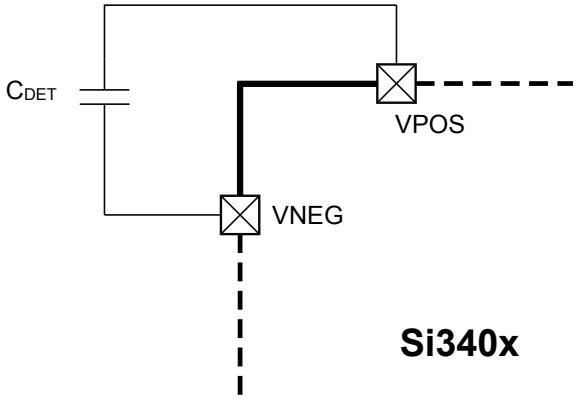


Figure 3.4. Detection Capacitance C_{DET}

3.3 Classification

After a successful detection, the PSE transitions to the classification stage and raises the voltage between 15.5 V and 20.5 V. The PSE measures the current draw and determines the requested Class. The PD will draw current in the range of the desired Class, as listed in the table below.

The Si340x sets the classification current by the value of the resistor R_{CLASS}. The table details the recommended R_{CLASS} values for each power Class, while the relationship of the selected R_{CLASS} to the classification current I_{CLASS}, is as follows:

$$R_{CLASS} = \frac{1.35V}{I_{CLASS}}$$

Equation 1.

Table 3.4. Si340x R_{CLASS} Selection

PoE Type	PoE Class	Class Current Min (mA)	Class Current Max (mA)	R_{CLASS} (Ω)	Minimum Package Size	Minimum Power Rating (W)
Type 1	Class 0	0	4	open	—	—
Type 1	Class 1	9	12	140	0201	1/20
Type 1	Class 2	17	20	75	0201	1/20
Type 1	Class 3	26	30	48.7	0201	1/20
Type 2	Class 4	36	44	33.2	0402	1/16

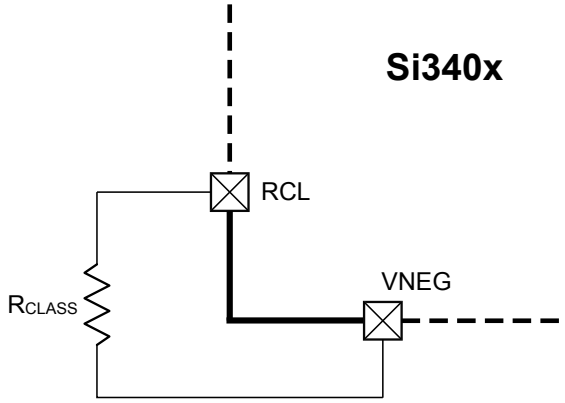


Figure 3.5. Classification Resistor R_{CLASS}

3.4 Type 1 Classification

If the PSE detects a current in the Class 0-3 range, then it will proceed to apply the full Type 1 PoE voltage to the PD (see Figure 3.1 Si340x PoE States (Type 1) on page 8). If the PSE detects a current in the Class 4 range, then a Type 2 classification is in progress.

3.5 Type 2 Classification

During a Type 2 classification (Class 4 for 802.3at), after detecting a valid Class 4 current, the PSE will drop the voltage to the Mark level (between 7 V and 10 V). It will then repeat this sequence again (Classification, Mark) in what is called a 2-Event Classification. If the 2-Event classification is successful, the PSE will proceed from the 2nd Mark state to apply the full Type 2 PoE voltage to the PD (see Figure 3.2 Si340x PoE States (Type 2) on page 8).

3.6 PD Behavior During Mark Event

Since the voltage range forced by the PSE during a Mark event (7 V to 10 V) overlaps the voltage range forced during the detection phase (2.7 V to 10.1 V), the PD must present an invalid detection signature during the Mark event. The Si340x will present a high impedance (>45 kΩ) during mark.

3.7 Type 2 PD Connections Status

The Si3406x devices provides a digital output pin, nT2P, to indicate that a successful Type 2 classification occurred. The nT2P pin is an active-low signal that is low during detection and classification and if a successful Type 2 classification occurred, nT2P will remain low after the full PoE voltage is applied. If the PSE did not support the Type 2 classification yet provided the full PoE voltage at the PD input, nT2P will transition high to indicate that only Type 1 power levels may be consumed (up to 12.95 W). See Figure 3.7 Full Start-up with Type 2 PD and Type 1 PSE, nT2P Transitions High on page 12 and 3.10 Output Voltage Protection for nT2P behavior.

3.8 Apply Power

After successful detection and classifications sequences, the PSE will grant power to the PD by ramping up the voltage at the PD input (PI). Once the voltage at the PI exceeds 37V (the Si340x's UVLO limit), the Si340x may now consume power up to the classified limit. To connect power to the PDs dc-dc converter, either the integrated low-side hotswap switch (HSSW) or an external FET is turned on (see 3.14 Using an External HSSW for more information on using an external FET). Connecting the dc-dc converter's depleted capacitor tanks and starting up the dc-dc converter requires significant current which must be limited at startup to comply with the IEEE 802.3 specification. The Si340x has multiple resources to manage current consumption to ensure compliance – inrush control, soft-start, overload protection and thermal shut-down.

3.9 Inrush Control

Depending on the PSE voltage ramp rate, the current to charge C_{IN} can be quite large and needs to be limited to protect the dc-dc capacitor tank. The HSSW will current limit the inrush current at 170 mA (see figure below) and remain in a current limiting mode until C_{IN} is charged to 99% of the PI voltage. As the dc-dc converter is starting up (covered in 5.1 Soft Start), the HSSW will continue to limit the inrush current as C_{IN} is depleted due to the high current demand.

For Type 1 PDs, the dc-dc converter may be turned on immediately after inrush current limiting stops. For Type 2 PDs, an 80ms delay is required from the time the HSSW stops inrush current limiting until the dc-dc is turned on. See 3.10 Output Voltage Protection for full Type 2 PD start up sequence.

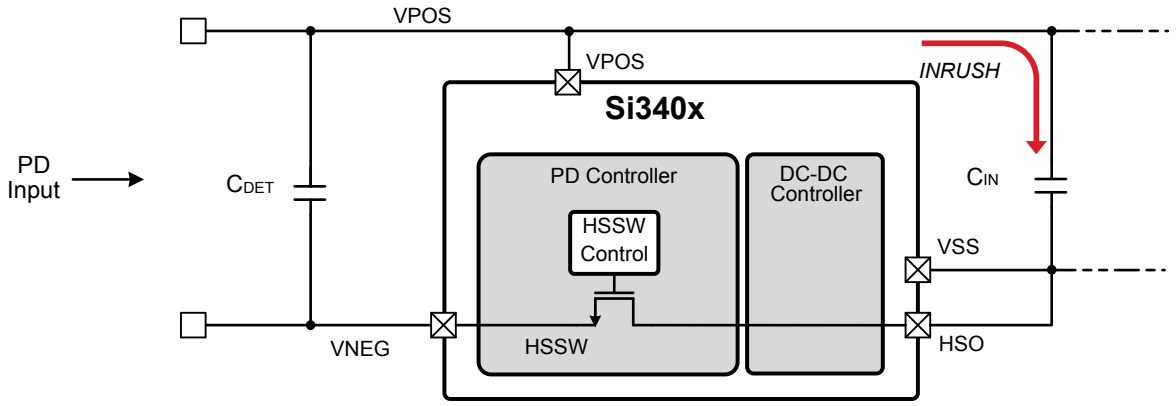


Figure 3.6. Inrush Control

3.10 Output Voltage Protection

Though the dc-dc controller turn-on is initiated by the Si340x's PD controller, the soft-start feature is part of the dc-dc controller functionality and is covered in 5.1 Soft Start. The Type 2 PD will be treated as a Class 0 device when it is connected to the Type 1 PSE. In this case, 15.4 W is granted to the PD.

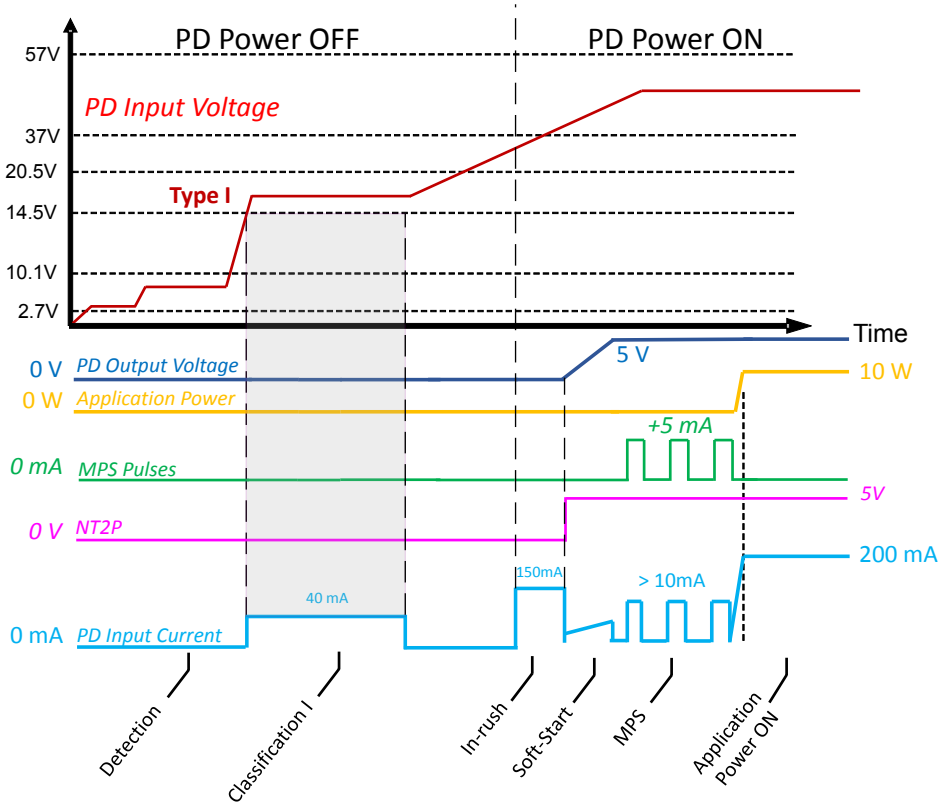


Figure 3.7. Full Start-up with Type 2 PD and Type 1 PSE, nT2P Transitions High

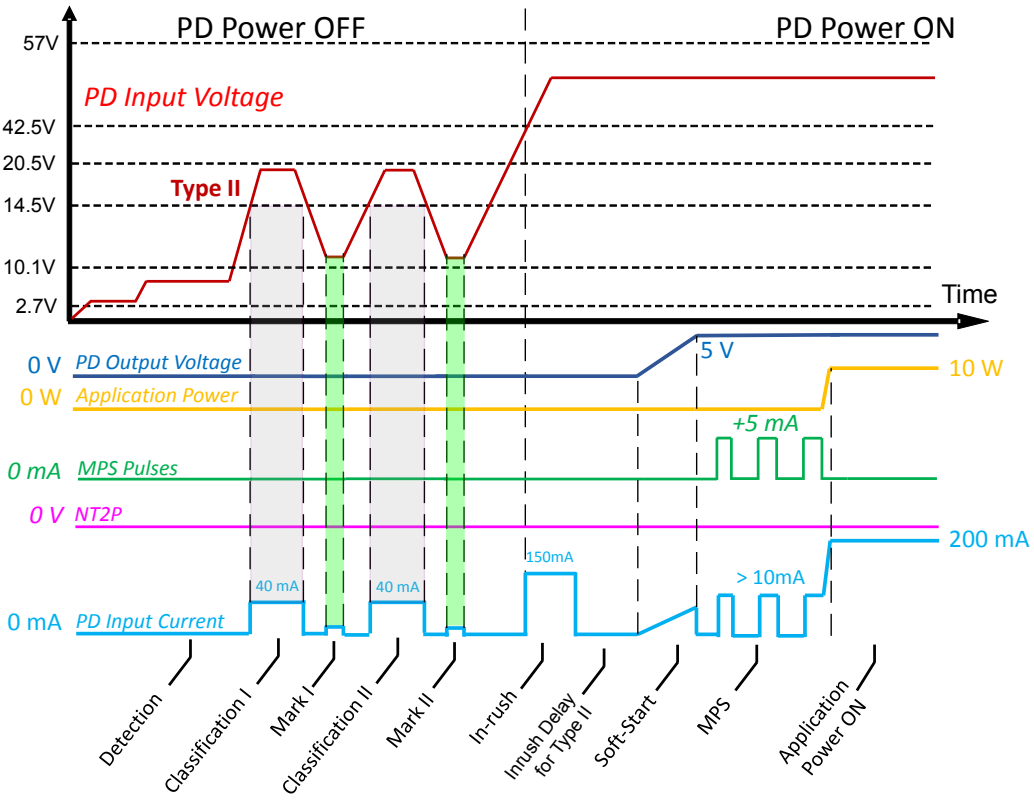


Figure 3.8. Full Start-up with Type 2 PD and Type 2 PSE, nT2P Remains Low

3.11 Overload Protection

During steady-state operation, by monitoring the HSSW drain-source voltage, the Si340x's HSSW control can detect an excessive overload condition and limit the current through the switch (internal or external) to 10 mA to prevent thermal stress. If the V_{DS} of the HSSW exceeds 3.5V for 140 µs, the overload state (OVLD) is entered. The OVLD condition is cleared once the V_{DS} of the HSSW falls below 380 mV for 80 ms, and the HSSW will return to the on state. The figure below highlights the HSSW control states.

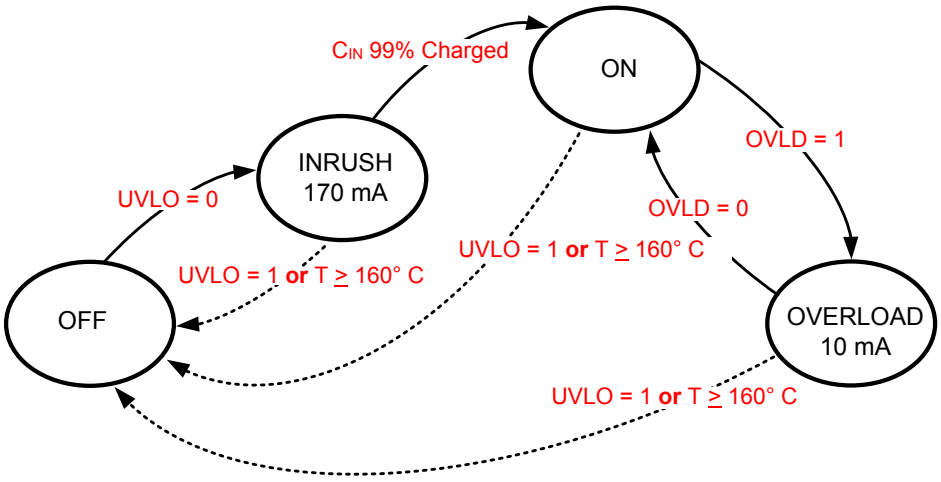


Figure 3.9. HSSW State Diagram

3.12 Thermal Shutdown

The HSSW has an integrated thermal sensor to protect the Si340x from thermal stress. If the temperature exceeds 160°C at any time, the HSSW is turned off.

3.13 Under-Voltage Lockout (UVLO)

The UVLO feature ensures the Si340x complies with the IEEE 802.3 specification and does not consume power if the voltage available at the PD input falls below the specified level. The figure below describes the UVLO behavior of the Si340x family.

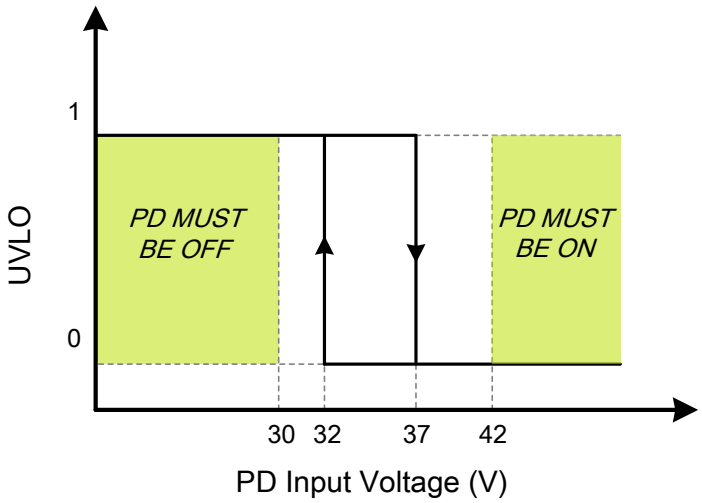


Figure 3.10. Si340x UVLO Behavior

3.14 Using an External HSSW

The Si34061 device supports the use of an external FET as the HSSW to reduce thermal stresses on the integrated HSSW and improve overall conversion efficiency. Silicon Labs recommends use of an external HSSW for continuous input currents that exceed 350mA to ensure the internal HSSW is not stressed at high ambient temperatures.

When using an external HSSW, an NMOS type FET needs to be connected directly to the EXTHSW pin, between VNEG and HSO. The added FET will be in parallel with the internal HSSW. Both FETs will be operational, but their loading will be tightly controlled by the HSSW controller. Based on the average input current (see 5.5 Average Current Sensing—ISNS and 6.7 Power Modes of the Converter for details), the controller decides whether the internal or external HSSW will conduct.

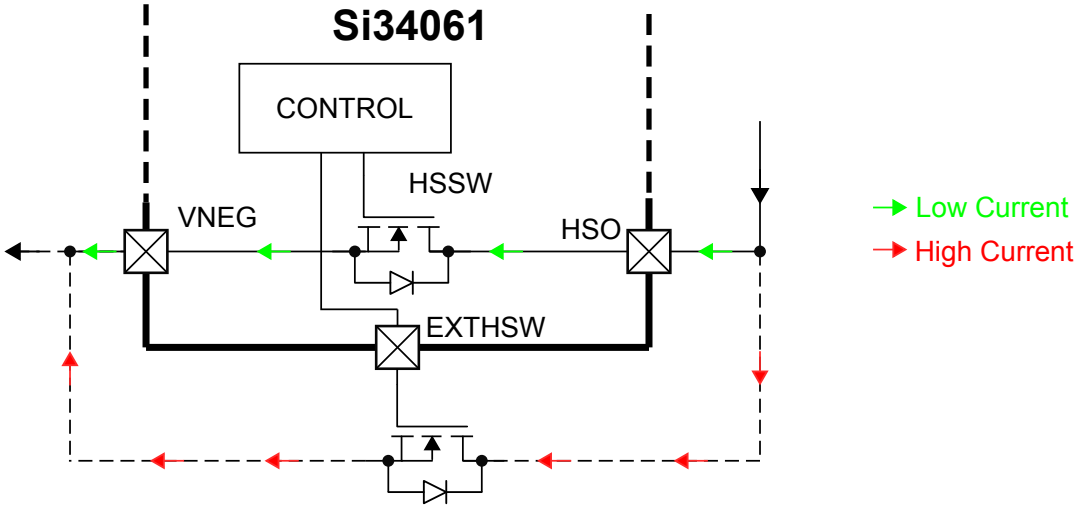


Figure 3.11. External HSSW Connections

If an external HSSW is not installed, the EXTHSW pin should be tied to VNEG, causing the current to flow through the internal HSSW. The EXTHSW driver controls the external FET with 10 V logic level, relative to VNEG.

See 6.6 External FET Detection for external FET detection details.

3.15 Maintain Power Signature

The PSE is required to continuously monitor for the presence of the PD once it has been powered on by either looking for the ac impedance signature of the PD's input filter or by verifying that it is drawing current. For this reason, the Si340x's dc-dc input capacitance is required to be > 5 µF. In addition, the PSE must detect an average current draw of > 10 mA in any 300 ms window. This mandatory current draw is called Maintain Power Signature, or MPS.

To achieve a current draw over the MPS limit when using the Si3404, the application must consume at least 250 mW in the lowest power state.

The Si3406x devices integrate an automatic MPS circuit that dynamically adds quiescent current draw to ensure the MPS condition is satisfied. This feature is enabled by pulling down the nSLEEP pin. When nSLEEP is active, the Si3406x will pulse current if the sensed application current is < 10 mA.

On the Si3406 and Si34061 devices, the nSLEEP pin is used to enable or disable the MPS pulse generation. MPS pulses can be generated in two ways:

1. in Automatic (consumption based) mode and
2. in User mode

The following figure shows the flowchart of the different MPS enabling schemes.

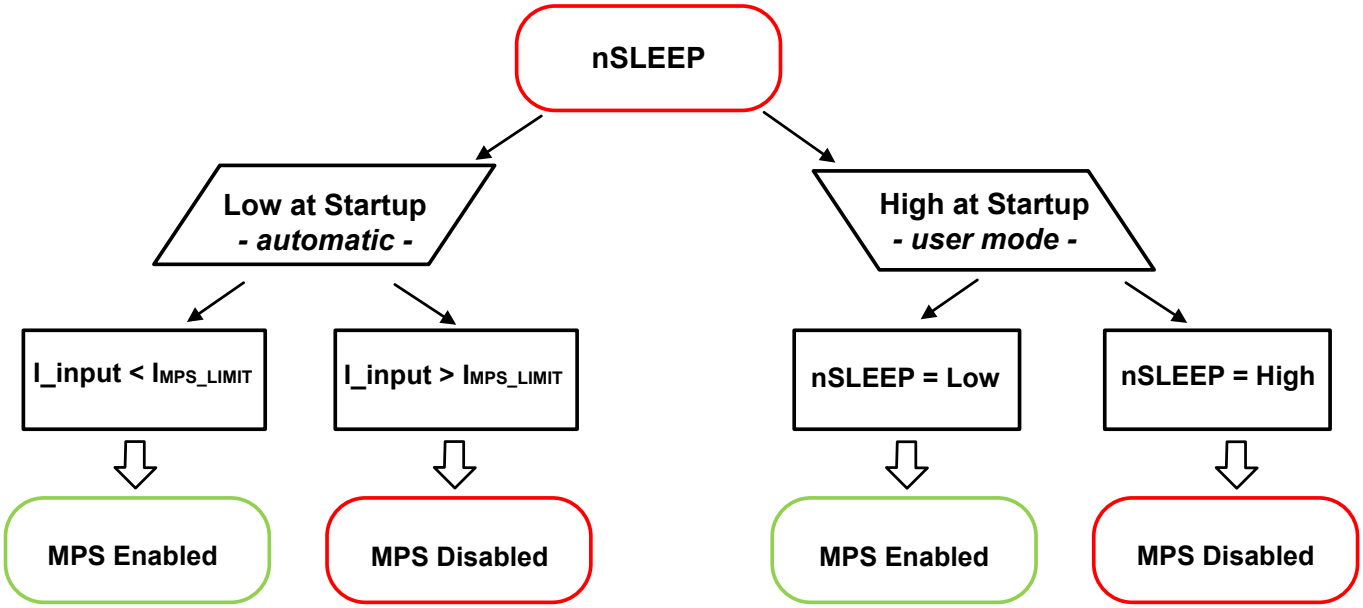


Figure 3.12. MPS Activation Flowchart

3.16 Automatic-Mode MPS (Consumption Based)

When nSLEEP is low at t0 (at HSSW turns ON), MPS generation depends on chip current consumption:

- If I_input < MPS ON LIMIT, MPS is enabled (to stay connected with the PSE)
- If I_input > MPS OFF LIMIT, MPS is disabled (not to degrade PD efficiency)

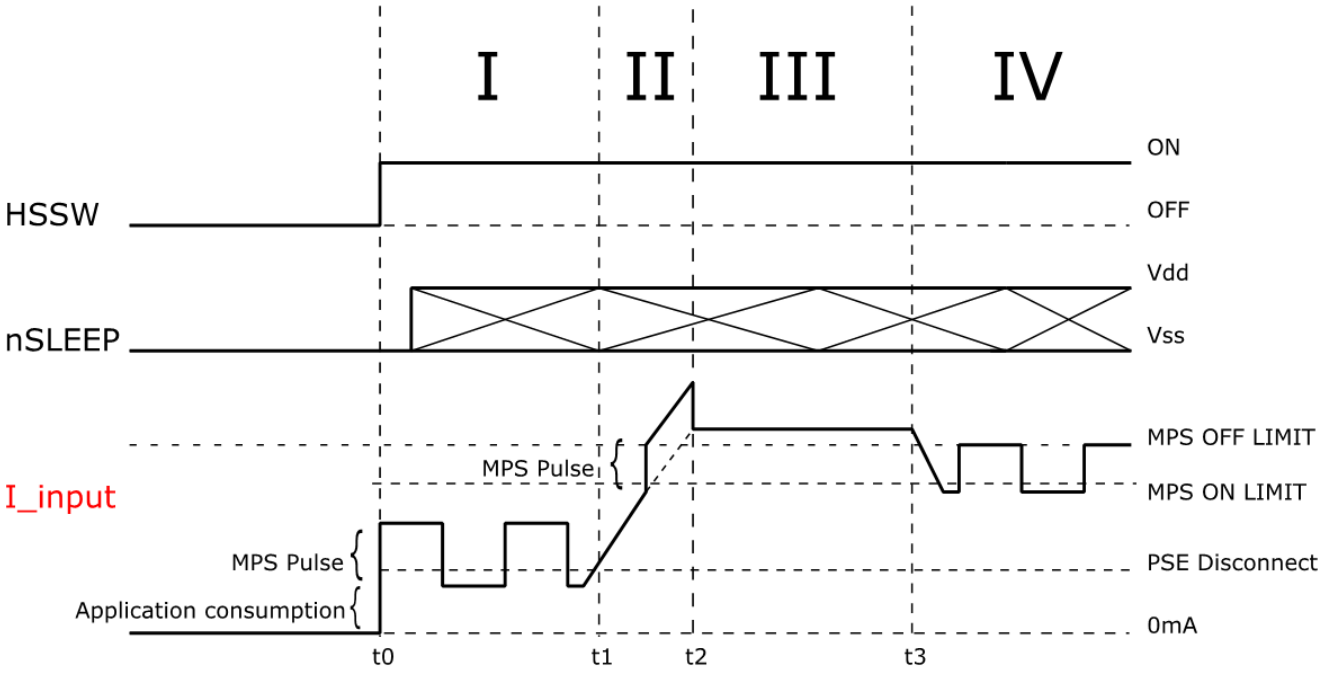


Figure 3.13. Automatic Mode MPS, Consumption Based

t0 – PD turns ON (HSSW gets enabled), I_input < MPS ON LIMIT, nSLEEP is low, MPS enabled

t1 – application consumption starts rising, MPS still enabled

t2 – application consumption + MPS pulses exceeds MPS OFF LIMIT, MPS disabled

t3 – application consumption drops below MPS ON LIMIT, MPS enabled

I: at t0 nSLEEP is low, automatic mode MPS activated, MPS pulses enabled because I_input < MPS ON LIMIT

II: application consumption starts rising, MPS pulses still enabled

III: application consumption is above MPS OFF LIMIT, MPS pulses disabled

IV: application consumption drops below MPS ON LIMIT, MPS pulses enabled again

3.17 User-Mode MPS

When nSLEEP is high at t0 (at HSSW turns ON), MPS generation depends on nSLEEP. The user controls MPS pulse generation by pulling nSLEEP high or low:

- if nSLEEP is high, MPS disabled (independent of the current consumption)
- if nSLEEP is low, MPS enabled (independent of the current consumption)

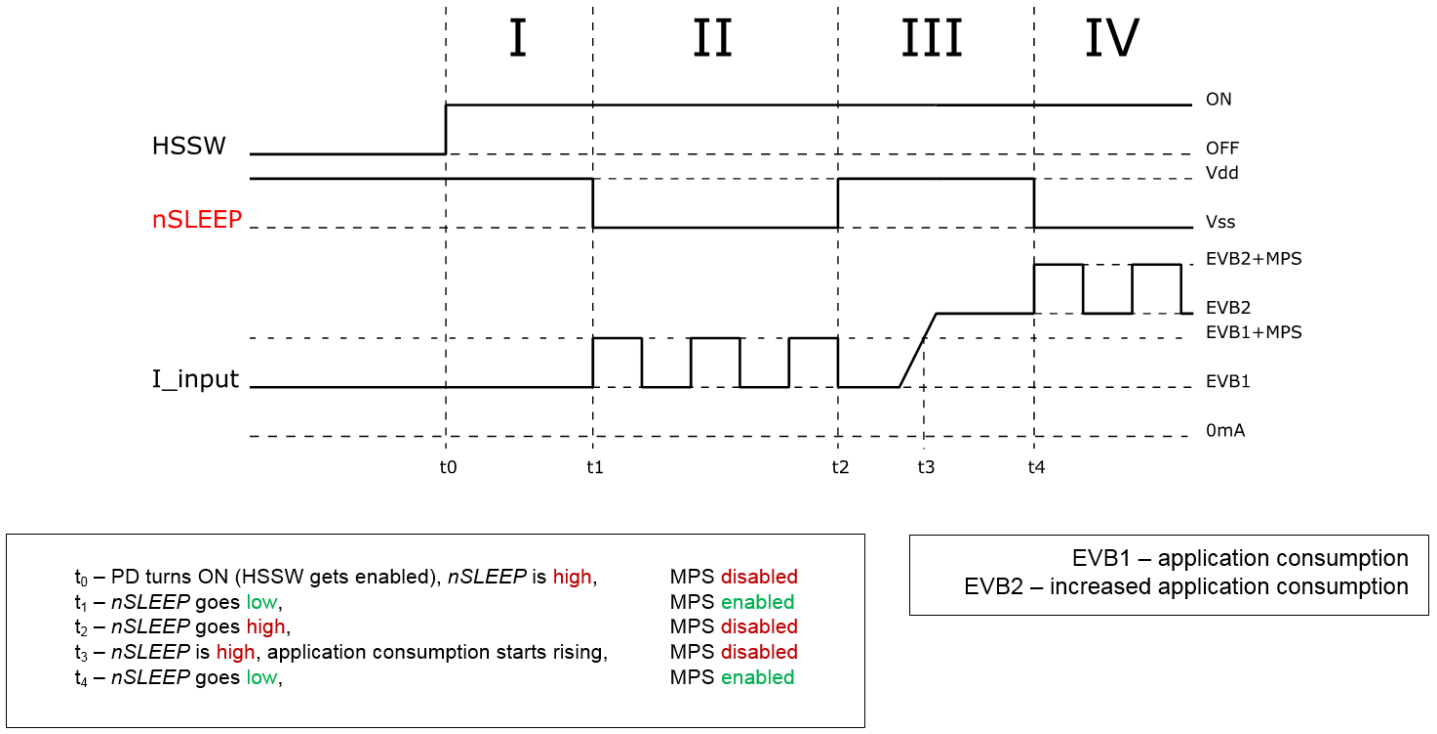


Figure 3.14. User Mode MPS

I: at t0 nSLEEP is high, user mode MPS activated, MPS circuit is disabled

II: nSLEEP is low, MPS is enabled

III: nSLEEP is high, MPS is disabled independently of current consumption

IV: nSLEEP is low, MPS is enabled independently of current consumption

4. Si340x PD Physical Interface

The power to the PD is delivered as a common mode signal on two of the four ethernet pairs. This can originate from a remote PSE or a local PoE power injector. Since the voltage may appear on either the ALT-A or ALT-B pairs and the polarity of the voltage is not known, a diode bridge is required on each pairset to ensure a positive polarity voltage is passed to the dc-dc converter.

The following section discusses the physical interface of the Si340x family to the Ethernet transformer, including the diode bridge, surge protection options and how to power from an auxiliary supply.

4.1 Using the Si3406x Internal Diode Bridge

The Si3406x devices include an integrated diode bridge as shown in the figure below with the pairsets connected to CT1/CT2 and SP1/SP2 respectively. This bridge will rectify the PoE voltage from either pairset and produce a positive voltage between VPOS and VNEG. Note that the Si3404 device does not include an integrated diode bridge, therefore an external bridge must be used.

The internal diode bridge has limited power capability and may only be used for Class 1 and Class 2 applications up to 10 W.***For applications > 10 W input power, use of an external diode bridge is required***.

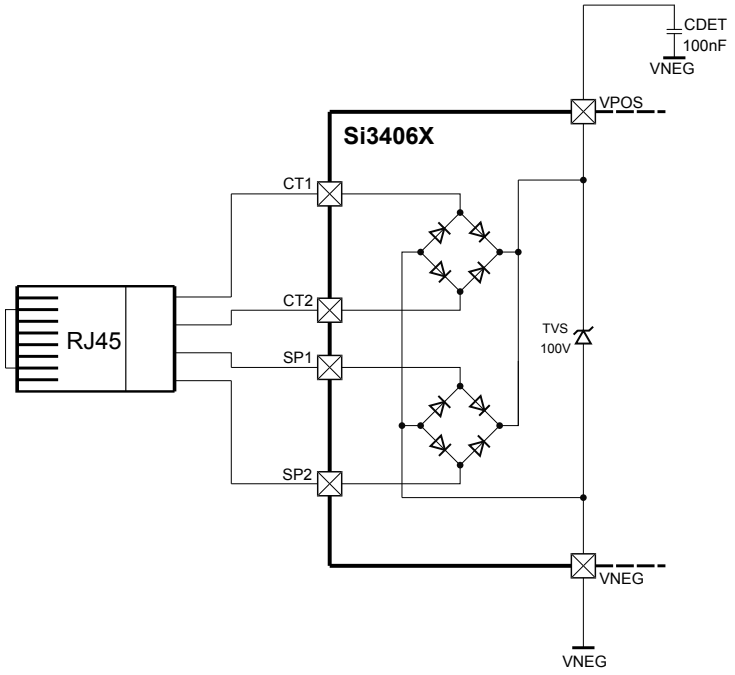


Figure 4.1. Si3406x Integrated Diode Bridge and Surge Protection

4.2 Using an External Diode Bridge on the Si3406x

All Si3406x devices support the use of an external diode bridge. For applications > 10W, an external diode bridge *must* be used.

When using an external diode bridge, if CTx/SPx are not connected, then the external bridge must be Schottky type. If CTx/SPx are connected in parallel with the external bridge (see figure below), then either Schottky or Silicon diodes may be used, however, the diode bridge must have a maximum forward voltage of 2 x 0.65 V = 1.3 V at 50 mA.

See the figure below for Si3406x connections to the external diode bridge. See 3.2 Detection regarding detection resistor selection when using an external Schottky bridge.

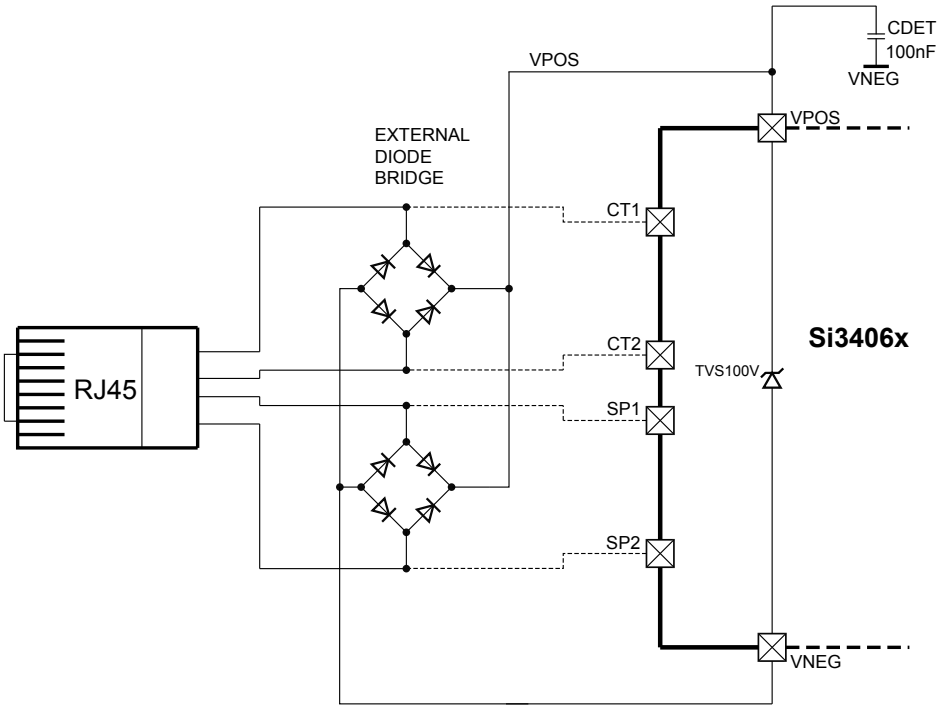


Figure 4.2. Si3406x with External Diode Bridge and Integrated Surge Protection

4.3 Using an External Diode Bridge on the Si3404

Since the Si3404 does not include an integrated diode bridge, an external diode bridge must be used. There are no restrictions on what type of diodes are used since there are no parallel connections. The external bridge connections to the Si3404 are shown in the figure below.

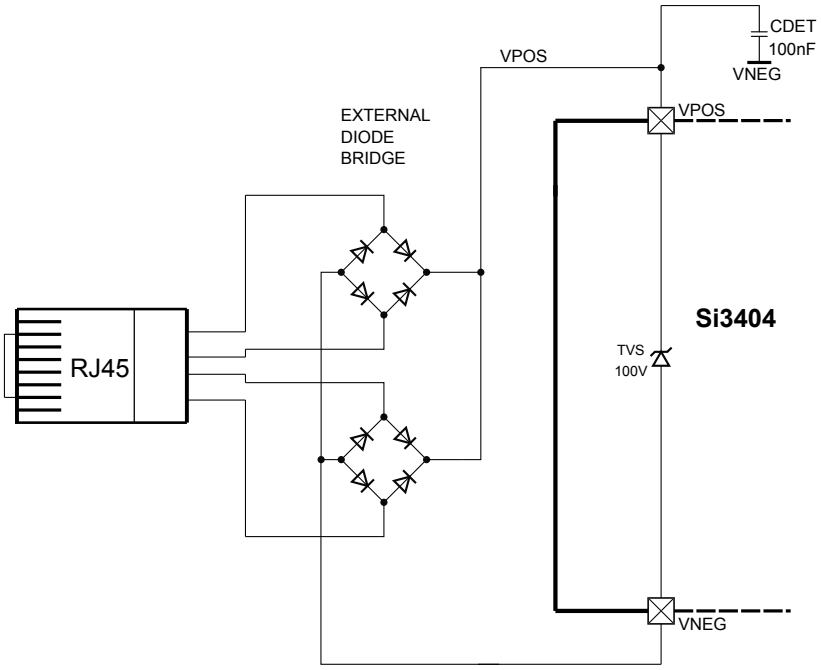


Figure 4.3. Si3404 with External Diode Bridge and Integrated Surge Protection

4.4 Basic Surge Protection

The Si340x family include integrated 100 V TVS device that offers adequate protection for indoor applications and passes the IEC 61000-4-5 combination wave (10/700 µs open circuit voltage, 5/320 µs short-circuit current) up to 4.4 kV common-mode and differentially to > 400 V.

4.5 Enhanced Surge Protection with External Diode Bridge

In special installation classes where high differential and common-mode surge immunity are required, an external TVS protection device (such as the SMDJ58A) may be installed between VNEG and VPOS to increase the surge immunity. Common-mode surge immunity up to 6 kV and differential immunity up to 2 kV can be achieved with the modifications shown in the figure below.

In this case it is recommended to leave CTx/SPx pins open to eliminate a parasitic path for the surge energy to travel and ensure it is absorbed by the external TVS device.

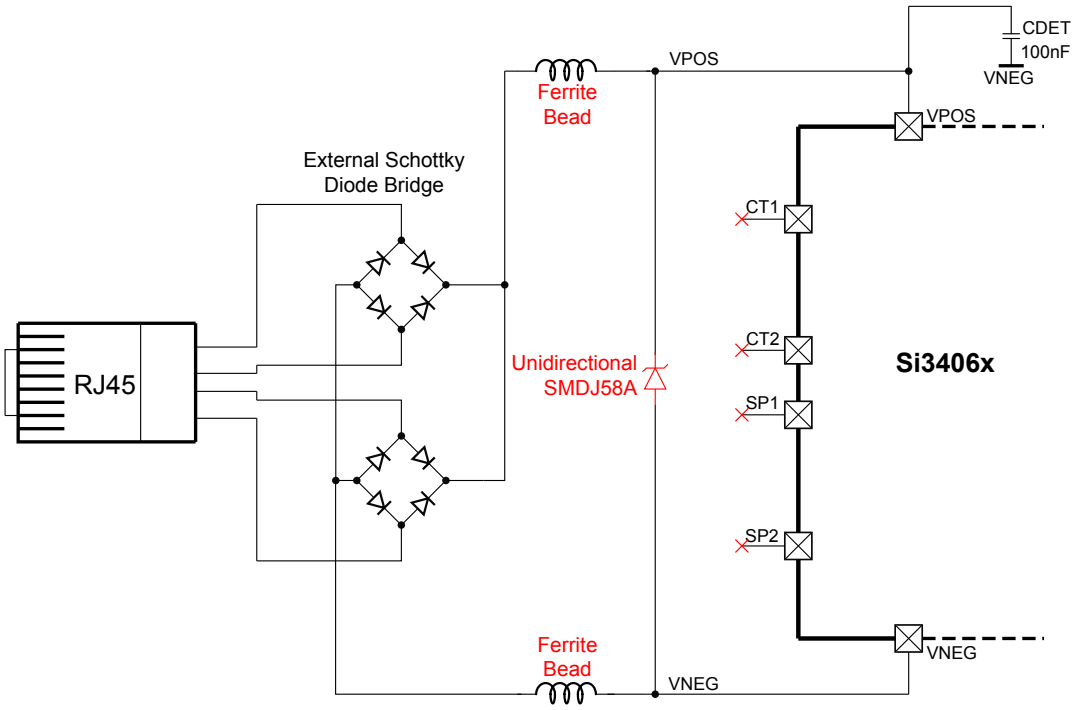


Figure 4.4. Enhanced Surge Protection Option with External Diode Bridge

The installed ferrite beads need to handle 50 A peak 5/320 µs current pulses. This performance was verified using Würth Electronics, part number: 74279220321. Also, the external diode bridge peak forward surge rating should be verified to support at least 50 A for 8.3 ms (half sine is required).

Table 4.1. Si3404, Si3406, Si34061 and Si34062 Surge Performance with External Protection Installed

IEC 61000-4-5 10/700 Combination Wave	Internal TVS Only	Enhanced Surge Modifications (External TVS & FB)
Common Mode	4.4 kV	6 kV
Differential Mode	400 V	2 kV

4.6 Enhanced Surge Protection with Internal Diode Bridge

Applications using the internal diode bridge may achieve advanced surge immunity as well by installing two external bidirectional TVS protection devices (such as the SMLJ58CA) between the ferrite beads and internal diode bridge. Common-mode surge immunity up to 6 kV and differential immunity up to 2 kV can be achieved with the modifications shown on the figure below.

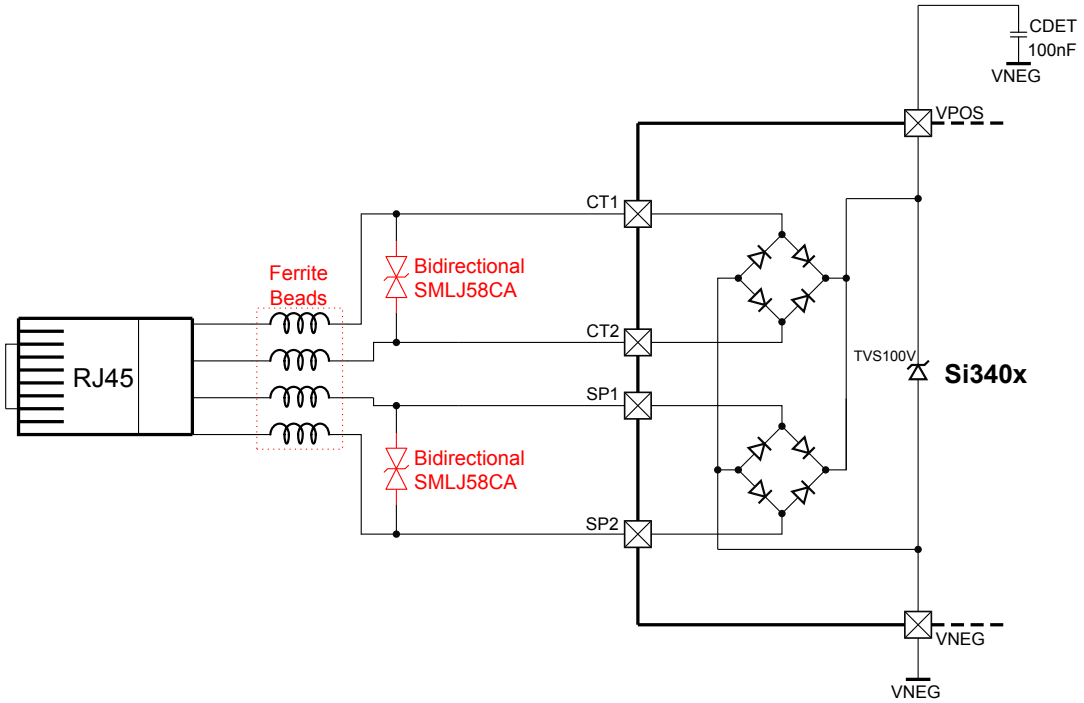


Figure 4.5. Enhanced Surge Protection Option with Internal Diode Bridge

As is the case for the external diode bridge, the installed ferrite beads need to handle 50 A peak 5/320 µs current pulses. This performance was verified using Würth Electronics, part number: 74279220321. The installed bidirectional TVS devices should be placed close to the ferrite beads on the board layout.

4.7 Auxiliary Power Supply Connection

In some applications, a backup power source, such as a power wall adapter, might be required. The Si34061 has a dedicated ASUP pin that enables the use of the dc-dc converter from an external 24 to 57 V supply.

In addition, all Si340x devices have an "ORing" feature between PoE power and wall adapter power. Depending on the connection, the wall adapter can be high-voltage (higher than the PSE voltage) or low-voltage (higher than the PD output voltage, but lower than standard PSE voltage). The high-voltage adapter needs to be connected between VPOS and HSO, and the low-voltage adapter should be installed between the VOUT and GNDI nodes. A series diode should be included in the wall adapter current path. For more details, refer to 4.7.2 Other Adapter Modes: Low- and High-Voltage Wall Adapter Connections.

4.7.1 ASUP Adapter Mode

For applications that require a backup power source, the Si34061 device can be powered from an auxiliary external 24 to 57 V dc power supply. With the connection shown in the figure below, the Si34061 detects the presence of an external supply by detecting the state of the ASUP pin. When the ASUP pin is active, the PD controller disables the HSSW, as the external supply connection to HSO closes the current loop to the dc-dc converter. In addition to opening the HSSW, detection, classification and MPS are all disabled while operating off of the external supply.

This feature can be implemented by installing the circuit shown in the figure below. This circuit drives the ASUP pin to ~4 V when an external supply is connected. R_{ASUP} forms a resistor divider with the internal 100 kΩ resistor, and an internal Zener diode protects the ASUP pin from being overdriven. The R_{ASUP} value should be chosen to ensure the voltage at the ASUP pin (V_{ASUP}) is greater than 3 V, but no more than 5 V. Also, R_{ASUP} should be at least 100 kΩ to ensure the current into the ASUP pin is limited to 300 µA or less.

Care should be taken to eliminate low frequency ripple and high frequency noise on the external supply. A 10 nF capacitor should be installed between ASUP and HSO and ferrite beads should be installed on both terminals of the external supply.

The diode D_{ASUP} prevents the PoE voltage from feeding into ASUP in the absence of an external supply. D_{ASUP} should have a low forward voltage drop to improve efficiency.

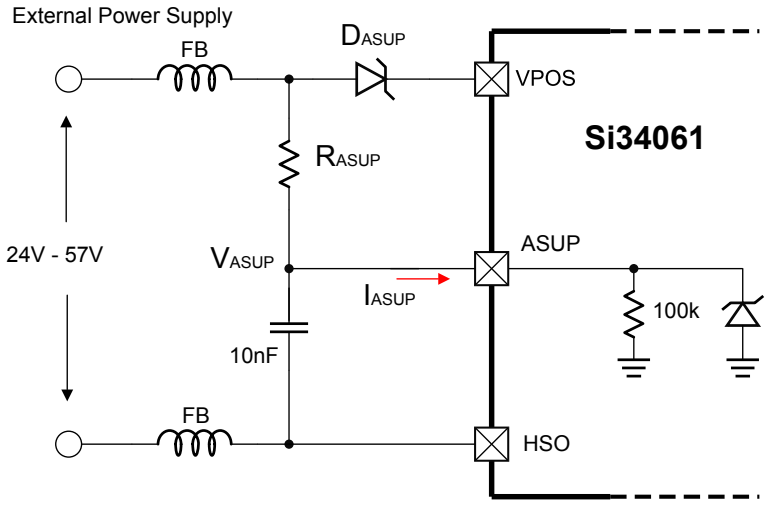


Figure 4.6. Si34061 External Power Supply Connection to ASUP

The following equations should be used when calculating a value for R_{ASUP} for a given external supply voltage, V_{EXT}:

$$V_{ASUP} = \frac{100k\Omega}{100k\Omega + RASUP} \times V_{EXT} > 3V$$

Equation 2. V_{ASUP} Constraint

$$R_{ASUP} = \frac{100k\Omega \times V_{EXT}}{V_{ASUP}} - 100k\Omega \geq 300k\Omega$$

Equation 3. R_{ASUP} Constraint

Example: For 24 V and targeting V_{ASUP} = 4.2 V, R_{ASUP} is calculated from V_{EXT}:

$$R_{ASUP} = \frac{24V \times 100k\Omega}{4.2V} - 100k\Omega = \sim 470k\Omega$$

Note that if the converter, which has been designed for nominal input voltage of 48 V, is running from a lower voltage input, the overall conversion efficiency will be lower and the output power capability of the converter may be limited. Users should verify that their output loading can be supported by the external supply.

When the PD is running from PoE voltage and the external power supply is applied, the dc-dc converter smoothly switches input sources without losing regulation. While connected to the external supply, the Si340x will continuously present and invalid signature to the PSE and never detect or classify.

4.7.2 Other Adapter Modes: Low- and High-Voltage Wall Adapter Connections

Beside using ASUP pin, all devices from Si340x PD family are capable to be driven from low or high voltage adapter using simple diode OR-ing. The figure below shows the way how to connect the wall adapter to the PD, only one option would be used in a particular design.

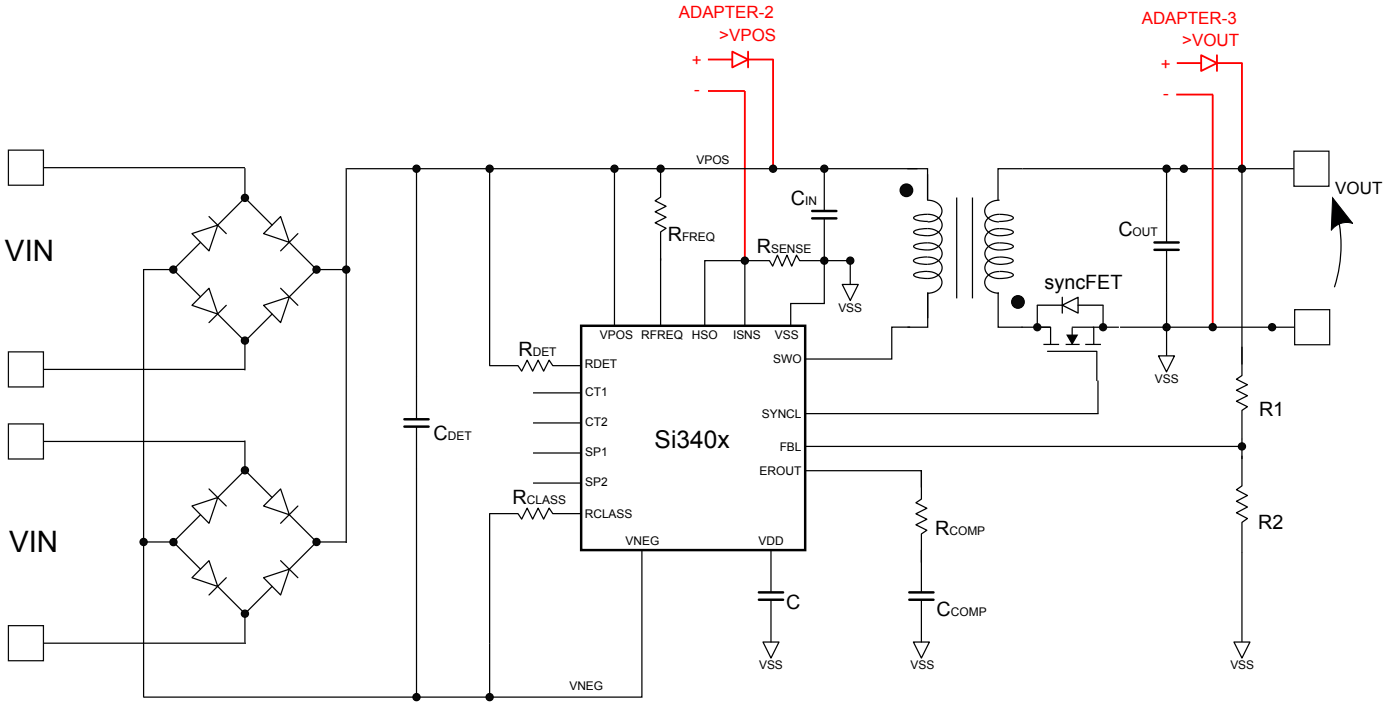


Figure 4.7. Powering the PD Using a Wall Adapter: High Voltage with Adapter-2 Option or Low Voltage with Adapter-3 Option

Adapter-2

The adapter voltage is preferably 57 V (higher than the PoE PSE voltage). In this mode, the Si340x converter is actively used, but the current path bypasses the HSSW. While the PD is running from the adapter, the PSE will disconnect the port.

Adapter-3

The adapter voltage needs to be slightly higher than the converters output voltage. In this mode Si340x goes into low power skipping mode based on the EROUT signal. Both the HSSW and power stage are actually bypassed. Therefore while running from Adapter-3 the MPS pulses can be activated to keep the connection with the PSE.

5. Si340x DC-DC Converter Features

The Si340x family contain integrated current-mode dc-dc controllers that are robust yet flexible enough to support a wide range of topologies and magnetics. This section provides an overview of the features of the Si340x's dc-dc architecture and available options.

Table 5.1. DC-DC I/O Signals

Signal	Description	Si3404 Pin	Si3406 Pin	Si34061 Pin	Si34062 Pin
VPOS	Rectified high-voltage supply rail	13	12	14	14
VSS	DC-DC primary ground	19	18	22	22
VDD	5V regulated output	5	4	4	4
FBH	High-side (VPOS referred) feedback input	2	1		1
FBL	Low-side (VSS referred) feedback input	4	3	3	3
EROUT	Error amplifier current output / compensation impedance input	3	2	2	2
SWO	Internal FET switch output (drain)	18	18	22	22
SYNCL	Synchronous rectification FET driver output		16	19	19
EXTGD	External FET gate drive output			21	
SWISNS	External FET peak current sense input			24	
ISNS	VSS average current sense input	1	20	1	24
RFREQ	Oscillator frequency tuning resistor	10	9	11	11
VT15	DC-DC transformer aux bias winding input	16		18	18
V11	11V regulator output for filter cap		17	20	20

5.1 Soft Start

To protect the output capacitor from a sudden high current event and to avoid start-up transients, the controller's peak current is internally limited at startup, which gradually ramps up in a function of the attached load.

The Si3404 and Si3406x devices integrate an intelligent adaptive soft-start mechanism, which does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller will let the output voltage to rise faster when no load (or light load) is attached. When a heavy load is connected to the output of the converter, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

The figure on the left shows the output voltage during soft-start with no load attached, and the figure on the right shows soft-start with heavy load attached.

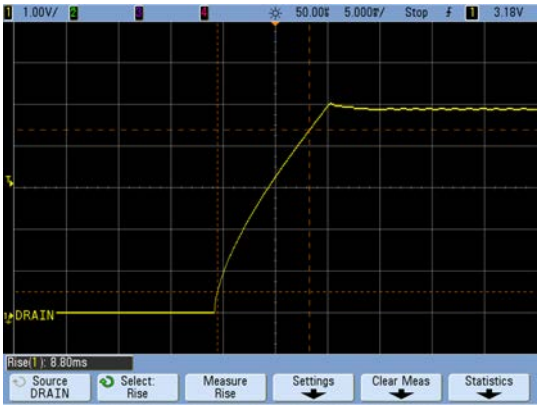


Figure 5.1. Output Voltage During Soft-Start - No Load

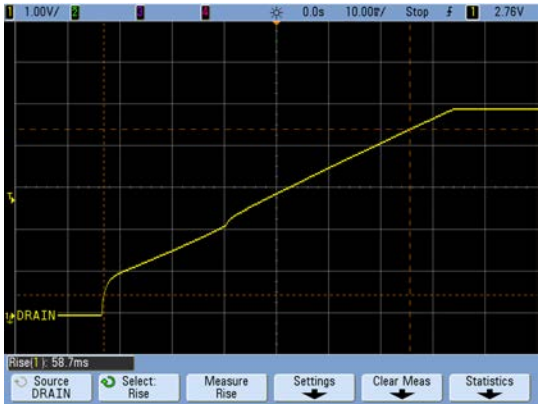


Figure 5.2. Output Voltage During Soft-Start - 25 W Load

5.2 Controller Ground—VSS

VSS is the reference ground of the dc-dc controller. The source of the internal dc-dc switcher MOSFET is internally connected to the VSS through an internal peak current sense circuit.

5.3 Internal Switch—SWO

SWO pin is connected to the drain of the internal switching FET. The magnetics (inductor or transformer) should be directly connected to this pin. This pin can handle voltages up to 120V. The internal dc-dc switcher is a PWM controlled MOSFET. To ensure normal operation, a low ESR 100nF capacitor should be connected to VDD pin, which supplies the driver of the SWO FET.

The PCB connection between SWO and the magnetic should be as short as possible to minimize parasitics and unwanted high frequency noise generation.

R1, C1, and D1 form a voltage clamp, which is needed at higher power levels to protect the switching FET and reduce high frequency noise. See 7.2.1 Practical Example of Primary RCD Clamp Design for information on designing an RCD clamp.

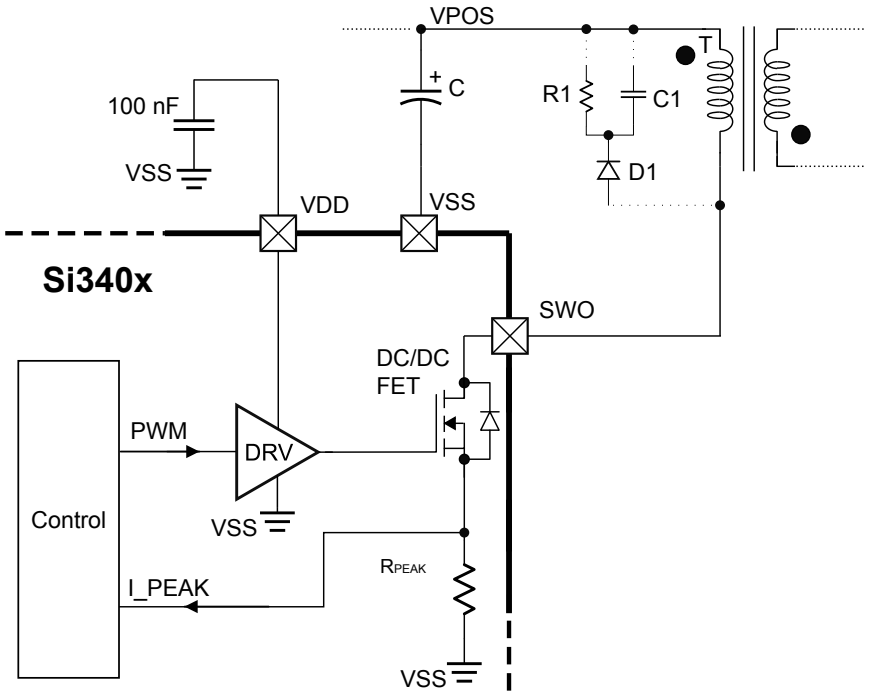


Figure 5.3. PWM Controller with Integrated Switching FET

5.4 External Switching FET—EXTGD, SWISNS

The Si34061 device integrates an external gate driver (EXTGD) to drive the external switcher FET instead of using the integrated FET through the SWO pin. An external FET will provide improved thermal performance and conversion efficiency, especially in high power applications.

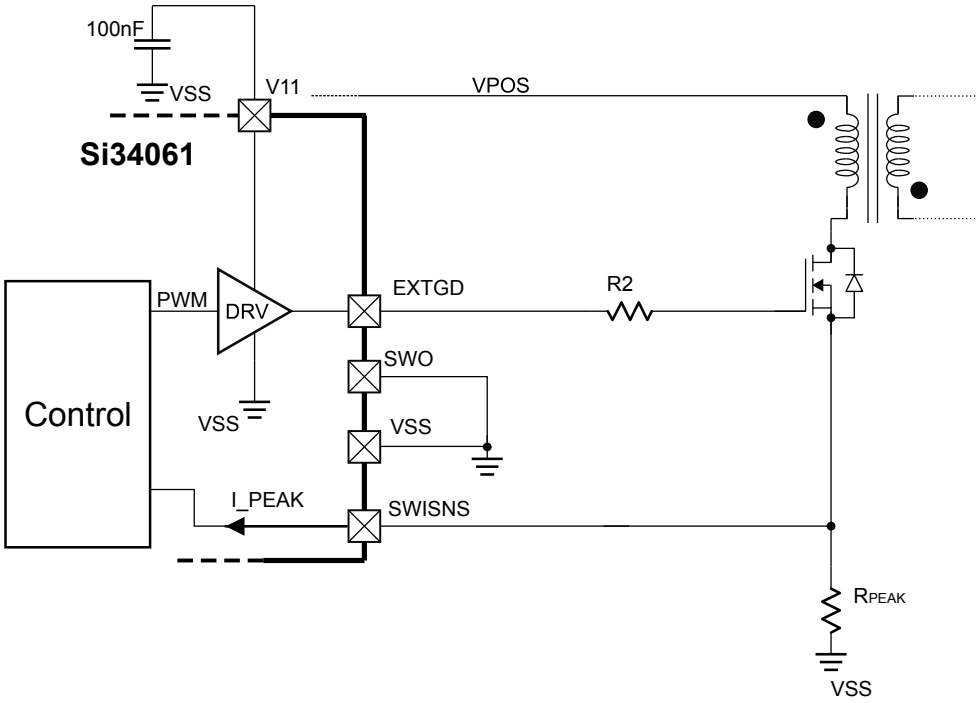


Figure 5.4. External Switching FET Driver Circuit

At startup the controller performs FET detection whether an external FET is connected to the EXTGD pin or not, see section 6.6 External FET Detection for details.

If the external FET is not installed, EXTGD should be tied to VSS. The controller detects the shorted EXTGD and disables the EXTGD driver. In this case the internal FET can be used. If the external FET is installed, at startup the controller detects the gate capacitance of the installed FET and enables the EXTGD driver, while SWO should be tied to VSS.

When using an external FET, the peak current of the transformer is measured on an external peak-sense resistor through SWISNS pin. Changing this resistor allows the application to set the maximum peak current to protect the magnetic components from saturation. The SWISNS input has internal filter circuit. In noisy environment an additional external low pass filter can be added. The trigger level of the internal circuit at pin SWISNS is 240 mV, typical.

The EXTGD controls the external FET with 10V logic level relative to VSS. To provide safe operation, a low ESR 100nF capacitor needs to be installed to V11 pin. If the EXTGD pin is used, SWO should be tied to VSS. If EXTGD is not used, EXTGD should be tied to VSS.

To have better control over EMI performance, a gate resistor R2 can be installed to control the turning ON and OFF speed of the external FET. The gate resistor reduces the speed of switching; therefore, it should be carefully chosen not to influence the non-overlap control of the drivers (between EXTGD and SYNCL).

For more details, see 6.5 FET Driver Non-Overlap Control.

5.4.1 External Switching FET Selection

In order to handle high voltage spikes coming from the leakage inductance of the transformer, the voltage rating of the external FET should be at least 100 V . The maximum allowed continuous current in PoE systems is 600 mA, but higher spikes are allowed; so, it is recommended to design with additional margin.

Silicon Laboratories recommends the following parameters for the external switching FET:

Table 5.2. External Switching FET Parameters

Switching-FET Minimum Voltage Rating VDS	Switching-FET Minimum Current Rating ID	Switching FET resistance RDS_ON
100 V	1 A	< 150 mΩ

The gate capacitance of the external switching FET is critical, as this FET switches all the time with the adjusted switching frequency. The maximum allowed gate capacitance for external switching FET is 2 nF; however, lower gate capacitance will improve overall conversion efficiency.

5.5 Average Current Sensing—ISNS

The application average current is sensed on the R_{SENSE} resistor connected between VSS and ISNS – note that this voltage goes below VSS.

Sizing the resistor allows the designer to set the average overcurrent limit according to the PoE class. The equation below can guide in the R_{SENSE} value selection.

$$I_{AVG\_LIMIT} = \frac{|\,270mV\,|}{R_{SENSE}}$$

Equation 4. Application Average Current Limit Calculation

In the table below, the R_{SENSE} value is listed for PoE classes with a safety margin:

Table 5.3. Measuring Average Output Current

PoE Class	IEEE PSE Current Limit	Calculated PD Current Limit with Margin	R_{SENSE} Value	Minimum Package Size	Minimum Power Rating
Class 1	105 mA	135 mA	2 Ω	0201	1/20 W
Class 2	175 mA	225 mA	1.2 Ω	0402	1/16 W
Class 3	350 mA	435 mA	0.62 Ω	0805	1/8 W
Class 4	600 mA	900 mA	0.3 Ω	0805	1/3 W

Refer to 6.7 Power Modes of the Converter for details on how ISNS controls the external HSSW and the synchronous rectification driver.

5.6 Switching Frequency—RFREQ

The Si340x family provides selectable switching frequency. The tunable switching frequency gives a flexibility for the designer to ensure the application is running on the optimal switching frequency. By fine tuning the switching frequency of the converter both the EMI and efficiency performance of the application can be improved.

The switching frequency of the dc-dc converter can be set in two ways:

1. by using the 250 kHz internal oscillator by shorting RFREQ with VPOS, or

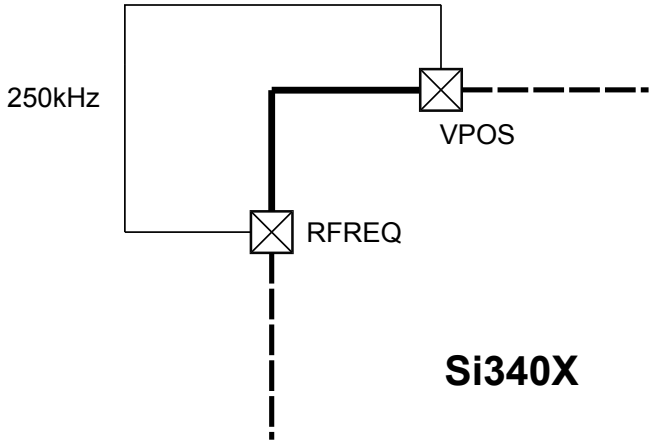


Figure 5.5. Switching Frequency Set to 250 kHz

2. by R_{FREQ} resistor between RFREQ and VPOS

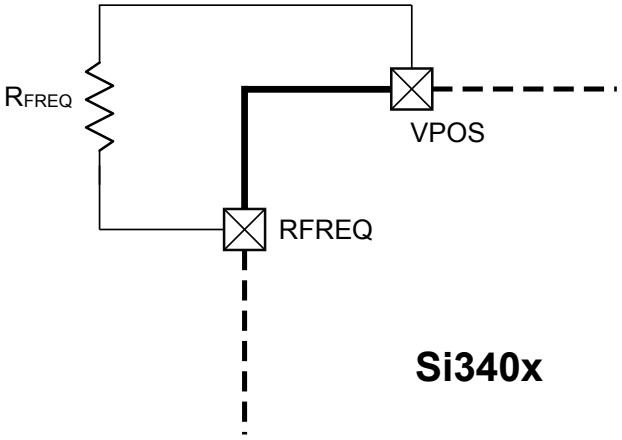


Figure 5.6. Switching Frequency Set by R_{FREQ}

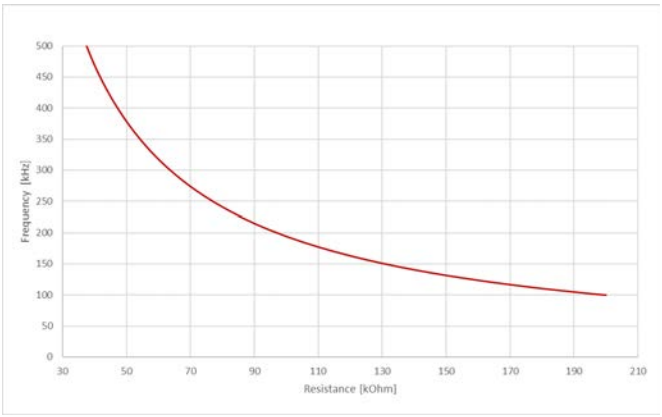


Figure 5.7. Switching Frequency as a Function of R_{FREQ}

Ensure that the connection between the RFREQ pin, R_{FREQ} resistor, and VPOS pin is as short as possible.

5.7 Synchronous Rectification—SYNCL

To achieve higher overall conversion efficiency, improve system reliability and thermal performance Si3406x devices provide a low side synchronous rectification driver, SYNCL.

A common secondary side rectification Schottky type diode forward voltage drop is around 0.5 V. At high loads this loss becomes one of the primary losses in the system. By replacing the rectification diode with a low RDS(on) FET, the overall efficiency can be significantly improved by reducing the 0.5 V voltage drop to below 0.1 V. This can provide a 3.5% to more than 5% efficiency boost, depending on the converter output voltage.

In low power mode, such as a no-load condition, SYNCL is disabled to maintain good efficiency. In this case, the current flows through the body diode of the sync-FET. To further improve efficiency at high power, a Schottky diode can be installed in parallel with the sync-FET`s body diode.

SYNCL operation controlled by the ISNS pin based on the average input current (sensed on R_{SENSE}). The controller decides whether the SYNCL driver is enabled or disabled.

If a synchronous FET is not used in the design, the SYNCL pin ***must not be connected*** and should be left floating.

5.7.1 Synchronous Rectification in Isolated Designs

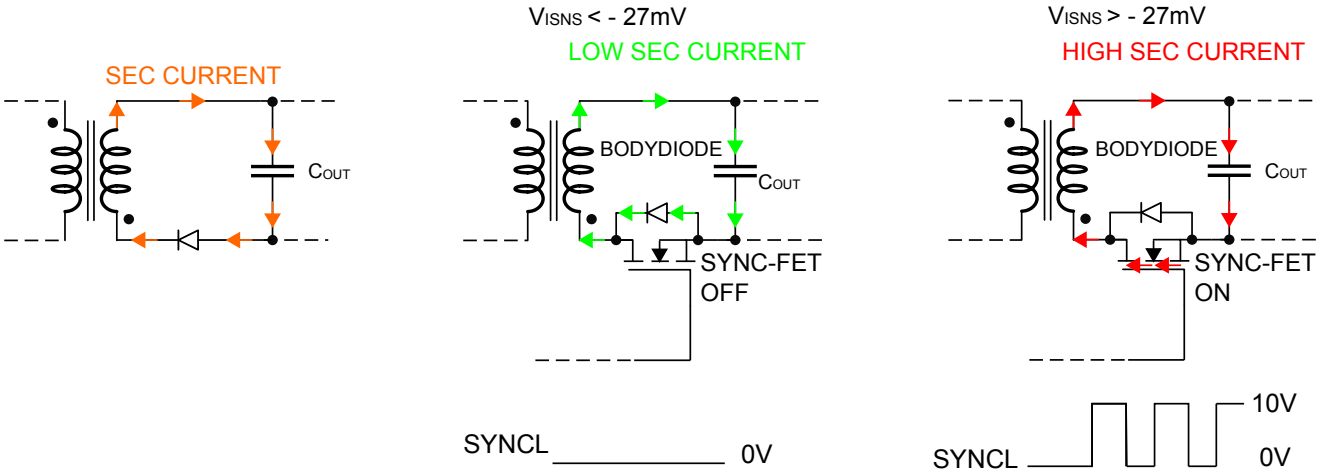


Figure 5.8. Secondary Side Current Path with Rectification Diode (Left), with Sync-FET at Low Power (Middle) and with Sync-FET at High Power (Right)

To control a sync-FET through an isolation barrier, a pulse (or gate drive) transformer is recommended. The SYNCL driver has been optimized for pulse transformers with the following design characteristics:

- ~ 1 mH primary inductance
- toroidal core
- turns ratio of 3:4 or 1:1
- isolation rating ≥ 1.5 kV to meet IEEE 802.3 safety requirements

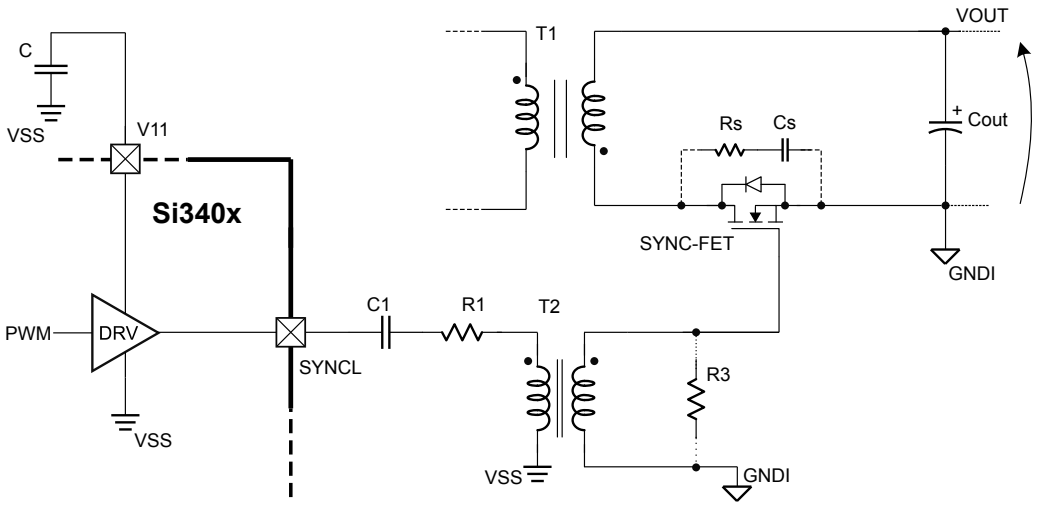


Figure 5.9. Driving a Synchronous Rectification FET in Isolated Flyback Designs

Referring to the sync-FET driver isolation circuit in the figure above, the following table describes the purpose of each component:

Table 5.4. Isolated Sync-FET Driver Circuit

Component(s)	Description
T2, C1, R1, R3	Pulse transformer with gate driver circuit to provide isolated driver for synchronous rectification.
Rs, Cs	Snubber circuit to dampen ringing when sync-FET turns off and improve EMI.

The SYNCL driver is referenced to VSS (low-side) and the driver is supplied from a 11 V internal regulator. A 100 nF low ESR ceramic capacitor is mandatory on the V11 pin. As the SYNCL driver is VSS referenced, it cannot be used in a Buck topology.

5.7.2 Synchronous Rectification in Non-Isolated Designs

The non-isolated Flyback is a popular choice for low cost applications where higher efficiency is required without isolation.

The SYNCL pin can be directly connected to the synchronous FET`s gate through the driver network without gate transformer as shown below. The R-C shunt snubber across the sync-FET is necessary to reduce ringing and improve EMI.

The maximum allowed gate capacitance of the synchronous FET is 2 nF. The voltage rating of the FET depends on the output voltage and can be calculated with the following formula:

$$\text{syncFET voltage rating} = \frac{1}{n} \times V_{IN\,MAX} + V_{OUT}$$

where:

n is the transformer turns ratio.

V_{INMAX} is the maximum input voltage (57 V)

V_{OUT} is the converter output voltage

Equation 5. FET Voltage Rating

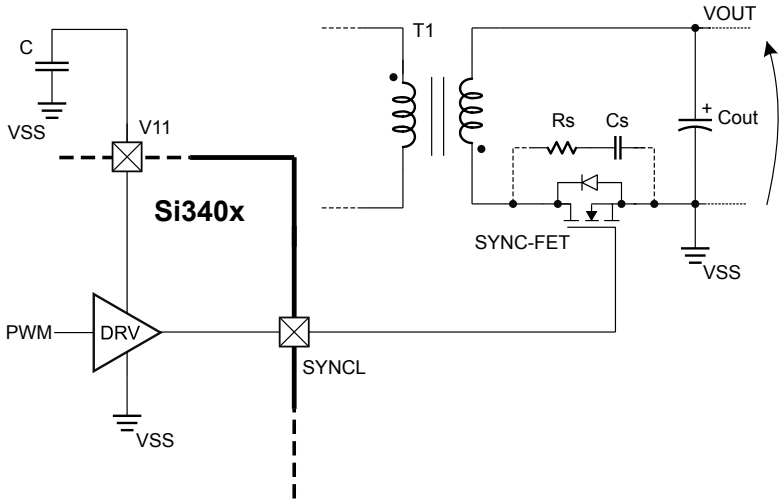


Figure 5.10. Driving a Synchronous Rectification FET in Non-Isolated Flyback Designs

5.8 Voltage Regulators—VDD, V11

The Si3406x IC provides a 5 V output (VDD pin) to drive LEDs, or optocouplers. This is a closed loop regulator. A low-ESR 100 nF capacitor needs to be connected to the VDD pin.

The 5 V regulator is supplied by an internal 11 V open loop regulator, which provides power for the internal driver when EXTGD is used. Therefore, a low-ESR 100 nF capacitor is required on the V11 pin, even if the EXTGD pin is not used.

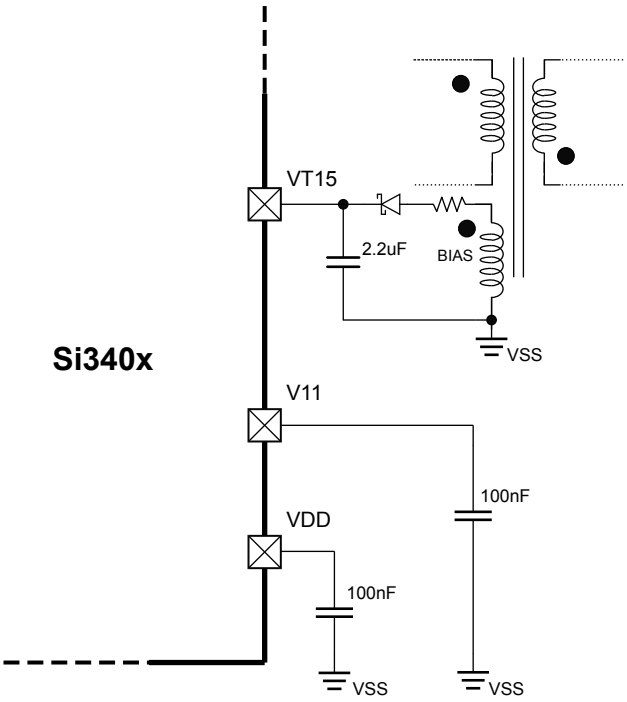


Figure 5.11. AUX Winding, V11 and VDD Regulator Connections

5.9 Auxiliary Winding—VT15

When VT15 is not used, the internally regulated 11 V is derived from VPOS with a course internal regulator. When VT15 is available, it can be used to source the 11 V supply from an optional auxiliary bias winding of the transformer. This will result in an overall reduction in power consumption and efficiency improvement of up to 2%.

VT15 should nominally be supplied with 15 V. Care should be taken to not exceed 16.5 V on VT15. Refer to Figure 5.11 AUX Winding, V11 and VDD Regulator Connections on page 34 for the recommended VT15 input circuit topology.

5.10 Feedback Loop: FBL, FBH, and EROUT Pins

The Si3406x supports a wide variety of topologies by providing options for isolated and non-isolated, as well as low-sided and high-sided feedback topologies.

Feedback signal can be provided to the controller in three ways:

- FBH: High side, referenced to VPOS (Buck)
- FBL: Low side, referenced to VSS (Non-Isolated Flyback)
- EROUT: Low side, referenced to VSS (Isolated Flyback)

5.10.1 FBH: High Side, Referenced to VPOS (Buck)

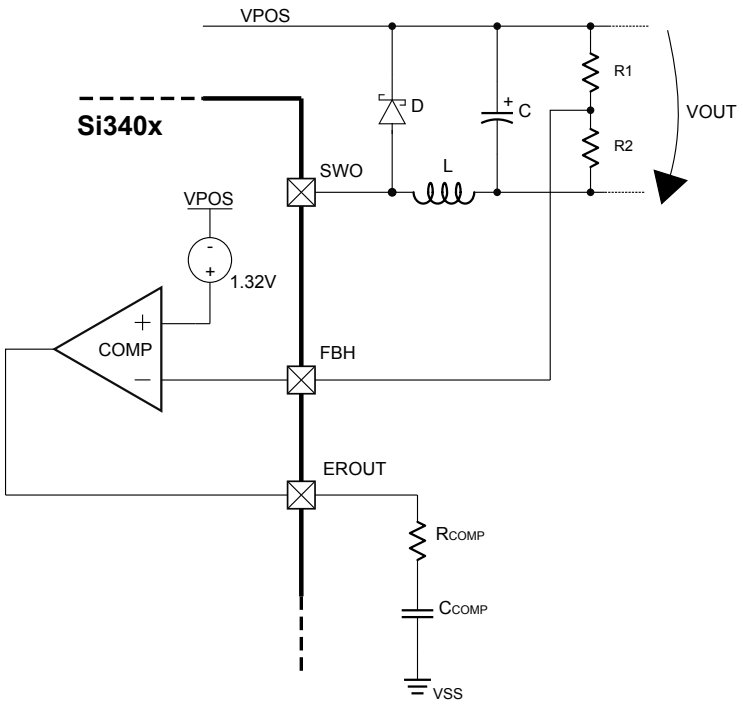


Figure 5.12. Feeding back the Output Voltage on High Side Topology

The internal voltage reference forces a stable voltage (1.32 V) on the FBH referenced to VPOS. In buck topology the output voltage is fed back to the FBH pin through the resistor divider (R1||R2) network to achieve regulated output voltage.

The output voltage is calculated by a simple formula:

$$V_{OUT} = 1.32V \times \left(1 + \frac{R_2}{R_1}\right)$$

Equation 6. Output Voltage

In the buck topology, the output voltage is VPOS referenced.

When FBH is not used, FBH must be tied to VPOS.

When FBH is employed, the control loops compensation network should be connected to the EROUT pin. When FBH is not used, tie FBH to VPOS.

A compensation network is connected to EROUT pin.

5.10.2 FBL: Low Side, Referenced to VSS (Non-Isolated Flyback)

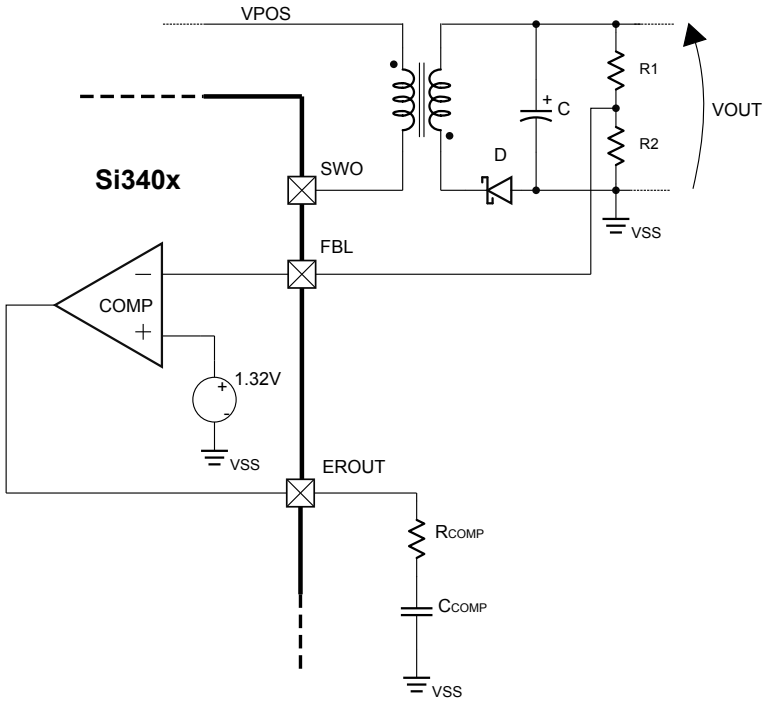


Figure 5.13. Feeding Back the Output Voltage on Low Side Non-Isolated Topology

The internal voltage reference forces a stable voltage (1.32 V) on the FBL referenced to VSS. In non-isolated Flyback, the output voltage is fed back to the FBL pin through the resistor divider (R1||R2) network to achieve regulated output voltage.

The output voltage is calculated by a simple formula:

$$V_{OUT} = 1.32V \times \left(1 + \frac{R_1}{R_2}\right)$$

Equation 7. Output Voltage

The output voltage in non-isolated Flyback is referenced to VSS.

When FBL is not used, tie FBL to VSS.

When FBL is employed, the control loops compensation network should be connected to the EROUT pin.

5.10.3 EROUT: Low Side, Referenced to VSS (Isolated Flyback)

In isolated designs, the converters output voltage is compared to the external voltage reference (TLV431) and the error signal is fed back to the controller, connected to the EROUT pin.

When the actual output voltage is lower than the desired value, EROUT is high, requesting the controller to increase the PWM width, to get the desired output voltage as soon as possible.

When the actual output voltage is higher than the desired value, EROUT is low, requesting the controller to decrease the PWM width.

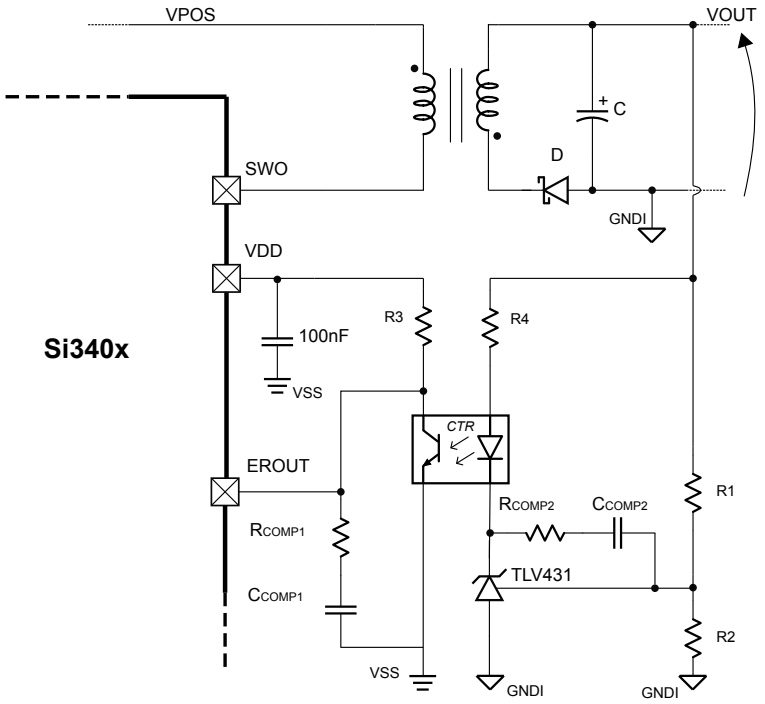


Figure 5.14. Feeding Back the Output Voltage in Isolated Design Using Opto-Coupler and TLV431 Voltage Reference

In isolated designs as shown in the above figure, the following components build up the compensation network:

- R1, R3, R4
- R_{COMP1}, C_{COMP1}
- R_{COMP2}, C_{COMP2}
- TLV431 and
- the current transfer ratio of the opto coupler, (CTR).

The output voltage for a Flyback output with TLV431 feedback network is calculated by a simple formula:

$$V_{OUT} = 1.24V^{*} \times \left(1 + \frac{R1}{R2}\right)$$

**1.24V is a reference voltage of the TLV431 device.*

Equation 8. Output Voltage for a Flyback Output with TLV431 Feedback Network

6. DC-DC Conversion Details

A dc-dc converter is an electronic circuit that converts the high PoE voltage (50 V) to a low regulated voltage to supply the end application. With different BOM configurations various output voltages and output power levels can be generated. The Si340x dc-dc converter application can provide isolation if needed. The Si340x dc-dc converter is a peak current mode controlled device. Current mode control offers many advantages including improved load line regulation, cycle-by-cycle current limiting and protection, and better flux balancing.

6.1 Leading Edge Blanking Time and Minimum Pulse Width

Due to high current switching and presence of different parasitics, the turning on a MOSFET device can generate a significant amount of ringing. This ringing can couple erroneous signals to the control circuitry and falsely terminate the PWM signal.

Peak current mode control needs a leading-edge blanking time which blanks those leading-edge spikes during turn-on event of the switch (see figure below). The leading-edge blanking time ensures that the controller remains insensitive to the turn-on voltage spikes observed during measuring the peak current. The figure below shows a simplified block diagram of the Si340x's PWM controller.

Due to the existence of the blanking time, there is a specified minimum pulse width, which can be produced by the controller (200 ns). Due to this limitation, the converter output voltage in Buck topology cannot be lower than 3.3 V.

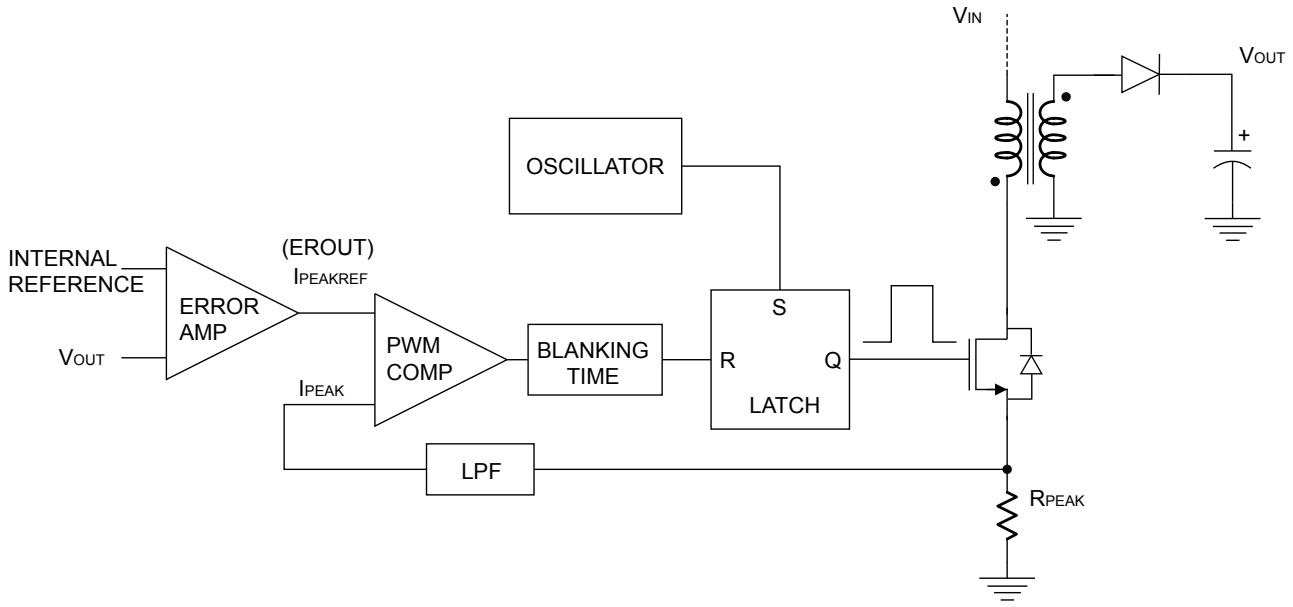


Figure 6.1. Simplified PWM Controller Block Diagram

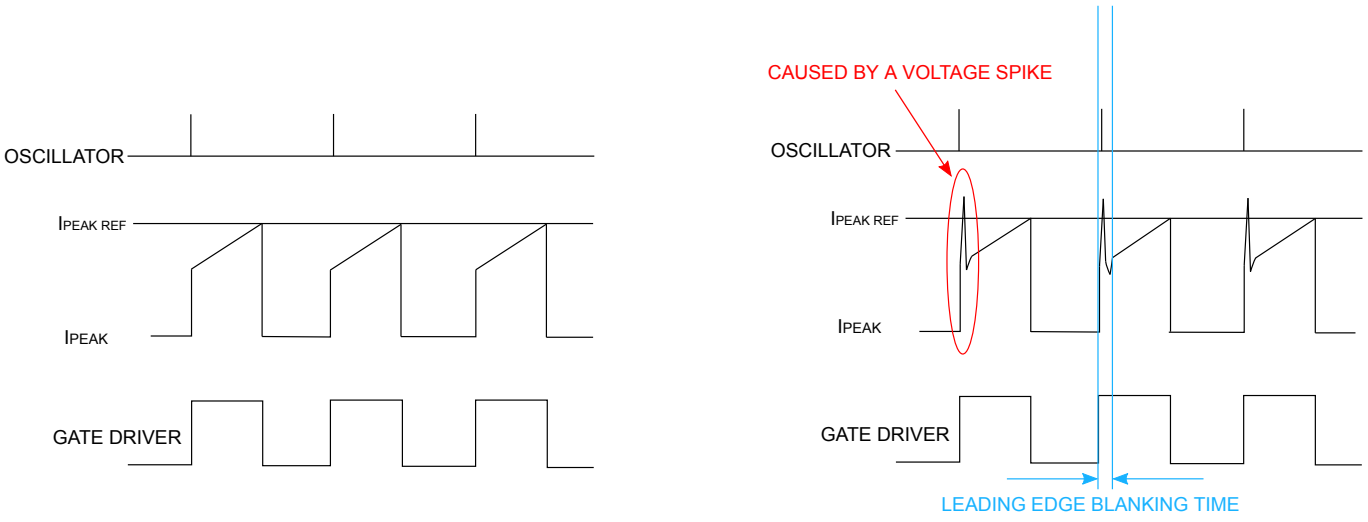


Figure 6.2. High-Current Transient During FET Turn-On— Ideal Waveform (L), Real Waveform (R)

6.2 Internal Slope Compensation

The Si3404x device is a traditional peak current mode controller. The output voltage is regulated by comparing inductor peak current information with control voltage. The current mode architecture requires slope compensation to be added to the current sensing loop to prevent subharmonic oscillations which can occur for duty cycles above 50%.

The Si340x dc-dc controller includes internal slope compensation circuitry in which a fixed ramp generated by the oscillator is added to the current ramp. The internal slope compensation circuit provides ease of use.

6.3 Load-Dependent Pulse Skipping

The Si3404x device family includes a current mode PWM controller which integrates two types of pulse skipping mechanisms:

- Heavy-load skipping
- Light-load skipping

6.3.1 Heavy-Load Skipping and Output Short Protection: Hiccup-Mode

Heavy-load skipping can occur in steady state operation, when the output is overloaded or shorted. At steady state, if the output is being shorted, the output voltage goes low and the EROUT signal goes high and engages the heavy-load skipping mode.

If the controller is in heavy-load skipping mode for 1ms, the controller performs a dc-dc reset to protect the application from overheating. The dc-dc reset is followed by a soft-start turn-on. If the short is still present on the output, the Si340x will again engage the heavy-load skipping mode for 1 ms and it will reset again. This cycle will continue indefinitely until the short is no longer present.

6.3.2 Light Load Skipping

As the output load decreases, the controller starts to reduce the pulse-width of the PWM signal (switcher ON time). At some point, even the minimum width pulse will provide higher energy than the application requires, which could result in loss of voltage regulation. When the controller detects light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or *light-load skipping mode*. In this mode, the Si340x prevents the switch from turning ON for multiple switching cycles to prevent the output from losing regulation.

6.4 Thermal Sensors

Both integrated switches (HSSW and dc-dc switching FET) include a localized thermal sensor, which protect the device from thermal run-away. When the Si340x is powered from the PSE, both sensors are employed.

When the PD is running from an auxiliary external power supply, the HSSW is turned OFF to allow the PD to run the dc-dc converter from a minimum input voltage of 12 V. In this case, the thermal sensor of the switching FET remains active.

6.5 FET Driver Non-Overlap Control

Dead-time is called when none of the primary or secondary switch conducts. During dead-time the body diode of the sync-FET is conducting, which has significantly higher losses than the conducting FET. The dead-time should be short to improve efficiency, but it must be ensured that overlap cannot occur. The Si340x dc-dc controller ensures automatic minimum MOSFET dead-time, while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs driver and adjusts the switching adaptively to ensure they do not conduct simultaneously.

All three switching drivers (internal FET, EXTGD, SYNCL) have output level detect (+1 V or –1V away from supply). This allows automatic non-overlap control to ensure only one switch conducts at a time.

Before turning ON the primary switch (based on the rising edge of the clock), the controller waits until the driver signal of the SYNCL goes below 1 V, which means synchronous FET does not conduct anymore, and the controller that way prevents overlap.

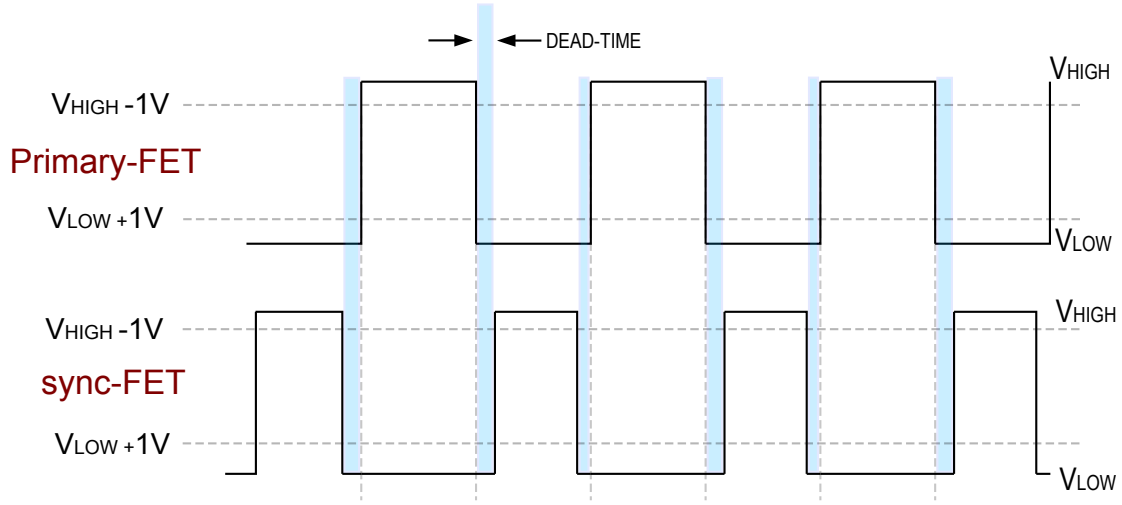


Figure 6.3. Non-Overlap Control: Gate Driver Signals for Primary and Secondary Switches

6.6 External FET Detection

To verify if an external switching FET is installed, the Si34061 performs a FET-detection sequence prior to startup. FET-detection works using a weak pull-up that tries to charge up the gate of the external FET (C_{GS}) to 600 mV.

If the gate voltage during FET-detect reaches the 600 mV limit in less than 44µs, the FET-detection was successful and the controller enables the external driver. If the gate voltage does not reach 600 mV, the Si340x disables the external driver and enables the internal switching FET. See the figures below for example detection waveforms.

The maximum allowed gate capacitance of the external switching FET is 2 nF. The FET-detection is a safe operation since the limit is only 600 mV, which is far below the threshold voltage of the external FET. After the FET-detection sequence and prior to startup, the FET gate is fully discharged.

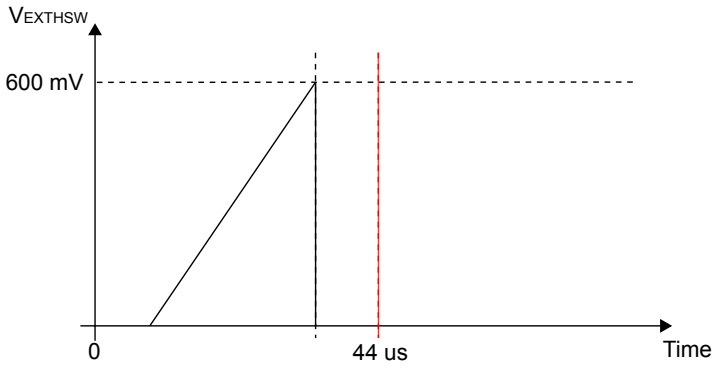


Figure 6.4. Successful External FET Detection

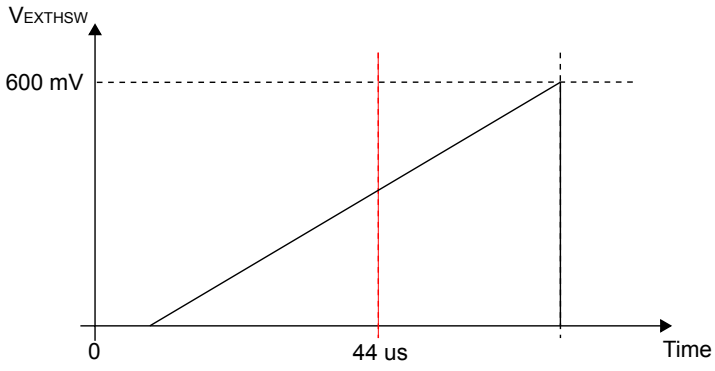


Figure 6.5. Unsuccessful External FET Detection

6.7 Power Modes of the Converter

From the power consumption point of view, the Si3406x PoE+ PD controller family has two modes of operation.

The mode is selected by the sensed voltage on R_{SENSE} resistor:

- V_{ISNS} is between 0 V and –27 mV -> Low power mode and
- V_{ISNS} is between –27 mV and –270 mV -> High power mode

If V_{ISNS} is more negative than –270 mV, the converter interprets it as an overcurrent case and the controller performs a reset.

6.7.1 Low Power Mode

The ISNS pin is used to sense the application average current by monitoring the voltage on the R_{SENSE} resistor.

When the controller senses a voltage between 0 V and –27 mV on ISNS-VSS, the EXTHSW and SYNCL pins are disabled to achieve extra low application idle consumption. In this condition the current supplied by the PSE flows through the internal HSSW (even if the EXTHSW is installed) and the sync-FET driver is disabled. The secondary side current of the converter then flows through the body diode of the sync-FET.

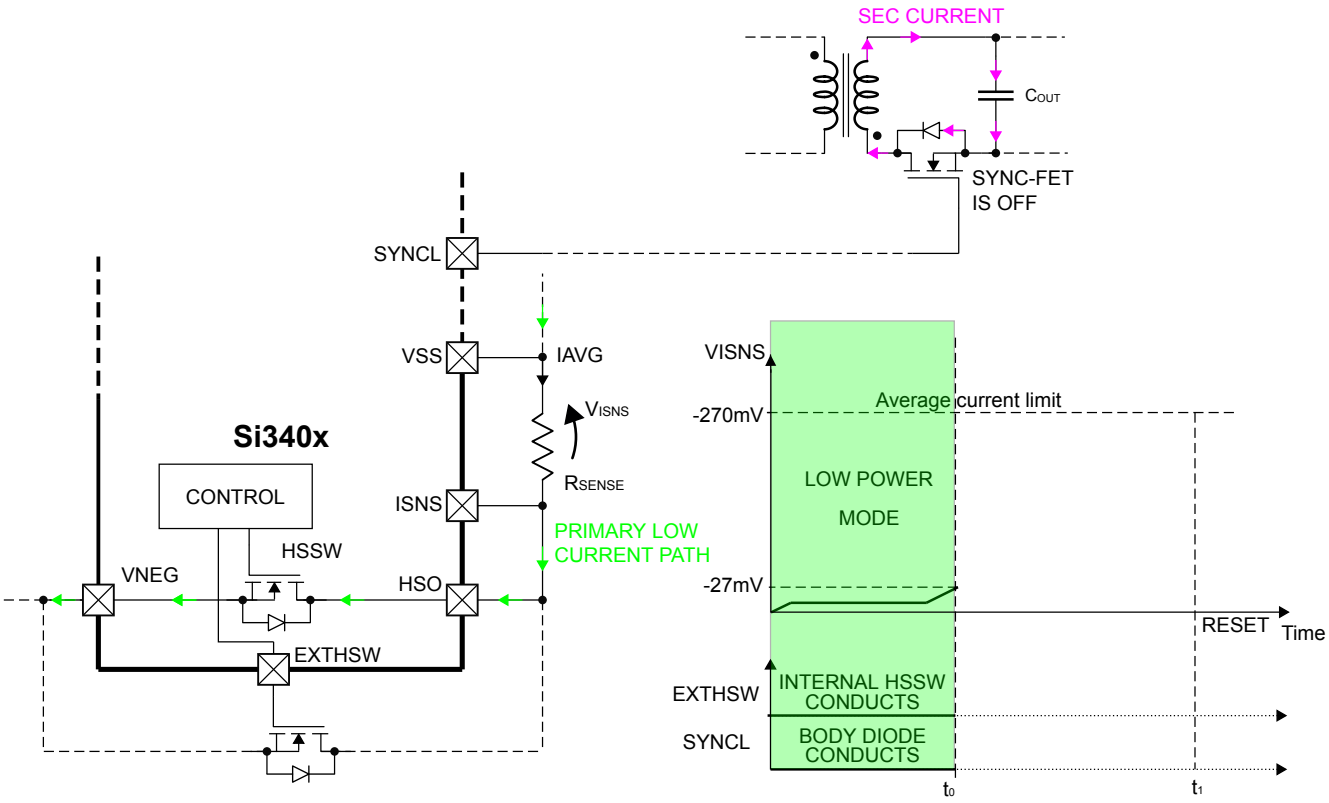


Figure 6.6. Low Power Mode, V_{ISNS} < |–27| mV, Sync-FET Disabled, EXTHSW Disabled

6.7.2 High Power Mode

As the application average current rises, the voltage rises on the R_{SENSE} resistor. When voltage V_{ISNS} is between –27 mV and –270 mV, the Si3406x controller enters into high power mode: turns ON the external hotswap switch and enables the synchronous rectification gate driver.

The primary current now flows through the external hotswap switch. This improves the design from thermal perspective.

The secondary current on the isolated side of the converter flows through the channel of the synchronous FET. In a function of the converters output voltage, the synchronous FET can provide significant efficiency boost:

- At 5 V output + 5-6% the efficiency boost
- At 12 V output + 3-4% efficiency boost

If the application average current rises even more, and V_{ISNS} hits the –270 mV limit, then the converter will perform a reset and try to re-start with the integrated soft-start mechanism. The converter will be in this reset-soft-start cycle until the V_{ISNS} is more negative than –270 mV.

If EXTHSW pin is not used, it should be connected to VNEG.

If SYNCL pin is not used, it should be left OPEN, never connect SYNCL to any ground or rail.

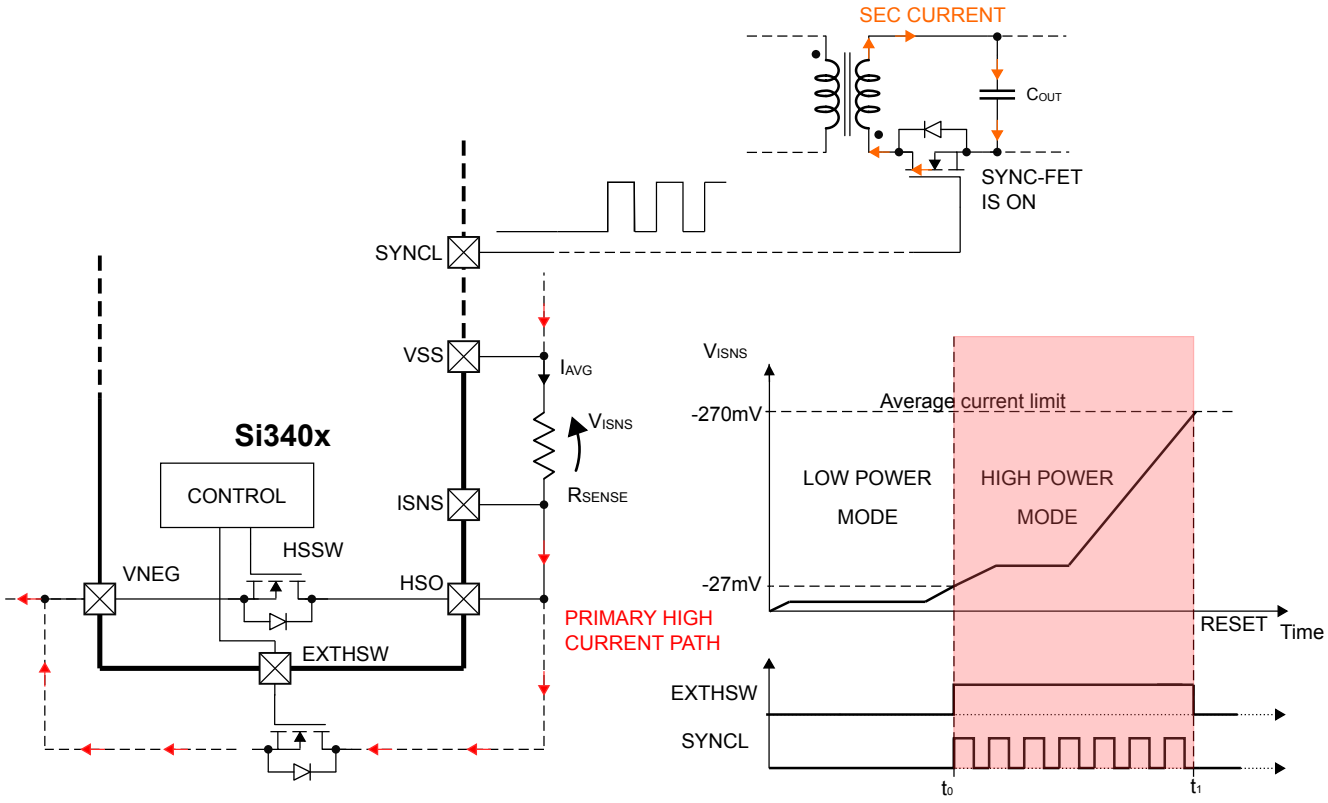


Figure 6.7. High Power Mode, V_{ISNS} > |–27| mV, Sync-FET Enabled, EXTHSW Enabled

6.7.3 DCM and CCM Operation

Depending on the parameters, such as inductance, input voltage, output voltage, and load, the converter can operate either in DCM (Discontinuous Current Mode) or either in CCM (Continuous Current Mode).

DCM and CCM each have advantages and disadvantages. These specifics are not covered in this application note.

Silicon Labs PoE PD reference designs are designed to operate in CCM at full power load. At low load conditions the converter goes into DCM operation.

The figures below represent the correct voltage waveforms of the switching drain.

In the left figure, there is no load attached to the output, which causes a low frequency voltage “swing” on the drain of the switching FET, this is a normal operation in DCM.

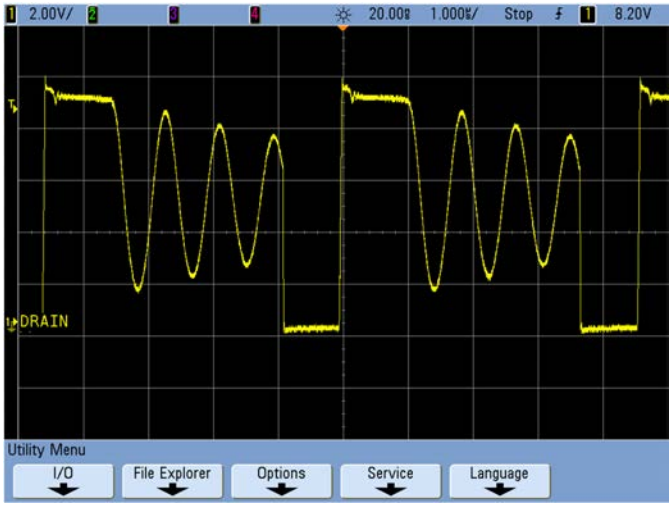


Figure 6.8. SWO Voltage in DCM Operation

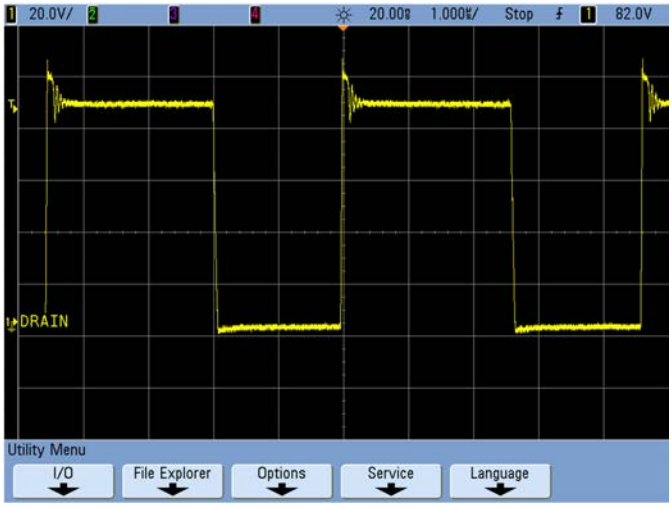


Figure 6.9. SWO Voltage in CCM Operation

In the right figure, a heavy load is attached to the output, which will force the converter into a CCM mode operation.

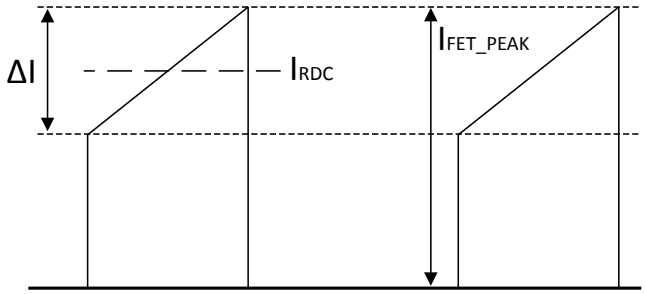
7. DC-DC Design Guide

7.1 Transformer Selection

The operation changes between CCM and DCM as the load condition and input voltage vary. For both operation modes, the worst case in designing the inductance of the transformer primary side (L_P) is full load and minimum input voltage condition.

220 kHz has been selected for switching frequency, which is a good compromise between transformer size and converter efficiency.

To get the L_P value, a current ripple factor K_R needs to be introduced.



$$K_R = \frac{\Delta I}{2 \times I_{RDC}}$$

When designing the Flyback converter to operate in CCM, it is reasonable to set K_R = 0.25–0.5 for the PoE voltage range. In our case K_R = 0.37 has been chosen, the optimal operation is at maximum 50% Duty Cycle.

Therefore, L_P is obtained in this condition as:

$$L_P = \frac{(V_{IN\min} \times DC_{\max})^2}{2 \times P_{IN} \times f_{sw} \times K_R}$$

V_{INmin} = minimum input voltage

DC_{max} = maximum Duty Cycle

P_{IN} = input power

f_{sw} = switching frequency

K_R = current ripple factor

$$L_P = \frac{(37V \times 0.5)^2}{2 \times 30W \times 220kHz \times 0.37}$$

$$L_P = 70\mu H$$

For DCM operation, K_R = 1 and for CCM operation K_R < 1. The ripple factor is closely related with the transformer size and the RMS value of the MOSFET current. The conduction loss in the switching FET can be reduced through reducing the ripple factor, but too small ripple factor will result in a physically big transformer size.

Once L_P is known, the maximum peak current and RMS current of the switching FET in normal operation are obtained as:

$$I_{RDC} = \frac{P_{IN}}{V_{IN\min} \times DC_{\max}}$$

$$I_{RDC} = \frac{30W}{37V \times 0.5} = 1.6A$$

$$\Delta I = \frac{V_{IN\min} \times DC_{\max}}{L_P \times f_{sw}} = \frac{37V \times 0.5}{70\mu H \times 220kHz} = 1.2A$$

$$I_{FET\_PEAK} = I_{RDC} + \frac{\Delta I}{2} = 1.6A + \frac{1.2A}{2} = 2.2A$$

$$I_{FET\_RMS} = \sqrt{\left[3 \times I_{RDC}^2 + \left(\frac{\Delta I}{2}\right)^2\right] \times \frac{DC_{\max}}{3}} = 1.15A$$

The Si340x Flyback converters are designed for CCM at minimum input voltage and full load condition. As the input voltage increases, or the load decreases, the converter goes into DCM, this is normal behavior.

The turns ratio n needs to be high enough to get the best efficiency in all cases. The turns ratio should be carefully chosen, to ensure the output voltage is maintained even at minimum input voltage.

The following turns ratios are recommended for 5 V output designs:

Table 7.1. Transformer Turns Ratio for 5 V Output Voltage

Power	Primary to Secondary Turns Ratio	Primary to Auxiliary Turns Ratio
Type 1	0.3	0.8
Type 2	0.136	0.45

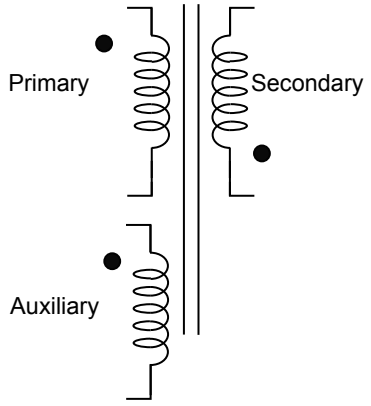


Figure 7.1. Transformer Schematic

The Auxiliary winding is optional, it provides biasing for the IC ensuring higher overall efficiency, the voltage on the Auxiliary winding should be between 12.5 V and 16.5 V. If 16.5 V is exceeded on VT15 pin, the IC could be damaged.

The optimal turns ratio is different for Type 1 and Type 2, because the minimum PoE input voltage is different.

Based on IEEE802.3 standard, the transformer isolation between primary and secondary should withstand at least 1500 V_{RMS}.

7.2 Clamp and Snubber Design

Due to fast switching of the current, high voltage transients occurs on the switching nodes. Those spikes can damage the device, and can cause EMI problems.

A traditional RCD clamp is used on the primary side to protect the switch, and an RC snubber is employed on the secondary side, this is shown below with reference designator R1-C1-D1.

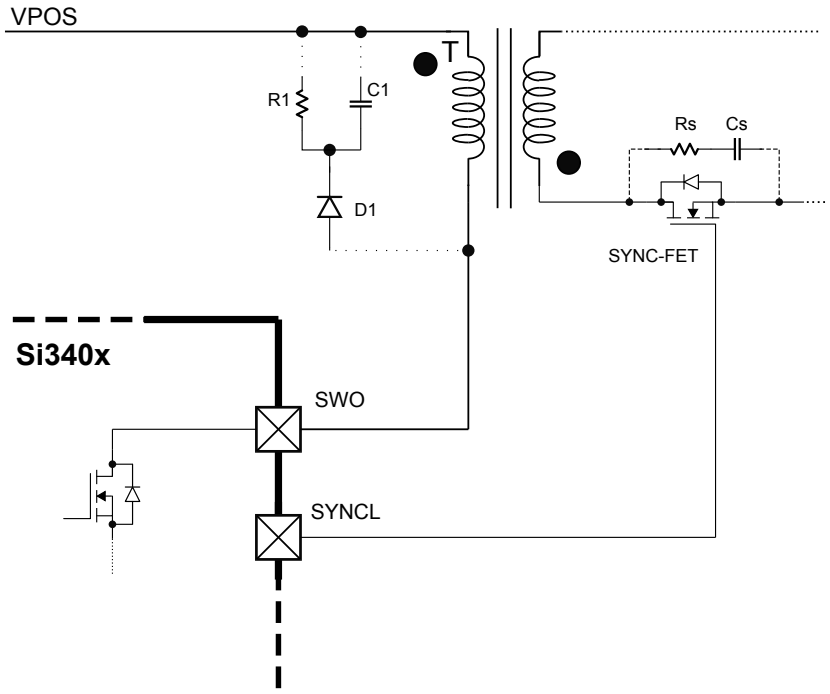


Figure 7.2. Primary Side RCD Clamp and Secondary Side RC Snubber

An RCD clamp circuit used to limit the peak voltage on the drain of the switching FET as an RC snubber is insufficient to prevent switch overvoltage.

The RCD clamp works by absorbing the current in the leakage inductor once the drain voltage exceeds the clamp capacitor voltage. The use of a relatively large capacitor keeps the voltage constant over a switching cycle.

The resistor of the RCD clamp always dissipates power. Even with very little load on the converter, the capacitor will always be charged up to the voltage reflected from the secondary of the converter.

The higher we let the clamp voltage rise on the switch, the lower the overall dissipation. But a balance must be found between dissipation (efficiency) and the total voltage seen across the power FET.

7.2.1 Practical Example of Primary RCD Clamp Design

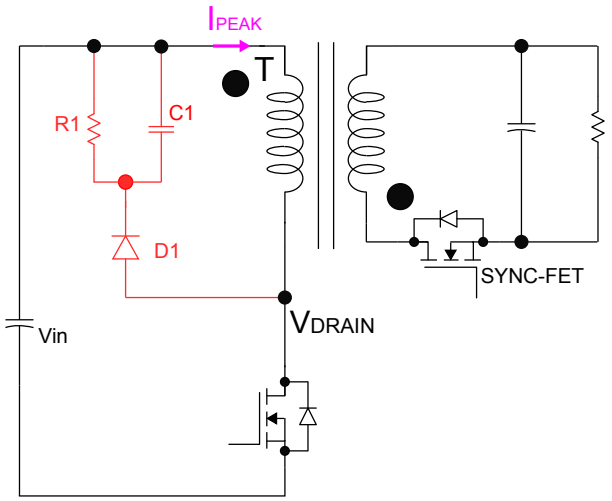


Figure 7.3. Primary RCD Clamp

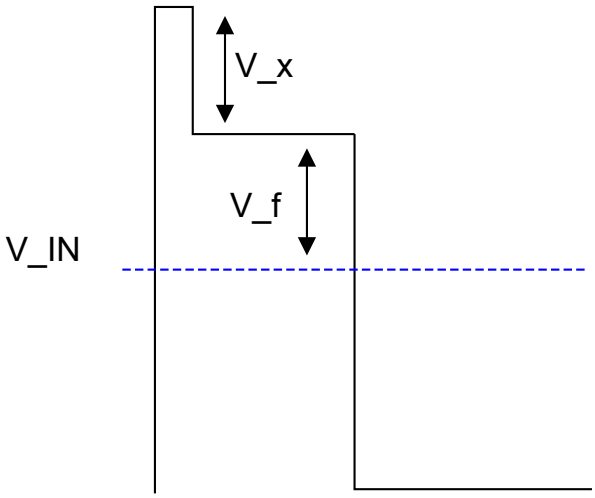


Figure 7.4. Drain (or SWO) Voltage Waveform

Verifying V_{DS_MAX} of Si7898DP from Vishay:

$$V_{DSmax} = 150V$$

Power calculation in leakage inductance:

$$P_{LEAK} = \frac{1}{2} \times L_{leak} \times I^2_{peak} \times f_{sw}$$

$$P_{LEAK} = \frac{1}{2} \times 1\mu H \times 1.55A^2 \times 220kHz$$

$$P_{LEAK} = 264mW$$

Calculation of power dissipated by the RCD clamp:

$$P_{clampMAX} = P_{LEAK} \left(1 + \frac{V\_f}{Vx\_max}\right)$$

$$P_{clampMAX} = 264mW \left(1 + \frac{34V}{150V}\right)$$

$$P_{clampMAX} = 325mW$$

R1 should be 325 mW rated

V_{DSmax} = FET drain-source maximum voltage, from FET datasheet

DC_{LEAK} = power stored in leakage inductance

L_{LEAK} = transformer leakage inductance, from transformer datasheet

I_{PEAK} = measured primary peak current

f_{SW} = switching frequency

Vx_max = targeted maximum voltage

7.2.1.1 R1 Clamp Resistor Calculation

Remove the RCD clamp and measure the voltage on the drain at full output power (30W) and maximum input voltage (57 V).

The left figure below represents the drain $-V_{SS}$ voltage with 57 V input voltage and maximum output power without RCD clamp installed.

It is visible that the RCD clamp is needed for two reasons:

1. To lower the drain-source voltage to protect the switching device.
2. To reduce high-frequency resonance, improving EMI performance.

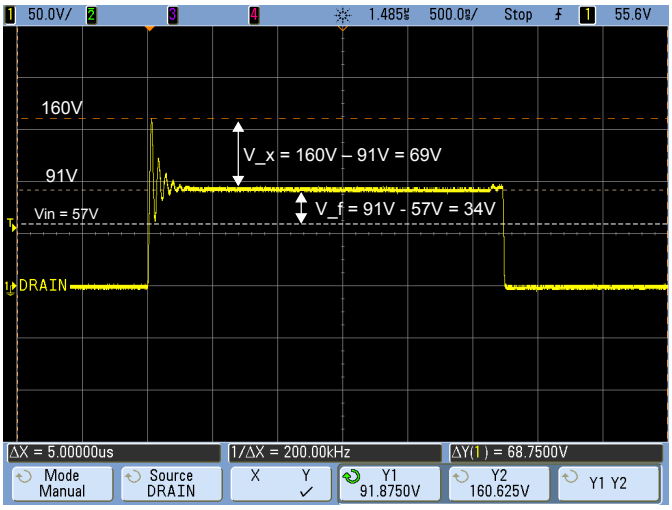


Figure 7.5. Drain Voltage Waveform: 30 W, 57 V Input, RCD Clamp Removed

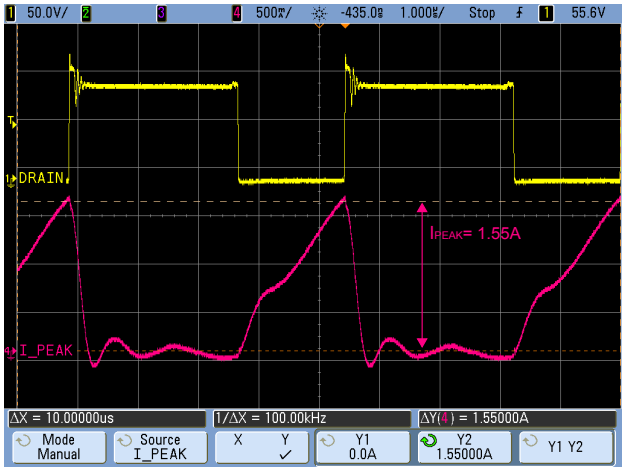


Figure 7.6. Drain Voltage and Transformer Current Waveform: 30 W, 57 V Input, RCD Clamp Removed

The R1 resistor is the element that is crucial in determining the peak voltage V_x, and it should be selected with the following equation:

$$R_1 = \frac{2 \times V\_x \times \left(V\_f + V_{x\_\max}\right)}{L_{LEAK} \times I^2_{PEAK} \times f_{SW}}$$

$$R_1 = \frac{2 \times 69V \times (34V + 150V)}{1\mu H \times 1.55^2 \times 220kHz}$$

$$R_1 = 48.04k\Omega$$

The closest standard resistor value is 47 kΩ.

$$R_1 = 47k\Omega$$

7.2.1.2 C1 Clamp Capacitor Selection

C1 capacitor of the clamp needs to be large enough to keep a relatively constant voltage while absorbing the leakage energy. Apart from this consideration, its value is not critical, and will not affect the peak voltage when the snubber is working properly.

$$C_1 = 10nF$$

7.2.1.3 D1 Clamp Diode Selection

After the clamping period is finished, the circuit resumes ringing. With ideal components, this would not happen. However, the diode of the RCD clamp has a finite reverse recovery time which allows the leakage inductor current to flow in the opposite direction in the diode, resulting in ringing. The type of diode chosen for the RCD snubber is crucial. It must be as fast as possible with the proper voltage rating.

RS1B fast switching diode with quite high (t_{RR} = 150 ns) reverse recovery time is recommended.

$$D_1 = RS1B$$

In the figure below, the drain voltage is shown with the RCD clamp installed:

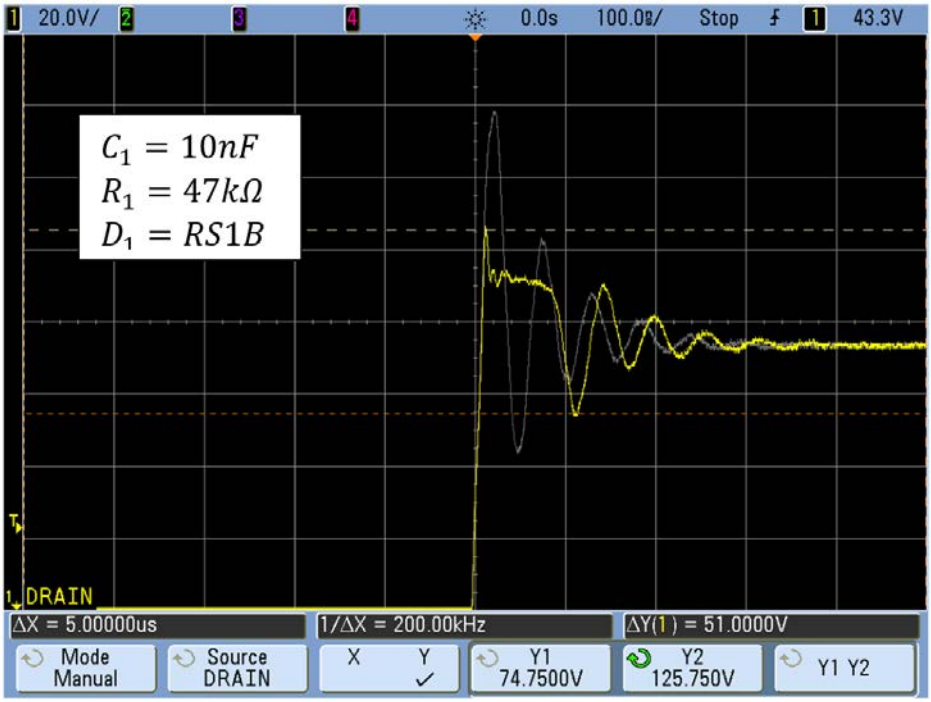
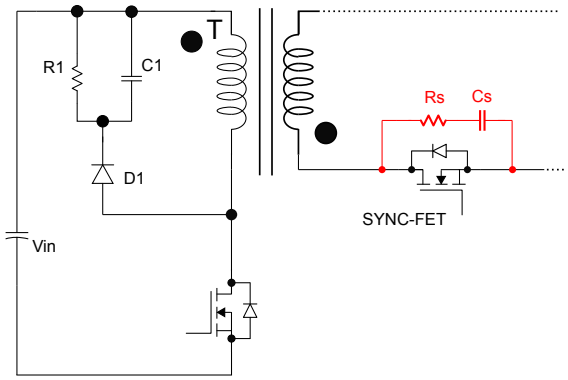


Figure 7.7. Drain Voltage without (Grey) and with (Yellow) RCD Clamp Installed

The installed RCD clamp reduced the drain voltage from 160 V to 126 V.

7.2.2 Practical Example of Secondary RC Snubber Design



V_{DSMAX}—FET drain-source maximum voltage, from FET data sheet

P_{LEAK}—power in leakage inductance

L_{LEAK}—transformer leakage inductance, from transformer data sheet

I_{PEAK}—primary peak current

f_{SW}—switching frequency

V_{x_max}—targeted maximum voltage

Figure 7.8. Secondary Side RC Snubber

When the primary-side MOSFET is turned on, severe voltage oscillation occurs across the secondary-side diode (or sync-FET). This is caused by the oscillation between the diode parasitic capacitance (C_D) and transformer secondary side leakage inductance (L_{LEAK_SEC}). To reduce the oscillation, an RC snubber is typically used.

Measure the resonance frequency on the diode (or Sync-FET) without snubber

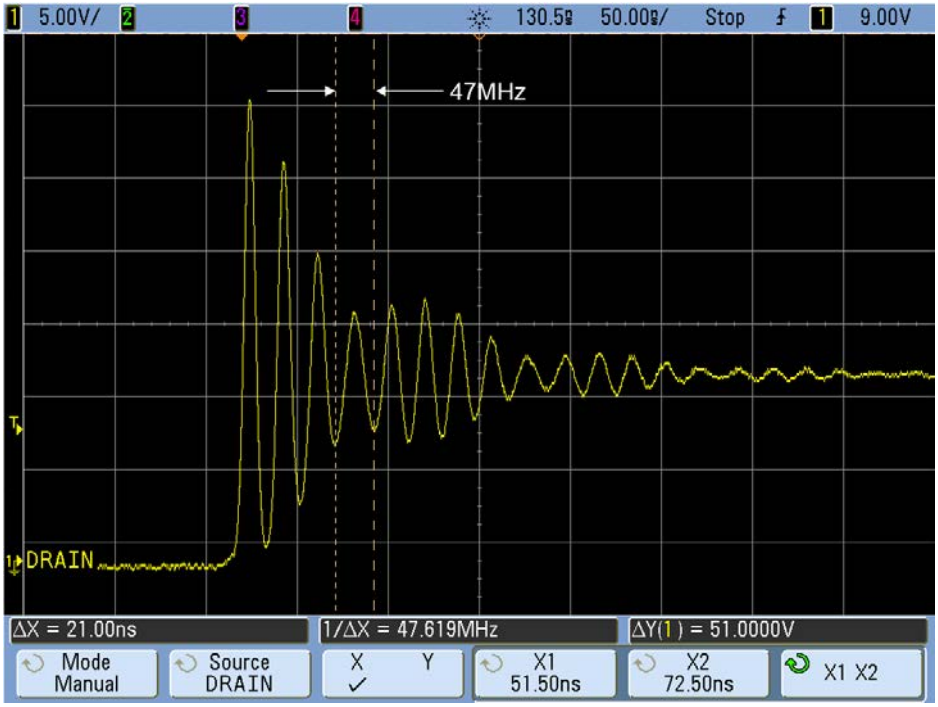


Figure 7.9. Ringing on Synchronous FET (or Diode) without RC Snubber

From the above figure, the ringing frequency is:

$$f_{RINGING} = 47MHz$$

Install a C_{TEST} capacitor such that the new resonance frequency becomes around half the $f_{RINGING}$.

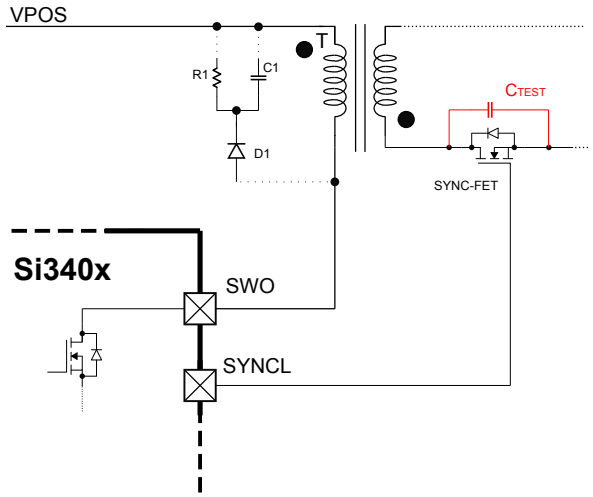


Figure 7.10. Adding C_{TEST} in Parallel with the Sync-FET

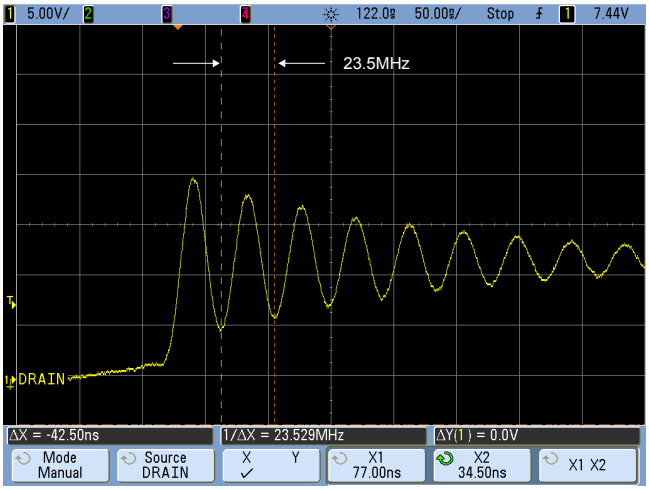


Figure 7.11. Resonant Frequency with C_{TEST} Added

C_{TEST} = 3 nF has been installed, the measured resonance frequency is:

$$f_{ringing\_test} = 23.5MHz$$

Calculate the capacitance of the sync-FET (or diode) C_D.

$$C_D = \frac{C_{TEST}}{\left[\left(\frac{f_{ringing}}{f_{ringing\_test}}\right)^2 - 1\right]} = \frac{3nF}{\left[\left(\frac{47MHz}{23.5MHz}\right)^2 - 1\right]} = 1nF$$

Calculate the secondary side leakage inductance L_{LEAK_SEC}

$$L_{LEAK\_SEC} = \left(\frac{1}{2\pi \times f_{ringing}}\right)^2 \times \frac{1}{C_D} = \left(\frac{1}{2\pi \times 47MHz}\right)^2 \times \frac{1}{1nF} = 11.47nH$$

Calculate the snubber resistor value R_S

$$R_S = \sqrt{\frac{L_{LEAK\_SEC}}{C_D}} = \sqrt{\frac{11.47nH}{1nH}}$$

$$R_S = 3.3\Omega$$

Calculate the snubber capacitor value C_S:

$$C_S = 3 \times C_D = 2 \times 1nF$$

$$C_S = 3nF$$

The following figure shows the voltage waveform on the synchronous FET (or diode) with R_S-C_S not installed (left) and installed (right):

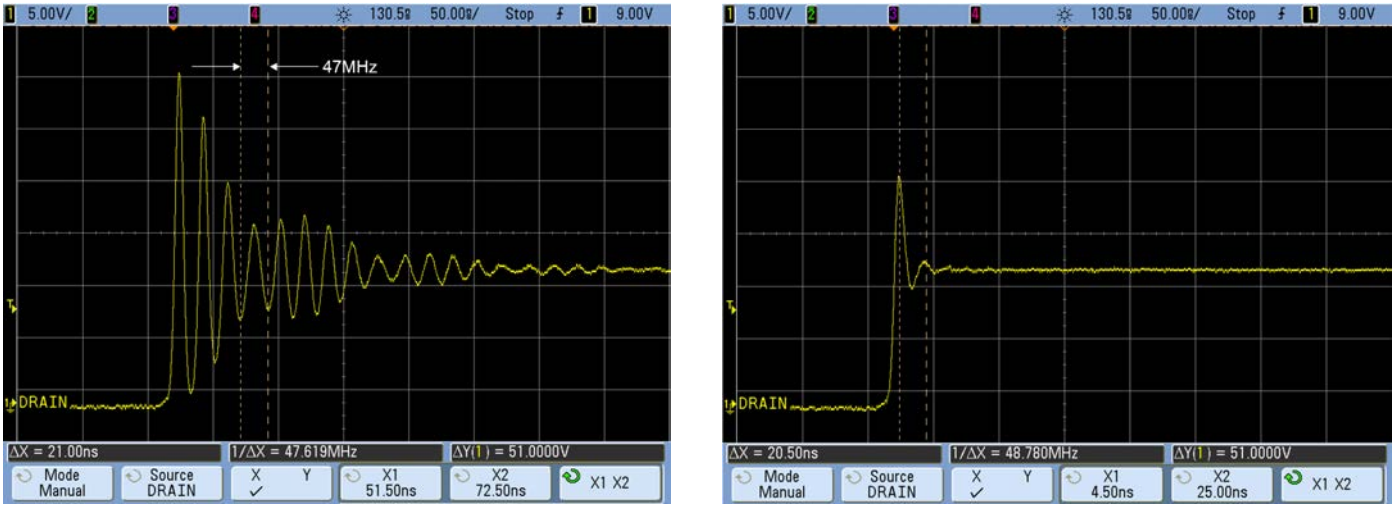


Figure 7.12. Voltage Waveform on Sync-FET (or Diode) without RC Snubber on the Left, and with RC Snubber Installed on the Right

The high frequency, high voltage ringing has been successfully damped with the installed RC snubber.

7.2.2.1 EMI Control

If further EMI performance improvement is required, an additional RC snubber can be added in parallel with the primary side clamp diode, as shown in the figure below:

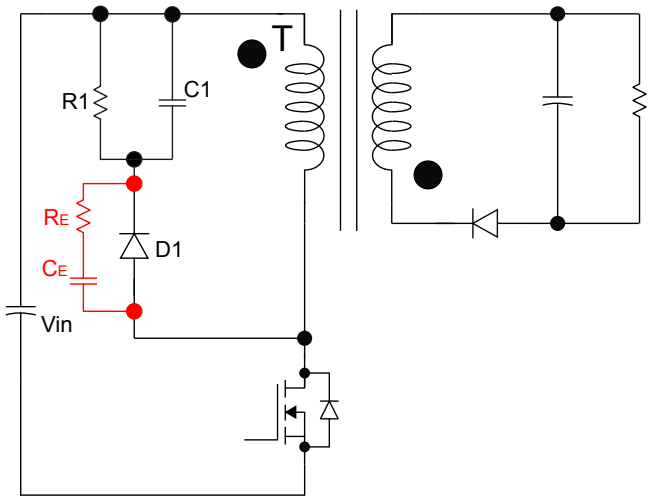
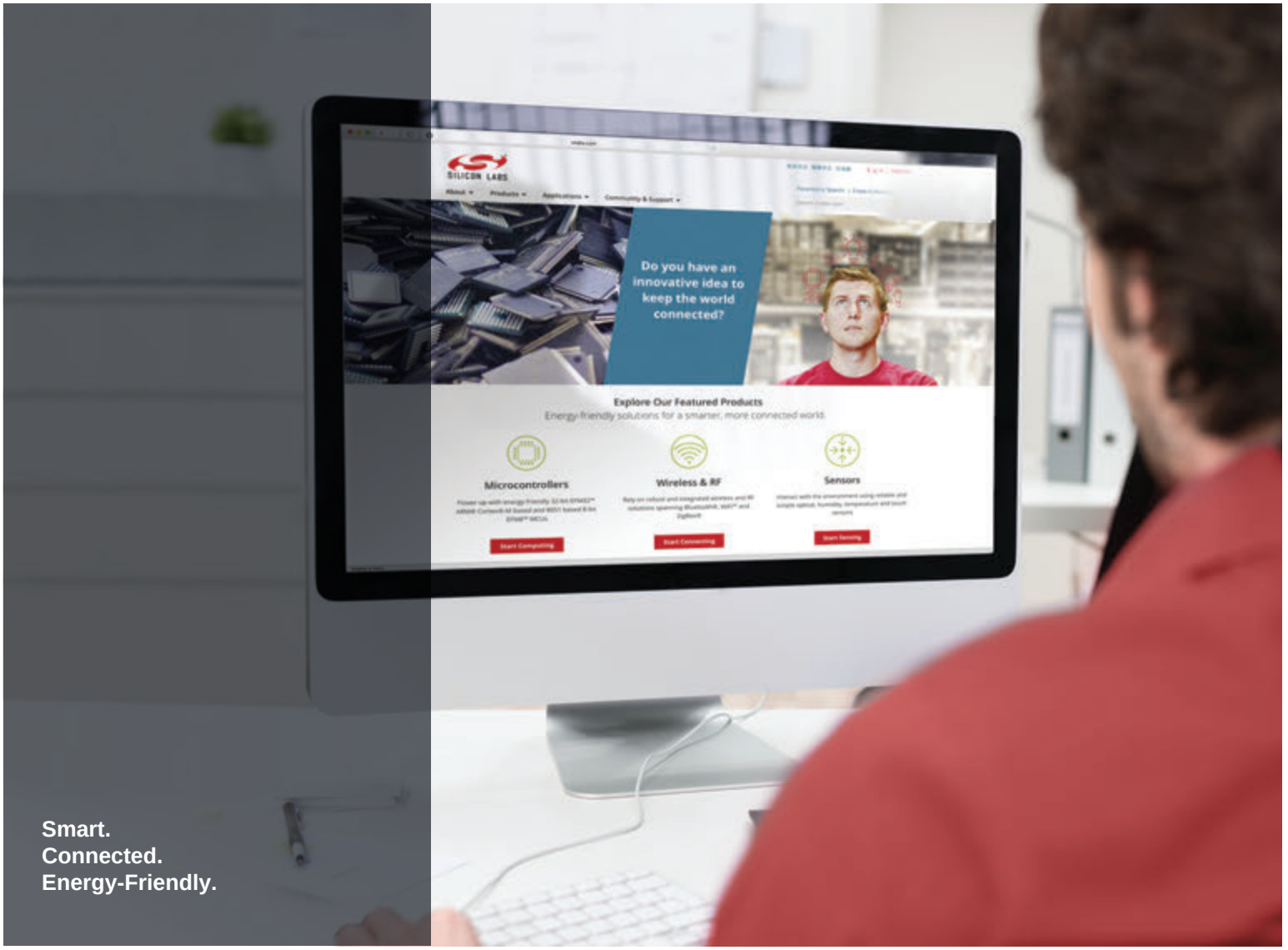


Figure 7.13. Additional RC Snubber Placement for EMI Improvements

To get the optimal values for R_E and C_E follow the same procedure as described in 7.2.2 Practical Example of Secondary RC Snubber Design.



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