



## PCB Layout Guidelines

This application note provides guidelines for successfully designing the PCB layout for Amulet AGB75LC04-QU-E.

It covers the following main topics:

- Number of PCB layers
- SDRAM memory interface
  - USB signals
  - Display signals
  - Backlight Noise

## PCB layers

Stack up should include a closely spaced power/ground plane pair. A minimum of 6 layers is necessary.

Recommendation:

Layer 1: signal

Layer 2: ground plane, unbroken

Layer 3: power plane/islands, signals

Layer 4: signal/power routing

Layer 5: ground plane, unbroken

Layer 6: signal

Use a 0.1uF X7R Bypass caps on every power pin on the chip.

Place the Crystal as close to the chip as possible.

## SDRAM memory interface

The DRAM placement and orientation should be given priority over other unassociated components in order to minimize trace lengths. Closely following the signal trace routing guidelines allows trace lengths to be reduced.

Minimum rule 5-mil trace width, 7 mil trace space, 15-mil space from different group signal

Maximum difference in Trace length is 250mils

Use a 0.1uF X7R Bypass caps on every power pin on the chip.

For improved EMI control put series resistance, 15 ohm or 22 ohm on signal

## USB signals

Keep the USB as close to the chip as possible.

Keep the USB signal pair trace no more than 50mils difference in length.

Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.

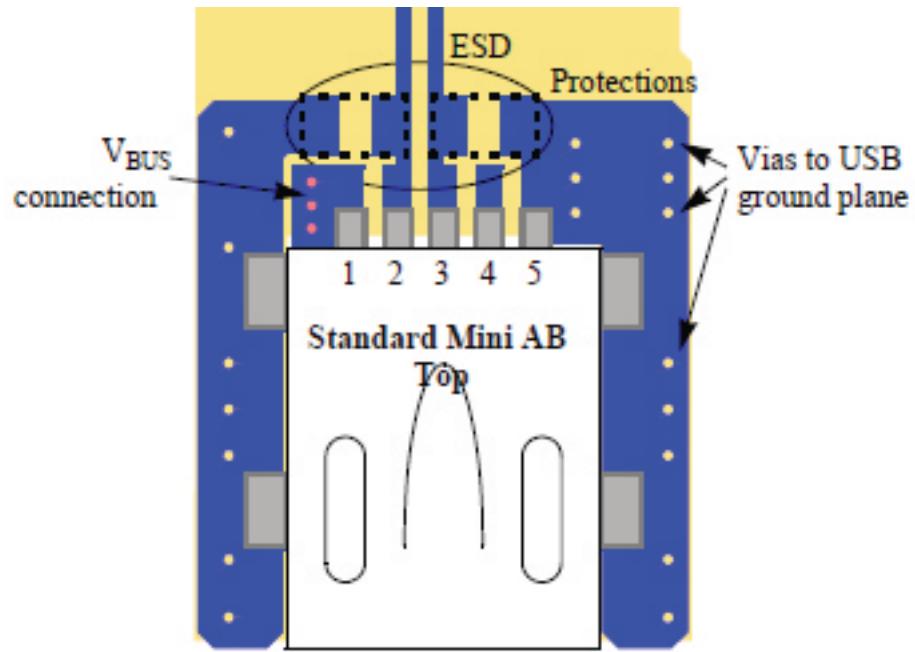
Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.

Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality.

Route all traces over continuous GND plane with no interruptions.

Minimum rule 10-mil trace width, 7 mil trace space, 20-mil space from different group signal

Full-speed USB provide ESD suppression using in-line ferrites and capacitors that form a lowpass filter. This technique doesn't work for high-speed USB due to the much higher signal rate of high-speed data. A recommended device that has been tested successfully is a Littelfuse® component, PulseGuard® PGB0010603MR (0603 package size). Proper placement of the devices is on the data lines as close as possible to the USB connector.



## Backlight Noise

Keep the backlight circuit away from the display signals and from all other chips.

Use a separate power plane.



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Tel (408) 374-4956  
Fax (408) 374-4941  
<http://www.AmuletTechnologies.com>  
[Sales@AmuletTechnologies.com](mailto:Sales@AmuletTechnologies.com)  
[Support@AmuletTechnologies.com](mailto:Support@AmuletTechnologies.com)  
1475 S. Bascom Ave, Suite 111  
Campbell, CA 95008 USA

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