Creating Custom LCDProfiles

Custom LCDProfiles are often needed to be created for GEMstudio. The entries to the LCDprofiles are found in the corresponding datasheet which are provided by the LCDManufacturer
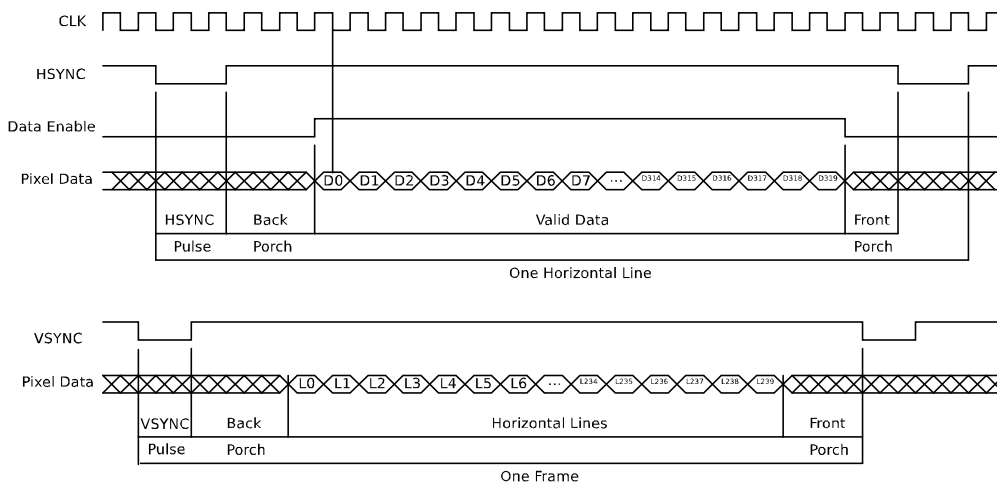
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Amulet

Introduction

One of Gem Graphical OS's core strengths is the ability to drive nearly any LCD with a dot clock interface up to 800x600 resolution. A LCD with a dot clock interface has a pixel clock as well as control signals typically labeled HSYNC and VSYNC or Data Enable driving the display. To accommodate the unique timing requirements of individual displays, a profile must be created to provide the Graphical OS the parameters it needs to drive the LCD. GEM studio includes a utility called LCD Profile Editor to enter this data and create the profile. It is accessible under the Tools menu as well as a workspace button upon program launch. The parameters needed to complete the LCD profile will be found in the datasheet for the LCD, contact the manufacturer if you do not have one for your display.

LCD Datasheets

Datasheets for LCDs run the gamut from fully documented with all needed parameters clearly indicated to incorrect or incomplete documentation requiring some experimentation with different settings to determine a usable configuration.

Within the datasheet there should be a table of timing parameters listed and some timing diagrams. Below is an example timing diagram and shows all parameters needed to create the profile, with the values needed provided in the table. Sometimes manufacturers label parameters by a different name; if this is the case, use the timing diagram as a legend by comparing it with the following reference timing diagram.
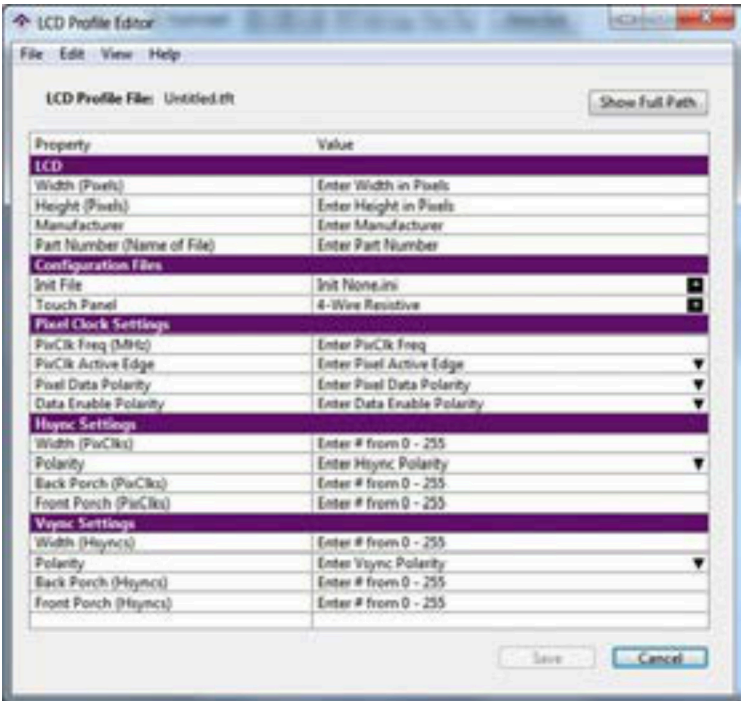
The diagram is a composite of two separate diagrams, the top four waveforms provide the Horizontal timing information and the bottom two waveforms provide the Vertical timing information. The Horizontal timing is measured in Pixel Clocks(PixClks) as expressed by the CLK waveform with a new pixel transmitted every clock cycle as represented by D0 through D319. The Vertical timing is measured in horizontal scan lines (Hsyncs) represented as L0 through L239. Frequently one or more parameters are missing in a datasheet with the addition of other parameters. Most commonly the Back Porch is not labeled and in its place a Blanking Period is provided. The Blanking Period is the sum of the SYNC pulse Width and Back Porch. To obtain the value for the Back Porch subtract the SYNC pulse Width from the Blanking Period. Other instances of alternate parameters should use the timing diagram to determine a formula for converting the provided parameters into the needed parameters.

LCD Profile Editor

Following is an image of the LCD Profile Editor dialog and the parameters necessary to define a new LCD profile. The first

two parameters are the pixel dimensions of the LCD, and the next two are used to categorize profiles by Manufacturer and name the profile. The next category is the Configuration Files where the first parameter is the initialization file needed for displays which have a SPI configuration port. Contact Amulet technical support (support@amulettechnologies.com) if your display requires SPI configuration to place it into dot clock mode, otherwise leave this parameter as Init None.ini. The Touch Panel configuration file specifies what type of touchscreen is used with the LCD, the options are 4-wire, 5-wire, none, or STK-CY-043 (capacitive). The specific model number for the capacitive module is given because the Amulet OS only supports the Amulet Capacitive Touch Module and will not work with other capacitive touch sensors.

The next three categories are the key parameters that are determined from the datasheet. The PixClock Freq is the frequency the LCD is driven; care must be used when entering this value to achieve the desired results. The Amulet chip does an integer divide of its clock (80 Mhz) to derive the pixel clock. This has the effect of rounding up the clock frequency to the next integer division of 80 when the calculated divisor is not an integer. For example, a LCD may state that the acceptable pixel clock range is 25 to 33 MHz. If you chose to use the mean value of 29 Mhz the Amulet would calculate the divisor to be 2.758, but since it is an integer division the divisor is truncated to 2. This yields a pixel clock of 40 MHz which is outside the LCD's acceptable frequency range. You must account for this when choosing a pixel clock fre-

quency for the LCD to be correctly driven. Using our example, the divisor of 3 yields a pixel clock of 26.667 MHz which is within the acceptable range. To assure that we don't accidentally round past the target frequency, selecting a pixel clock of 26MHz will guarantee a pixel clock of 26.667 MHz. If you find that two integer divisors yield acceptable clock frequencies you may choose either; but we recommend choosing the lower frequency because more processing time will be available to the OS, resulting in a faster GUI.

The Pixel Clock Active Edge is the clock edge the LCD samples the pixel data, in the example timing diagram it is represented by the vertical line descending from the clock waveform to D0 in the pixel data waveform and in the example it is falling. The Pixel Data Polarity should be positive unless otherwise stated in the datasheet. Data Enable Polarity specifies the signal's polarity for the active data region and in the example Data Enable Polarity is positive.

The next two categories specify the parameters for the SYNC pulses. The Width is the actual width of the SYNC pulse, the Polarity is the level of the SYNC pulse which is negative in the example. The Front Porch is the period of time after valid data but before the SYNC pulse and the Back Porch is the period of time after the SYNC pulse but before valid data.

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Miscellaneous LCD Modes

Some displays provide both a Data Enable and HSYNC/VSYNCdot clock interface. These displays use either interface but not both at the same time. Some LCDsuse the activity of the control signals to determine which interface is being used. The Amulet OSdrives all signals simultaneously, so for these displays you must not connect the control signal(s) you are not using, failure to do so will result in a non-operational LCD. The LCDdatasheet will typically state this requirement if it is necessary for the LCD's correct operation. When we develop a board which has this type of dual inter-face, we choose the HSYNC/VSYNCinter-face because it provides more control over the frame positioning on the screen in the rare circumstance this level of control is needed.

Some displays provide what is called a VSYNCinterface, its name may lead some to believe it is the same as the HSYNC/VSYNCdot clock interface, but it is not. VSYNCinterfaces are employed on LCDs which have internal frame buffers and can accept data in a relaxed timing format so long as an entire frame is written within a specified time period. These displays can be driven using the Graphical OS's SYNC pulse interface because the meaning of the VSYNCpulse is the same and the LCD will operate correctly with the VSYNCgen-erated by the Graphical OS.

Small LCDs(less than 3" diagonal)will typi-cally have what is called a microprocessor

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