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Agilex™ 5 FPGA E-Series 065B Modular Development Kit User Guide

Online Version
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Contents

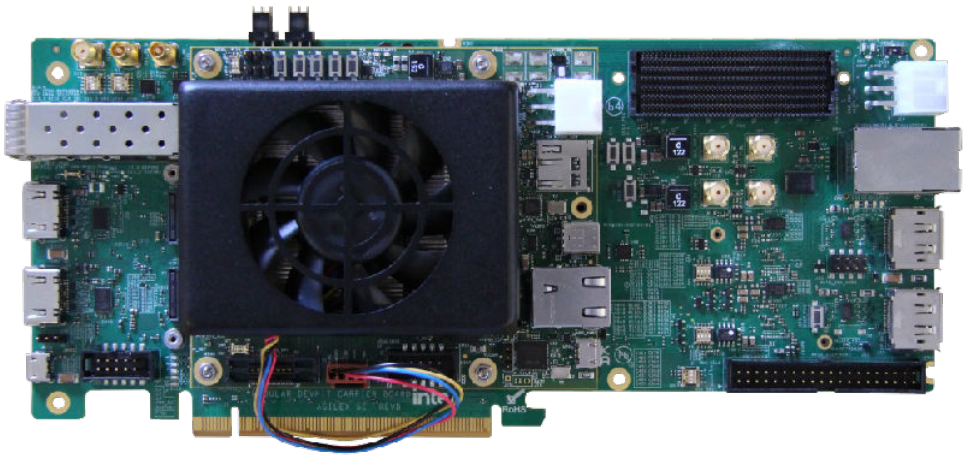
1. Overview

Agilex™ 5 FPGA E-Series 065B Modular Development Kit is a complete design environment that includes both hardware and software you need to develop the Agilex 5 FPGA E-Series 065B designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of the Agilex 5 FPGA E-Series 065B designs.

Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Starting Serial Number Identifier
Agilex 5 FPGA E-Series 065B Modular Development Kit (ES)	MK-A5E065BB32AES1	A5ED065BB32AE6SR0	A5E565BMK0000011

Figure 1. Agilex 5 FPGA E-Series 065B Modular Development Kit (Top View)



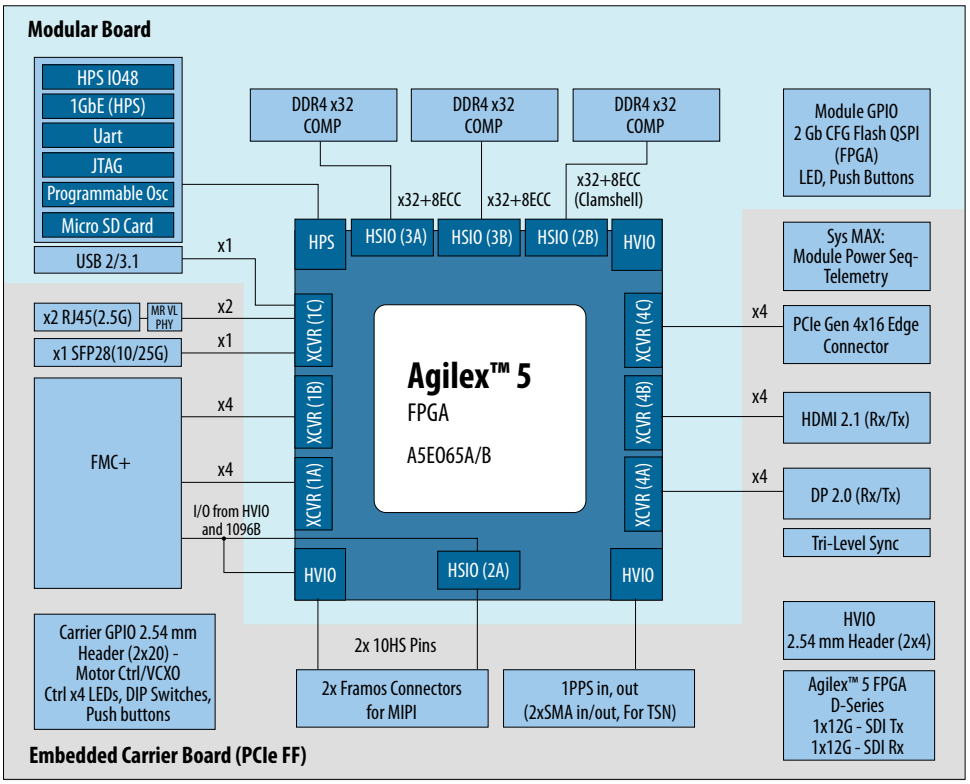
Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 5 FPGA E-Series 065B Modular Development Kit.

Related Information

Development Kit Components on page 64

1.1. Block Diagram

Figure 2. Agilex 5 FPGA E-Series 065B Modular Development Kit Block Diagram



Refer to the *Agilex 5 ES Device Errata and User Guidelines* for more information.

Note: 2.5G SGMII Ethernet on transceiver bank (1C) and USB3.1 are not supported with the current release of the ES development kit. Updates are scheduled for publication with the future release of the software and production version of the development kit.

Related Information

Agilex 5 ES Device Errata and User Guidelines

1.2. Feature Summary

- Agilex 5 E-Series A5E065X device in 32 mm x 32 mm, 1591B Package
  - Dual core Arm* Cortex*-A76, Dual core Arm Cortex-A55
  - 65K logic elements
  - High-voltage I/O (HVIO)-120 (6 banks)
  - High-speed I/O (HSIO)-384 (IO96B, 4 banks)
  - Low-voltage differential signaling (LVDS)-192 (IO96B)
  - Transceivers-24 (6 banks, 4 lane each)
- FPGA configuration:
  - 2 Gb flash for Active Serial (AS) x4 configuration mode
  - JTAG header for device programming
  - Built-in Intel® FPGA Download Cable II for device programming
- Programmable clock sources
- Transceiver (XCVR) interfaces:
  - 1A: FPGA mezzanine card (FMC) XCVR Lane 4 to Lane 7 (17 Gbps max)
  - 1B: FMC XCVR Lane 0 to Lane 3 (17 Gbps max)
  - 1C:
    - UX0, UX1: 2.5G Time-sensitive networking (TSN)
    - UX2: USB3.1 (on Modular board)
    - UX3: SFP28 (10G)
  - 4A: DisplayPort (DP) 2.0
  - 4B: High-Definition Multimedia Interface (HDMI) 2.1
  - 4C: PCIe* Gen 3/4 x4

    Note: The ES development kit is installed with –6S speed grade FPGA and only supports up to PCIe Gen 3.0.
- Memory interfaces:
  - 1x 8GB DDR4-1600 (x32 w/o ECC) for fabric I/O memory on Bank 2B
  - 1x 8GB DDR4-1600 (x32 with ECC) for fabric I/O memory on Bank 3B
  - 1x 8GB DDR4-1600 (x32 with ECC) for HPS processor memory on Bank 3A
- Other interfaces:
  - IO48 interface for HPS
  - 8 channel MIPI interface to high-speed I/Os (HSIO) bank
- Mechanical
  - Modular board: 113 mm x 94 mm x 1.6 mm
  - Carrier board: 255 mm x 111 mm x 1.6 mm
  - Active heatsink solution for FPGA
- Operating environment:
  - Maximum ambient temperature of 0°C–30°C

1.3. Box Contents

- Agilex 5 E-Series 065B Modular board (with heatsink)
- Carrier board
- 12V DC power adapter
- RJ45 cable
- Micro USB cable
- Micro SD card

Related Information

Agilex 5 FPGA E-Series 065B Modular Development Kit Website
More information about the Agilex 5 FPGA E-Series 065B Modular Development Kit unboxing video.

1.4. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0ºC to 30ºC
ICC load current	36 A
ICC load transient percentage	204 A/us
FPGA maximum power supported by active heat sink/fan	60 W

Related Information

Handling the Board on page 8

2. Getting Started

2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit of installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix C.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

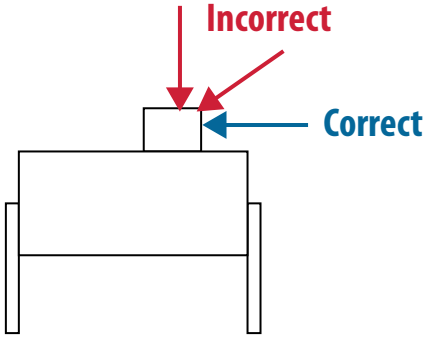
Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a vibration environment.

2.2.1. Handling the DIP Switches

Operating the DIP Switch Safely

- Do not apply excessive force when operating the slide-type switch, as this might cause damage or deformation, leading to malfunction.
- Apply the operating load from the side of the striker.
- Avoid applying force at an angle or from above the striker, as this might deform the switch contact.



Setting the DIP Switch

- To set the slide-type switch, use a small, rounded object like the end of a ballpoint pen or a tiny screwdriver.
- Do not use sharp tools, such as tweezers, to set the switch as they might damage it.
- Do not use a mechanical pencil, as its point could leave lead particles behind. These particles might interfere with the switch and the internal circuit board, potentially causing malfunction. Lead buildup can also reduce the dielectric strength of the circuit board.

2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Pro Edition software
- Agilex 5 FPGA E-Series 065B Modular Development Kit software
- Ashling* RiscFree* Integrated Development Environment (IDE)
- Intel FPGA Download Cable II driver

2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the FPGA Software Download Center webpage of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Altera® FPGA Software Installation and Licensing*.

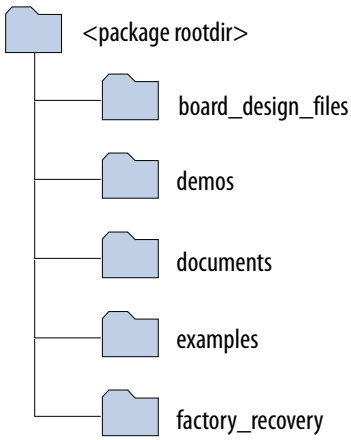
Related Information

- Quartus Prime Pro Edition User Guide: Getting Started
- Altera FPGA Software Installation and Licensing

2.3.2. Installing the Development Kit

1. Download the Agilex 5 FPGA E-Series 065B Modular Development Kit installer package from the Agilex 5 FPGA E-Series 065B Modular Development Kit webpage on the Intel website.
2. Unzip the Agilex 5 FPGA E-Series 065B Modular Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 3. Agilex 5 FPGA E-Series 065B Modular Development Kit Directory Structure



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

Table 3. Installed Development Kit Directory Description

Lists the file directory names and a description of their contents.

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
`documents`	Contains the development kit documentation.
`examples`	Contains the sample design files for the Agilex 5 FPGA E-Series 065B Modular Development Kit: • Board Test System (BTS): BTS GUI, Power GUI, and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3.3. Installing the Ashling* RiscFree Integrated Development Environment (IDE)

RiscFree is Ashling's Eclipse* C/C++ Development Toolkit (CDT) based integrated development environment (IDE) for Altera FPGAs Arm*-based HPS and RISC-V based Nios® V processors. The RiscFree IDE provides a complete, seamless environment for C and C++ software development.

RiscFree IDE has two types of installation options:

- Bundled installation option when installing the Quartus Prime software
- Standalone installation which requires you to install one of the following to use the debugger:
  - The Quartus Prime Programmer and Tools
  - The Quartus Prime software

For the installation instructions of the RiscFree IDE, refer to the *Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide*.

Related Information

Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide

2.3.4. Installing the Intel FPGA Download Cable II Driver

The Agilex 5 FPGA E-Series 065B Modular Development Kit includes onboard Intel FPGA Download Cable II circuits for FPGA and system MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

- Cable and Adapter Drivers Information
- Intel FPGA Download Cable II User Guide

2.4. Quick Start Guide

Refer to the Agilex 5 FPGA E-Series 065B Modular Development Kit Quick Start Guide to learn how the development kit works by default after power up.

Related Information

Agilex 5 FPGA E-Series 065B Modular Development Kit Quick Start Guide

3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 5 FPGA E-Series 065B Modular Development Kit for specific use cases.

3.1. Default Settings

The Agilex 5 FPGA E-Series 065B Modular Development Kit ships with its board switches, which are pre-configured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the *Factory Default Switch Settings* tables to return to its factory settings before proceeding ahead.

Note: "X" refers to Don't Care in the table below.

Table 4. Factory Default Switch Settings (Modular Board)

Switch	Default Position	Function
S4.1	ON	• ON—MSEL 1 Low • OFF—MSEL 1 High *Note:* If you want to control the configuration over BTS, set this switch to OFF state.
S4.2	ON	• ON—MSEL 2 Low • OFF—MSEL 2 High *Note:* If you want to control the configuration over BTS, set this switch to OFF state.
S1.1	X	• ON—SWITCH0 (GPIO) • OFF—SWITCH0 (GPIO)
S1.2	X	• ON—SWITCH1 Low • OFF—SWITCH1 High

Table 5. Factory Default Switch Settings (Carrier Board)

Switch	Default Position	Function
S13.1	OFF	• ON—PCIe edge clock • OFF—Clock from onboard Si52202
S13.2	OFF	• ON—USER_DIPSW3 Low • OFF—USER_DIPSW3 High
S13.3	OFF	• ON—EXT header JTAG selected • OFF—USB JTAG selected
S13.4	OFF	• ON—FPGA bypassed from JTAG chain • OFF—FPGA Selected

continued...

Switch	Default Position	Function
S7.1	OFF	• ON—USER_DIPSW0 Low • OFF—USER_DIPSW0 High
S7.2	OFF	• ON—USER_DIPSW1 Low • OFF—USER_DIPSW1 High
S7.3	OFF	• ON—USER_DIPSW2 Low • OFF—USER_DIPSW2 High
S7.4	ON	• ON—Disable FMC JTAG mode • OFF—Enable FMC JTAG mode
S1.[3:4]	OFF (1) ON (0)	1PPS_MUX_SEL[1:0] • 00—No output at J26 SMA • 01—CLK_10M_OUT_SMA at J26 • 10—TSN_HPS_1PPS_OUT_1V8 at J26 • 11—TSN_HVIO_1PPS_OUT_1V8 at J26
SW2	POS-3	• POS-3—ATX 12V input powers the system • POS-1—PCIe EF 12 V powers the system
SW4	OFF	• ON—Enables PCIe JTAG mode • OFF—Enables onboard UBII mode
S5[1:4]	ON, OFF, OFF, OFF	PHY 0 CONFIG0: • PHY ADDRESS—00000
S2[1:4]	OFF, ON, OFF, OFF	PHY 1 CONFIG0: • PHY ADDRESS—00001
S6.1	OFF	MIPI 0 Vertical Sync (XVS) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI0 module OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI0 module
S6.2	OFF	MIPI 0 Horizontal Sync (XHS) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI0 module • OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI0 module
S6.3	OFF	MIPI 0 Trigger (XTRIG) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI0 module • OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI0 module

continued...

Switch	Default Position	Function
S11.1	OFF	MIPI 1 Vertical Sync (XVS) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI1 module • OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI1 module
S11.2	OFF	MIPI 1 Horizontal Sync (XHS) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI1 module • OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI1 module
S11.3	OFF	MIPI 1 Trigger (XTRIG) • ON—Enables Signal connection from Agilex 5 FPGA device to MIPI1 module • OFF—Disable Signal connection from Agilex 5 FPGA device to MIPI1 module

3.2. Powering Up the Development Kit

If you are using the board in a bench-top setup, follow these steps:

1. Make sure the switch SW2 is set to **POS-3** position.
2. Use the provided 240 W power adapter to supply power through 2x3 ATX connector J14 on the Carrier board.

When the board powers up, the LED DS2 on the Carrier board illuminates, indicating that the board power up is successful. If the LED DS2 is not turned on, it indicates that one of the voltage regulators is not turned on.

Related Information

Development Kit Components on page 64
Details about the J14, SW2, and DS2 components on the Agilex 5 FPGA E-Series 065B Modular Development Kit.

3.3. Performing Board Restore

This development kit ships with GHRD design stored in the QSPI flash device U24 for the Active Serial (AS) x4 configuration.

You must perform board restore using the following instructions through the Quartus Prime Programmer GUI.

3.3.1. Restoring Board QSPI Flash U24 with Default Factory Image

Note: The QSPI flash is pre-programmed with GHRD image. Completing the steps overwrites the ASx4 image. Refer to RocketBoards.org to recover and update GHRD image on QSPI flash.

1. Make sure SW4[2:1] on the Modular board are [off off] (JTAG mode).
2. Open the Quartus Prime Programmer GUI, and click **Auto Detect**.
3. Right click on the FPGA device, and choose **change file** to use the GHRD image.
4. Start the Programmer until it is 100% successful.
5. Power off the board and set SW4[2:1] as ASx4 fast mode [on on].

3.3.2. Restoring SD Card with the Default Factory Image

Note: The SD card is pre-programmed with sdimage. Completing the steps overwrites this image. Refer to RocketBoards.org to recover and update sdimage on SD card.

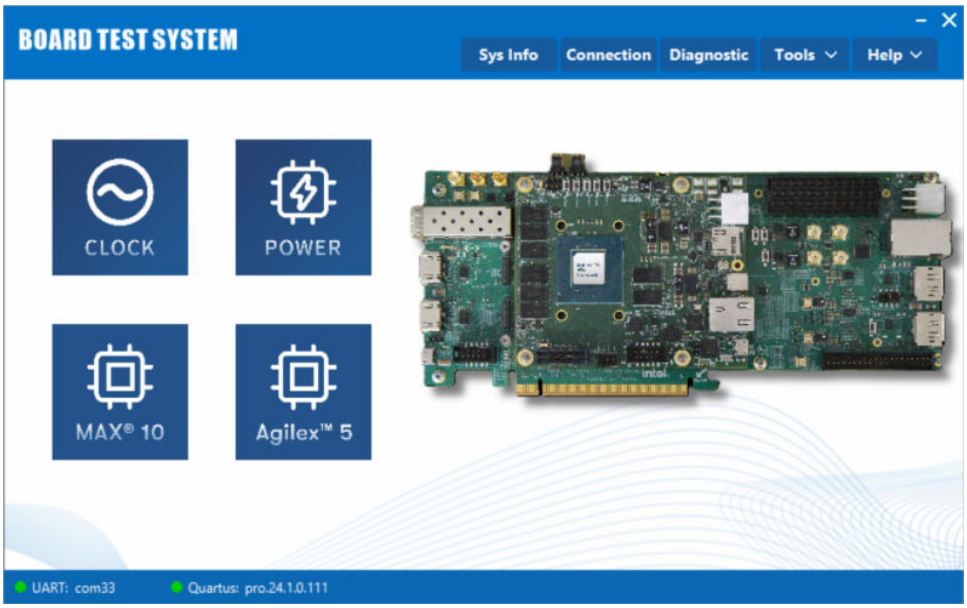
1. Download SD card image from RocketBoards.org and extract the archive, obtaining the `.wic` file.
2. Write the SD card image to the micro SD card using `dd` on Linux* or Win32DiskImager on Windows*.

4. Board Test System

The Agilex 5 FPGA E-Series 065B Modular Development Kit includes design examples and the board test system (BTS) graphical user interface (GUI) to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

The following figure shows the GUI of a board that is in factory configuration.

Figure 4. BTS GUI



4.1. Set Up BTS GUI Running Environment

4.1.1. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `readme.txt` file in the top level of the package directory.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Nios II JTAG Debug Module and the Signal Tap logic analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

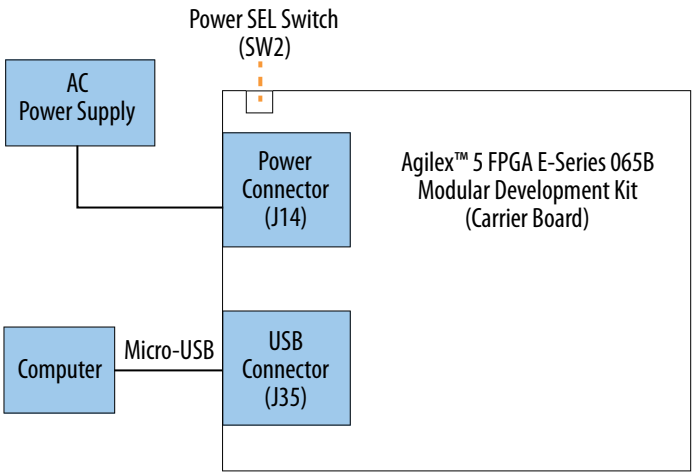
The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable *QUARTUS_ROOTDIR*. You can also change it through **Environment Variables** in the **System Properties** in Windows*. The BTS uses this environment variable to locate the Quartus Prime library.

4.1.2. Running the BTS GUI

With the power to the board off, follow these steps.

1. Connect the micro-USB cable to your PC and the board.

Figure 5. USB and Power Connection to Run BTS GUI

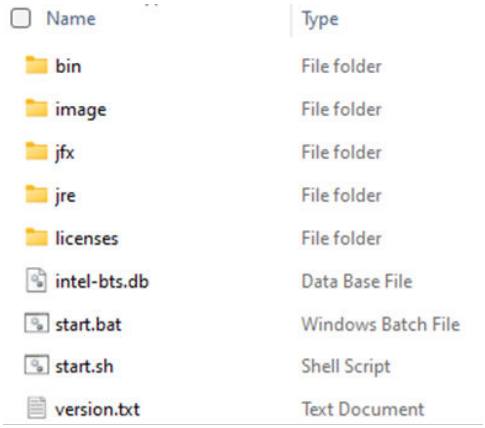


2. Check the development board switches and jumpers are set according to your preferences. Refer to the Development Kit Setup section.
3. Turn on the board power switch.

   Note: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application.

Navigate to the <*packagedir*>`\examples\board_test_system` directory to run BTS. The BTS release folder always includes the following files, as shown in the figure below.

Figure 6. BTS Package Folder



You can run BTS GUI with the following scripts:

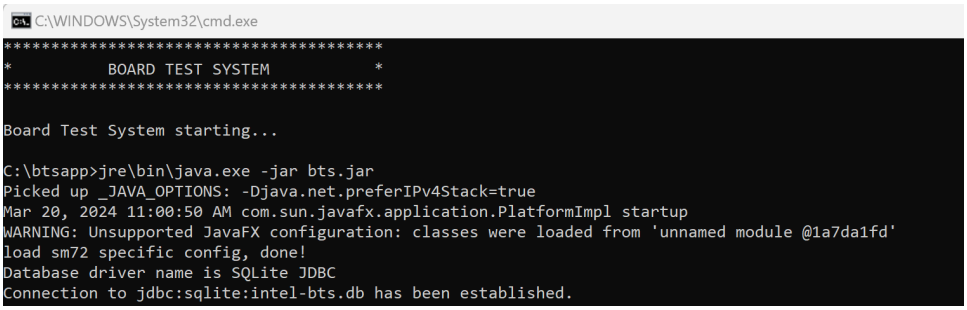
1. On **Windows** system, double click the `.bat` files to run BTS GUI.
2. On **Linux** system, add current user to the group "dialout" to ensure the access to UART, using the following commands:

```
# ls -l /dev/ttyUSB*
# sudo usermod -a -G dialout $USER
# groups
```

Then, set permissions correctly and run the shell script using the following commands:

```
# cd  $TOP_LEVEL/examples/board_test_system
# chmod +x ./start.sh
# chmod +x -R ./jre/
# sh start.sh
```

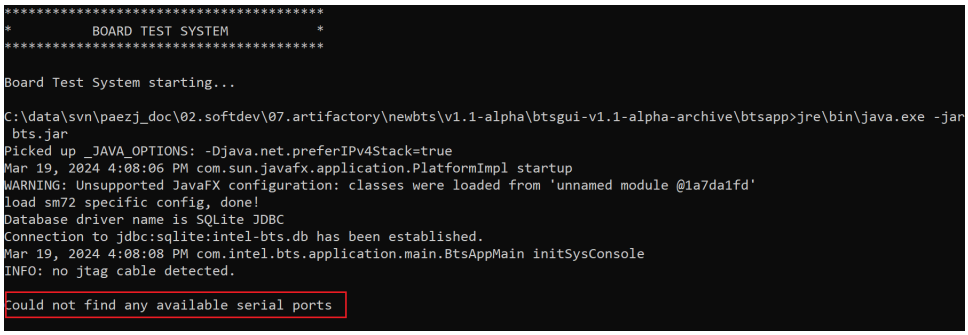
Figure 7. Windows Console of BTS Launching



4.2. Troubleshooting for Launching BTS

No Available Serial Ports

Figure 8. Failure of "Could not find any available serial ports"



1. Check if the micro-USB is connected physically.
2. Check if the USB Serial Port driver is installed successfully.
   a. On your Windows taskbar, right click **Start (Windows logo) ➤ Computer Management**.
   b. Check if the UART ports of the Agilex 5 FPGA E-Series 065B Modular Development Kit can be recognized by the operating system. The UART ports have the following characteristics:
      - Manufacturer = FTDI
      - Four consecutive serial ports number. For example, COM8/COM9/COM10/COM11.
   c. If no valid UART ports are in the list, it may be due to USB Serial Port driver is not installed. You can download and install the FTDI* USB Serial Port driver. Refer to the related information for the download link.

Figure 9. UART Port List

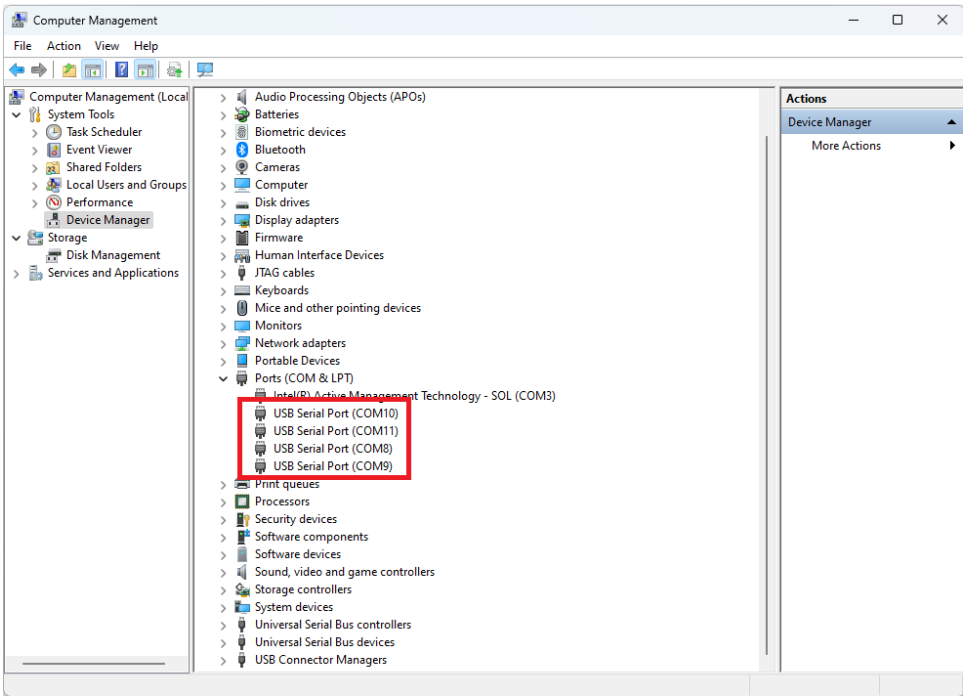
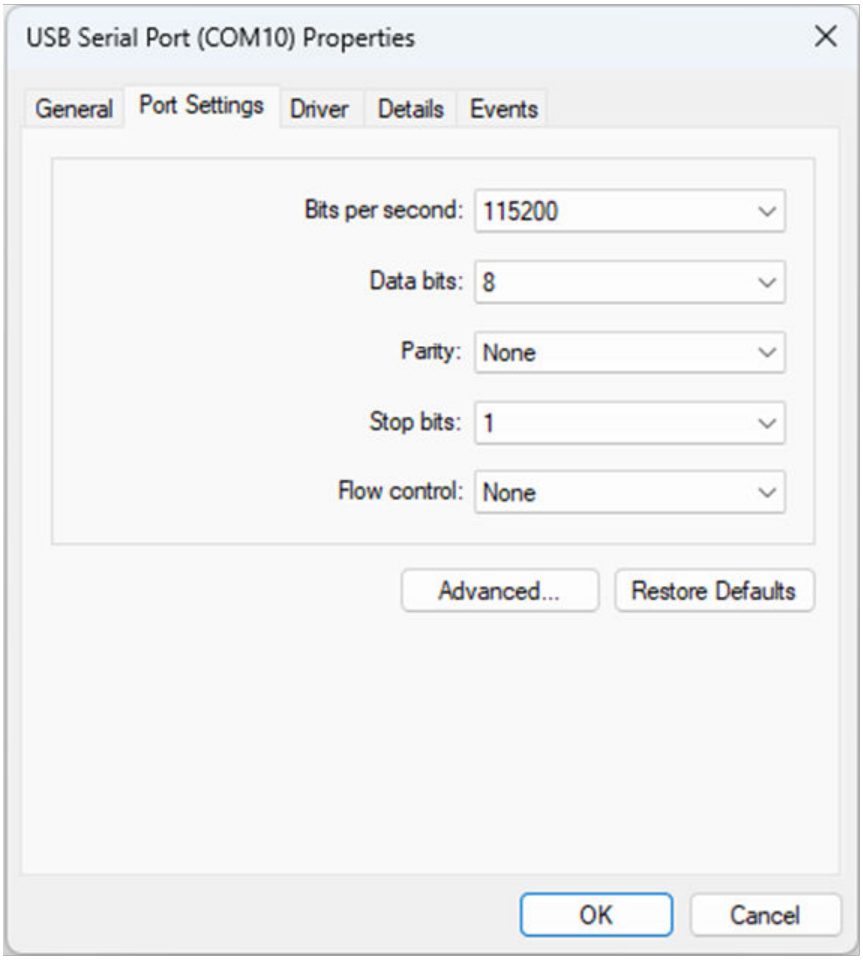
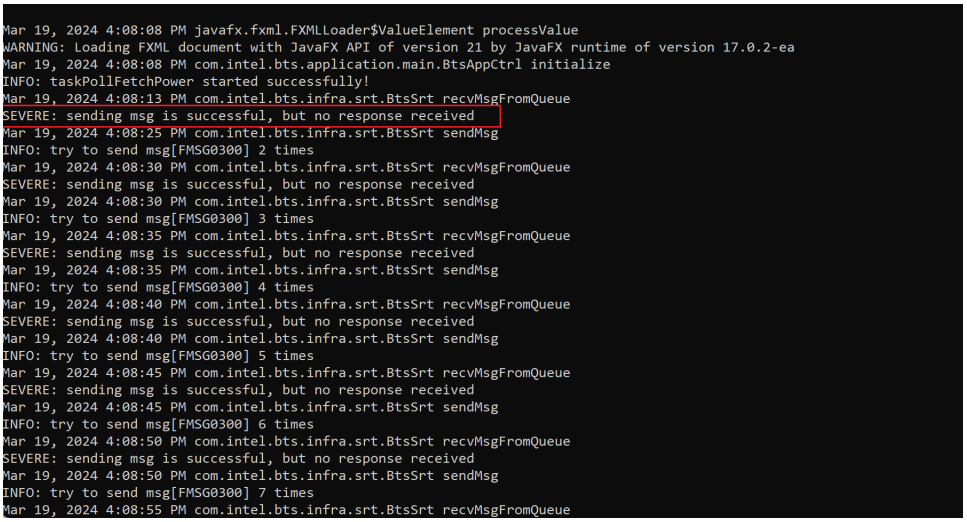


Figure 10. UART Port Configuration



No Response after Message Sent

Figure 11. Failure of "sending msg is successful, but no response received"



The issue roots that the UART does not work correctly or the Nios software in the System MAX 10 does not work well, follow the check list below:

1. Check if the BTS is launched before the board is ready.
2. Check if there are some third-party UART tools that have occupied the port.
3. Check if there are other BTS instances and close them.
4. Check if uninstall and install UART device in "Computer Management" can solve the issue.
5. Check if the LED DS8 on the Carrier board is blinking, as it indicates that the Nios software is running well. Otherwise, power cycle the board or reprogram the System MAX 10.

Related Information

USB Serial Port Driver

4.3. BTS Functionalities

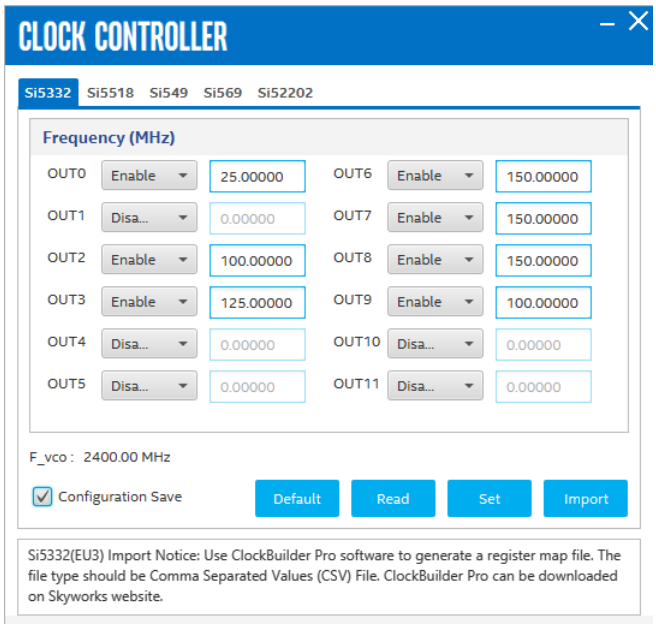
This section describes each control in the BTS.

4.3.1. The Clock Functionality

The Clock Controller tool can change the onboard programmable PLLs to a large range of customized frequency. The Clock Controller communicates with the System MAX 10 device through UART, and only a micro-USB cable is required. Select the **Clock** icon on the BTS GUI to start the Clock Controller feature.

4.3.1.1. Si5332

Figure 12. The Si5332 Setting Page



- **Read**: Reads the current frequency setting for the oscillator associated with the active tab.
- **Set**: Sets the programmable oscillator frequency for the selected clock to the value in the OUTx output controls. Frequency changes might take several milliseconds to take effect. Altera recommends resetting the FPGA logic after changing frequencies.
- **Import**: Imports the register list generated from the tool of the Skyworks* Clockbuilder Pro software. Register changes are volatile after power cycling.
- **Default**: Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.
- **Configuration Save**: Clock GUI supports to save the configuration to flash if you want the board to load the user settings on power-up next time. To do so, follow these steps:
  1. Select the **Configuration Save** checkbox.
  2. Click the **Import** or **Set** button to change the clock frequency setting, meanwhile the new configuration is saved in flash.

  You can also erase the configuration in flash by following these steps:
  1. Select the **Configuration Save** checkbox.
  2. Click the **Default** button to change the clock frequency setting to default value and erase the flash.

Related Information

Skyworks Solution
More information about the ClockBuilder Pro software.

4.3.1.2. Si5518

Figure 13. The Si5518 Setting Page

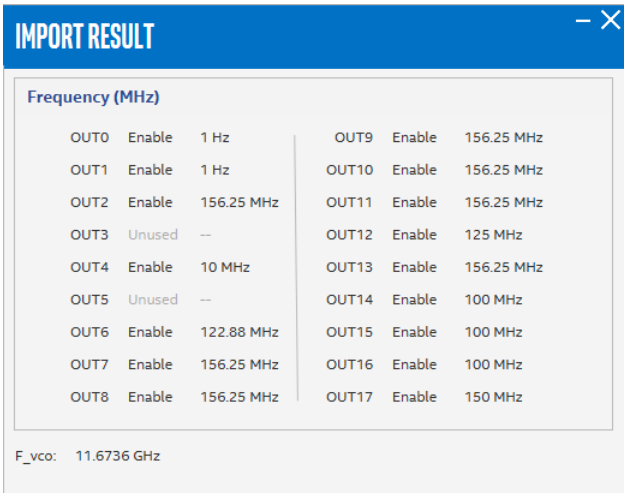
- **Status**: Displays more detail status.
- **Default**: Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.
- **Soft Reset**: Initiates a global soft reset. The global soft reset does not download the firmware and frequency plan from the NVM. Instead, it starts the firmware and frequency plan currently running on the device. The device behaves like it has been rebooted.
- **Import**: Imports configurable Si5518 firmware and user boot binary files, which are generated from the tool of the Skyworks* Clockbuilder Pro software. The current settings can be displayed after importing of the design.
- **Configuration Save**: Clock GUI supports to save the configuration to flash if you want the board to load the user settings on power-up next time. To do so, follow these steps:

  1. Select the **Configuration Save** checkbox.
  2. Click the **Import** button to change the clock frequency setting, meanwhile the new configuration is saved in flash.

  You can also erase the configuration in flash by following these steps:

  1. Select the **Configuration Save** checkbox.
  2. Click the **Default** button to change the clock frequency setting to default value and erase the flash.

Figure 14. The Import Result of Si5518

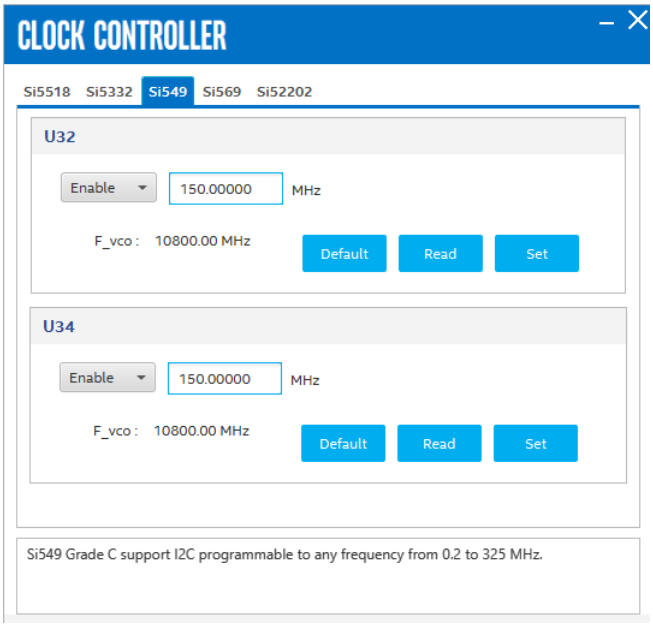


Related Information

Skyworks Solution
More information about the ClockBuilder Pro software.

4.3.1.3. Si549

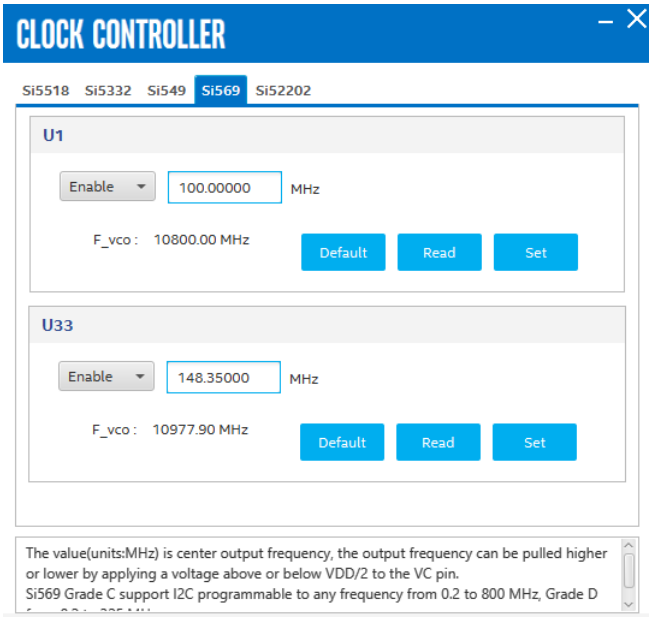
Figure 15. The Si549 Setting Page



- **Read**: Reads the current frequency setting for the oscillator associated with the active tab.
- **Set**: Sets the programmable oscillator frequency for the selected clock to the value in the output controls.
- **Default**: Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

4.3.1.4. Si569

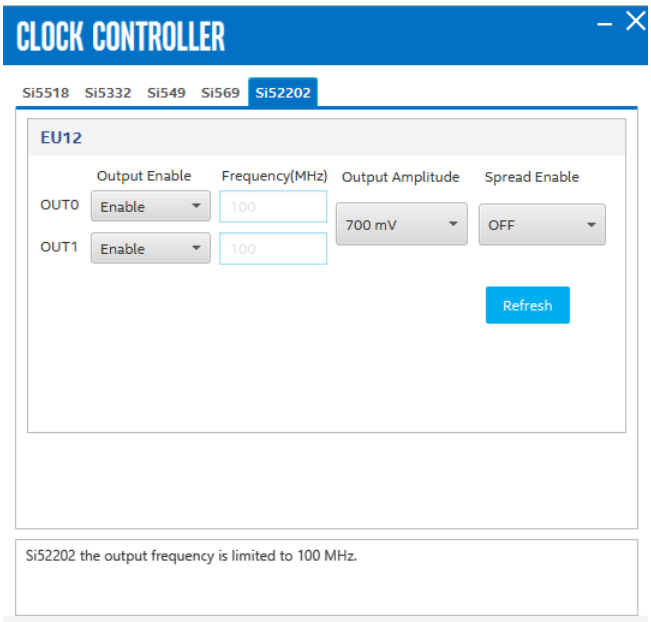
Figure 16. The Si569 Setting Page



Note: This tab has similar control functions as the Si549 tab.

4.3.1.5. Si52202

Figure 17. The Si52202 Setting Page



Note: The output frequency of Si52202 is fixed to 100 MHz. The GUI supports for enabling or disabling the output, and changing the output amplitude and spread enable.

4.3.2. The Power Functionality

The Power Monitor tool reports most power rails' voltage, current, and power information on the board. It also collects temperature from the FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor communicates with the System MAX 10 device through UART, and only a micro-USB cable is required.

Select the **Power** icon on BTS GUI to launch the Power Monitor feature. The Power Monitor GUI includes two modules:

- Power Monitor
- Temperature Monitor

4.3.2.1. Power Monitor

The Power Monitor module reads the real-time data from power chips.

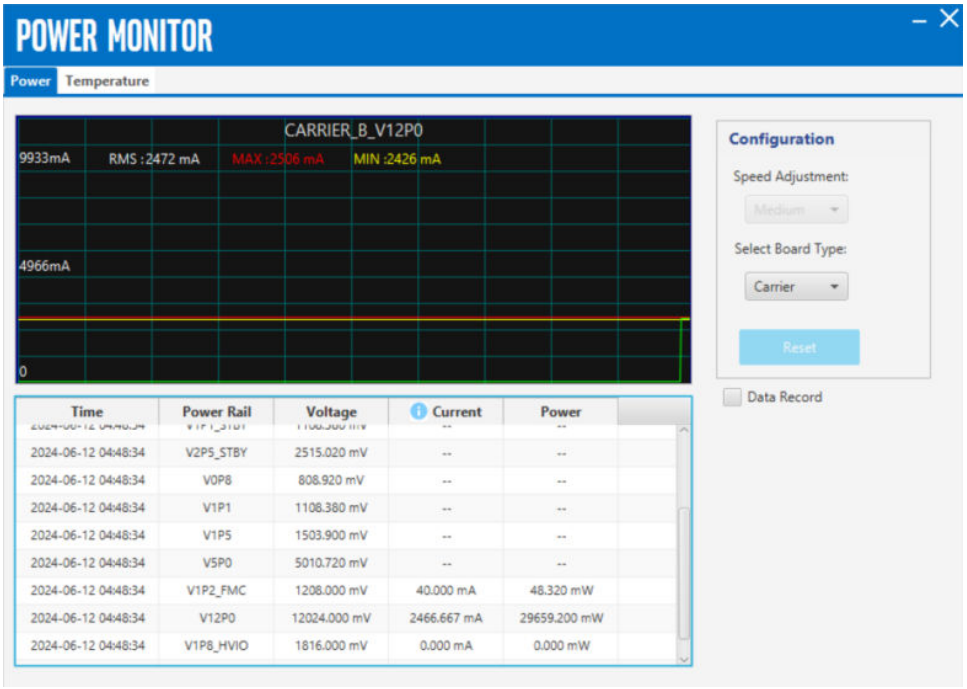
The Carrier board supports the rails listed below:

- V1P8_STBY
- V3P3
- V3P3_STBY
- V1P2_STBY

- V1P1_STBY
- V2P5_STBY
- V0P8
- V1P1
- V1P5
- V5P0
- V1P2_FMC
- V12P0
- V1P8_HVIO
- V12P0_PCIE

For detailed information, refer to the power tree in the schematic document under *<packagedir>\board_design_files\Carrier_board\schematic* directory.

Figure 18. Power Tab—Carrier Board



The Modular board supports the rails listed below:

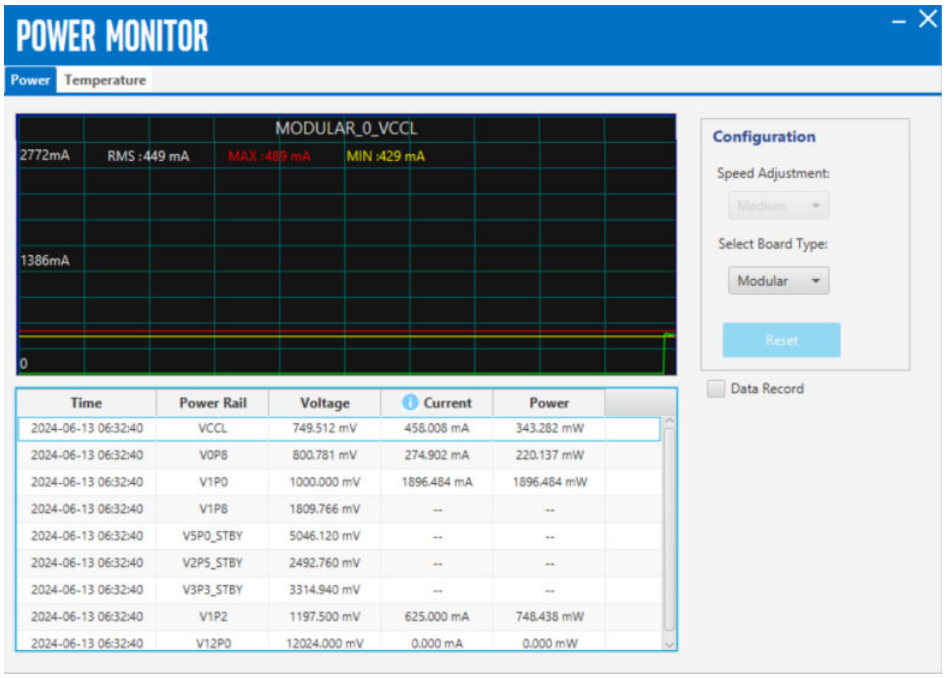
- VCCL
- V0P8
- V1P0
- V1P8
- V5P0_STBY
- V2P5_STBY

- V3P3_STBY
- V1P2
- V12P0

Note: If the BTS displays "--" for any rail, it means that the reporting of the current of that rail is not supported (applies to both Carrier and Modular boards).

For detailed information, refer to the power tree in the schematic document under `<packagedir>\board_design_files\Modular_board\schematic` directory.

Figure 19. Power Tab—Modular Board



Display Configure

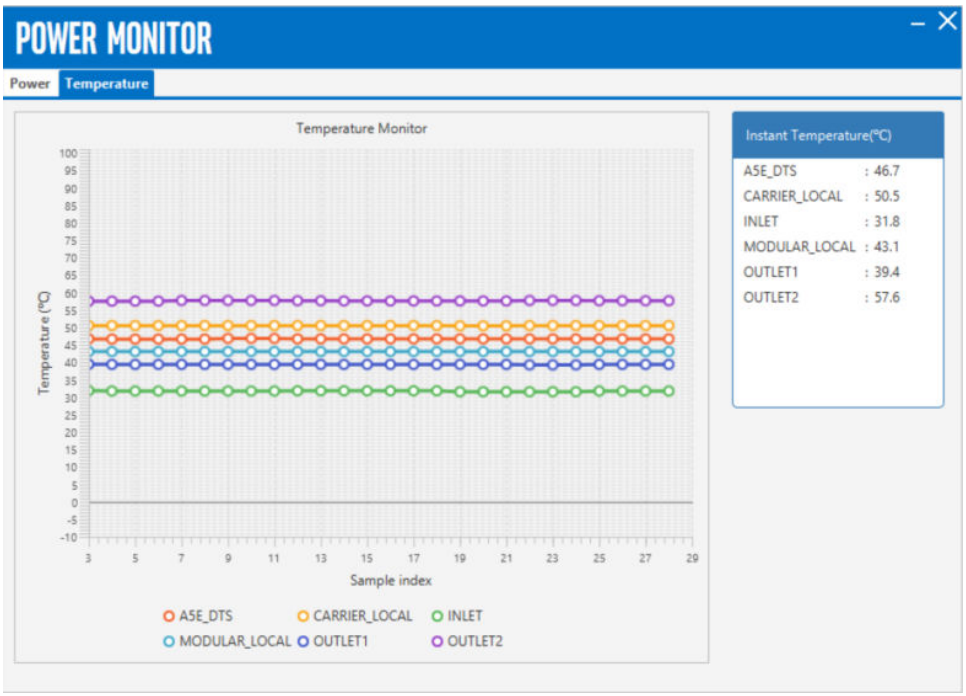
- **Speed Adjustment**: Adjusts the update rate of the current curve.
- **Select Board Type**: Select to show the rails of the Carrier or Modular board.
- **Reset**: Regenerates the graph.

Data Record

When the box is checked, the telemetry data of all the power rails can be recorded. It saves the data into a `.csv` file in the log directory.

4.3.2.2. Temperature Monitor

Figure 20. Temperature Tab



The BTS can monitor the temperature and presents the data visually.

The BTS can also show the locations of the temperature sensors in main interface.

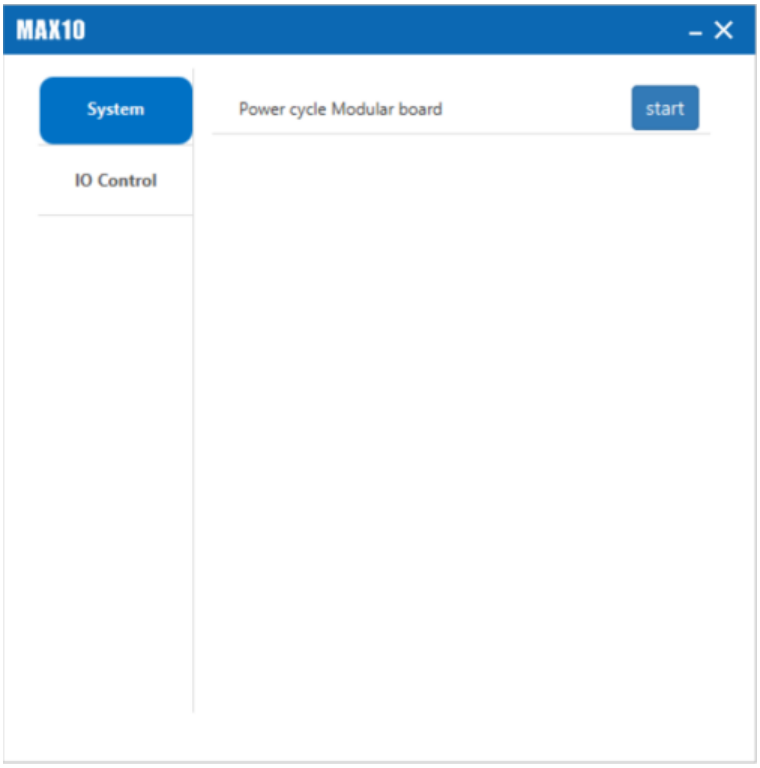
4.3.3. The MAX 10 Functionality

The Agilex 5 FPGA E-Series 065B Modular Development Kit uses a MAX 10 as Board Management Control (BMC) master. It provides you with a UART based controller to power cycle the Modular board and set the MSEL.

Select the **MAX** icon on BTS GUI to launch the MAX 10 feature.

4.3.3.1. The System Tab

Figure 21. System Tab



You can power cycle the Modular board by clicking the **start** button.

4.3.3.2. The IO Control Tab

Figure 22. IO Control Tab—MSEL

You can use MSEL to set the configuration mode of the Agilex 5 FPGA device. The MSEL functions like a real DIP switch S4 on the board. The virtual switches only take effect when the physical switches are turned off.

Note: You must power cycle the Modular board after the MSEL setting for the configuration mode takes effect.

Type	Switch	Board Label
DIP Switch	S4.1	MSEL1
DIP Switch	S4.2	MSEL2

Figure 23. IO Control Tab—CLOCK MUX

MAX 10 supports to set the CLOCK MUX, set the new configuration by clicking the **Apply** button.

4.3.4. The Agilex 5 FPGA Functionality

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Agilex 5 device.

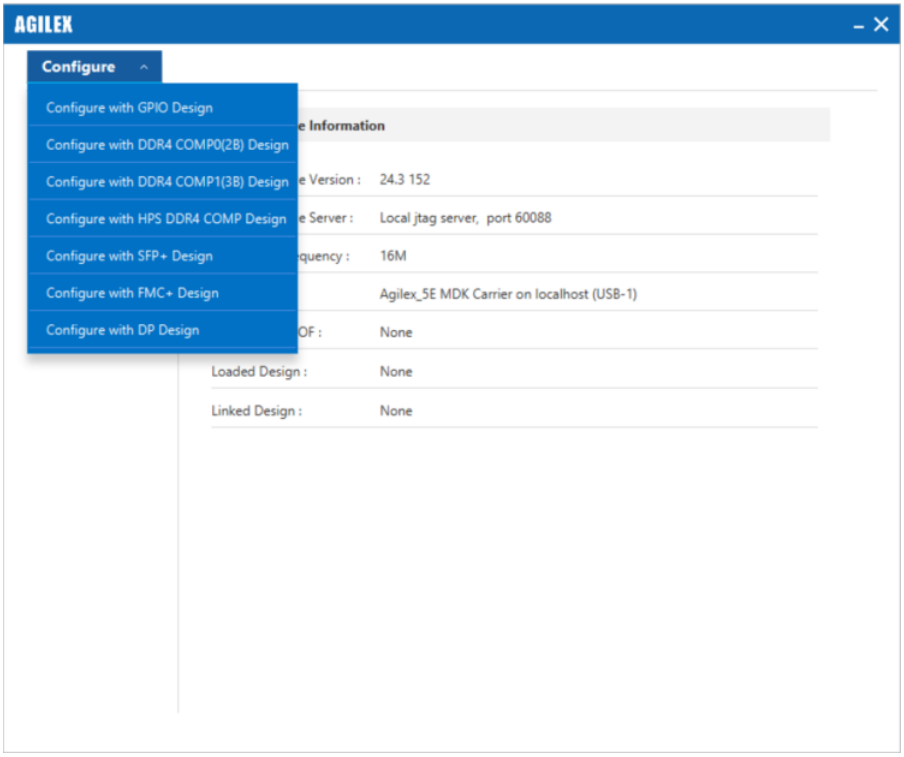
The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

Select the **Agilex** icon on BTS GUI to launch the Agilex 5 FPGA feature.

4.3.4.1. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 24. The Configure Menu



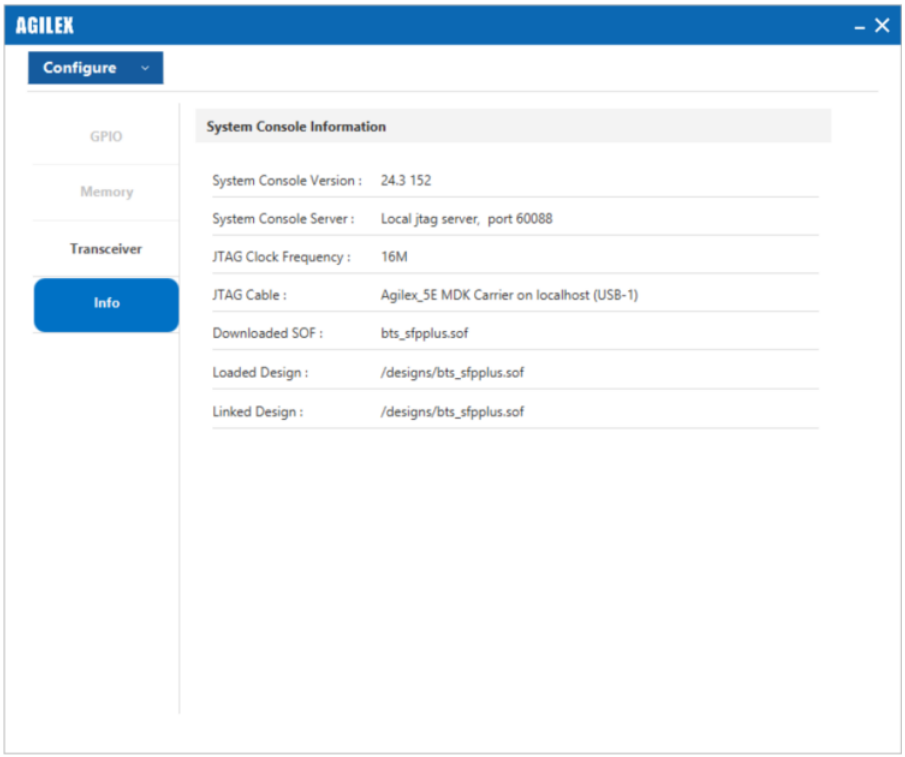
To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (`.sof`) to the FPGA. The download process usually takes less than a minute.

When configuration is completed, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design is now enabled. If you use the Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.3.4.2. The Info Tab

Figure 25. The Info Tab



The **Info** tab shows the information about the System Console.

- **System Console Version**: Displays the current Quartus Prime version installed and active on your system. Change the *QUARTUS_ROOTDIR* environment variable to the required version.
- **System Console Server**: Displays the TCP port number communicate with System Console.
- **JTAG Clock Frequency**: Displays the JTAG working clock frequency.
- **JTAG Cable**: Displays the cable name of the board.
- **Downloaded SOF**: Indicates the design name which have been downloaded to the FPGA device.
- **Loaded Design**: Indicates the design name which have been loaded to System Console.
- **Linked Design**: Indicates the design name which have been linked to System Console.

4.3.4.3. The Transceiver Tab

The Transceiver tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

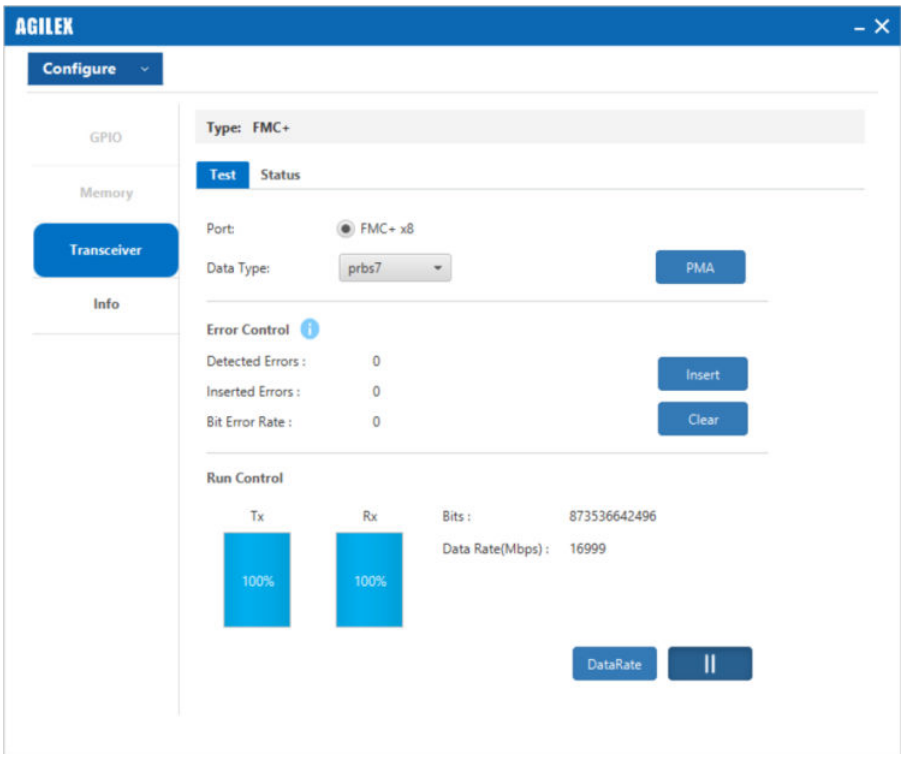
The following port tests are available:

- **FMC+ x8**
- **SFP+**
- **DP x4**

4.3.4.3.1. The FMC+ Tab

The FMC+ Test Tab

Figure 26. The FMC+ Test Tab



Use the following controls to select an interface to apply PMA settings, data type, and error control.

Port

Allows you to specify which interface to test. The following port test is available:

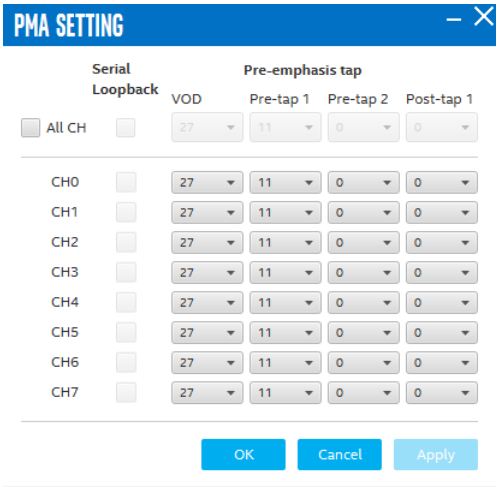
- **FMC+ x8**

PMA Setting

This setting allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**: Displays the signal status between the transmitter and the receiver.
- **VOD**: Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**:
  - **Pre-tap 1**: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - **Pre-tap 2**: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - **Post-tap 1**: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 27. FMC+ Test—PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7**: pseudo-random 7-bit binary sequences
- **PRBS15**: pseudo-random 15-bit binary sequences
- **PRBS23**: pseudo-random 23-bit binary sequences
- **PRBS31**: pseudo-random 31-bit binary sequences

Error Control

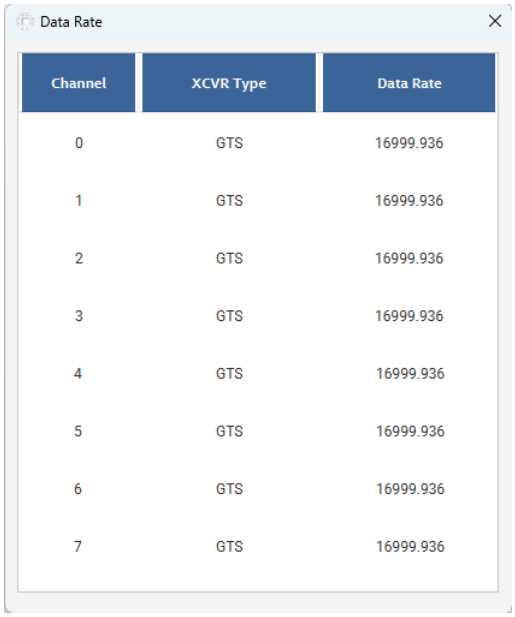
This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the received bit stream.
- **Inserted Errors**: Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transmit data stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
- **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.

Run Control

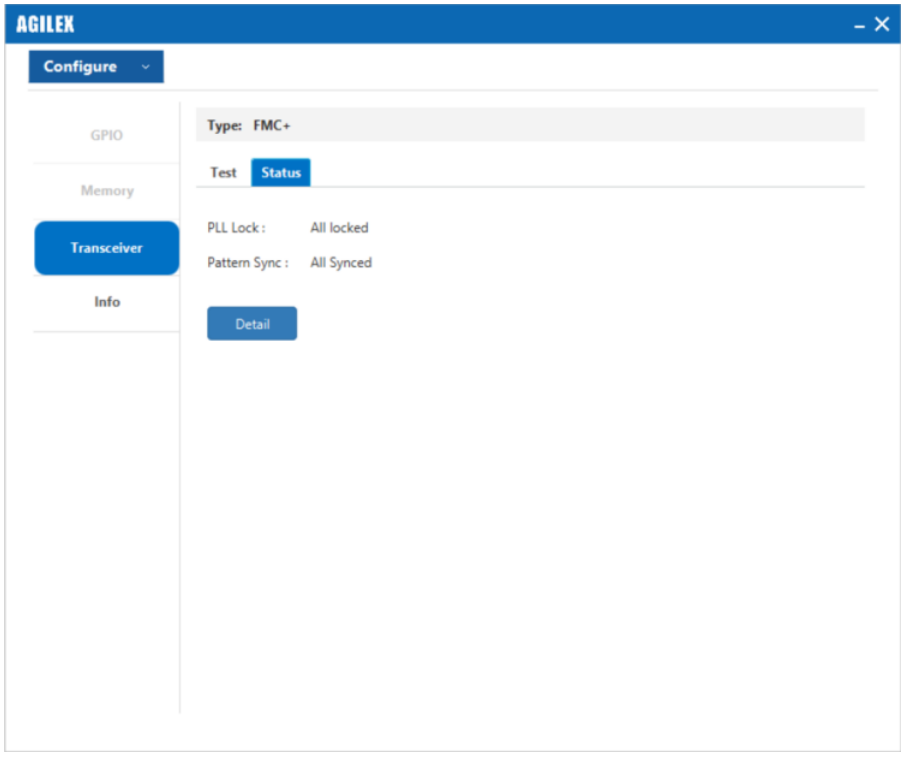
- **TX and RX performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions can achieve.
- **Start**: This control initiates the loopback tests.
- **Data Rate**: Displays the XCVR type and data rate of each channel.

Figure 28. FMC+ Test—Data Rate



The FMC+ Status Tab

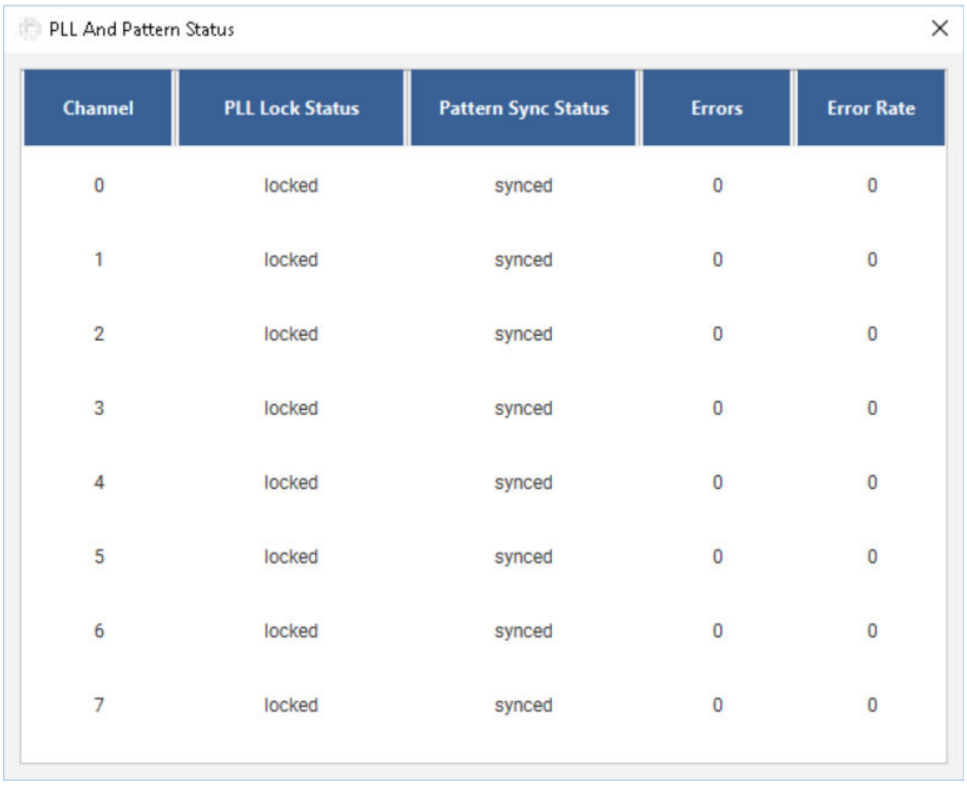
Figure 29. The FMC+ Status Tab



The **Status** tab displays the following status information during the loopback test:

- **PLL Lock**: Shows the PLL locked or unlocked state.
- **Pattern Sync**: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail**: Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

Figure 30. FMC+ Status—PLL and Pattern Status



Channel	PLL Lock Status	Pattern Sync Status	Errors	Error Rate
0	locked	synced	0	0
1	locked	synced	0	0
2	locked	synced	0	0
3	locked	synced	0	0
4	locked	synced	0	0
5	locked	synced	0	0
6	locked	synced	0	0
7	locked	synced	0	0

4.3.4.3.2. The SFP+ Tab

This tab has similar control functions as the **FMC+** tab.

Figure 31. The SFP+ Test Tab

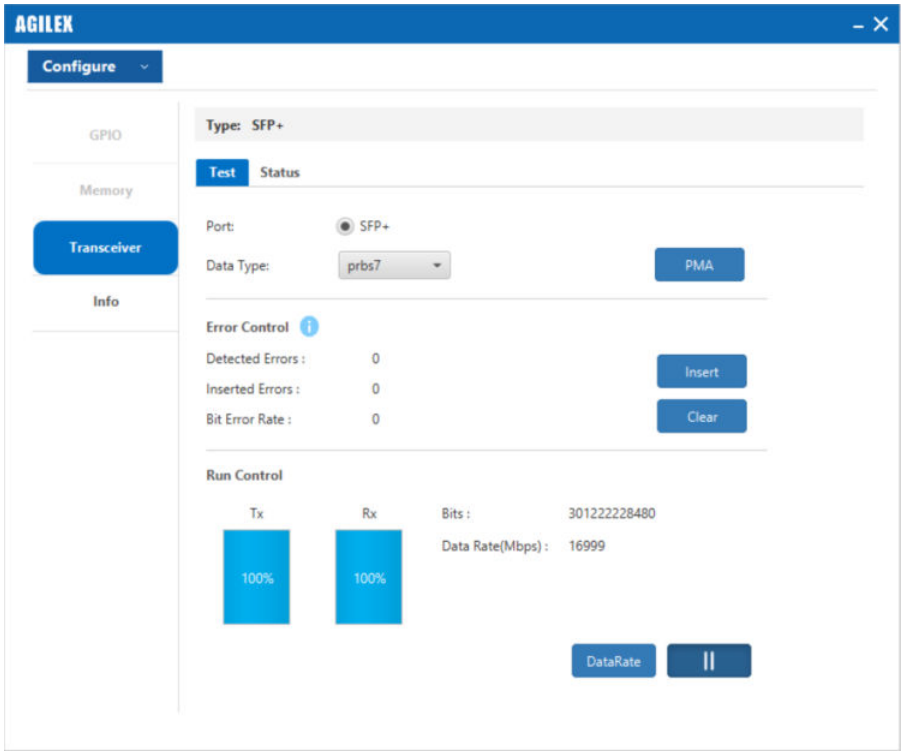
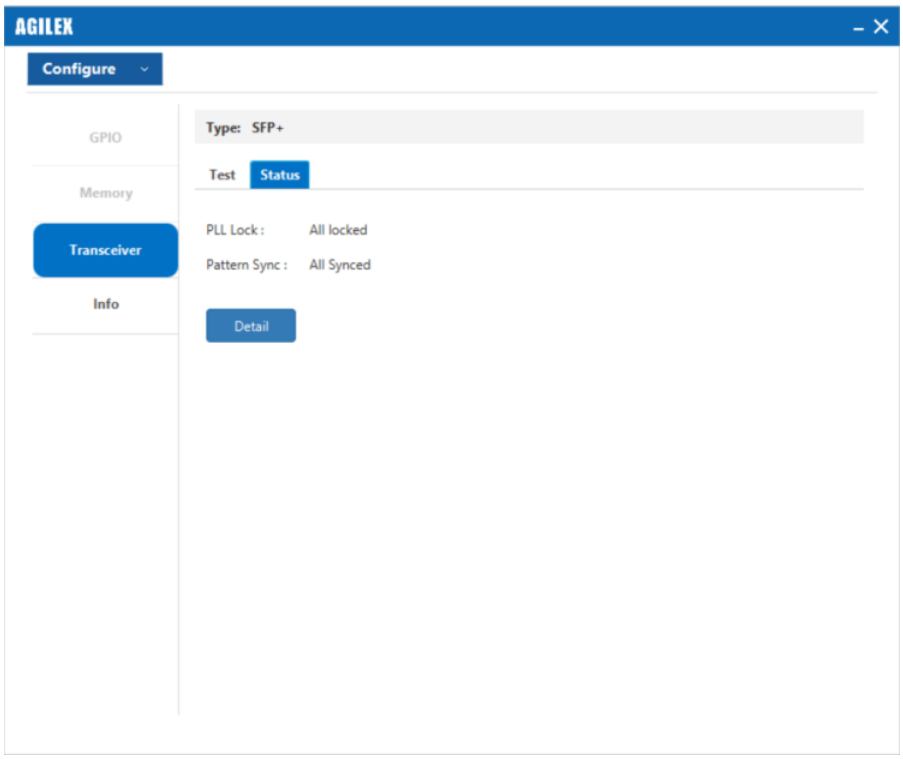


Figure 32. The SFP+ Status Tab



4.3.4.3.3. The DP Tab

This tab has similar control functions as the **FMC+** tab.

Figure 33. The DP Test Tab

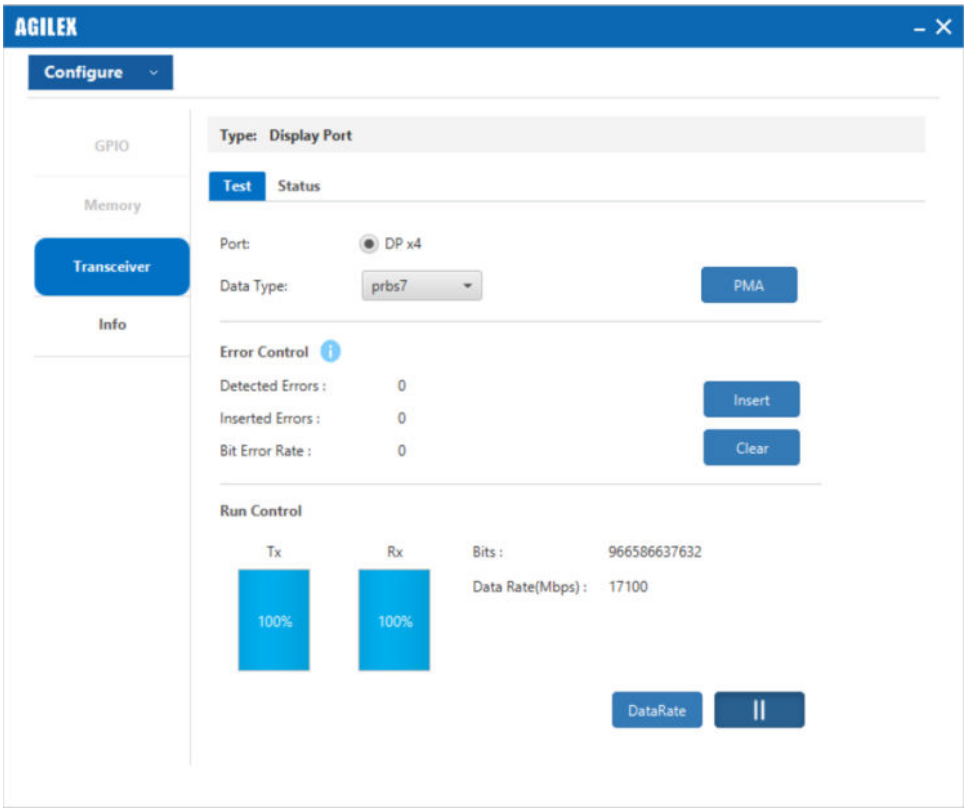
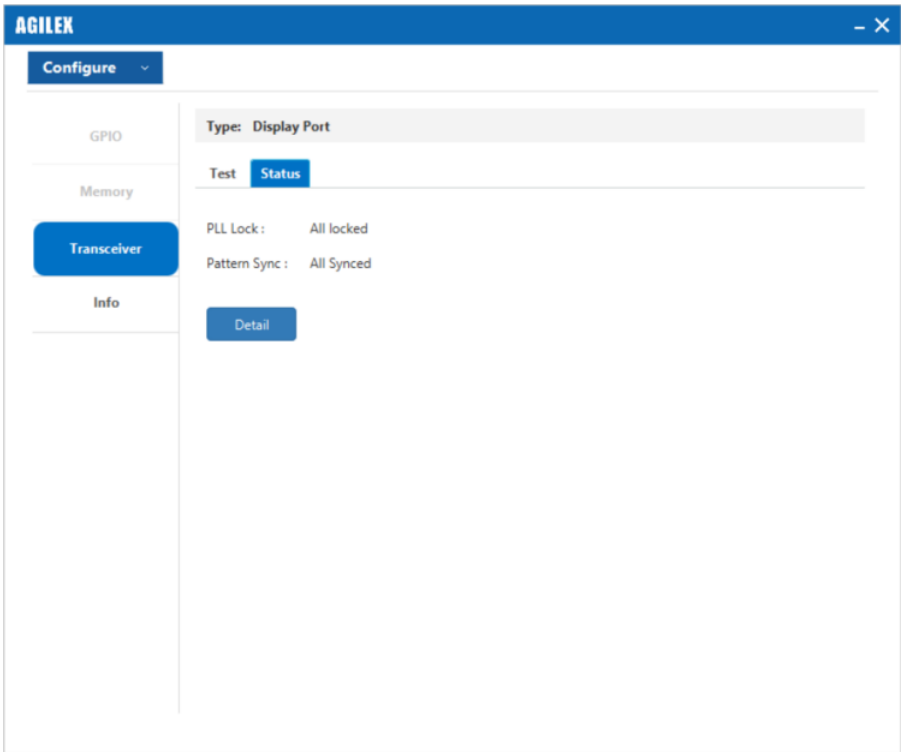


Figure 34. The DP Status Tab



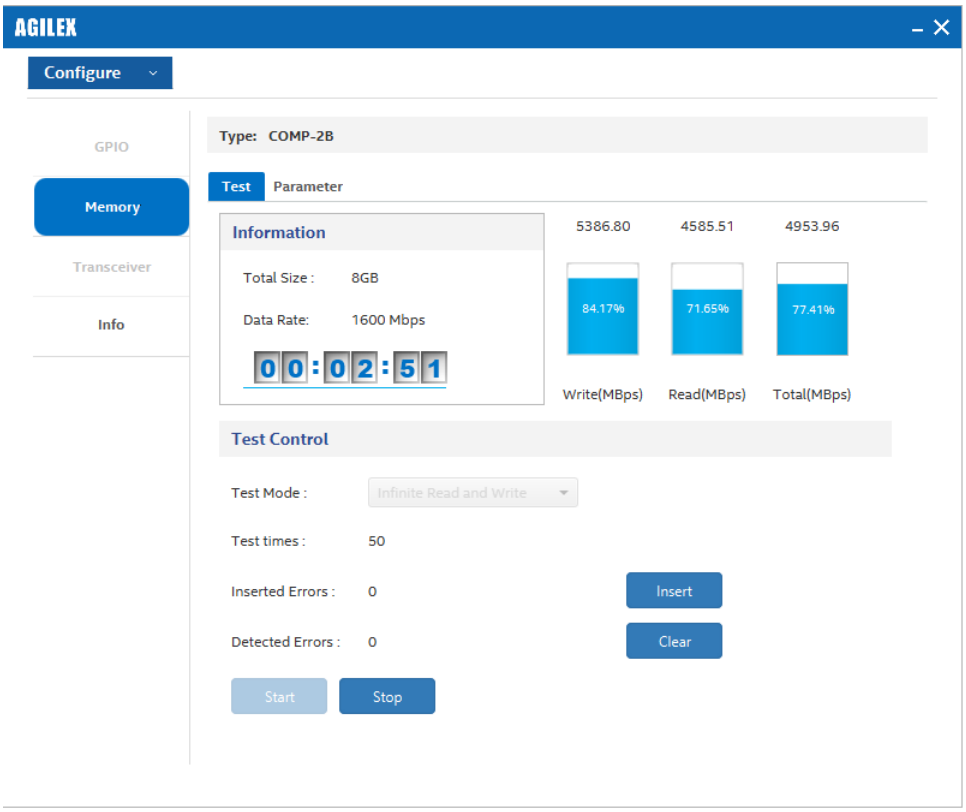
4.3.4.4. The Memory Tab

This tab allows you to read and write DDR4-COMP memory on your board. Download the design through BTS **Configure** menu.

4.3.4.4.1. The COMP0 Tab

The COMP0 Test Tab

Figure 35. The COMP0 Test Tab



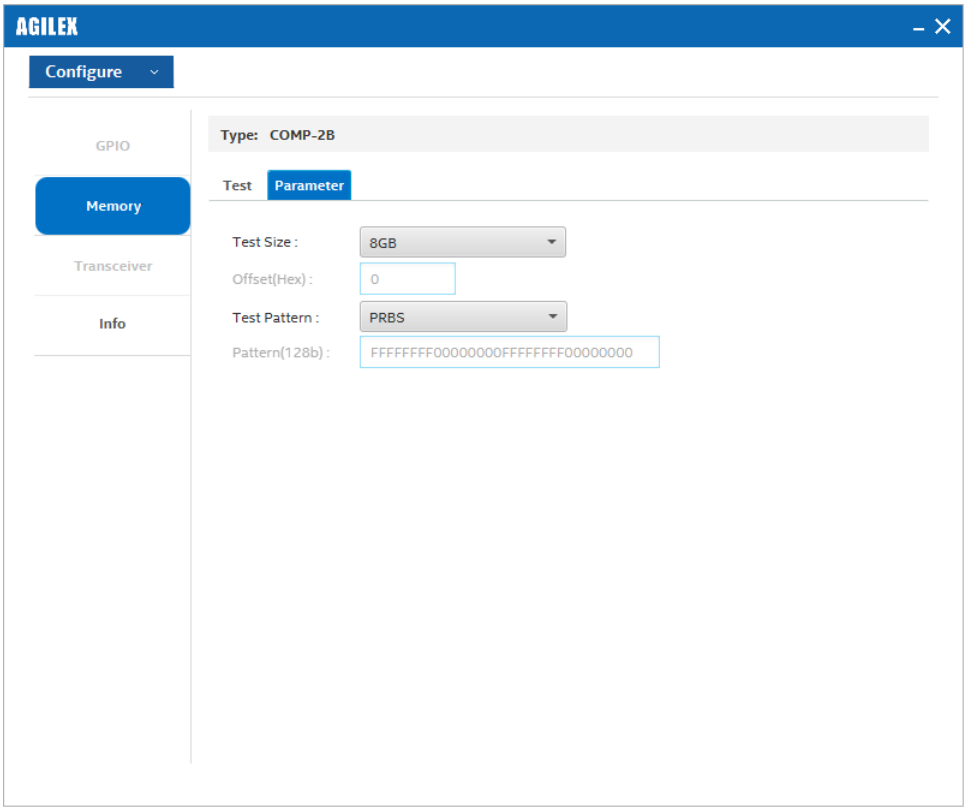
The following sections describe controls on this tab.

- **Start**: Initiates DDR4 memory transaction performance analysis.
- **Stop**: Terminates transaction performance analysis.
- **Test Control**
  - **Test Mode**: Infinite Read and Write (default), Single Read and Write.
  - **Test times**: Number of times that write and read DDR once.
  - **Detected Errors**: Displays the number of data errors detected in the hardware.
  - **Inserted Errors**: Displays the number of errors inserted into the transaction stream.
  - **Insert**: Insert a one-word error into the transaction stream each time you click the button. **Insert** is only enabled during transaction performance analysis.
  - **Clear**: Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.
- **Performance Indicators**:

  These controls display current transaction performance analysis information collected since you last clicked **Start**:
  - **Write**, **Read**, and **Total Performance** bars: Show the percentage (%) of maximum theoretical data rate that the requested transactions are able to achieve.
  - **Write (MBps)**, **Read (MBps)**, **Total (Mbps)**: Show the number of bytes analyzed per second.

The COMP0 Parameter Tab

Figure 36. The COMP0 Parameter Tab



- **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, and 8 GB (default).
- **Offset (Hex)**: You can define the memory start address to test.
- **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

4.3.4.4.2. The COMP1 Tab

The COMP1 tab shares the same settings with the DDR4 COMP0 tab.

Figure 37. The COMP1 Test Tab

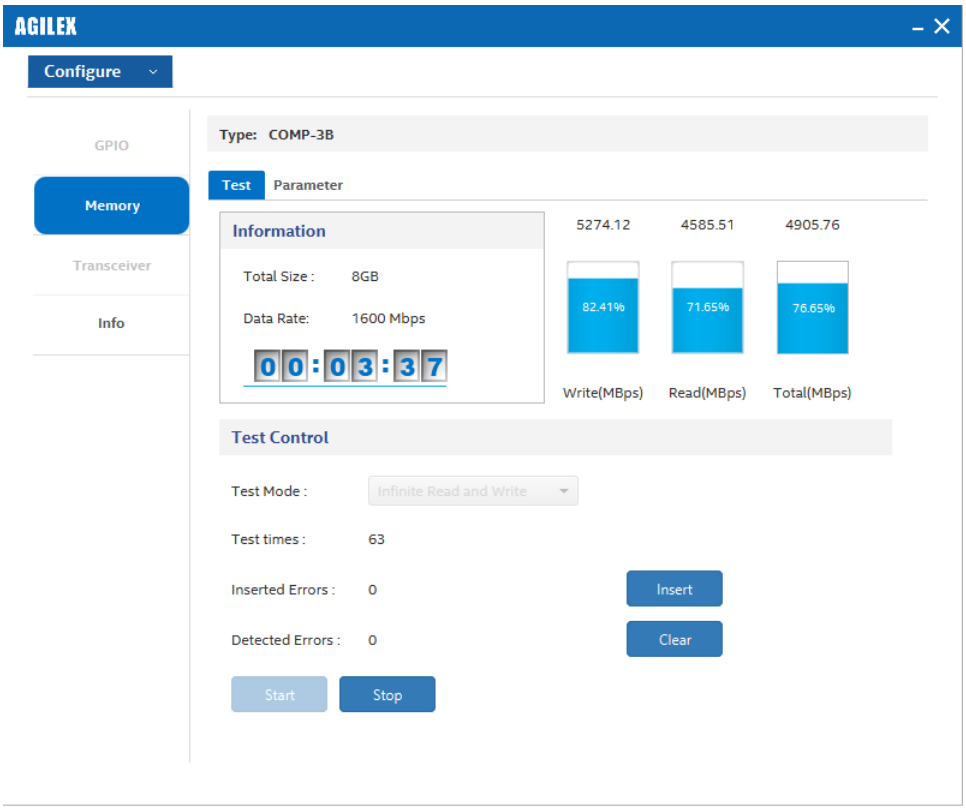
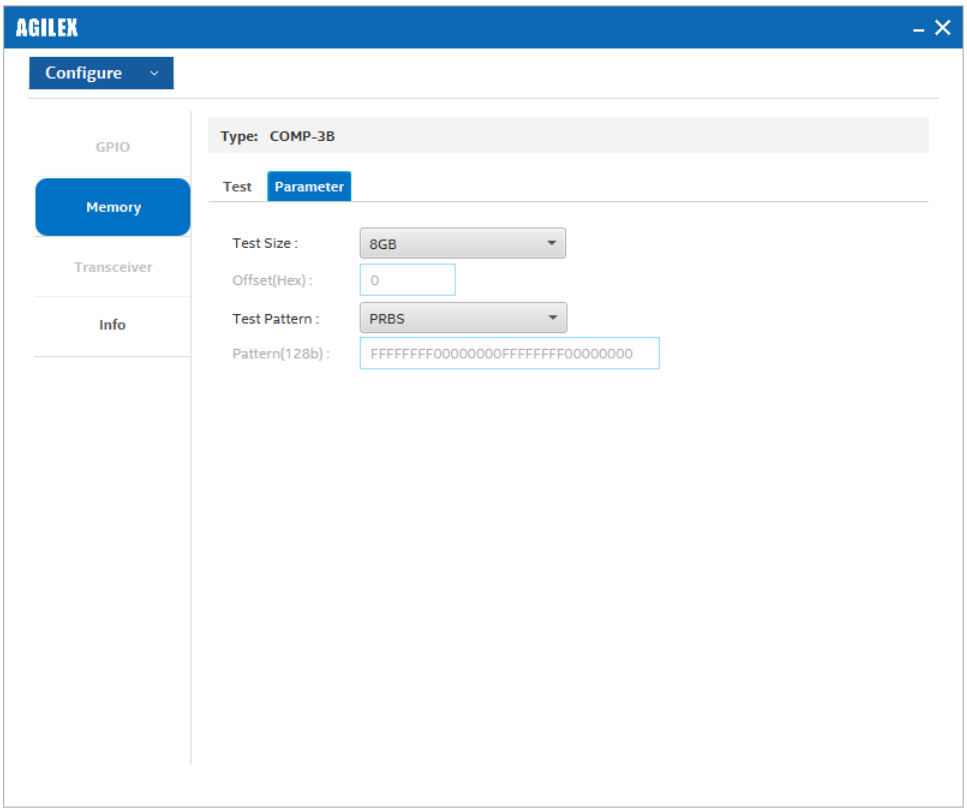


Figure 38. The COMP1 Parameter Tab



4.3.4.4.3. The HPS COMP Tab

The HPS COMP tab shares the same settings with the DDR4 COMP0 tab.

Figure 39. The HPS COMP Test Tab

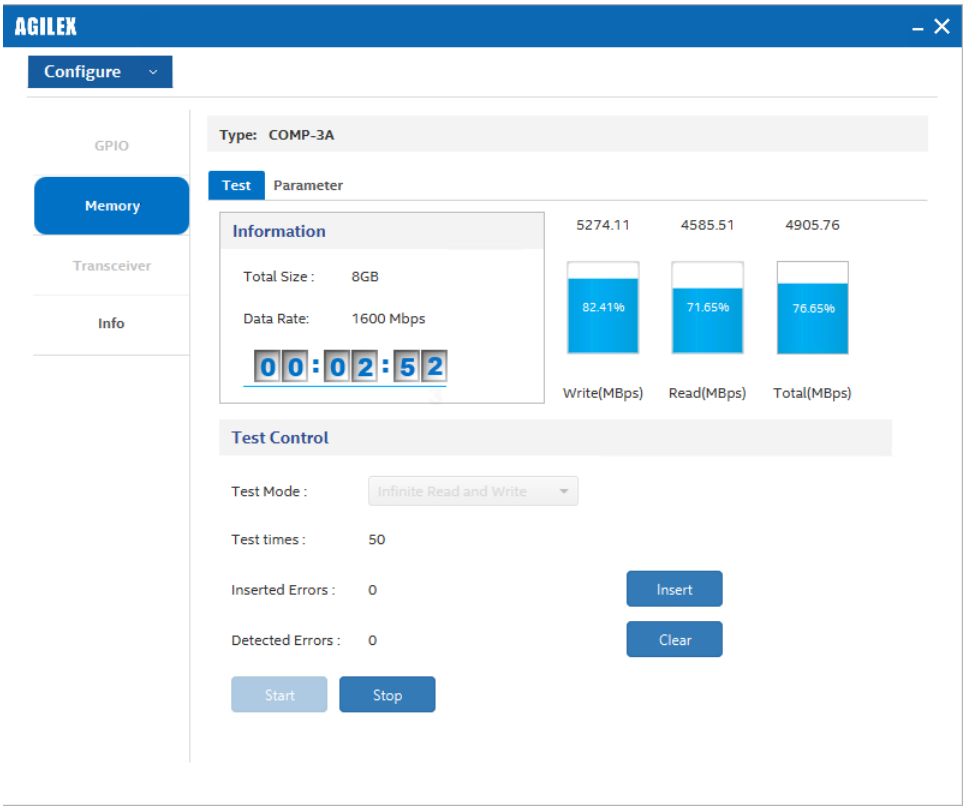
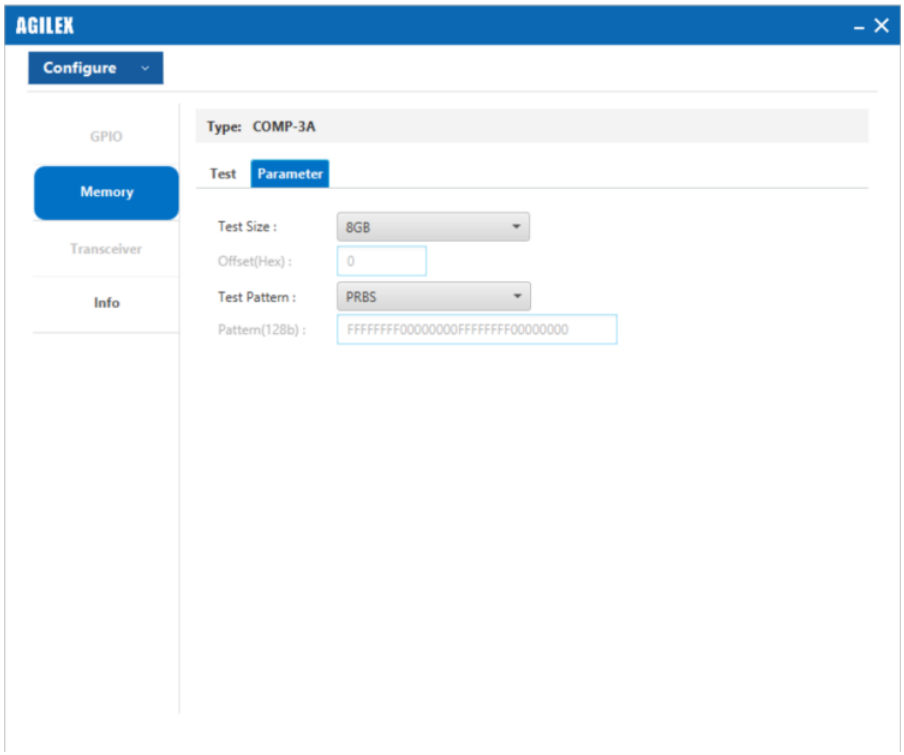


Figure 40. The HPS COMP Parameter Tab

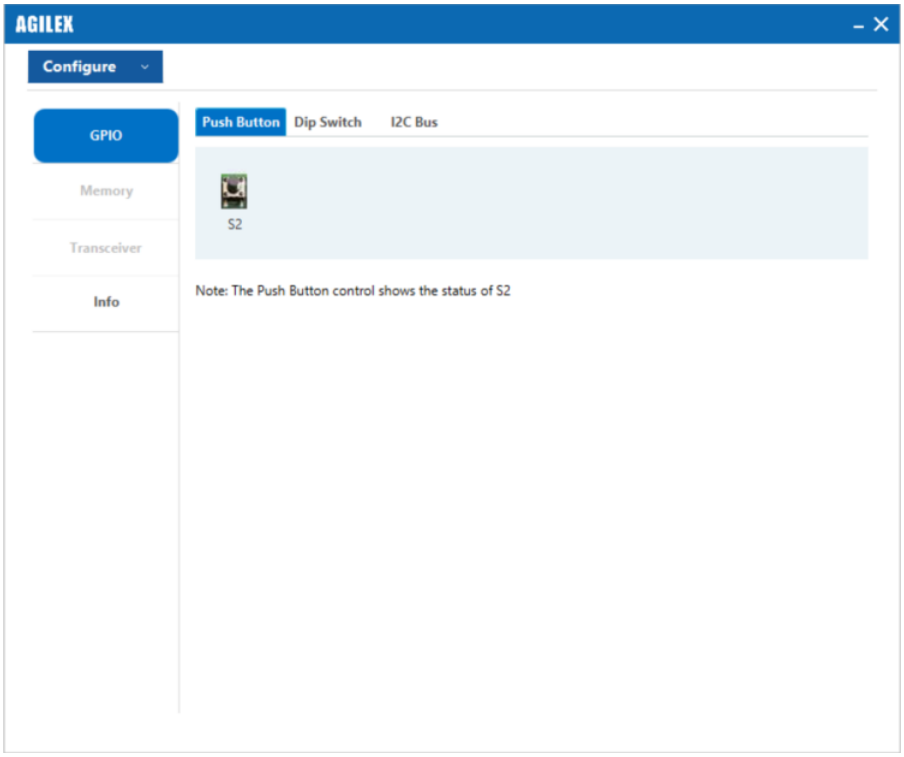


4.3.4.5. The GPIO Tab

The **GPIO** tab allows you to interact with the general-purpose user I/O components on your board. You can see the status of push buttons and DIP switches, and detected I^2C slaves on the I^2C bus. Download the design through the BTS **Configure** menu.

4.3.4.5.1. The Push Button Tab

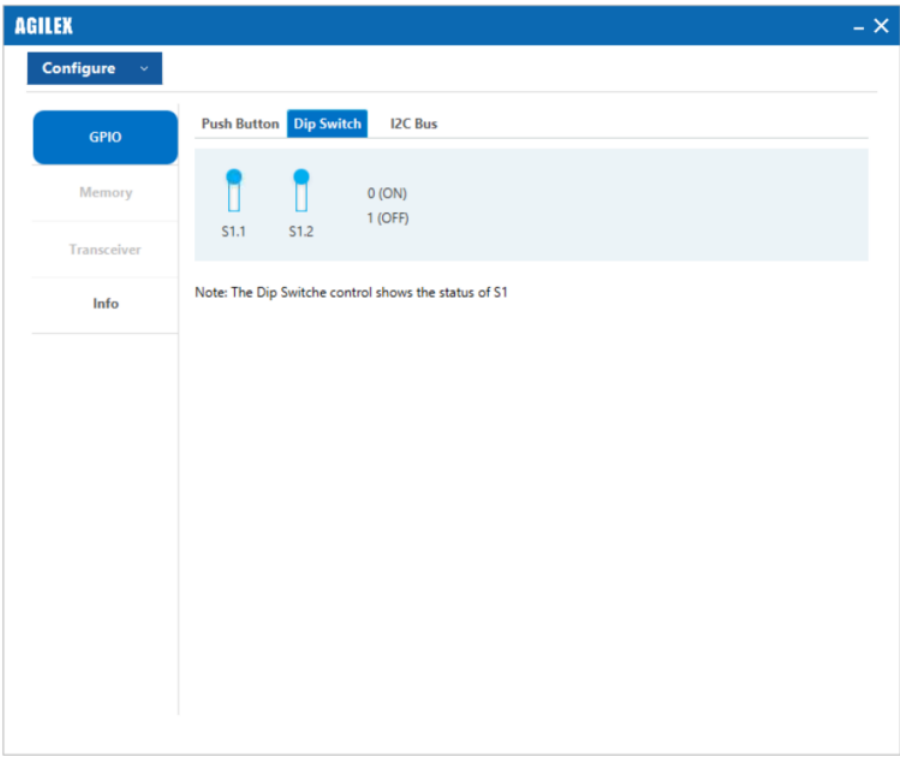
Figure 41. The Push Button Tab



The **Push Button** control shows the status of S2 on the Modular board.

4.3.4.5.2. The Dip Switch Tab

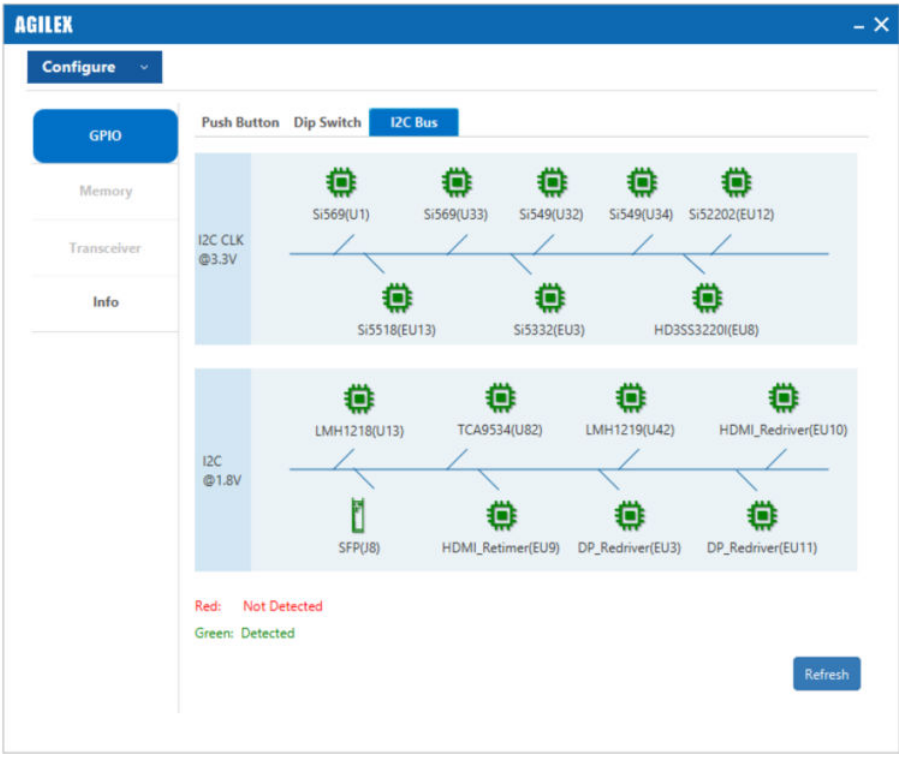
Figure 42. The Dip Switch Tab



The **Dip Switch** control shows the status of S1 on the Modular board.

4.3.4.5.3. The I2C Bus Tab

Figure 43. The I2C Bus Tab



The **I2C Bus** tab shows the detection status of the I^2C slaves on the I^2C bus from the Agilex 5 FPGA.

4.3.5. Other Functionalities

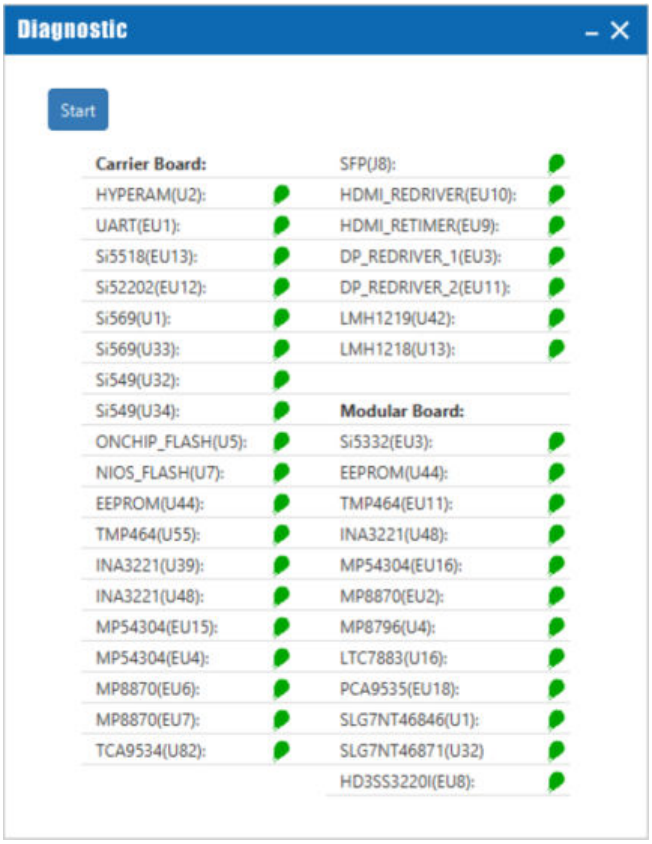
4.3.5.1. The Diagnostic Functionality

The Diagnostic menu provides the functionality of checking the status of the main devices on the Carrier and Modular boards. To trigger a basic board diagnostic, click the **Start** button. After it is completed, the color of the light indicates if the test is a pass or a fail.

Table 6. Diagnostic GUI—Light Indicator

Color	Description
Green	The tested item has passed.
Red	The tested item has failed.

Figure 44. Diagnostic Functionality of BTS



4.3.5.2. The Sys Info

The **Sys Info** menu presents the basic system information of the development kit.

- **Board Name**: The official development kit name.
- **Board Revision**: The board hardware version.
- **MAX Version**: The firmware version that runs on MAX 10 chip.
- **Nios Version**: The Nios software version that runs on MAX 10 chip.

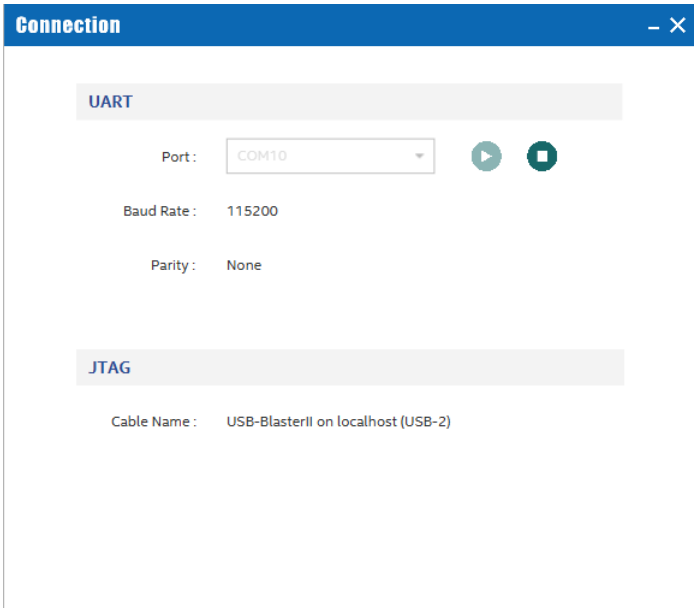
Figure 45. System Information

4.3.5.3. The Connection Information

The **Connection** menu presents the current connection information.

- **UART Port**: The current recognized and activated UART port.
- **UART Baud Rate**: The baud rate of the UART, with a fixed value of 115200, could not be configured.
- **UART Parity**: Describes the evenness or oddness of a number, current design set to none.
- **JTAG Cable**: Displays the current selected JTAG cable name.

Figure 46. The Connection Page



4.3.5.4. The Bottom Info Bar

The bottom information bar shows the status of the UART connection, the recognized Quartus Prime software version.

- **UART**: Shows if the board is connected to BTS successfully.
- **Quartus Prime Version**: Displays the current installed and active Quartus Prime software version on your system. The text turns red if your version is older than the required version. Change the `QUARTUS_ROOTDIR` environment variable to the required version.

5. Development Kit Hardware and Configuration

The Agilex 5 FPGA E-Series 065B Modular Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting or reprogram system images for these cases.

Table 7. Supported Configuration Modes

S4[2:1]	MSEL[2:0]	Configuration Mode
ON/ON	001	AS (Fast mode)
ON/OFF	011	AS (Normal mode)
OFF/OFF	111	JTAG

5.1. Configuring the FPGA and Accessing HPS Debug Access Port by JTAG

1. Set S4 on the Modular board (or use BTS for remote control) to JTAG mode.
2. Plug the micro-USB cable to J35 or Intel FPGA Download Cable II to J10.
3. Open the Quartus Prime Programmer to configure the FPGA.
4. Open the RiscFree IDE to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.
5. Observe that CONF_DONE LED (DS2/Blue on the Modular board) is blinking.

5.2. Configuring the FPGA Device by Active Serial (AS) Modes (Default Mode)

1. Set S4 on the Modular board to AS x4 fast or normal mode. The AS x4 fast mode is the default configuration mode for the board shipped from factory.
2. Power on the board. The FPGA configures itself with programming file stored within the QSPI flash.
3. Observe that CONF_DONE LED (DS2/Blue on the Modular board) is blinking.

6. Custom Projects for the Development Kit

6.1. Golden Top

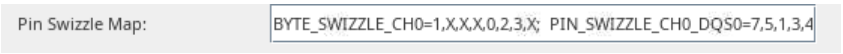
You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, define I/O standard, direction, and general termination.

6.2. EMIF Pin Swizzling Setting

DQ pins within a DQS group or/and DQS group are swapped to simplify board design.

To achieve the swizzling, you must enter swizzling setting in the **Pin Swizzle Map** option in the External Memory Interfaces (EMIF) IP parameter editor.

Figure 47. Entering a PIN_SWIZZLE Specification



1. For DDR4 Bank 2B, use the following settings:

```
BYTE_SWIZZLE_CH0=1,X,X,X,0,2,3,X;
PIN_SWIZZLE_CH0_DQS0=7,5,1,3,4,2,0,6;
PIN_SWIZZLE_CH0_DQS1=9,15,13,11,14,12,8,10;
PIN_SWIZZLE_CH0_DQS2=19,23,21,17,16,18,20,22;
PIN_SWIZZLE_CH0_DQS3=31,29,27,25,26,30,24,28;
```

2. For DDR4 Bank 3A, use the following settings:

```
BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
PIN_SWIZZLE_CH0_DQS0=2,0,6,4,7,5,3,1;
PIN_SWIZZLE_CH0_DQS1=14,11,12,8,10,9,13,15;
PIN_SWIZZLE_CH0_DQS2=16,20,22,18,23,21,19,17;
PIN_SWIZZLE_CH0_DQS3=26,30,28,24,25,27,29,31;
PIN_SWIZZLE_CH0_ECC=4,6,2,0,1,7,5,3;
```

3. For DDR4 Bank 3B, use the following settings:

```
BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
PIN_SWIZZLE_CH0_DQS0=2,0,6,4,7,3,5,1;
PIN_SWIZZLE_CH0_DQS1=12,14,13,10,8,11,15,9;
PIN_SWIZZLE_CH0_DQS2=16,17,18,19,20,21,22,23;
PIN_SWIZZLE_CH0_DQS3=24,25,26,27,28,29,30,31;
PIN_SWIZZLE_CH0_ECC=0,2,6,4,1,3,7,5;
```

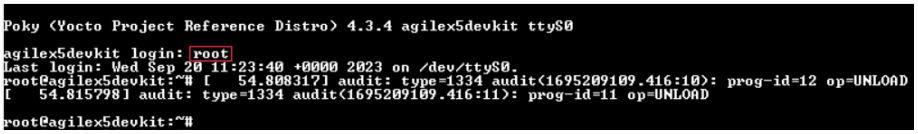
Related Information

External Memory Interfaces (EMIF) IP User Guide: Agilex 5 FPGAs and SoCs

7. HPS Boot

This section presents how to boot HPS from SD card.

1. Power down the board.
2. Set MSEL DIP switch (S4 on the Modular board) to AS x4 mode.
3. Insert the programmed SD card into the socket of uSD (J4 on the Modular board).
4. Connect micro-USB cable (J2 on the Modular board) to the host PC.
5. Launch UART terminal application on host PC, and follow the setting list:
   - Speed: 115200
   - Data: 8 bit
   - Parity: none
   - Stop bits: 1 bit
   - Flow control: none
6. Power up the board.
7. After Linux boots, log in using *root* as username, no password is required.



8. Document Revision History for the Agilex 5 FPGA E-Series 065B Modular Development Kit User Guide

Document Version	Changes
2025.03.07	• Update the *Overview* chapter: — Updated Figure: *Agilex 5 FPGA E-Series 065B Modular Development Kit Block Diagram*. • Updated the *Getting Started* chapter: — Added new topics: • *Before You Begin* • *Handling the Board* • *Handling the DIP Switches* • *Installing the Quartus Prime Pro Edition Software* • *Installing the Intel SoC EDS* • *Installing the Development Kit* • *Installing the Intel FPGA Download Cable II Driver* — Retitled topic *Quartus Software and Driver Installation* to *Software and Driver Installation* • Updated the *Development Kit Setup* chapter: — Updated Table: *Factory Default Switch Settings (Carrier Board)* to change the default position of the SW.2 switch from POS-1 to POS-3. — Updated the *Powering Up the Development Kit* topic for clarity. — Updated step 2 in the *Restoring SD Card with the Default Factory Image* topic for clarity.

continued...

Document Version	Changes
	• Updated the *Board Test System* chapter: — Updated and retitled topic *Installing Quartus Prime Software* to *Setting Up the Quartus Prime Software for BTS Operation*. — Updated the steps in the *Running the BTS GUI* topic. — Updated Figure: *BTS Package Folder*. — Added Figure: *UART Port Configuration* to the *Troubleshooting for Launching BTS* topic. — Updated the *Power Monitor* topic. — Added information about the CLOCK MUX option in *The IO Control Tab* topic. — Updated Figure: *The Configure Menu*. — Retitled topic and figure *The Main Info Tab* to *The Info Tab*. — Updated the *The Info Tab* topic. — Added **DP x4** to the list of port tests in the *The Transceiver Tab* topic. — Updated Figure: *The FMC+ Test Tab*. — Updated Figure: *The FMC+ Status Tab*. — Updated Figure: *The SFP+ Test Tab*. — Updated Figure: *The SFP+ Status Tab*. — Updated the *The COMP0 Tab* topic: • Updated Figure: *The COMP0 Test Tab*. • Updated information about the COMP0 **Test** tab. • Added Figure: *The COMP0 Parameter Tab*. • Added information about the COMP0 **Parameter** tab. • Removed information about the COMP0 **Traffic Generator** tab. • Removed Figure: *The COMP0 Control Tab—Traffic Generator*. — Updated *The COMP1 Tab* topic: • Updated Figure: *The COMP1 Test Tab*. • Added Figure: *The COMP1 Parameter Tab*. • Removed Figure: *The COMP1 Control Tab—Traffic Generator*. — Updated *The HPS COMP Tab* topic: • Updated Figure: *The HPS COMP Test Tab*. • Added Figure: *The HPS COMP Parameter Tab*. • Removed Figure: *The COMP1 Control Tab—Traffic Generator*. — Added new topics: • *The DP Tab* • *The GPIO Tab* • *The Push Button Tab* • *The Dip Switch Tab* • *The I2C Tab* — Updated Figure: *Diagnostic Functionality of BTS*. • Updated the *Custom Projects for the Development Kit* chapter: — Updated the description in *EMIF Pin Swizzling Setting*. — Updated Figure: *Entering a PIN_SWIZZLE Specification*. • Updated the *Development Kit Components* appendix chapter: — Updated Table: *MAX 10 BMC* in *General Input/Output*. — Updated Figure: *Clock Tree* in *Clocks*. — Updated Figure: *I^2C Serial Bus* in *Communication Interfaces*. • Added new Appendix chapter—*Developer Resources*. • Restructured the document for clarity. • Made editorial edits throughout the document.
2024.07.12	Initial release.

A. Development Kit Components

A.1. Board Overview

This section describes all the components on the development board. A complete set of schematics, a physical layout database, and Gerber files for the development board reside in the development kit documents directory.

Figure 48. Components in Agilex 5 FPGA E-Series 065B Modular Development Kit—Modular and Carrier Boards (Top View)

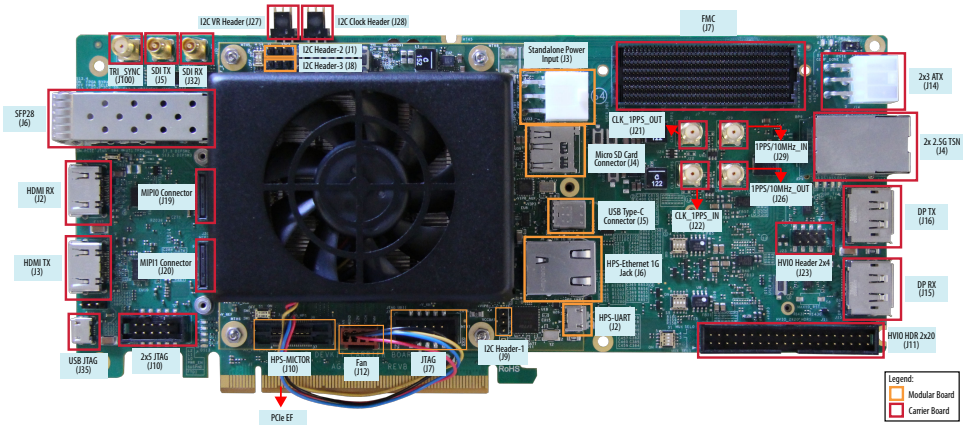


Figure 49. Carrier Board (Top View)

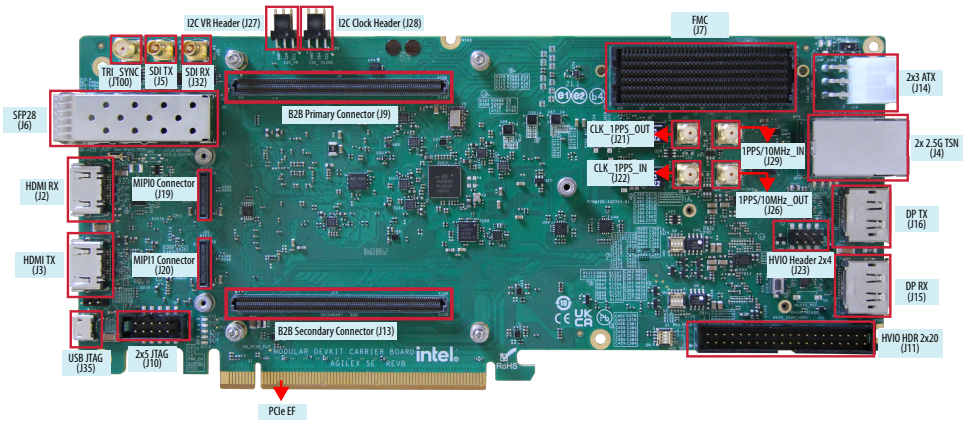
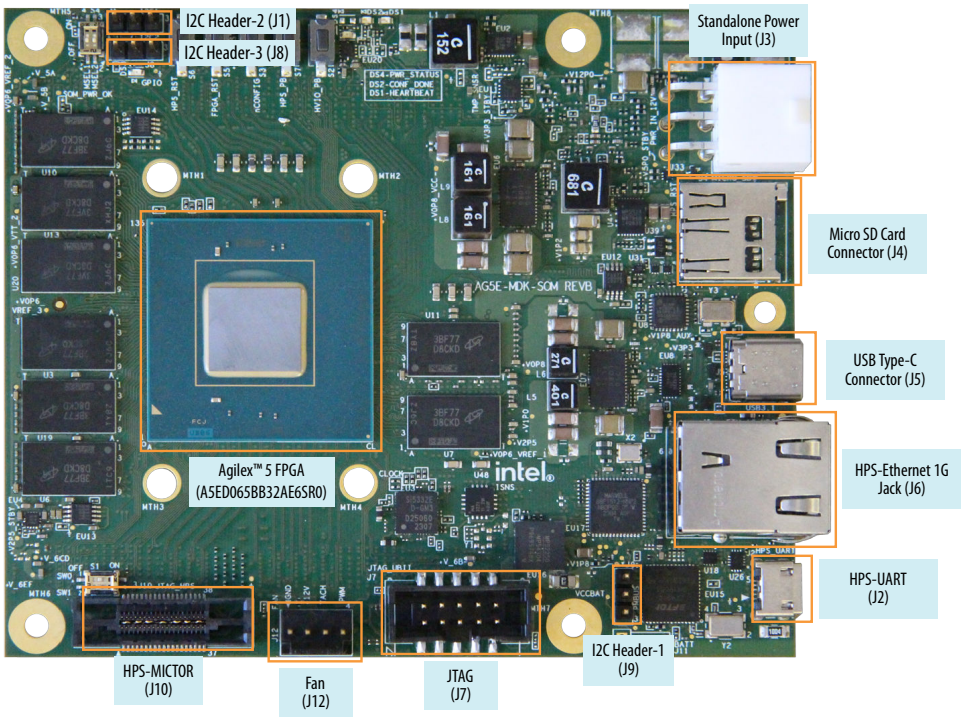


Figure 50. Modular Board (Top View)



A.1.1. Board Components

Table 8. Board Connector/Switch Description (Modular Board)

Connector/Switch	Functionality
J3	Standalone power input
J4	Micro SD card connector
J5	USB Type-C connector
J6	HPS-Ethernet 1G jack
J2	HPS- UART
J9	I²C Header-1
J1	I²C Header-2
J8	I²C Header-3
J7	JTAG
J12	Fan
J10	HPS-Mictor
S4	MSEL switch
S1	GPIO switch
S2	User push button terminated to BW19

continued...

Connector/Switch	Functionality
S3	Reconfigures the FPGA
S5	Triggers A5E_FPGA_RESET_N_3V3 (BU28)
S6	• Press for less than 3 seconds: FPGA WARM reset triggered (BP31) • Press for more than 3 seconds: A5E_HPS_COLD_NRESET is triggered (CH109/SDMIO10)
S7	HPS PB at IOB_5 (B134)

Table 9. Board Connector/Switch Description (Carrier Board)

Connector/Switch	Functionality
J7	FMC connector
J14	2x3 ATX connector
J4	Dual stacked RJ45
J16	Display Port TX
J15	Display Port RX
J11	HVIO header (2x20)
J23	HVIO header (2x4)
J10	JTAG header (2x5)
J35	Micro USB header
J2	HDMI RX
J3	HDMI TX
J6	SFP28 connector
J19	MIPI0 connector
J20	MIPI1 connector
J9	B2B primary connector
J13	B2B secondary connector
J100	Trisync connector
J5	SDI TX connector
J32	SDI RX connector
J27	I^2C VR header
J28	I^2C clock header
J33	I^2C peripherals header
S1	PPS clock selection switch
S2	TSN PHY 1 configuration control switch
S5	TSN PHY 0 configuration control switch
S6	MIPI0 control signals control switch
S11	MIPI1 control signals control switch

continued...

Connector/Switch	Functionality
SW2	12 V Input source selection switch
SW4	JTAG input source selection switch
S7	User DIP switch [0:2], FMC JTAG bypass control switch
S13.1	PCIe reference clock selection switch
S13.2	User DIP switch
S13.3	JTAG source selection switch
S13.4	FPGA JTAG bypass control switch

A.2. System Management

The development kit utilizes MAX 10 FPGA (10M16DAF256I6G) for power management, system management, and onboard JTAG controller.

- **Power management**:
  - Controls systems and FPGA power up and optional down sequence
  - Supervises power regulators/switches status and manages power faults
  - Supervises temperature sensor interrupt signals and manages temperature faults
  - Supervises current sensor interrupt signals and manages over-current faults
- **JTAG controller**: Manages JTAG chain topology, JTAG master source, and JTAG slaves through switch settings at S13.

A.3. Power

Figure 51. Power Tree

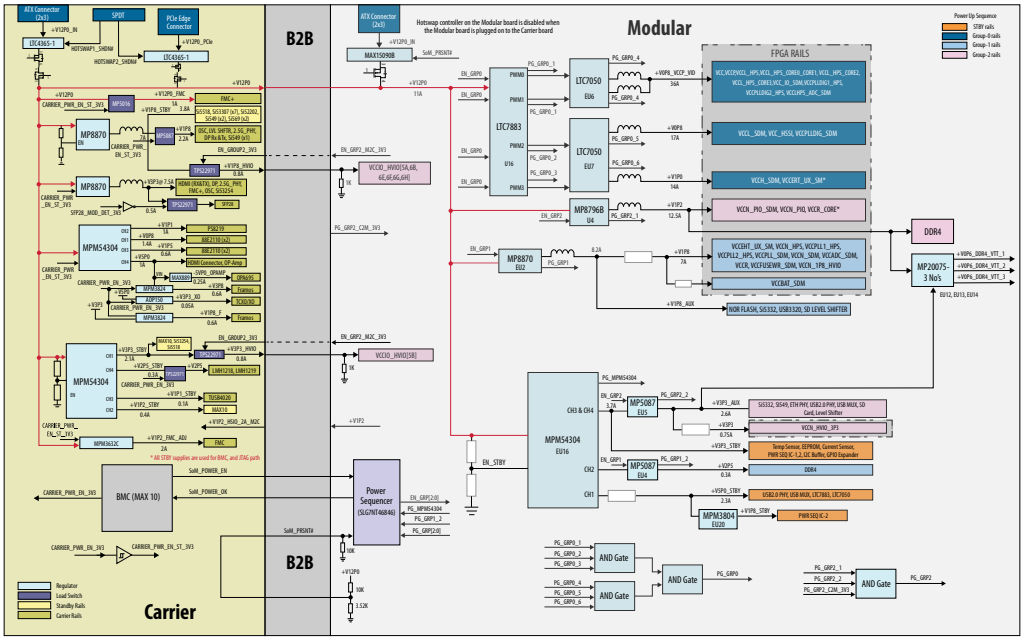


Figure 52. Power Sequence—Agilex 5 E-Series Modular Board

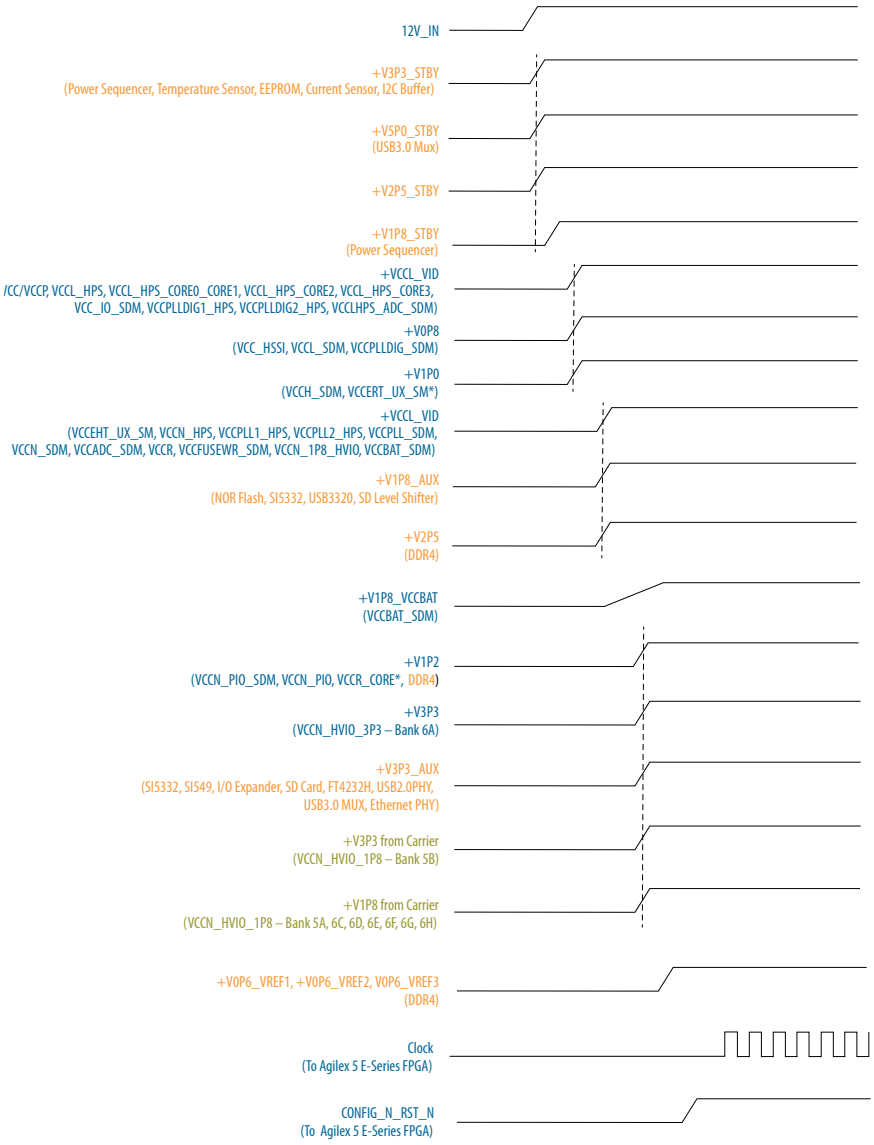
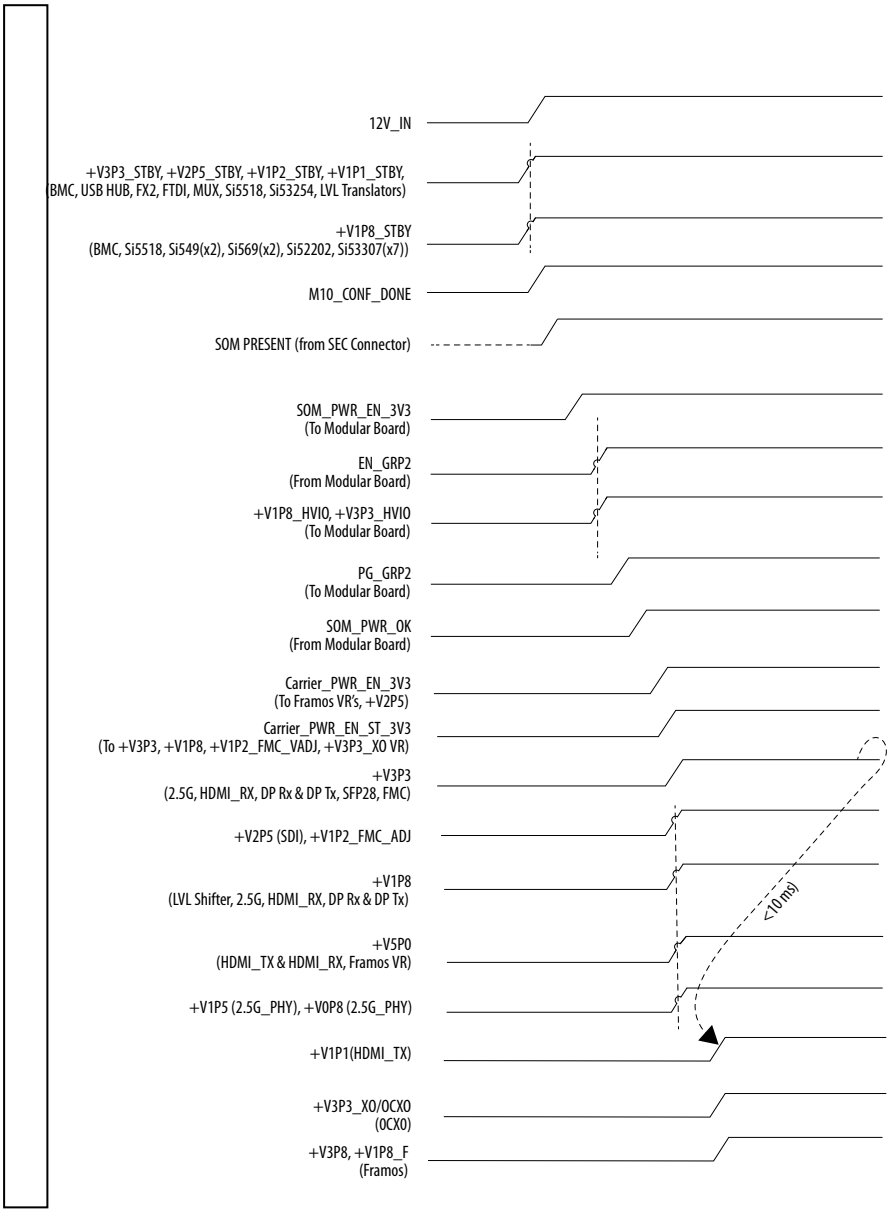


Figure 53. Power Sequence—Agilex 5 E-Series Carrier Board



The overall system power sequence is handled by MAX 10.

On the Modular board, the power sequencing is handled by SLG7NT46846 (U1). The MAX 10 on the Carrier board handles the Power enable of Modular board (SOM_PWR_EN_C2M_3V3) and waits for SOM_PWR_OK_M2C_3V3 to go high, which indicates that the Modular board has powered on successfully.

A.4. Clocks

Table 10. Default Clock Frequency (Modular Board)

Schematic Signal Name	Default Frequency (MHz)	Clock I/O Standard
CLK_A5E_UX_1C_G_100M_DP/DN	100	LVDS Fast 1.8 V
CLK_SDM_REFCLK_125M	125	LVCMOS 1.8 V
CLK_IO96B_3A_DDR4_150M_DP/DN	150	LVDS Fast 1.8 V
CLK_IO96B_2B_DDR4_150M_DP/DN	150	LVDS Fast 1.8 V
CLK_IO96B_3B_DDR4_150M_DP/DN	150	LVDS Fast 1.8 V
CLK_A5E_HVIO_6A_100M	100	LVCMOS 3.3 V
CLK_A5E_HPS_25M_1V8	25	LVCMOS 1.8 V

Table 11. Carrier Board Clocks

Schematic Signal Name	Default Frequency	Clock I/O Standard
CLK_SI5518_OUT0_DP	1 Hz	LVCMOS 1.8 V
CLK_SI5518_OUT1_1PPS	1 Hz	LVCMOS 1.8 V
CLK_1PPS_OUT_SMA	1 Hz	LVCMOS 1.8 V
CLK_TOD_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
SI5518_OUT3_DP/DN_MUX_IN	—	—
CLK_10M_OUT_SMA	10 MHz	LVCMOS 1.8V
CLK_SI5518_OUT5_FMC_A_DP/DN	—	—
CLK_SI5518_OUT6_122.88M_DP/DN	122.88 MHz	LVDS 1.8 V
CLK_SI5518_OUT7_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT8_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT9_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT10_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT11_156.25M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT12_125M_DP/DN	125 MHz	LVDS 1.8 V
FMC_CLK2_C2M_DP/DN	156.25 MHz	LVDS 1.8 V
CLK_SI5518_OUT14_100M_DP/DN	100 MHz	LVDS 1.8 V
CLK_SI5518_OUT15_100M_DP/DN	100 MHz	LVDS 1.8 V
CLK_SI5518_OUT16_100M_DP/DN	100 MHz	LVDS 1.8 V
CLK_SI5518_OUT17_150M_DP/DN	150 MHz	LVDS 1.8 V

The clocks in the following table are fed to the Modular board transceiver banks from the Carrier board.

Table 12. Input Clock Sources, Clock Selection Control for Various Modular Board Banks

Pin Name	I/O Bank	Pin Name (Agilex 5 E-Series FPGA)	Signal Connected	Carrier Clock Net	Clock Source 1	Clock Source 2	Clock Selection Control	Default Frequency (MHz)
BB120	1A	REFCLK_GTSL1A_CH1p	CLK_A5E_UX_1A_R_DP	CLK_FMC_GBTCLK1_C_DP	FMC Add-in card	—	—	—
BB115	1A	REFCLK_GTSL1A_CH1n	CLK_A5E_UX_1A_R_DN	CLK_FMC_GBTCLK1_C_DN	FMC Add-in card	—	—	—
BC111	1A	REFCLK_GTSL1A_RX_P	CLK_A5E_UX_1A_G_DP	CLK_MUX_SI5518_OUT5_SI569_DP	CLK(EU13)/OUT5	VCXO CLK (U33)	clk_mux_1_sel (EU8)	148.35
BC107	1A	REFCLK_GTSL1A_RX_N	CLK_A5E_UX_1A_G_DN	CLK_MUX_SI5518_OUT5_SI569_DN	CLK(EU13)/OUT5	VCXO CLK (U33)	clk_mux_1_sel (EU8)	148.35
AV120	1B	REFCLK_GTSL1B_CH1p	CLK_A5E_UX_1B_R_DP	CLK_MUX_SI549_FMC_GBTCLK0_DP	VCXO CLK(U34)	FMC Add-in card	clk_mux_6_sel (EU21)	150
AV115	1B	REFCLK_GTSL1B_CH1n	CLK_A5E_UX_1B_R_DN	CLK_MUX_SI549_FMC_GBTCLK0_DN	VCXO CLK(U34)	FMC Add-in card	clk_mux_6_sel (EU21)	150
AY120	1B	REFCLK_GTSL1B_RX_P	CLK_A5E_UX_1B_G_DP	CLK_MUX_SI5518_OUT6_OUT10_156.25M_DP	CLK(EU13)/OUT6	CLK(EU13)/OUT10	clk_mux_3_sel (EU17)	156.25
AY115	1B	REFCLK_GTSL1B_RX_N	CLK_A5E_UX_1B_G_DN	CLK_MUX_SI5518_OUT6_OUT10_156.25M_DN	CLK(EU13)/OUT6	CLK(EU13)/OUT10	clk_mux_3_sel (EU17)	156.25
BB16	4A	REFCLK_GTSR4A_CH1p	CLK_A5E_UX_4A_R_DP	CLK_SI549_DISP_PORT_150M_DP	VCXO CLK(U32)	—	—	150
BB21	4A	REFCLK_GTSR4A_CH1n	CLK_A5E_UX_4A_R_DN	CLK_SI549_DISP_PORT_150M_DN	VCXO CLK(U32)	—	—	150
BC29	4A	REFCLK_GTSR4A_RX_P	CLK_A5E_UX_4A_G_DP	CLK_SI5518_OUT17_150M_DP	CLK(EU13)/OUT17	—	—	150
BC25	4A	REFCLK_GTSR4A_RX_N	CLK_A5E_UX_4A_G_DN	CLK_SI5518_OUT17_150M_DN	CLK(EU13)/OUT17	—	—	150
AV16	4B	REFCLK_GTSR4B_CH1p	CLK_A5E_UX_4B_R_DP	CLK_HDMI_RX_DP	HDMI RETIMER(EU9)	—	—	—

continued...

Pin Name	I/O Bank	Pin Name (Agilex 5 E-Series FPGA)	Signal Connected	Carrier Clock Net	Clock Source 1	Clock Source 2	Clock Selection Control	Default Frequency (MHz)
AV21	4B	REFCLK_GTSR4B_CH1n	CLK_A5E_UX_4B_R_DN	CLK_HDMI_RX_DN	HDMI RETIMER(EU9)	—	—	—
AY16	4B	REFCLK_GTSR4B_RX_P	CLK_A5E_UX_4B_G_DP	CLK_MUX_SI5518_OUT16_SI569_100M_DP	CLK(EU13)/OUT16	VCXO CLK (U1)	clk_mux_5_sel (EU5)	100
AY21	4B	REFCLK_GTSR4B_RX_N	CLK_A5E_UX_4B_G_DN	CLK_MUX_SI5518_OUT16_SI569_100M_DN	CLK(EU13)/OUT16	VCXO CLK (U1)	clk_mux_5_sel (EU5)	100
AP16	4C	REFCLK_GTSR4C_CH1p	CLK_A5E_UX_4C_R_DP	CLK_SI5518_OUT15_100M_DP	CLK(EU13)/OUT15	—	—	100
AP21	4C	REFCLK_GTSR4C_CH1n	CLK_A5E_UX_4C_R_DN	CLK_SI5518_OUT15_100M_DN	CLK(EU13)/OUT15	—	—	100
AT16	4C	REFCLK_GTSR4C_RX_P	CLK_A5E_UX_4C_G_DP	CLK_SI53254_OUT0_100M_DP	CLK(EU26)/OUT0	—	—	100
AT21	4C	REFCLK_GTSR4C_RX_N	CLK_A5E_UX_4C_G_DN	CLK_SI53254_OUT0_100M_DN	CLK(EU26)/OUT0	—	—	100

When there are input clocks from multiple sources, the clock selection is performed through multiplexers. The following table shows the details of the multiplexers, clock sources, and default clock selected.

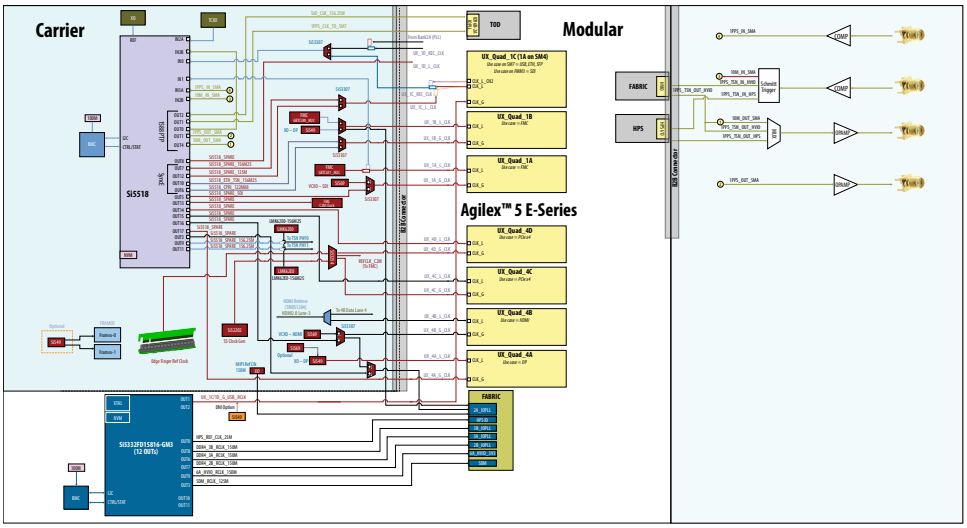
Table 13. Clock Mux Selection

Control Signal	Low CLOCK0)	High CLOCK1)	Output 0	Output 1	Mux Select Default
clk_mux_1_sel	CLK_SI5518_OUT5_FMC_A_DP/N	CLK_SI569_FMC_A_DP/N	CLK_MUX_SI5518_OUT5_SI569_DP/N	—	High
clk_mux_2_sel	CLK_SI5518_OUT7_156.25M_DP/N	CLK_SI5518_OUT12_125M_DP/N	CLK_MUX_SI5518_OUT9_OUT12_125M_DP/N	—	High
clk_mux_3_sel	CLK_SI5518_OUT6_122.88M_DP/N	CLK_SI5518_OUT10_156.25M_DP/N	CLK_MUX_SI5518_OUT6_OUT10_156.25M_DP/N	—	High
clk_mux_4_sel	CLK_A5E_1D_REC_DP/N	CLK_A5E_1C_REC_DP/N	CLK_MUX_A5E_1C_1D_REC_DP/N	—	High
clk_mux_5_sel	CLK_SI5518_OUT16_100M_DP/N	CLK_SI569_HDMI_100M_DP_MUX_IN	CLK_MUX_SI5518_OUT16_SI569_100M_DP/N	REFCLK_4B_DP_MUX_IN	Low

continued...

Control Signal	Low CLOCK0)	High CLOCK1)	Output 0	Output 1	Mux Select Default
clk_mux_6_sel	CLK_SI549_FMC_B_DP_MUX_IN	FMC_GBTCLK0_M2C_DP/N	CLK_MUX_SI549_FMC_GBTCLK0_DP/N	CLK_HDMI_1B_100M_DP/N	Low
clk_mux_7_sel	SI5518_OUT3_DP_MUX_IN	REFCLK_4B_DP_MUX_IN	CLK_HDMI_4B_100M_DP/N	—	High
CLK_SI53254_CLKIN_SEL (S13.1)	CLK_PCIE_EDGE_100M_DP (from PCIe Golden Fingers)	CLK_PCIE_100M_DP/DN (from PCIe clock generator Si52202)	CLK_SI53254_OUT0_100M_DP/DN	CLK_SI53254_OUT1_100M_DP/DN	High (S13.1 = OFF)

Figure 54. Clock Tree



A.5. General Input/Output

Table 14. MAX 10 and Modular Board

Schematic Signal Name	Description
REMOTE_EN_BMC	Enable remote control of GPIOs of the Modular and Carrier boards, i.e., IP switch, push button through soft commands
SOM_PWR_EN_BMC	Enable Modular board power sequencing
SOM_PWR_OK_M2C_3V3	Power OK indication from Modular board to BMC
FAN_PWM_C2M_3V3	FAN PWM control for the Modular board active heatsink
FAN_TACH_C2M_3V3	FAN Tachometer feedback to BMC
SOM_RESET_C2M_3V3	Mapped to HPS_COLD_RESET on the Modular board
INIT_DONE_M2C_1V8	Initialization done indication of the Agilex 5 E-Series FPGA to BMC
CONF_DONE_M2C_1V8_BMC	Configuration done indication of Agilex 5 E-Series FPGA to BMC
NSTATUS_M2C_1V8	Nstatus Output from Agilex 5 E-Series FPGA

continued...

Schematic Signal Name	Description
NCONFIG_C2M_1V8	nCONFIG control from BMC to Agilex 5 E-Series FPGA
INT_N_C2M_1V8	Active low interrupt signal generated by MAX 10 to Agilex 5 E-Series FPGA
SOM_PRSNT_SEC_2	Modular Board Present indication to BMC
BMC_SPI_CS_3V3	Chip Select signal between Agilex 5 E-Series FPGA and BMC (SPI interface)
BMC_SPI_MISO_R_3V3	MISO signal between Agilex 5 E-Series FPGA and BMC (SPI interface)
BMC_SPI_MOSI_R_3V3	MOSI signal between Agilex 5 E-Series FPGA and BMC (SPI interface)
BMC_SPI_SCLK_3V3	Clock signal between Agilex 5 E-Series FPGA and BMC (SPI interface)

Table 15. MAX 10 BMC

Schematic Signal Name	Description
PG_V1P2_FMC_1V8	Power Good indication of +V1P2 (Active High)
PG_V1P8_CAR_3V3	Power Good indication of +V1P8 (Active High)
PG_V1P8_STBY_3V3	Power Good indication of +V1P8_STBY (Active High)
PG_V2P5_CAR_3V3	Power Good indication of 2.5 V rail (Active High)
PG_V3P3_CAR_1V8	Power Good indication 3.3 V used in the Carrier board (Active High)
PG_V3P3_SFP_1V8	Power Good indication SFP28 rail (Active High)
PG_MDK_BMC	Carrier board Power OK Indication (AND of all Power Goods), Active High
PG_FRAMOS_3V3	FRAMOS supply Power Good indication (Active High)
PG_MPM54304_CAR_IO_1V8	Power Good indication of MPM54304 VR generating non-standby rails (Active High)
PG_MPM54304_STBY_RAILS	Carrier board standby rails Power Good indication (Active High)
FMC_PG_M2C	Power Good indication from FMC card (Active High)
FMC_POK_C2M	Power Good Indication from BMC to FMC add-on card (Active High)
CARRIER_PWR_EN_3V3	EN control to Carrier board VRs (Active High)
BMC_SI569_1_FS_3V3_R	Si569 Frequency Select (FS) control • Logic 0: 100 MHz • Logic 1: 150 MHz
BMC_SI569_3_FS_3V3_R	Si569 Frequency Select (FS) control • Logic 0: 148.35 MHz • Logic 1: 148.5 MHz
CLK_MUX_1_SEL SI53307	Mux select line control signal • Low—CLK0 • High—CLK1
CLK_MUX_2_SEL SI53307	Mux select line control signal

continued...

Schematic Signal Name	Description
	• Low—CLK0 • High—CLK1
CLK_MUX_3_SEL SI53307	Mux select line control signal • Low—CLK0 • High—CLK1
CLK_MUX_4_SEL SI53307	Mux select line control signal • Low—CLK0 • High—CLK1
CLK_MUX_5_SEL SI53307	mux select line control signal • Low—CLK0 • High—CLK1
CLK_MUX_6_SEL SI53307	Mux select line control signal • Low—CLK0 • High—CLK1
CLK_MUX_7_SEL SI53307	Mux select line control signal • Low—CLK0 • High—CLK1
SI5518_GPIO0_1V8	Global output from Si5518 (Interrupt)
SI5518_GPIO1_1V8	Output from Si5518, loss of lock (LoL) indication
SI5518_GPIO2_1V8	Global input to Si5518, Output Enable (OE_b)
SI5518_RST_N	Reset control input to Si5518
BMC_JTAG_TMS	MAX 10 JTAG TMS signal
BMC_JTAG_TCK	MAX 10 JTAG TCK signal
BMC_JTAG_TDI	MAX 10 JTAG TDI signal
BMC_JTAG_TDO	MAX 10 JTAG TDO signal
JTAG_EXT_PCIE_TMS	PCIe/EXT header JTAG TMS
JTAG_EXT_PCIE_TCK	PCIe/EXT header JTAG TCK
JTAG_EXT_PCIE_TDI	PCIe/EXT header JTAG TDI
JTAG_EXT_PCIE_TDO	PCIe/EXT header JTAG TDO
FMC_TMS	FMC JTAG TMS
FMC_TCK	FMC JTAG TCK
FMC_TDI	FMC JTAG TDI
FMC_TDO	FMC JTAG TDO
JTAG_TMS_C2M_1V8	Modular Board FPGA JTAG TMS signal
JTAG_TCK_C2M_1V8	Modular Board FPGA JTAG TCK signal
JTAG_TDI_C2M_1V8	Modular Board FPGA JTAG TDI signal
JTAG_TDO_M2C_1V8	Modular Board FPGA JTAG TDO signal
BMC_CLK_I2C_SCL	BMC I^2C bus SCL for clock devices
BMC_CLK_I2C_SDA	BMC I^2C bus SDA for clock devices

continued...

Schematic Signal Name	Description
I2C_SCL1_C2M_B2B_3V3_HM	Clock signal for I^2C bus for health monitoring data collection from temperature and current sensors
I2C_SDA1_C2M_B2B_3V3_HM	Data signal for I^2C bus for health monitoring data collection from temperature and current sensors.
PCIE_EDGE_SMBCLK_3V3	PCIe SMBus clock signal
PCIE_EDGE_SMBDAT_3V3	PCIe SMBus data
PMBUS_SCL_BMC BMC	I^2C bus SCL for VRs
PMBUS_SDA_BMC BMC	I^2C bus SDA for VRs
I2C_HDMI_DP_SDI_SFP_SCL_3V3	I^2C bus SCL signal for HDMI, SFP, SDI, and DP
I2C_HDMI_DP_SDI_SFP_SDA_3V3	I^2C bus SDA signal for HDMI, SFP, SDI, and DP
BMC_UART_3V3_FTDI_RXD BMC	UART Output to FT4232H chip for UART interface
BMC_UART_3V3_FTDI_TXD BMC	UART input from FT4232H for UART interface
BMC_UART_RXD_I2C_SCL_3V3	UART RX between BMC and Modular board
BMC_UART_TXD_I2C_SDA_3V3	UART TX between BMC and Modular board
SFP28_INT_1V8	Spare pin
SFP28_LOS_3V3_R	SFP28 loss of signal (LOS) indication
SFP28_MOD_DET_3V3_R	SFP28 module detect indication
SFP28_TX_DISABLE_3V3_R	SFP28 transmit disable control
SFP28_TX_FAULT_3V3_R	SF28 transmit fault indication
ETH0_INT_N_3V3	Ethernet0 interrupt for Agilex 5 D-Series Modular board
ETH0_RESET_N	Ethernet0 reset control signal
ETH1_INT_N_3V3	Ethernet1 interrupt for Agilex 5 D-Series Modular board
ETH1_RESET_N	Ethernet1 reset control signal
MIPI0_PWR_EN_0_1V8	Drive Power Enable pin of Framos Sensor Module (FSM). High=Normal, Low=Pwr Down (MIPI0 interface related).
MIPI0_RST_0_1V8	General reset of FSM (MIPI0 interface related)
MIPI0_XMASTER0_1V8	Drive XMASTER Pin of FSM, MIPI0
MIPI0_SPI_CS_1V8	SPI Chip Select signal for Framos0 (MIPI0)
MIPI1_PWR_EN_0_1V8	Drive Power Enable pin of FSM. High=Normal, Low=Pwr Down (MIPI1 interface related).
MIPI1_RST_0_1V8	General reset of FSM (MIPI1 interface related)
MIPI1_XMASTER0_1V8	Drive XMASTER pin of FSM, MIPI1
MIPI1_SPI_CS_1V8	SPI Chip Select signal for Framos1 (MIPI1)
MIPI_SPI_CS_1V8	Chip Select signal for MIPI interface
DISP_PORT_TX_CON_CONFIG2_DRIVE_N	DisplayPort TX Config2 Drive signal
DISP_PORT_TX_CON_CONFIG2_SENSE_N	DisplayPort TX Config Sense signal

continued...

Schematic Signal Name	Description
MSEL0_C2M_1V8	Agilex 5 E-Series FPGA configuration Mode Select 0 signal
MSEL1_C2M_1V8	Agilex 5 E-Series FPGA configuration Mode Select 1 signal
MSEL2_C2M_1V8	Agilex 5 E-Series FPGA configuration Mode Select 2 signal
JTAG_EXT_PROC_RSTN	External JTAG reset indication
JTAG_EXT_PRSNT#	External JTAG present indication
JTAG_FPGA_BYPASSN	Input from Switch for JTAG FPGA Bypass
JTAG_INPUT_SOURCE	Switch selection for JTAG external or UB-II mode
FMC_JTAG_BYPASS	FMC JTAG bypass control
MUX_SEL_JTAG_EXT_USB_R	Select between external dongle or USB JTAG
MAX10_DEV_OE	Loss of signal (LOS) indication from Si53254
MAX10_JTAG_EN	MAX 10 JTAG enable pin
MAX10_NCONFIG	MAX 10 nConfig input signal
MAX10_NSTATUS	MAX 10 nstatus indication signal
MAX10_CONF_DONE	MAX 10 config done indication signal
CARRIER_ADDR0	Carrier Board Revision Bit 0
CARRIER_ADDR1	Carrier Board Revision Bit 1
CARRIER_ADDR2	Carrier Board Revision Bit 2
FMC_PRSNT_N	FMC card present indication
FTDI_RESET_N	FT4232H device reset control
I2C_LTC4312_EN1	LTC4312 I^2C bus control between I^2C's from the Agilex 5 E-Series FPGA (HVIO vs HPS)
SEU_ERROR_M2C_1V8	SEU Error indication from Modular board to Carrier board
OVERTEMP_SHDN_N_3V3	Over temp indication to shutdown all powers. If triggered "Low", initiate power down sequence.
OVERTEMP_WARN_N_3V3	Over temperature warning (Active Low)
CURR_SNS_CRTCL_3V3	Current sense critical signal from INA3321. If triggered "Low", initiate power down sequence
WAKE_PCIE	PCIe wake signal
CLKREQ_PCIE PCIe	PCIe CLK REQ signal
USER_DIPSW0	General-purpose User DIP switch0
USER_DIPSW1	General-purpose User DIP switch1
USER_DIPSW2	General-purpose User DIP switch2
USER_DIPSW3	General-purpose User DIP switch3
USER_PB1	User push button switch 1 signal (by default, high)
USER_PB2	User push button switch 2 signal (by default, high)
USER_PB3	User push button switch 3 signal (by default, high)

continued...

Schematic Signal Name	Description
USER_LED_G0	General-purpose user LED0 green. Blinks to indicate BMC Nios is up and running.
USER_LED_G1	General-purpose user LED1 green
USER_LED_R0	General-purpose user LED0 red. Glows when there is no clock to Si53254.
USER_LED_R1	General-purpose user LED1 red

A.6. Memory Interfaces

FPGA Dedicated External Memory Interface (DDR4 Component)

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 2x 8 GB DDR4 component down interface. Three quantity MT40A2G16TBB-062E:F from Micron* are soldered down on the development kit per HSIO Bank 2B and 3B. The data rate supported is maximum 1600 MT/s for -6S speed grade FPGA device.

Bank 2B supports x32 interface with clamshell x8ECC. The current version of the FPGA loaded onto development kit do not support clamshell. Bank 3B supports x32 + 8 bit ECC.

FPGA and HPS Shared External Memory Interface (DDR4 Component)

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 8 GB DDR4 component down interface terminated to HSIO Bank 3A. Three quantity MT40A2G16TBB-062E:F from Micron are soldered down on the development kit. This interface supports x32 + 8bit ECC. The data rate supported is maximum 1600 MT/s for -6S speed grade FPGA device.

A.7. Board to Board Connector

A.7.1. Modular Board Primary Connector

Table 16. Modular Board Primary Connector (J14)

	A	B	C	D
1	+V_HVIO_5A_C2M	GND	+V_HVIO_5B_C2M	SOM_PRSNT_PRI_1
2	GND	A5E_JTAG_TDO_M2C_1V8	GND	I2C_SCL2_C2M_3V3
3	A5E_JTAG_TCK_C2M_1V8	A5E_JTAG_TDI_C2M_1V8	SOM_RESET_C2M_3V3	I2C_SDA2_C2M_3V3
4	A5E_JTAG_TMS_C2M_1V8	REMOTE_EN_C2M_3V3	A5E_INTN_C2M_1V8	GND
5	SOM_PWR_EN_C2M_3V3	SOM_PWR_OK_M2C_3V3	A5E_NSTATUS_M2C_B2B_1V8	PMBUS_SDA_C2M_3V3
6	PMBUS_SCL_C2M_3V3	A5E_NCONFIG_C2M_B2B_1V8	A5E_INIT_DONE_M2C_B2B_1V8	EN_GROUP2_M2C_3V3
7	GND	FAN_PWM_C2M_3V3	A5E_CONF_DONE_M2C_B2B_1V8	PG_GROUP2_C2M_3V3_R
8	I2C_SCL1_C2M_3V3	FAN_TACH_C2M_3V3	A5E_AS_NCSO_MSEL0_C2M_1V8	AG5E_MSEL1_C2M_1V8

continued...

	A	B	C	D
9	I2C_SDA1_C2M_3V3	GND	AG5E_MSEL2_C2M_1V8	GND
10	GND	A5E_UX_1C_TX3_DN	GND	A5E_UX_1C_RX3_DN
11	GND	A5E_UX_1C_TX3_DP	GND	A5E_UX_1C_RX3_DP
12	A5E_UX_1C_TX0_DN	GND	A5E_UX_1C_RX0_DN	GND
13	A5E_UX_1C_TX0_DP	GND	A5E_UX_1C_RX0_DP	GND
14	GND	A5E_UX_1C_RX1_DN	GND	SEU_ERROR_M2C_1V8
15	GND	A5E_UX_1C_RX1_DP	GND	NC
16	A5E_UX_1C_TX1_DN	GND	ADDR0_M2C_3V3	GND
17	A5E_UX_1C_TX1_DP	GND	ADDR1_M2C_3V3	GND
18	GND	A5E_UX_1C_REC_CLK_DN	GND	CLK_A5E_UX_1C_R_C_DN
19	GND	A5E_UX_1C_REC_CLK_DP	GND	CLK_A5E_UX_1C_R_C_DP
20	NC	GND	NC	GND
21	NC	GND	NC	GND
22	GND	NC	GND	NC
23	GND	NC	GND	NC
24	NC	GND	NC	GND
25	NC	GND	NC	GND
26	GND	NC	GND	NC
27	GND	NC	GND	NC
28	NC	GND	NC	GND
29	NC	GND	NC	GND
30	GND	A5E_UX_1B_TX2_DN	GND	A5E_UX_1B_TX3_DN
31	GND	A5E_UX_1B_TX2_DP	GND	A5E_UX_1B_TX3_DP
32	A5E_UX_1B_RX2_DN	GND	A5E_UX_1B_RX3_DN	GND
33	A5E_UX_1B_RX2_DP	GND	A5E_UX_1B_RX3_DP	GND
34	GND	A5E_UX_1B_TX0_DN	GND	A5E_UX_1B_TX1_DN
35	GND	A5E_UX_1B_TX0_DP	GND	A5E_UX_1B_TX1_DP
36	A5E_UX_1B_RX0_DN	GND	A5E_UX_1B_RX1_DN	GND
37	A5E_UX_1B_RX0_DP	GND	A5E_UX_1B_RX1_DP	GND
38	GND	CLK_A5E_UX_1B_R_DN	GND	CLK_A5E_UX_1B_G_DN
39	GND	CLK_A5E_UX_1B_R_DP	GND	CLK_A5E_UX_1B_G_DP
40	A5E_UX_1A_RX2_DN	GND	A5E_UX_1A_RX3_DN	GND
41	A5E_UX_1A_RX2_DP	GND	A5E_UX_1A_RX3_DP	GND
42	GND	A5E_UX_1A_TX0_DN	GND	A5E_UX_1A_TX3_DN
43	GND	A5E_UX_1A_TX0_DP	GND	A5E_UX_1A_TX3_DP
44	A5E_UX_1A_RX0_DN	GND	A5E_UX_1A_RX1_DN	GND

continued...

	A	B	C	D
45	A5E_UX_1A_RX0_DP	GND	A5E_UX_1A_RX1_DP	GND
46	GND	A5E_UX_1A_TX1_DN	GND	A5E_UX_1A_TX2_DN
47	GND	A5E_UX_1A_TX1_DP	GND	A5E_UX_1A_TX2_DP
48	CLK_A5E_UX_1A_R_DN	GND	CLK_A5E_UX_1A_G_DN	GND
49	CLK_A5E_UX_1A_R_DP	GND	CLK_A5E_UX_1A_G_DP	GND
50	GND	A5E_HVIO_5B_2	GND	A5E_HVIO_5B_18
51	A5E_HVIO_5B_1	GND	A5E_HVIO_5B_7	GND
52	A5E_HVIO_5B_9	A5E_HVIO_5B_20	A5E_HVIO_5B_3	A5E_HVIO_5B_13
53	GND	A5E_HVIO_5B_19	GND	A5E_HVIO_5B_11
54	A5E_HVIO_5B_4	A5E_HVIO_5B_5	A5E_HVIO_5B_15	A5E_HVIO_5B_14
55	A5E_HVIO_5B_10	GND	A5E_HVIO_5B_17	GND
56	A5E_HVIO_5B_6	A5E_HVIO_5B_8	A5E_HVIO_5B_12	A5E_HVIO_5B_16
57	GND	A5E_HVIO_5A_1	GND	A5E_HVIO_5A_7
58	A5E_HVIO_5A_3	A5E_HVIO_5A_2	A5E_HVIO_5A_14	A5E_HVIO_5A_12
59	A5E_HVIO_5A_4	GND	A5E_HVIO_5A_13	GND
60	A5E_HVIO_5A_15	A5E_HVIO_5A_16	A5E_HVIO_5A_8	A5E_HVIO_5A_11
61	GND	A5E_HVIO_5A_10	GND	A5E_HVIO_5A_6
62	A5E_HVIO_5A_19	A5E_HVIO_5A_5	A5E_HVIO_5A_17	A5E_HVIO_5A_9
63	A5E_HVIO_5A_20	GND	A5E_HVIO_5A_18	GND
64	A5E_HSIO_2A_T23_DN	A5E_HSIO_2A_T23_DP	A5E_HSIO_2A_T24_DP	A5E_HSIO_2A_T24_DN
65	GND	A5E_HSIO_2A_B5_DP	GND	A5E_HSIO_2A_B23_DP
66	A5E_HSIO_2A_B6_DP	A5E_HSIO_2A_B5_DN	A5E_HSIO_2A_B24_DP	A5E_HSIO_2A_B23_DN
67	A5E_HSIO_2A_B6_DN	GND	A5E_HSIO_2A_B24_DN	GND
68	A5E_HSIO_2A_B17_DP	A5E_HSIO_2A_B17_DN	A5E_HSIO_2A_B4_DP	A5E_HSIO_2A_B4_DN
69	GND	A5E_HSIO_2A_B3_DP	GND	A5E_HSIO_2A_B22_DP
70	A5E_HSIO_2A_B18_DP	A5E_HSIO_2A_B3_DN	A5E_HSIO_2A_T22_DP	A5E_HSIO_2A_B22_DN
71	A5E_HSIO_2A_B18_DN	GND	A5E_HSIO_2A_T22_DN	GND
72	A5E_HSIO_2A_T21_DP	A5E_HSIO_2A_T21_DN	A5E_HSIO_2A_B2_DP	A5E_HSIO_2A_B2_DN
73	GND	A5E_HSIO_2A_T5_DP	GND	A5E_HSIO_2A_B21_DP
74	A5E_HSIO_2A_B1_DP	A5E_HSIO_2A_T5_DN	A5E_HSIO_2A_T20_DP	A5E_HSIO_2A_B21_DN
75	A5E_HSIO_2A_B1_DN	GND	A5E_HSIO_2A_T20_DN	GND
76	A5E_HSIO_2A_B16_DP	A5E_HSIO_2A_B16_DN	A5E_HSIO_2A_T6_DP	A5E_HSIO_2A_T6_DN
77	GND	A5E_HSIO_2A_T19_DP	GND	A5E_HSIO_2A_B20_DP
78	A5E_HSIO_2A_B15_DP	A5E_HSIO_2A_T19_DN	A5E_HSIO_2A_T4_DP	A5E_HSIO_2A_B20_DN
79	A5E_HSIO_2A_B15_DN	GND	A5E_HSIO_2A_T4_DN	GND
80	A5E_HSIO_2A_T18_DP	A5E_HSIO_2A_T18_DN	A5E_HSIO_2A_B14_DP	A5E_HSIO_2A_B14_DN

continued...

	A	B	C	D
81	GND	A5E_HSIO_2A_T2_DP	GND	A5E_HSIO_2A_B13_DN
82	A5E_HSIO_2A_B11_DP	A5E_HSIO_2A_T2_DN	NC	A5E_HSIO_2A_B13_DP
83	A5E_HSIO_2A_B11_DN	GND	A5E_HSIO_2A_T17_DN	GND
84	A5E_HSIO_2A_T16_DP	A5E_HSIO_2A_T16_DN	A5E_HSIO_2A_T11_DP	A5E_HSIO_2A_T11_DN
85	GND	A5E_HSIO_2A_T12_DP	GND	A5E_HSIO_2A_B19_DP
86	A5E_HSIO_2A_T3_DP	A5E_HSIO_2A_T12_DN	A5E_HSIO_2A_B12_DP	A5E_HSIO_2A_B19_DN
87	A5E_HSIO_2A_T3_DN	GND	A5E_HSIO_2A_B12_DN	GND
88	A5E_HSIO_2A_T15_DP	A5E_HSIO_2A_T15_DN	A5E_HSIO_2A_T10_DP	A5E_HSIO_2A_T10_DN
89	GND	A5E_HSIO_2A_B10_DP	GND	A5E_HSIO_2A_T9_DP
90	A5E_HSIO_2A_T1_DN	A5E_HSIO_2A_B10_DN	A5E_HSIO_2A_B9_DP	A5E_HSIO_2A_T9_DN
91	A5E_HSIO_2A_T1_DP	GND	A5E_HSIO_2A_B9_DN	GND
92	A5E_HSIO_2A_T14_DN	A5E_HSIO_2A_T14_DP	A5E_HSIO_2A_T8_DP	A5E_HSIO_2A_T8_DN
93	GND	A5E_HSIO_2A_B8_DP	GND	A5E_HSIO_2A_B7_DP
94	A5E_HSIO_2A_T13_DN	A5E_HSIO_2A_B8_DN	A5E_HSIO_2A_T7_DP	A5E_HSIO_2A_B7_DN
95	A5E_HSIO_2A_T13_DP	GND	A5E_HSIO_2A_T7_DN	GND
96	SOM_PRSNT_PRI_2	+V1P2	GND	+V1P2
97	GND	GND	GND	GND
98	+V12P0	+V12P0	+V12P0	+V12P0
99	GND	GND	GND	GND
100	+V12P0	+V12P0	+V12P0	+V12P0

A.7.2. Modular Board Secondary Connector

Table 17. Modular Board Secondary Connector (J13)

	A	B	C	D
1	SOM_PRSNT_SEC_1	+V_HVIO_6CD_C2M	GND	+V_HVIO_6EF_C2M
2	GND	A5E_HVIO_6D_17	GND	A5E_HVIO_6D_14
3	A5E_HVIO_6D_11	A5E_HVIO_6D_15	A5E_HVIO_6D_18	A5E_HVIO_6D_19
4	A5E_HVIO_6D_16	GND	A5E_HVIO_6D_13	GND
5	A5E_HVIO_6D_20	A5E_HVIO_6D_12	A5E_HVIO_6D_10	A5E_HVIO_6D_7
6	GND	A5E_HVIO_6D_8	GND	A5E_HVIO_6D_2
7	A5E_HVIO_6D_5	A5E_HVIO_6D_9	A5E_HVIO_6D_6	A5E_HVIO_6D_4
8	A5E_HVIO_6D_3	GND	A5E_HVIO_6D_1	GND
9	A5E_HVIO_6C_6	A5E_HVIO_6C_5	A5E_HVIO_6C_13	A5E_HVIO_6C_17
10	GND	A5E_HVIO_6C_7	GND	A5E_HVIO_6C_1
11	A5E_HVIO_6C_8	A5E_HVIO_6C_4	A5E_HVIO_6C_3	A5E_HVIO_6C_18
12	A5E_HVIO_6C_11	GND	A5E_HVIO_6C_20	GND

continued...

	A	B	C	D
13	A5E_HVIO_6C_12	A5E_HVIO_6C_9	A5E_HVIO_6C_2	A5E_HVIO_6C_19
14	GND	A5E_HVIO_6C_14	GND	A5E_HVIO_6C_10
15	A5E_HVIO_6C_16	A5E_HVIO_6C_15	A5E_HVIO_6E_12	A5E_HVIO_6E_10
16	A5E_HVIO_6E_18	GND	A5E_HVIO_6E_1	GND
17	A5E_HVIO_6E_17	A5E_HVIO_6E_14	A5E_HVIO_6E_13	A5E_HVIO_6E_15
18	GND	A5E_HVIO_6E_19	GND	A5E_HVIO_6E_20
19	A5E_HVIO_6E_7	A5E_HVIO_6E_4	A5E_HVIO_6E_2	A5E_HVIO_6E_11
20	A5E_HVIO_6E_5	GND	A5E_HVIO_6E_3	GND
21	A5E_HVIO_6E_6	A5E_HVIO_6E_8	A5E_HVIO_6E_9	A5E_HVIO_6E_16
22	GND	A5E_HVIO_6F_20	GND	A5E_HVIO_6F_16
23	A5E_HVIO_6F_18	A5E_HVIO_6F_19	A5E_HVIO_6F_15	A5E_HVIO_6F_17
24	A5E_HVIO_6F_14	GND	A5E_HVIO_6F_13	GND
25	A5E_HVIO_6F_12	A5E_HVIO_6F_11	A5E_HVIO_6F_10	A5E_HVIO_6F_9
26	GND	A5E_HVIO_6F_8	GND	A5E_HVIO_6F_4
27	A5E_HVIO_6F_3	A5E_HVIO_6F_7	A5E_HVIO_6F_1	A5E_HVIO_6F_2
28	A5E_HVIO_6F_5	GND	A5E_HVIO_6F_6	GND
29	GND	A5E_UX_4C_RX3_DN	GND	A5E_UX_4C_RX2_DN
30	GND	A5E_UX_4C_RX3_DP	GND	A5E_UX_4C_RX2_DP
31	A5E_UX_4C_TX3_DN	GND	A5E_UX_4C_TX2_DN	GND
32	A5E_UX_4C_TX3_DP	GND	A5E_UX_4C_TX2_DP	GND
33	GND	A5E_UX_4C_RX1_DN	GND	A5E_UX_4C_RX0_DN
34	GND	A5E_UX_4C_RX1_DP	GND	A5E_UX_4C_RX0_DP
35	A5E_UX_4C_TX1_DN	GND	A5E_UX_4C_TX0_DN	GND
36	A5E_UX_4C_TX1_DP	GND	A5E_UX_4C_TX0_DP	GND
37	GND	CLK_A5E_UX_4C_R_DN	GND	CLK_A5E_UX_4C_G_DN
38	GND	CLK_A5E_UX_4C_R_DP	GND	CLK_A5E_UX_4C_G_DP
39	A5E_UX_4D_RX3_DN	GND	A5E_UX_4D_RX2_DN	GND
40	A5E_UX_4D_RX3_DP	GND	A5E_UX_4D_RX2_DP	GND
41	GND	A5E_UX_4D_TX3_DN	GND	A5E_UX_4D_TX2_DN
42	GND	A5E_UX_4D_TX3_DP	GND	A5E_UX_4D_TX2_DP
43	A5E_UX_4D_RX1_DN	GND	A5E_UX_4D_RX0_DN	GND
44	A5E_UX_4D_RX1_DP	GND	A5E_UX_4D_RX0_DP	GND
45	GND	A5E_UX_4D_TX1_DN	GND	A5E_UX_4D_TX0_DN
46	GND	A5E_UX_4D_TX1_DP	GND	A5E_UX_4D_TX0_DP
47	NC	GND	NC	GND
48	NC	GND	NC	GND

continued...

	A	B	C	D
49	GND	A5E_UX_4B_RX3_DN	GND	A5E_UX_4B_RX2_DN
50	GND	A5E_UX_4B_RX3_DP	GND	A5E_UX_4B_RX2_DP
51	A5E_UX_4B_TX3_DN	GND	A5E_UX_4B_TX2_DN	GND
52	A5E_UX_4B_TX3_DP	GND	A5E_UX_4B_TX2_DP	GND
53	GND	A5E_UX_4B_RX1_DN	GND	A5E_UX_4B_RX0_DN
54	GND	A5E_UX_4B_RX1_DP	GND	A5E_UX_4B_RX0_DP
55	A5E_UX_4B_TX1_DN	GND	A5E_UX_4B_TX0_DN	GND
56	A5E_UX_4B_TX1_DP	GND	A5E_UX_4B_TX0_DP	GND
57	GND	CLK_A5E_UX_4B_R_DN	GND	CLK_A5E_UX_4B_G_DN
58	GND	CLK_A5E_UX_4B_R_DP	GND	CLK_A5E_UX_4B_G_DP
59	A5E_UX_4A_RX3_DN	GND	A5E_UX_4A_RX2_DN	GND
60	A5E_UX_4A_RX3_DP	GND	A5E_UX_4A_RX2_DP	GND
61	GND	A5E_UX_4A_TX3_DN	GND	A5E_UX_4A_TX2_DN
62	GND	A5E_UX_4A_TX3_DP	GND	A5E_UX_4A_TX2_DP
63	A5E_UX_4A_RX1_DN	GND	A5E_UX_4A_RX0_DN	GND
64	A5E_UX_4A_RX1_DP	GND	A5E_UX_4A_RX0_DP	GND
65	GND	A5E_UX_4A_TX1_DN	GND	A5E_UX_4A_TX0_DN
66	GND	A5E_UX_4A_TX1_DP	GND	A5E_UX_4A_TX0_DP
67	CLK_A5E_UX_4A_R_DN	GND	CLK_A5E_UX_4A_G_DN	GND
68	CLK_A5E_UX_4A_R_DP	GND	CLK_A5E_UX_4A_G_DP	GND
69	GND	A5E_HVIO_6G_14	GND	A5E_HVIO_6G_17
70	A5E_HVIO_6G_13	A5E_HVIO_6G_10	A5E_HVIO_6G_16	A5E_HVIO_6G_11
71	A5E_HVIO_6G_2	GND	A5E_HVIO_6G_19	GND
72	A5E_HVIO_6G_5	A5E_HVIO_6G_1	A5E_HVIO_6G_8	A5E_HVIO_6G_15
73	GND	A5E_HVIO_6G_7	GND	A5E_HVIO_6G_20
74	A5E_HVIO_6G_4	A5E_HVIO_6G_6	A5E_HVIO_6G_9	A5E_HVIO_6G_18
75	A5E_HVIO_6G_3	GND	A5E_HVIO_6G_12	GND
76	A5E_HVIO_6H_18	A5E_HVIO_6H_17	A5E_HVIO_6H_3	A5E_HVIO_6H_5
77	GND	A5E_HVIO_6H_2	GND	A5E_HVIO_6H_6
78	A5E_HVIO_6H_7	A5E_HVIO_6H_11	A5E_HVIO_6H_12	A5E_HVIO_6H_4
79	A5E_HVIO_6H_20	GND	A5E_HVIO_6H_15	GND
80	A5E_HVIO_6H_19	A5E_HVIO_6H_8	A5E_HVIO_6H_16	A5E_HVIO_6H_1
81	GND	A5E_HVIO_6H_14	GND	A5E_HVIO_6H_13
82	A5E_HVIO_6H_10	A5E_HVIO_6H_9	NC	NC
83	NC	GND	NC	GND

continued...

	A	B	C	D
84	NC	NC	NC	A5E_4C_PERSTN_HVIO_6A_7_3V3
85	GND	NC	GND	NC
86	NC	NC	A5E_HPS_1PPS_OUT	A5E_HVIO_6A_20_3V3
87	NC	GND	A5E_HPS_1PPS_IN	GND
88	NC	NC	NC	NC
89	GND	A5E_HVIO_6B_17	GND	A5E_HVIO_6B_18
90	A5E_HVIO_6B_14	A5E_HVIO_6B_19	A5E_HVIO_6B_16	A5E_HVIO_6B_20
91	A5E_HVIO_6B_10	GND	A5E_HVIO_6B_11	GND
92	A5E_HVIO_6B_13	A5E_HVIO_6B_2	A5E_HVIO_6B_1	A5E_HVIO_6B_15
93	GND	A5E_HVIO_6B_8	GND	A5E_HVIO_6B_12
94	A5E_HVIO_6B_5	A5E_HVIO_6B_7	A5E_HVIO_6B_6	A5E_HVIO_6B_4
95	A5E_HVIO_6B_3	GND	A5E_HVIO_6B_9	GND
96	GND	+V_HVIO_6B_C2M	GND	+V_HVIO_6GH_C2M
97	GND	GND	GND	SOM_PRSNT_SEC_2
98	+V12P0	+V12P0	+V12P0	+V12P0
99	GND	GND	GND	GND
100	+V12P0	+V12P0	+V12P0	+V12P0

A.7.3. Carrier Board Primary Connector

Table 18. Carrier Board Primary Connector (J9)

	A	B	C	D
1	+V1P8_HVIO	GND	+V3P3_HVIO	SOM_PRSNT_PRI_1
2	GND	JTAG_TDO_M2C_1V8	GND	I2C_SCL2_C2M_B2B_3V3
3	JTAG_TCK_C2M_1V8	JTAG_TDI_C2M_1V8	SOM_RESET_C2M_3V3	I2C_SDA2_C2M_B2B_3V3
4	JTAG_TMS_C2M_1V8	REMOTE_EN_C2M_3V3	INT_N_C2M_1V8	GND
5	SOM_PWR_EN_C2M_3V3	SOM_PWR_OK_M2C_3V3	NSTATUS_M2C_1V8	PMBUS_SDA_C2M_3V3
6	PMBUS_SCL_C2M_3V3	NCONFIG_C2M_1V8	INIT_DONE_M2C_1V8	EN_GROUP2_M2C_3V3
7	GND	FAN_PWM_C2M_3V3	CONF_DONE_M2C_1V8	PG_GROUP2_C2M_3V3
8	I2C_SCL1_C2M_B2B_3V3	FAN_TACH_C2M_3V3	MSEL0_C2M_1V8	MSEL1_C2M_1V8
9	I2C_SDA1_C2M_B2B_3V3	GND	MSEL2_C2M_1V8	GND
10	GND	SFP28_TX_DN	GND	SFP28_RX_DN
11	GND	SFP28_TX_DP	GND	SFP28_RX_DP
12	ETH0_SGMII_TX_DN	GND	ETH0_SGMII_RX_DN	GND
13	ETH0_SGMII_TX_DP	GND	ETH0_SGMII_RX_DP	GND
14	GND	ETH1_SGMII_RX_DN	GND	SEU_ERROR_M2C_1V8

continued...

	A	B	C	D
15	GND	ETH1_SGMII_RX_DP	GND	NC
16	ETH1_SGMII_TX_DN	GND	ADDR0_M2C_3V3	GND
17	ETH1_SGMII_TX_DP	GND	ADDR1_M2C_3V3	GND
18	GND	CLK_A5E_1C_REC_DN	GND	CLK_MUX_SI5518_OUT9_OUT12_125M_DN
19	GND	CLK_A5E_1C_REC_DP	GND	CLK_MUX_SI5518_OUT9_OUT12_125M_DP
20	SDI_RX_N	GND	NC	GND
21	SDI_RX_P	GND	NC	GND
22	GND	SDI_TX_N	GND	NC
23	GND	SDI_TX_P	GND	NC
24	A5E_UX_1D_RX_DN	GND	NC	GND
25	A5E_UX_1D_RX_DP	GND	NC	GND
26	GND	A5E_UX_1D_TX_DN	GND	NC
27	GND	A5E_UX_1D_TX_DP	GND	NC
28	CLK_SI5518_OUT8_156.25M_DN	GND	CLK_A5E_1D_REC_DN	GND
29	CLK_SI5518_OUT8_156.25M_DP	GND	CLK_A5E_1D_REC_DP	GND
30	GND	FMC_TX2_DN	GND	FMC_TX3_DN
31	GND	FMC_TX2_DP	GND	FMC_TX3_DP
32	FMC_RX2_DN	GND	FMC_RX3_DN	GND
33	FMC_RX2_DP	GND	FMC_RX3_DP	GND
34	GND	FMC_TX0_DN	GND	FMC_TX1_DN
35	GND	FMC_TX0_DP	GND	FMC_TX1_DP
36	FMC_RX0_DN	GND	FMC_RX1_DN	GND
37	FMC_RX0_DP	GND	FMC_RX1_DP	GND
38	GND	CLK_MUX_SI549_FMC_GBTCLK0_DN	GND	CLK_MUX_SI5518_OUT6_OUT10_156.25M_DN
39	GND	CLK_MUX_SI549_FMC_GBTCLK0_DP	GND	CLK_MUX_SI5518_OUT6_OUT10_156.25M_DP
40	FMC_RX6_DN	GND	FMC_RX7_DN	GND
41	FMC_RX6_DP	GND	FMC_RX7_DP	GND
42	GND	FMC_TX4_DN	GND	FMC_TX7_DN
43	GND	FMC_TX4_DP	GND	FMC_TX7_DP
44	FMC_RX4_DN	GND	FMC_RX5_DN	GND
45	FMC_RX4_DP	GND	FMC_RX5_DP	GND
46	GND	FMC_TX5_DN	GND	FMC_TX6_DN
47	GND	FMC_TX5_DP	GND	FMC_TX6_DP

continued...

	A	B	C	D
48	CLK_FMC_GBTCLK1_C_DN	GND	CLK_MUX_SI5518_OUT5_SI569_DN	GND
49	CLK_FMC_GBTCLK1_C_DP	GND	CLK_MUX_SI5518_OUT5_SI569_DP	GND
50	GND	LMH1219_LOCK_N_3V3	GND	SI569_PWM_VCXO_3_3V3
51	LMH1218_LOCK_3V3	GND	SI569_PWM_VCXO_4_3V3	GND
52	LMH1218_LOS_INT_N_3V3	PCIE_EDGE_SMBCLK_3V3	PCIE_EDGE_SMBDAT_3V3	SI569_PWM_VCXO_2_3V3
53	GND	BMC_SPI_MISO_3V3	GND	SI569_PWM_VCXO_1_3V3
54	BMC_SPI_MOSI_3V3	BMC_SPI_SCLK_3V3	ETH_MDIO_3V3	I2C_FMC_SDA_3V3
55	BMC_UART_TXD_I2C_SDA_3V3	GND	ETH_MDC_3V3	GND
56	BMC_UART_RXD_I2C_SCL_3V3	BMC_SPI_CS_3V3	TSN_HVIO_1PPS_OUT_3V3	I2C_FMC_SCL_3V3
57	GND	HDMI_RX_HPD_N_1V8	GND	TRISYNC_1V8
58	HDMI_TX_HPD_N_1V8	HDMI_TX_CON_SCL_1V8	HDMI_RX_5V_SENSE_1V8	SFP28_INT_1V8
59	HDMI_RX_CON_SDA_1V8	GND	MIPI_SPI_CS_1V8	GND
60	HDMI_RX_CON_SCL_1V8	HDMI_TX_CON_SDA_1V8	MIPI_SPI_MISO_1V8	MIPI_XTRIG0_1V8
61	GND	MIPI0_FSTROBE_1V8	GND	MIPI_XHS0_1V8
62	I2C_HDMI_DP_SDI_SFP_SDA_1V8	MIPI1_FSTROBE_1V8	MIPI_I2C_SDA_SPI_MOSI_1V8	MIPI_XVS0_1V8
63	I2C_HDMI_DP_SDI_SFP_SCL_1V8	GND	MIPI_I2C_SCL_SPI_SCLK_1V8	GND
64	FMC_LA_29_1V2_DN	FMC_LA_29_1V2_DP	FMC_LA_24_1V2_DP	FMC_LA_24_1V2_DN
65	GND	FMC_LA_11_1V2_DP	GND	FMC_LA_2_1V2_DP
66	CLK_IO96B_2A_150M_DP	FMC_LA_11_1V2_DN	FMC_LA_1_1V2_DP	FMC_LA_2_1V2_DN
67	CLK_IO96B_2A_150M_DN	GND	FMC_LA_1_1V2_DN	GND
68	MIPI0_DATA1_DP	MIPI0_DATA1_DN	FMC_LA_10_1V2_DP	FMC_LA_10_1V2_DN
69	GND	FMC_LA_17_1V2_DP	GND	FMC_CLK1_M2C_DP
70	MIPI0_DATA0_DP	FMC_LA_17_1V2_DN	FMC_LA_25_1V2_DP	FMC_CLK1_M2C_DN
71	MIPI0_DATA0_DN	GND	FMC_LA_25_1V2_DN	GND
72	FMC_LA_22_1V2_DP	FMC_LA_22_1V2_DN	FMC_LA_3_1V2_DP	FMC_LA_3_1V2_DN
73	GND	FMC_LA_15_1V2_DP	GND	FMC_LA_9_1V2_DP
74	FMC_LA_5_1V2_DP	FMC_LA_15_1V2_DN	FMC_LA_12_1V2_DP	FMC_LA_9_1V2_DN
75	FMC_LA_5_1V2_DN	GND	FMC_LA_12_1V2_DN	GND
76	MIPI0_CLK_DP	MIPI0_CLK_DN	FMC_LA_14_1V2_DP	FMC_LA_14_1V2_DN
77	GND	CLK_HDMI_4B_100M_DP	GND	FMC_LA_23_1V2_DP
78	MIPI0_DATA2_DP	CLK_HDMI_4B_100M_DN	FMC_LA_16_1V2_DP	FMC_LA_23_1V2_DN
79	MIPI0_DATA2_DN	GND	FMC_LA_16_1V2_DN	GND

continued...

	A	B	C	D
80	CLK_HDMI_1B_100M_DP	CLK_HDMI_1B_100M_DN	MIPI0_DATA3_DP	MIPI0_DATA3_DN
81	GND	FMC_LA_20_1V2_DP	GND	FMC_LA_26_1V2_DN
82	MIPI1_DATA1_DP	FMC_LA_20_1V2_DN	NC	FMC_LA_26_1V2_DP
83	MIPI1_DATA1_DN	GND	CLK_SI5518_OUT1_1PPS_1V2	GND
84	FMC_LA_18_1V2_DP	FMC_LA_18_1V2_DN	FMC_LA_28_1V2_DP	FMC_LA_28_1V2_DN
85	GND	FMC_LA_30_1V2_DP	GND	FMC_CLK0_M2C_DP
86	FMC_LA_19_1V2_DP	FMC_LA_30_1V2_DN	MIPI1_DATA0_DP	FMC_CLK0_M2C_DN
87	FMC_LA_19_1V2_DN	GND	MIPI1_DATA0_DN	GND
88	FMC_LA_8_1V2_DP	FMC_LA_8_1V2_DN	FMC_LA_6_1V2_DP	FMC_LA_6_1V2_DN
89	GND	MIPI1_CLK_DP	GND	FMC_LA_7_1V2_DP
90	FMC_LA_21_1V2_DN	MIPI1_CLK_DN	MIPI1_DATA2_DP	FMC_LA_7_1V2_DN
91	FMC_LA_21_1V2_DP	GND	MIPI1_DATA2_DN	GND
92	FMC_LA_0_1V2_DN	FMC_LA_0_1V2_DP	FMC_LA_4_1V2_DP	FMC_LA_4_1V2_DN
93	GND	MIPI1_DATA3_DP	GND	CLK_TOD_156.25M_DP
94	FMC_LA_27_1V2_DN	MIPI1_DATA3_DN	FMC_LA_13_1V2_DP	CLK_TOD_156.25M_DN
95	FMC_LA_27_1V2_DP	GND	FMC_LA_13_1V2_DN	GND
96	SOM_PRSNT_PRI_2	+V1P2_HSIO_2A_M2C	GND	+V1P2_HSIO_2A_M2C
97	GND	GND	GND	GND
98	+V12P0	+V12P0	+V12P0	+V12P0
99	GND	GND	GND	GND
100	+V12P0	+V12P0	+V12P0	+V12P0

A.7.4. Carrier Board Secondary Connector

Table 19. Carrier Board Secondary Connector (J13)

	A	B	C	D
1	SOM_PRSNT_SEC_1	+V1P8_HVIO	GND	+V1P8_HVIO
2	GND	DISP_PORT_RX_AUX_DP_SENSE	GND	A5E_HVIO_6D_14_1V8
3	DISP_PORT_TX_AUX_DRV_OE_1V8	DISP_PORT_RX_AUX_DN_SENSE	DISP_PORT_TX_CON_CONFIG1_N_1V8	A5E_HVIO_6D_19_1V8
4	DISP_PORT_TX_AUX_DRV_OUT_1V8	GND	DISP_PORT_TX_CON_HPD_N_1V8	GND
5	DISP_PORT_TX_AUX_DRV_IN_1V8	DISP_PORT_RX_AUX_DRV_OE_1V8	DISP_PORT_RX_CON_HPD_1V8	A5E_HVIO_6D_7_1V8
6	GND	DISP_PORT_RX_AUX_DRV_OUT_1V8	GND	A5E_HVIO_6D_2_1V8
7	A5E_HVIO_6D_5_1V8	DISP_PORT_RX_AUX_DRV_IN_1V8	A5E_HVIO_6D_6_1V8	A5E_HVIO_6D_4_1V8

continued...

	A	B	C	D
8	A5E_HVIO_6D_3_1V8	GND	A5E_HVIO_6D_1_1V8	GND
9	A5E_HVIO_6C_6_1V8	A5E_HVIO_6C_5_1V8	A5E_HVIO_6C_13_1V8	A5E_HVIO_6C_17_1V8
10	GND	A5E_HVIO_6C_7_1V8	GND	A5E_HVIO_6C_1_1V8
11	A5E_HVIO_6C_8_1V8	A5E_HVIO_6C_4_1V8	A5E_HVIO_6C_3_1V8	ETH0_INT_N_1V8
12	A5E_HVIO_6C_11_1V8	GND	A5E_HVIO_6C_20_1V8	GND
13	A5E_HVIO_6C_12_1V8	A5E_HVIO_6C_9_1V8	A5E_HVIO_6C_2_1V8	ETH1_INT_N_1V8
14	GND	A5E_HVIO_6C_14_1V8	GND	A5E_HVIO_6C_10_1V8
15	A5E_HVIO_6C_16_1V8	A5E_HVIO_6C_15_1V8	A5E_HVIO_6E_12_1V8	A5E_HVIO_6E_10_1V8
16	A5E_HVIO_6E_18_1V8	GND	A5E_HVIO_6E_1_1V8	GND
17	A5E_HVIO_6E_17_1V8	A5E_HVIO_6E_14_1V8	A5E_HVIO_6E_13_1V8	A5E_HVIO_6E_15_1V8
18	GND	A5E_HVIO_6E_19_1V8	GND	A5E_HVIO_6E_20_1V8
19	A5E_HVIO_6E_7_1V8	A5E_HVIO_6E_4_1V8	A5E_HVIO_6E_2_1V8	A5E_HVIO_6E_11_1V8
20	A5E_HVIO_6E_5_1V8	GND	A5E_HVIO_6E_3_1V8	GND
21	A5E_HVIO_6E_6_1V8	A5E_HVIO_6E_8_1V8	A5E_HVIO_6E_9_1V8	A5E_HVIO_6E_16_1V8
22	GND	A5E_HVIO_6F_20_1V8	GND	A5E_HVIO_6F_16_1V8
23	A5E_HVIO_6F_18_1V8	A5E_HVIO_6F_19_1V8	A5E_HVIO_6F_15_1V8	A5E_HVIO_6F_17_1V8
24	A5E_HVIO_6F_14_1V8	GND	A5E_HVIO_6F_13_1V8	GND
25	A5E_HVIO_6F_12_1V8	A5E_HVIO_6F_11_1V8	A5E_HVIO_6F_10_1V8	A5E_HVIO_6F_9_1V8
26	GND	A5E_HVIO_6F_8_1V8	GND	A5E_HVIO_6F_4_1V8
27	A5E_HVIO_6F_3_1V8	A5E_HVIO_6F_7_1V8	A5E_HVIO_6F_1_1V8	A5E_HVIO_6F_2_1V8
28	A5E_HVIO_6F_5_1V8	GND	A5E_HVIO_6F_6_1V8	GND
29	GND	PCIE_RX_0_DN	GND	PCIE_RX_1_DN
30	GND	PCIE_RX_0_DP	GND	PCIE_RX_1_DP
31	PCIE_TX_0_DN	GND	PCIE_TX_1_DN	GND
32	PCIE_TX_0_DP	GND	PCIE_TX_1_DP	GND
33	GND	PCIE_RX_2_DN	GND	PCIE_RX_3_DN
34	GND	PCIE_RX_2_DP	GND	PCIE_RX_3_DP
35	PCIE_TX_2_DN	GND	PCIE_TX_3_DN	GND
36	PCIE_TX_2_DP	GND	PCIE_TX_3_DP	GND
37	GND	CLK_SI5518_OUT15_100M_DN	GND	CLK_SI53254_OUT0_100M_DN
38	GND	CLK_SI5518_OUT15_100M_DP	GND	CLK_SI53254_OUT0_100M_DP
39	PCIE_RX_4_DN	GND	PCIE_RX_5_DN	GND
40	PCIE_RX_4_DP	GND	PCIE_RX_5_DP	GND
41	GND	PCIE_TX_4_DN	GND	PCIE_TX_5_DN
42	GND	PCIE_TX_4_DP	GND	PCIE_TX_5_DP

continued...

	A	B	C	D
43	PCIE_RX_6_DN	GND	PCIE_RX_7_DN	GND
44	PCIE_RX_6_DP	GND	PCIE_RX_7_DP	GND
45	GND	PCIE_TX_6_DN	GND	PCIE_TX_7_DN
46	GND	PCIE_TX_6_DP	GND	PCIE_TX_7_DP
47	CLK_SI5518_OUT14_100M_DN	GND	CLK_SI53254_OUT1_100M_DN	GND
48	CLK_SI5518_OUT14_100M_DP	GND	CLK_SI53254_OUT1_100M_DP	GND
49	GND	HDMI_RX_3_DN	GND	HDMI_RX_2_DN
50	GND	HDMI_RX_3_DP	GND	HDMI_RX_2_DP
51	HDMI_TX_CLK_DN	GND	HDMI_TX_2_DN	GND
52	HDMI_TX_CLK_DP	GND	HDMI_TX_2_DP	GND
53	GND	HDMI_RX_1_DN	GND	HDMI_RX_0_DN
54	GND	HDMI_RX_1_DP	GND	HDMI_RX_0_DP
55	HDMI_TX_1_DN	GND	HDMI_TX_0_DN	GND
56	HDMI_TX_1_DP	GND	HDMI_TX_0_DP	GND
57	GND	CLK_HDMI_RX_DN	GND	CLK_MUX_SI5518_OUT16_SI569_100M_DN
58	GND	CLK_HDMI_RX_DP	GND	CLK_MUX_SI5518_OUT16_SI569_100M_DP
59	DISP_PORT_RX_3_DN	GND	DISP_PORT_RX_2_DN	GND
60	DISP_PORT_RX_3_DP	GND	DISP_PORT_RX_2_DP	GND
61	GND	DISP_PORT_TX_3_DN	GND	DISP_PORT_TX_2_DN
62	GND	DISP_PORT_TX_3_DP	GND	DISP_PORT_TX_2_DP
63	DISP_PORT_RX_1_DN	GND	DISP_PORT_RX_0_DN	GND
64	DISP_PORT_RX_1_DP	GND	DISP_PORT_RX_0_DP	GND
65	GND	DISP_PORT_TX_1_DN	GND	DISP_PORT_TX_0_DN
66	GND	DISP_PORT_TX_1_DP	GND	DISP_PORT_TX_0_DP
67	CLK_SI549_DISP_PORT_100M_DN	GND	CLK_SI5518_OUT17_100M_DN	GND
68	CLK_SI549_DISP_PORT_100M_DP	GND	CLK_SI5518_OUT17_100M_DP	GND
69	GND	A5E_HVIO_6G_14_1V8	GND	A5E_HVIO_6G_17_1V8
70	A5E_HVIO_6G_13_1V8	A5E_HVIO_6G_10_1V8	A5E_HVIO_6G_16_1V8	A5E_HVIO_6G_11_1V8
71	A5E_HVIO_6G_2_1V8	GND	A5E_HVIO_6G_19_1V8	GND
72	A5E_HVIO_6G_5_1V8	A5E_HVIO_6G_1_1V8	A5E_HVIO_6G_8_1V8	A5E_HVIO_6G_15_1V8
73	GND	A5E_HVIO_6G_7_1V8	GND	A5E_HVIO_6G_20_1V8
74	A5E_HVIO_6G_4_1V8	A5E_HVIO_6G_6_1V8	A5E_HVIO_6G_9_1V8	A5E_HVIO_6G_18_1V8
75	A5E_HVIO_6G_3_1V8	GND	A5E_HVIO_6G_12_1V8	GND

continued...

	A	B	C	D
76	A5E_HVIO_6H_18_1V8	A5E_HVIO_6H_17_1V8	A5E_HVIO_6H_3_1V8	A5E_HVIO_6H_5_1V8
77	GND	A5E_HVIO_6H_2_1V8	GND	A5E_HVIO_6H_6_1V8
78	A5E_HVIO_6H_7_1V8	A5E_HVIO_6H_11_1V8	A5E_HVIO_6H_12_1V8	A5E_HVIO_6H_4_1V8
79	A5E_HVIO_6H_20_1V8	GND	A5E_HVIO_6H_15_1V8	GND
80	A5E_HVIO_6H_19_1V8	A5E_HVIO_6H_8_1V8	A5E_HVIO_6H_16_1V8	A5E_HVIO_6H_1_1V8
81	GND	A5E_HVIO_6H_14_1V8	GND	A5E_HVIO_6H_13_1V8
82	A5E_HVIO_6H_10_1V8	A5E_HVIO_6H_9_1V8	NC	NC
83	NC	GND	NC	GND
84	NC	NC	NC	PCIE0_EDGE_PERST_R_N_3V3
85	GND	NC	GND	NC
86	NC	NC	TSN_HPS_1PPS_OUT_1V8	TSN_HVIO_1PPS_IN_3V3
87	NC	GND	TSN_HPS_1PPS_IN_1V8	GND
88	NC	NC	NC	NC
89	GND	A5E_HVIO_6B_17_3V3	GND	A5E_HVIO_6B_18_3V3
90	SFP28_MOD_DET_3V3	A5E_HVIO_6B_19_3V3	A5E_HVIO_6B_16_3V3	A5E_HVIO_6B_20_3V3
91	SFP28_LOS_3V3	GND	A5E_HVIO_6B_11_3V3	GND
92	SFP28_TX_FAULT_3V3	A5E_HVIO_6B_2_3V3	A5E_HVIO_6B_1_3V3	A5E_HVIO_6B_15_3V3
93	GND	A5E_HVIO_6B_8_3V3	GND	A5E_HVIO_6B_12_3V3
94	SFP28_TX_DISABLE_3V3	A5E_HVIO_6B_7_3V3	A5E_HVIO_6B_6_3V3	A5E_HVIO_6B_4_3V3
95	A5E_HVIO_6B_3_3V3	GND	A5E_HVIO_6B_9_3V3	GND
96	GND	+V3P3_HVIO	GND	+V1P8_HVIO
97	GND	GND	GND	SOM_PRSNT_SEC_2
98	+V12P0	+V12P0	+V12P0	+V12P0
99	GND	GND	GND	GND
100	+V12P0	+V12P0	+V12P0	+V12P0

A.8. Communication Interfaces

SFP+

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 1x SFP ports. The SFP port fans out from the transceiver channel 1C and port UX3. SFP supports 10G data rate.

TSN/SGMII

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 2x 2.5G TSN over the SGMII interface from the transceiver bank 1C. Ports UX0 and UX1 realize this interface on the Carrier board.

FMC

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 1x FMC+ slot for functional expandability. The x8 FGT lanes from banks 1A and 1B are terminated to FMC J7.

Serial Buses

The Agilex 5 FPGA E-Series 065B Modular Development Kit supports 4 major I^2C masters from the MAX 10 BMC.

PMBus

All the voltage regulators with I^2C/PMBus support can be accessed through this bus. The bus is shared among the VRs on the Carrier and Modular boards. Over the Modular board, there is a provision to isolate the PMBus from the SDM SVID bus. Refer to I^2C tree for further details.

Telemetry

Temperature sensors, current sensors, and EEPROM on the Carrier board are communicated over this bus. This bus is shared with current monitoring, temperature monitoring, power sequences, and reset control components.

This telemetry bus is shared with HPS I^2C bus on the Modular board.

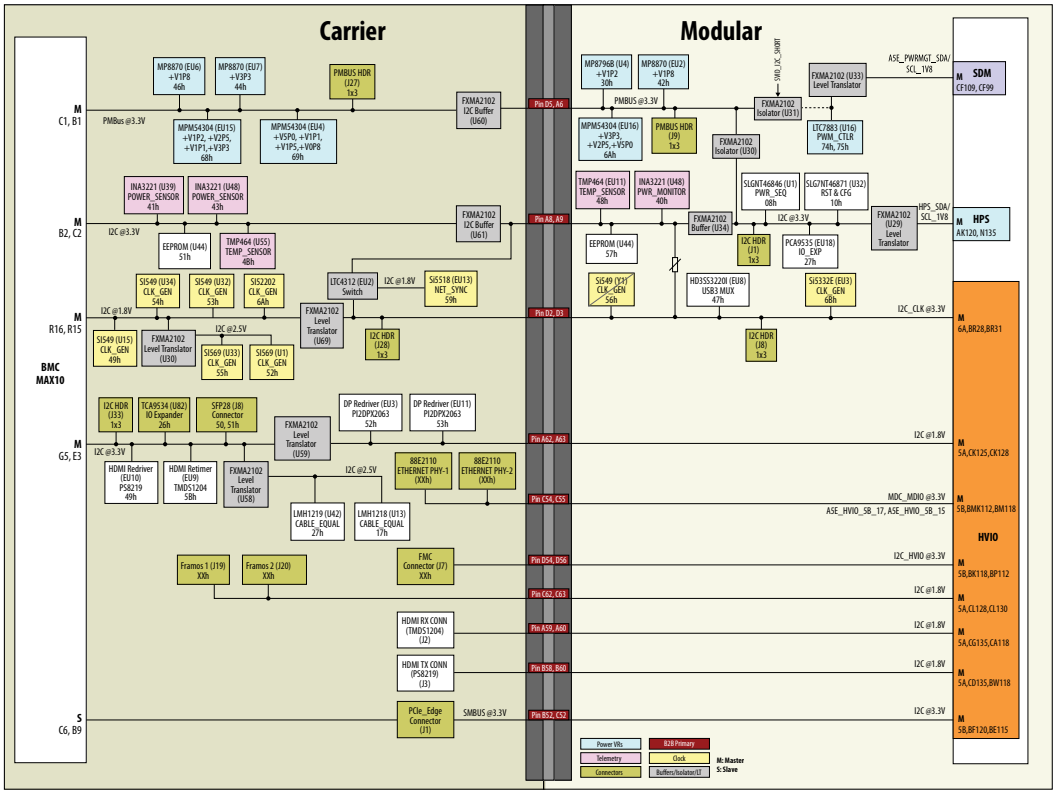
Clock

Dedicated bus for all the clock devices supporting I^2C on both Modular and Carrier boards.

Table 20. I^2C Debug Headers

Schematic Signal Name	Description
PMBUS_SCL_C2M_3V3/SDA	PMBus I^2C header J9 on the Modular board.
I2C_COM_SCL_C2M_3V3	I^2C bus header at J1 on the Modular board.
I2C_SCL2_C2M_3V3/SDA	I^2C bus header at J8 on Modular board for clock configuration.
PMBUS_SCL_C2M_3V3/SDA	PMBus I^2C header J27 on the Carrier board.
I2C_SCL2_C2M_B2B_3V3/SDA	I^2C bus header at J28 on the Carrier board for clock configuration.
I2C_HDMI_DP_SDI_SFP_SCL_3V3/SDA	I^2C bus header at J33 on the Carrier board for the peripheral device configuration or monitor.

Figure 55. I²C Serial Bus



B. Developer Resources

Use the following links to check the Intel website for other related information.

Table 21. Agilex 5 FPGA E-Series 065B Modular Development Kit References

Reference	Description
Agilex 5 FPGA E-Series 065B Modular Development Kit page	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
Rocketboard.org	Open-source community website supporting SoC development including Altera and Partner SoC development kit targets and related designs and documentation.
Ashling* RiscFree* Integrated Development Environment (IDE) for Altera FPGAs User Guide	Describes the RiscFree integrated development environment (IDE) for Altera FPGAs Arm-based HPS and Nios V core processors.
Agilex 5 FPGA Board Design Guided Journey	The interactive FPGA Board Guided Journey provides step-by-step guidance for developing printed circuit boards (PCBs) using Agilex 5 devices.
Device Design Guidelines: Agilex 5 FPGAs and SoCs	Guidelines, recommendations, and a list of factors to consider for designs that use the Agilex 5 SoC devices.
AN 958: Board Design Guidelines	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
Power Management User Guide: Agilex 5 FPGAs and SoCs	Describes the power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems, and power optimization techniques for the Agilex 5 FPGAs and SoCs.
Power Distribution Network Design Guidelines: Agilex 5 FPGAs and SoCs	Provides information for the Agilex 5 device family power distribution network (PDN) design guidelines.
FPGA SmartVID	SmartVID is a feature on select Altera FPGAs where the device identifies the optimal voltage that it should be operated at, and provides this information to the power regulator via the PMBus. The term represents Smart Voltage IDentification (SmartVID).
SmartVID Debug Checklist and Voltage Regulator Guidelines	Provides the checklist to assist you to rule out the possible causes of configuration failure due to SmartVID.
Device Configuration User Guide: Agilex 5 FPGAs and SoCs	Agilex 5 FPGAs and SoCs support configuration using the following interfaces: Avalon® streaming, JTAG, CvP, and Active Serial (AS) normal and fast modes. This user guide explains the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
Documentation: Agilex 5	Agilex 5 device documentation.
Cadence* Capture CIS Schematic Symbols	Agilex 5 OrCAD symbols.
Nios II Processor Reference Guide	Nios II 32-bit embedded processor solutions.

C. Safety and Regulatory Compliance Information

C.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

C.1.1. Safety Warnings

Power Supply Hazardous Voltage

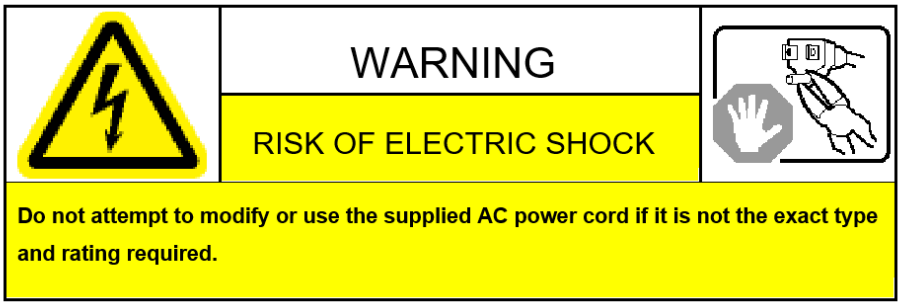
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

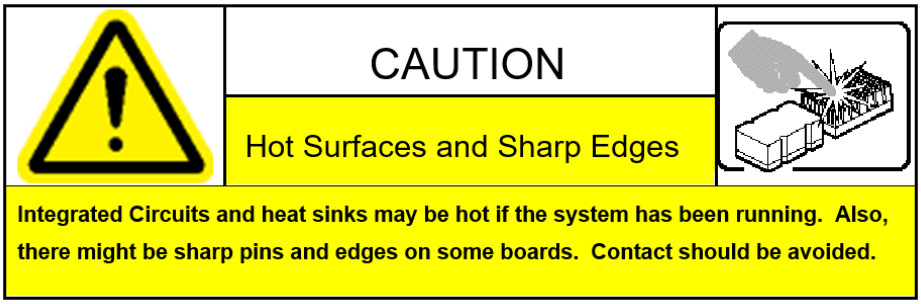
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

C.1.2. Safety Cautions



Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

C.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.