AsahiKASEI MICRODEVICES

= Preliminary =

AK4498EX

Quality Oriented Multi-bit Stereo DAC

1. General Description

The AK4498EX is a premium Multi-bit stereo DAC with VELVET SOUND™ technology, achieving low distortion characteristics and wide dynamic range. The OSR-Doubler technology establishes wide signal band, low power consumption and low distortion characteristics. It is suitable for playback of high-resolution audio sources that are becoming widespread in Network Audio, USB-DACs and Car Audio systems. Multi-bit Modulator input for a high-precision audio source playback.

Application: AV Receivers, CD/SACD player, Network Audio systems, USB DACs, USB Headphones, Measurement equipment, Control systems, Public Address (PA).

2. Features

- **THD+N: -117dB (2 Vrms), -113dB (2.6Vrms)**
- **DR, S/N: 129dB (2 Vrms), 131dB (2.6 Vrms)**
- **Multi-bit Modulator Data Interface with 11.2896 MHz Clock**
  - **6-bit Modulator Data**
- **Mono Mode**
- **Power Supply:**
  TVDD = AVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V,
  VDDL/R= 4.75 to 5.25V
- **Digital Input Level: CMOS**
- **Package: 64-pin HTQFP**
- **Temperature: -40 to 105°C**
- **Pin Control**

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

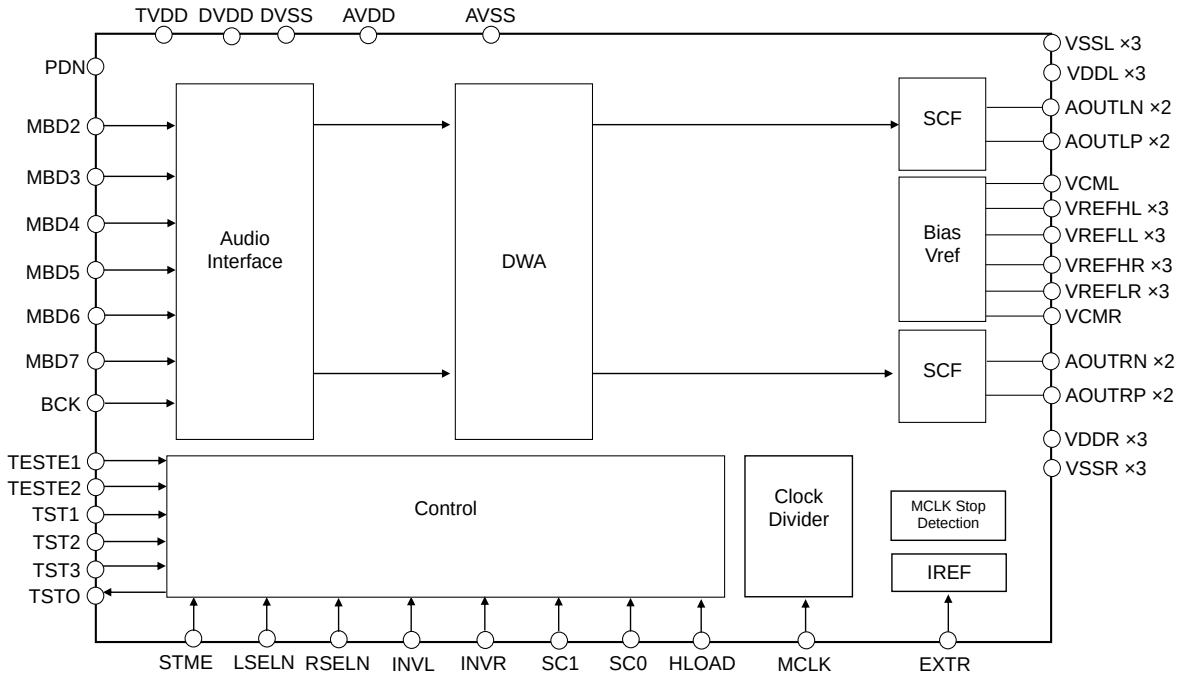


Figure 1. Block Diagram

4.2. Block Functions

Block	Functions
Audio Interface	BCK is used to clock MBD7-2 data into the shift register.
DWA	It is processing two's compliment MBD7-2 data by Data Weighted Average.
SCF	Switched Capacitor Filter block (1st-order) converts MBD7-2 data from DWA output to analog voltage signal. Its cut-off frequency is proportional to 128fs or 256fs over sampling rate.
Control	It sets operation mode by each pin's condition.
Clock Divider	It outputs the clock for SCF from MCLK.
MCLK Stop Detection	It is the detection circuit of MCLK input or no input.
IREF	It outputs the reference current that is made from reference voltage and external resistor.
Bias Vref	It outputs common voltage VCML/R that is generated by reference voltages VREFHL/R and VREFLL/R.

5. Pin Configurations and Functions

5.1. Pin Configurations

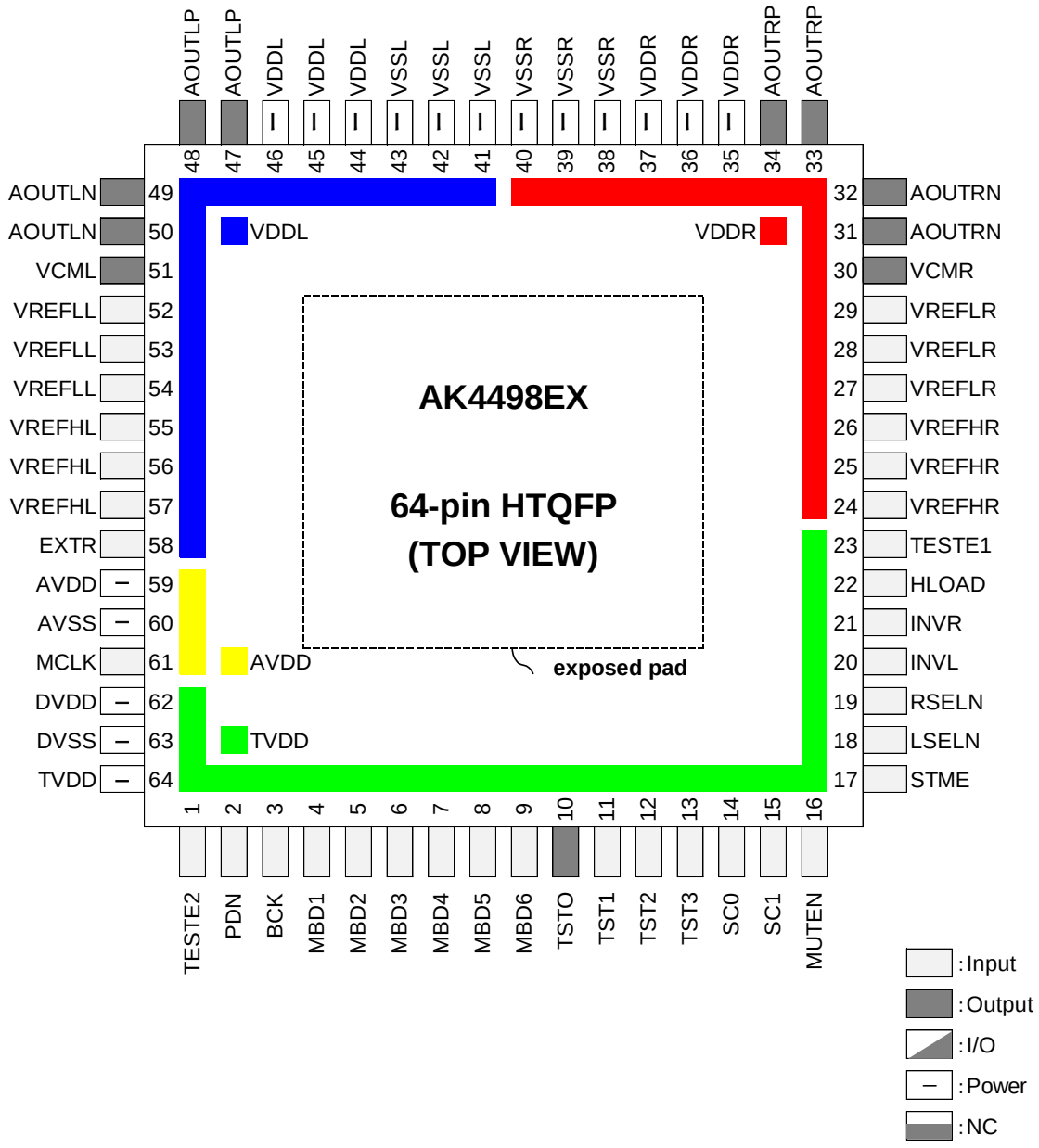


Figure 2. Pin Configuration

The exposed pad on the bottom surface of the package must be connected to AVSS.

5.2. Pin Functions

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
1	TESTE2	I	TVDD/DVSS	Test mode Enable pin (Internal pull-down pin)	Hi-Z
2	PDN	I	TVDD/DVSS	Power Up, Power Down pin When at “L”, the AK4498EX is in power down mode and is held in reset. The AK4498EX must always be reset upon power up.	Hi-z (PDN = “L”)
3	BCK	I	TVDD/DVSS	Multi-bit Data Clock pin	Hi-z
4	MBD2	I	TVDD/DVSS	Multi-bit Data 2 Input pin	Hi-z
5	MBD3	I	TVDD/DVSS	Multi-bit Data 3 Input pin	Hi-z
6	MBD4	I	TVDD/DVSS	Multi-bit Data 4 Input pin	Hi-z
7	MBD5	I	TVDD/DVSS	Multi-bit Data 5 Input pin	Hi-z
8	MBD6	I	TVDD/DVSS	Multi-bit Data 6 Input pin	Hi-z
9	MBD7	I	-/DVSS	Multi-bit Data 7 Input pin	Hi-z
10	TSTO	O	-/DVSS	Test Output pin	Pull down to DVSS (100 kΩ)
11	TST1	I	TVDD/DVSS	Test input 1 pin	Pull down to DVSS (100 kΩ)
12	TST2	I	TVDD/DVSS	Test input 2 pin	Pull down to DVSS (100 kΩ)
13	TST3	I	TVDD/DVSS	Test input 3 pin	Hi-z
14	SC0	I	TVDD/DVSS	Sound Control 0 pin	Hi-z
15	SC1	I	TVDD/DVSS	Sound Control 1 pin	Hi-z
16	MUTEN	I	TVDD/DVSS	When this pin is changed to “L”, mute cycle is initiated. When returning “H”, the output mute releases.	Hi-z
17	STME	I	TVDD/DVSS	Stereo mode Enable pin	Hi-z
18	LSELN	I	TVDD/DVSS	Lch Output Data Select pin	Hi-z
19	RSELN	I	TVDD/DVSS	Rch Output Data Select pin	Hi-z
20	INVL	I	TVDD/DVSS	Lch signal Invert Select pin	Hi-z
21	INVR	I	TVDD/DVSS	Rch signal Invert Select pin	Hi-z
22	HLOAD	I	TVDD/DVSS	Heavy Load Mode Enable pin	Hi-z
23	TESTE1	I	TVDD/DVSS	Test mode Enable pin (Internal pull-down pin)	Pull down to DVSS (100 kΩ)
24-26	VREFHR	I	VDDR/VSSR	Rch High Level Voltage Reference Input pin	Hi-z
27-29	VREFLR	I	VDDR/VSSR	Rch Low Level Voltage Reference Input pin	Connected to VCMR (5 kΩ)
30	VCMR	O	VDDR/VSSR	Right channel Common Voltage pin, Normally connected to VREFLR with a 10μF electrolytic capacitor. This pin is inhibited to connect other devices.	Connected to VREFLR (5 kΩ)
31,32	AOUTRN	O	VDDR/VSSR	Rch Negative Analog Output pin	Connected to AOUTRP (300 kΩ)

No.	Pin Name	I/O	Protection Diode	Function	Power Down State
33,34	AOUTRP	O	VDDR/VSSR	Rch Positive Analog Output pin	Connected to AOUTRN (300 kΩ)
35-37	VDDR	-	-	Rch Analog Power Supply pin	-
38-40	VSSR	-	-	Analog Ground pin	-
41-43	VSSL	-	-	Analog Ground pin	-
44-46	VDDL	-	-	Lch Analog Power Supply pin	-
47,48	AOUTLP	O	VDDL/VSSL	Lch Positive Analog Output pin	Connected to AOUTLN (300 kΩ)
49,50	AOUTLN	O	VDDL/VSSL	Lch Negative Analog Output pin	Connected to AOUTLP (300 kΩ)
51	VCML	O	VDDL/VSSL	Left channel Common Voltage pin, Normally connected to VREFLL with a 10μF electrolytic capacitor. This pin is inhibited to connect other devices.	Connected to VREFLL (5 kΩ)
52-54	VREFLL	I	VDDL/VSSL	Lch Low Level Voltage Reference Input pin	Connected to VCML (5 kΩ)
55-57	VREFHL	I	VDDL/VSSL	Lch High Level Voltage Reference Input pin	Hi-z
58	EXTR	I	VDDL/VSSL	External Resistor Connect pin Connect 33 kΩ (±0.1%) to AVSS	Hi-z
59	AVDD	-	-	Analog Power Supply pin, AVDD = DVDD to 3.6 V	-
60	AVSS	-	-	Analog Ground pin	-
61	MCLK	I	AVDD/AVSS	Master Clock Input pin	Hi-z
62	DVDD	-	-	Digital 1.8 V Power Supply pin	-
63	DVSS	-	-	Digital Ground pin	-
64	TVDD	-		Digital Power Supply pin, TVDD = DVDD to 3.6 V	-
Exposed Pad			-	Connect to AVSS	-

Note 1: All input pins except internal pull-up/down pins must not be left floating.

5.3. Handling of Unused Pin

Unused I/O pins must be connected appropriately.

Classification	Pin name	Status
Analog	AOUTLP, AOUTLN	Open
	AOUTRP, AOUTRN	Open
Digital	TESTE1, TESTE2	Connect to DVSS
	TST1 TST2 TST3	Connect to DVSS
	TSTO	Open

Pull - down pin List

Classification	Pin name	Status
pull-down pin (Typ = 100 kΩ)	TESTE1, TESTE2	Connect to DVSS

6. Absolute Maximum Ratings

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Digital I/O	TVDD	–0.3	4.0	V
	Digital Core	DVDD	–0.3	2.35	V
	Clock Interface	AVDD	–0.3	4.0	V
	Analog	VDDL/R	–0.3	6.0	V
	|AVSS - DVSS|	ΔGND	0	0.3	V
	|AVSS - VSSL|	ΔGND	0	0.3	V
	|AVSS - VSSR|	ΔGND	0	0.3	V
	|DVSS - VSSL|	ΔGND	0	0.3	V
	|DVSS - VSSR|	ΔGND	0	0.3	V
	|VSSL - VSSR| (Note 2)	ΔGND	0	0.3	V
Voltage Reference	"H" Voltage Reference (Note 4)	VREFHL/R	–0.3	VDDL/R+0.3 or 6.0	V
	"L" Voltage Reference	VREFLL/R	-0.3	+0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 4)		VIND	–0.3	TVDD+0.3 or 4.0	V
Ambient Temperature (Power Supplied)		Ta	–40	105	°C
Storage Temperature		Tstg	–65	150	°C

Note 2. All voltages with respect to ground.
Note 3. AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.
Connect the exposed pad on the bottom surface of the package to AVSS.
Note 4. Regarding VREFHL/R pins, maximum value which is lower value (VDDL/R + 0.3) or 6.0 V.
Note 5. Regarding Digital input pins, maximum value which is lower value (VDDL/R + 0.3) or 4.0 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS = DVSS = VSSL = VSSR = VREFLL = VREFLR = 0 V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital I/O	TVDD	DVDD	1.8	3.6	V
	Clock Interface	AVDD	DVDD	TVDD	3.6	V
	Digital Core	DVDD	1.7	1.8	1.98	V
	Analog	VDDL/R	4.75	5.0	5.25	V
Voltage Reference (Note 6Note 6)	"H" voltage reference	VREFHL/R	VDDL/R-0.5	-	VDDL/R	V
	"L" voltage reference	VREFLL/R	-	VSSL/R	-	V

Note 6. The analog output voltage scales with the voltage of (VREFHL/R-VREFLL/R).
Note 7. TVDD must be powered up before DVDD or at the same time.
Other than that, there are no restrictions on the order of power-up.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

8.1. Analog Characteristics

(Ta = 25 °C; AVDD = TVDD = 1.8 V, DVDD = 1.8 V, VREFHL/R = VDDL/R = 5.0 V, AVSS = DVSS = VSSL/R = VREFLL/R = 0 V; Sampling Frequency = MCLK = BCK = 11.2896 MHz, Measurement bandwidth = 20 Hz to 20 kHz; Signal Frequency = 1kHz; Input Signal is modulated by 3rd order sigma delta, bit length 6-bits; Input Signal Level=0.56 × FS = 0dBr; External Circuit: Figure 16; SC1, SC0 pins = "LL"; HLOAD pin = "L"; unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Dynamic Characteristics (Note 8)						
THD+N (Note 9)	BW = 20 kHz	0 dBr	-	–117	-	dB
		–60 dBr	-	–66	-	dB
	BW = 40 kHz	0dBr	-	–114	-	dB
		–60 dBr	-	–63	-	dB
	BW = 80 kHz	0 dBr	-	–113	-	dB
		–60 dBr	-	–60	-	dB
Dynamic Range (–60dBr with A-weighted)			-	129	-	dB
S/N (A-weighted)		Stereo mode	125	129	-	dB
		Mono mode (Note 10)	-	131	-	dB
Interchannel Isolation (1 kHz)			110	120	-	dB
DC Accuracy						
Output Voltage	0 dBr	Data Input Level = 0.56 × FS (Note 11)	±2.65	±2.8	±2.95	Vpp
	+2.5 dBr	Data Input Level = 0.75 × FS	-	±3.75	-	Vpp
Interchannel Gain Mismatch			-	0.1	0.3	dB
Gain Drift			-	20	-	ppm/°C
Load Resistance (Note 12)	HLOAD = "L"		8	10	-	kΩ
	HLOAD = "H"		120	-	-	Ω
Load Capacitance (Note 13)			-	-	25	pF

Note 8. Measured by Audio Precision APx555. Averaging mode.
And the AK4191 is used as the input source with DSMSEL[1:0] bits = "00", OBIT[1:0] bits = "01" and OSR bit = "0".

Note 9. Measured with AKM evaluation board

Note 10. This mode is shown in Figure 17.

Note 11. The analog output voltage with 0 dBFS input signal is calculated by the following formula.
AOUTL (typ.@0 dBr) = (AOUTL+) - (AOUTL-) = ±2.8 Vpp × (VREFHL - VREFLL) / 5.
AOUTR (typ.@0 dBr) = (AOUTR+) - (AOUTR-) = ±2.8 Vpp × (VREFHR - VREFLR) / 5.

Note 12. Regarding Load Resistance, AC load is 8kΩ (min) with a DC cut capacitor when the HLOAD pin = "L". DC load is 120Ω (min) without a DC cut capacitor if the HLOAD pin = "H". The load resistance value is with respect to ground. Analog characteristics are sensitive to capacitive load that is connected to the output pin. Therefore, the capacitive load must be minimized.

Note 13. It is recommended to use a resistor with 0.1% absolute error for the output stage of the adding circuit.

Power Supplies					
Parameter		**Min.**	**Typ.**	**Max.**	**Unit**
Power Supply Current					
Normal operation (PDN pin = “H”)					
	VDDL+VDDR	-	60	90	mA
	VREFHL+VREFHR	-	2	3	mA
	AVDD	-	1	1.5	mA
	TVDD	-	1	1.5	mA
	DVDD	-	4	6	mA
Total Idd per channel (HLOAD pin = “H”)		-	45	70	mA/ch
Power down (PDN pin = “L”) (Note) TVDD + AVDD + VDDL + VDDR + DVDD		-	10	100	μA

Note 14. In power down mode, all digital input pins including clock pins (MCLK and BCK pins) are held to DVSS.

8.2. DC Characteristics

(Ta = −40 to 105°C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V)

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
AVDD = TVDD = 1.7 to 3.0 V					
High-Level Input Voltage	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	20%TVDD	V
AVDD = TVDD = 3.0 V to 3.6V					
High-Level Input Voltage	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%TVDD	V
Input Leakage Current (Note)	Iin	-	-	±10	μA

Note 15. The TESTE1 and TESTE2 pins have internal pull-down devices. Therefore, the TESTE1 and TESTE2 pins are not included in this specification.

8.3. Switching Characteristics

(Ta = –40 to 105°C; VDDL/R = 4.75 to 5.25 V, AVDD = TVDD = 1.7 to 3.6 V, DVDD = 1.7 to 1.98 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Timing					
Frequency	fCLK	5	11.2896	13.824	MHz
Duty Cycle	dCLK	45	50	55	%
Minimum Pulse Width High	tCLKH	32	-	-	nsec
Minimum Pulse Width Low	tCLKL	32	-	-	nsec
BCK Timing					
Frequency	fBCK	5	11.2896	13.824	MHz
Duty Cycle	dBCK	45	50	55	%
Minimum Pulse Width High	tBCKH	32	-	-	nsec
Minimum Pulse Width Low	tBCKL	32	-	-	nsec
Multi bit Audio Interface Timing					
Mono mode (STME pin = "L")					
MBD7/6/5/4/3/2 Hold Time	tMBH	5	-	-	nsec
MBD7/6/5/4/3/2 Setup Time	tMBS	5	-	-	nsec
Stereo mode (STME pin = "H")					
BCK Edge to MBD7/6/5/4/3/2	tBMD	–5	-	5	nsec
Power down & Reset Timing (Note)					
PDN Accept Pulse Width	tAPD	600	-	-	nsec
PDN Reject Pulse Width	tRPD	-	-	30	nsec

Note 16. The AK4498EX should be reset by bringing the PDN pin "L" upon power up.

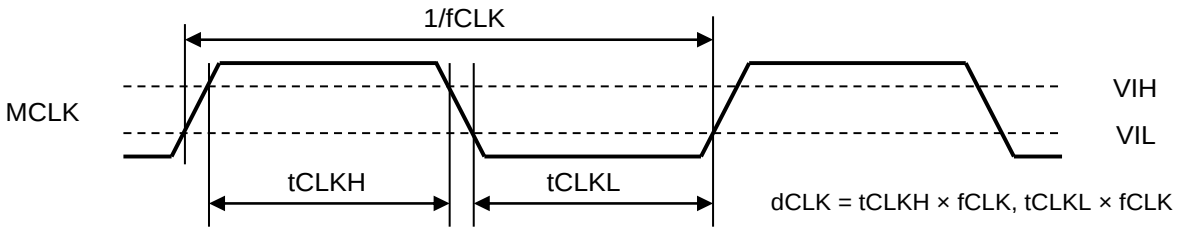


Figure 3. Clock Timing

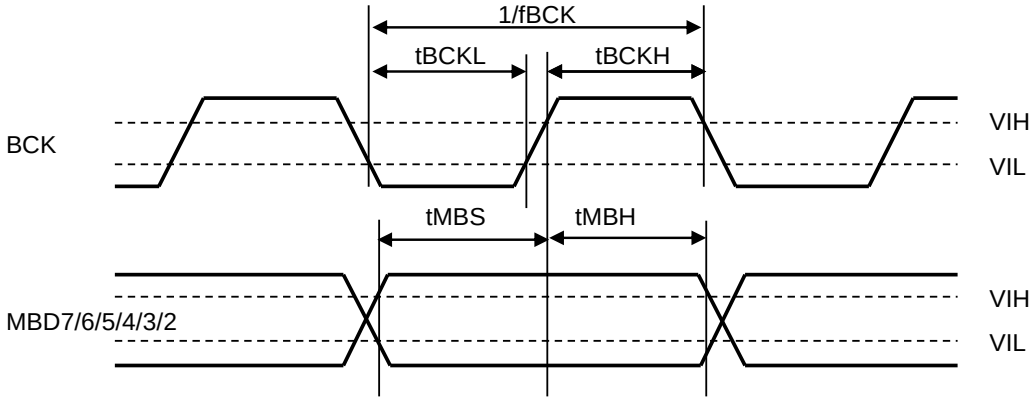


Figure 4. Audio Interface Timing (STME pin = "L")

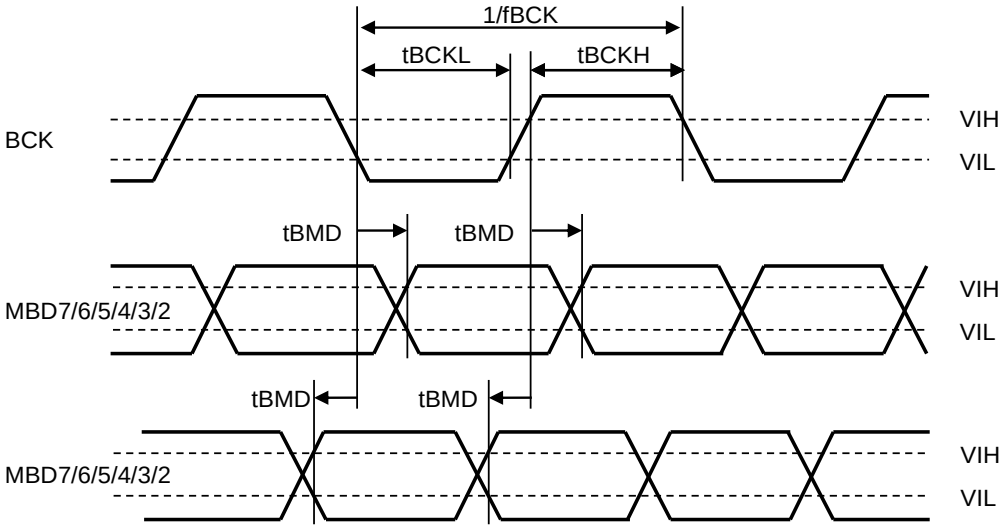


Figure 5. Audio Interface Timing (STME pin = “H”)

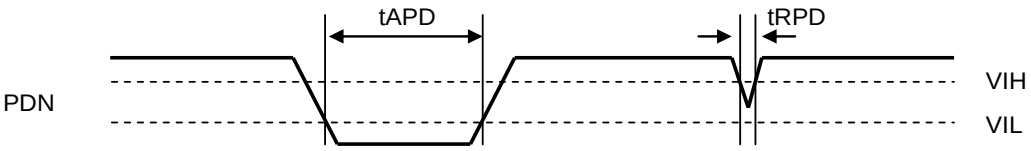


Figure 6. Power Down & Reset Timing

9. Functional Descriptions

9.1. System Clock

The external clocks, which are required to operate the AK4498EX, are MCLK and BCK. The BCK and MCLK must be the same frequency, but the phase is not critical. The MCLK is used to operate SCF. The frequency of operating SCF is same as MCLK.

The AK4498EX is automatically placed in standby state when MCLK is stopped for more than 1μsec during a normal operation (PDN pin = “H”), and the analog output becomes Hi-z state. When MCLK is input again, the AK4498EX exits standby state and starts operation. The AK4498EX is in power down mode until MCLK and BCK are supplied and the analog output is floating state when power down is released (PDN pin = “L” → “H”).

9.2. Audio Inerface Format

9.2.1. Multi Bit Mono Interface mode

By setting the STME pin = “L” the AK4498EX receives one channel audio data. D0[7:2], D1[7:2], D2[7:2] and D3[7:2] are one channel data. Data must be input to the MBD7/6/5/4/3/2 pins, respectively by synchronizing to BCK.

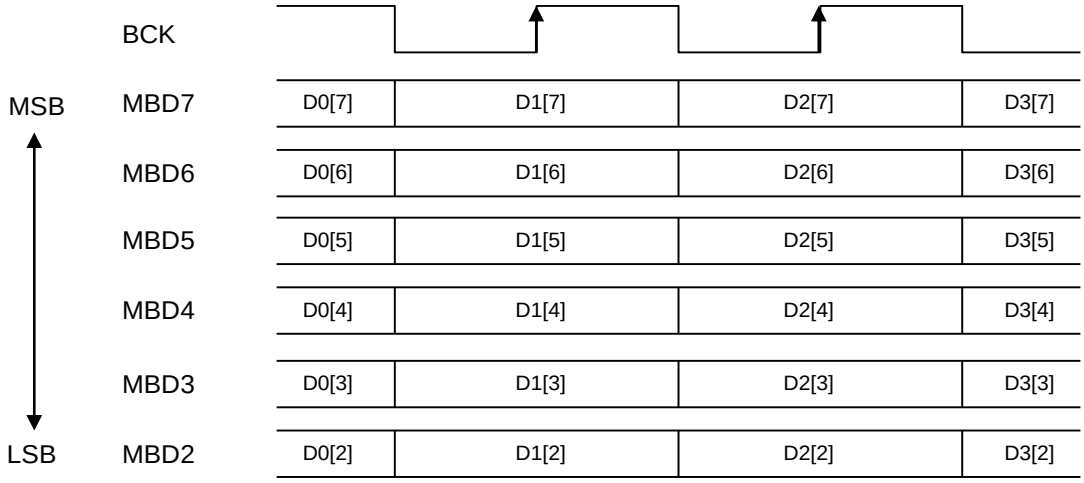


Figure 7. Multi Bit Mono Interface mode

9.2.2. Multi Bit Stereo Interface mode

By setting the STME pin = “H” the AK4498EX receives stereo audio data. R0[7:2], L1[7:2], R1[7:2], L2[7:2], R2[7:2] and L3[7:2] are stereo data. Data must be input to the MBD7/6/5/4/3/2 pins, respectively by synchronizing to BCK.

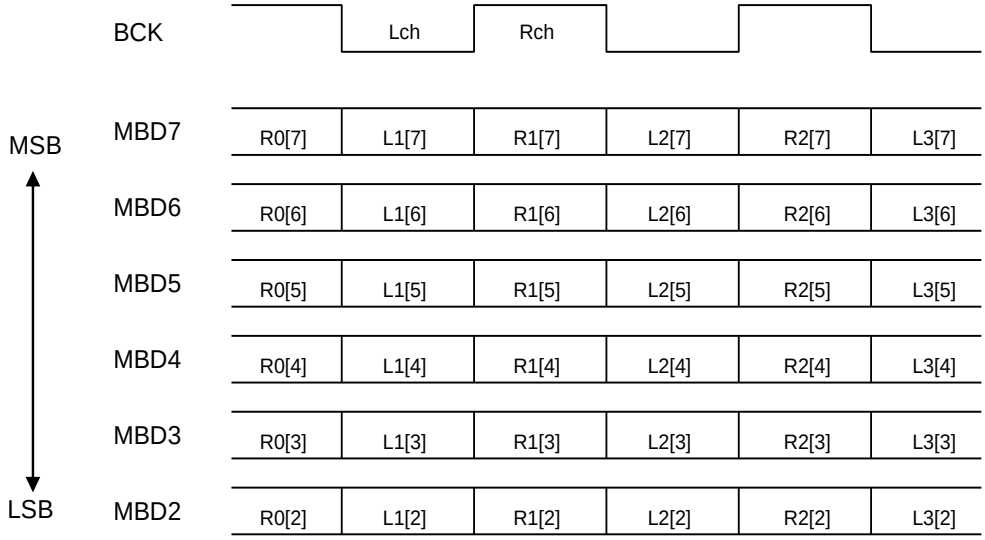


Figure 8. Multi Bit Stereo Interface mode

9.3. Output Signal Select

Input and output combination of the AK4498EX can be changed by LSELN pin and RSELN pin (Table 1). These functions are available on Multibit Stereo Interface audio format (STME pin = “H”).

Table 1. Output Signal Selection

LSELN	RSELN	AOUTLP/N Output	AOUTRP/N Output
L	L	Lch Input	Rch Input
L	H	Lch Input	Lch Input
H	L	Rch Input	Rch Input
H	H	Rch Input	Lch Input

9.4. Phase Inversion Function

The output signal phase can be inverted by INVL pin and INVR pin. (Table 2) These functions are available on all audio formats and are controlled in Audio Interface.

Table 2. Phase Inversion Function

INVL	INVR	AOUTLP/N Output	AOUTRP/N Output
L	L	Normal	Normal
L	H	Normal	Invert
H	L	Invert	Normal
H	H	Invert	Invert

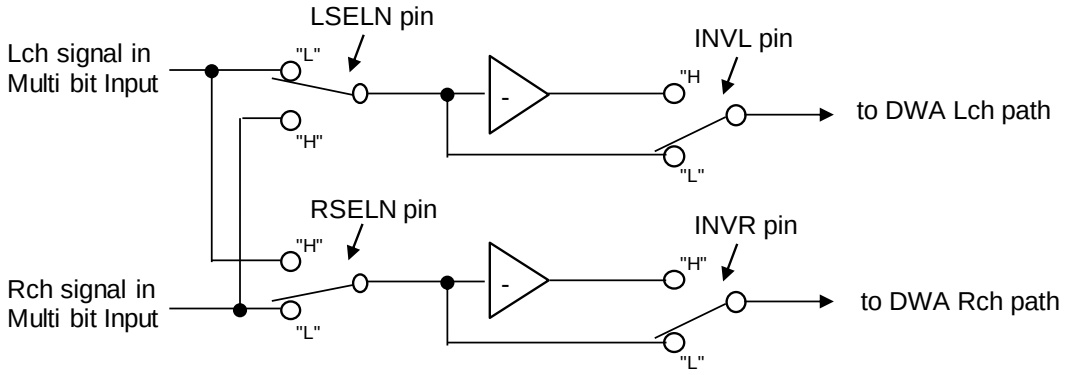


Figure 9. Output Signal Select and Phase Inversion Block Diagram

9.5. Sound Quality Selection

Sound quality selection of the AK4498EX can be selected by SC0 pin and SC1 pin. The analog characteristics specification of the AK4498EX is applicable to Setting 1 and Setting 3.

Table 3. Sound Quality select mode

SC0	Internal Operation
L	Analog internal current, normal (setting 1)
H	Analog internal current, minimum (setting 2)

Table 4. Sound Quality select mode

SC1	Sound
L	Measurement Mode (setting 3)
H	High Sound Quality Mode (setting 4)

9.6. Over Current Protection for Analog Output Pins

The AK4498EX has channel independent over current detection function for analog output pins (AOUTLP/LN and AOUTRP/RN pins). This function limits the current not to exceed approximately 120 mA when an excessive current over about 120 mA (min) is detected. This function is invalid when the PDN pin = “L” or when the MCLK is stopped.

9.7. Power Up/Down Function

The AK4498EX is powered down when the PDN pin is “L”. In power down state, all circuits stop operation and initialized, and the analog output becomes floating (Hi-z) state. The PDN pin must held “L” for more than 600 nsec for a certain reset after all power supplies are on. There is a possibility of malfunctions with the “L” pulse less than 600 nsec. Power down is released by setting the PDN pin to “H” from “L”. In this time IREF-block is powered up.

All circuits will be powered up by inputting MCLK and BCK clocks after the PDN pin = “H”. The analog circuit starts operation just after supplying MCLK and the digital circuit starts operation about 1024 MCLK cycle after supplying all necessary clocks (MCLK and BCK). Figure 10 shows system timing example of power down/up. TVDD must be powered up before or at the same time as the DVDD.

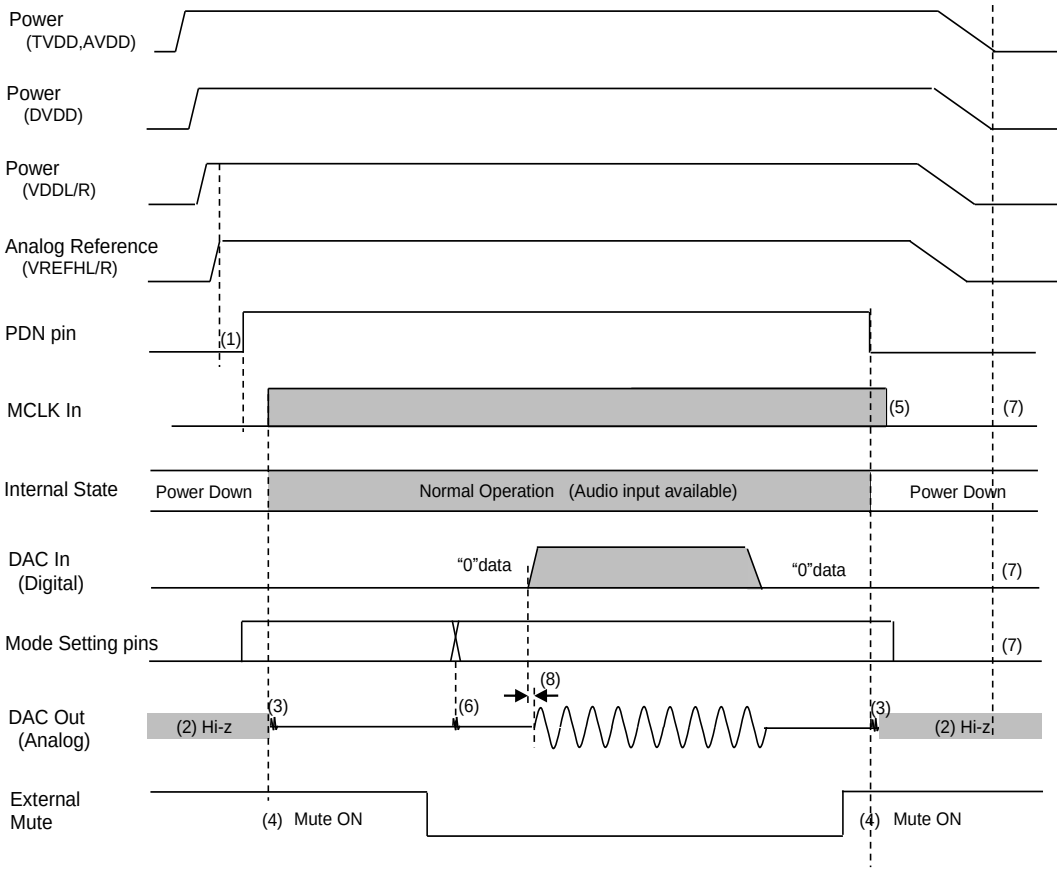


Figure 10. Power down/up sequence example

Notes:

(1) The PDN pin must be “L” when start supplying AVDD, TVDD and VDDL/R. It must be held “L” for more than 600ns after supplying AVDD, TVDD, VDDL/R and VREFHL/R reached 90%.
(2) Analog outputs are floating (Hi-z) in power down mode.
(3) Click noise occurs at the switching point of internal state. This noise is output even if “0” data is input.
(4) Mute the analog output externally if click noise (3) adversely affect system performance.
(5) Clock inputs (MCLK and BCK) can be stopped in power down state.
(6) Click noise occurs at the edge of mode setting signals (STME, INVL, INVR, SC1, SC0 and HLOAD pins) This noise is output even if “0” data is input.
(7) All clocks, data and mode setting signals must be “L” until after the power supplies are turned on.
(8) It takes about 7MCLK cycles to output the analog signal corresponding to the digital input.

9.8. Power Down, Standby and Mute Function

Standby and Mute function of the AK4498EX are controlled by MUTEN pin and MCLK. (Table 5)

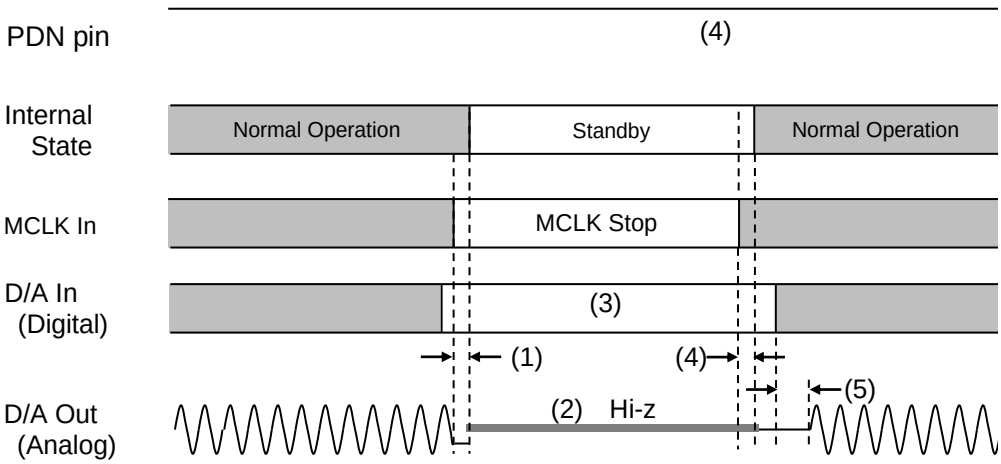
Table 5. Power Down, Standby and MUTE function

Mode	PDN pin	MCLK Input	MUTEN pin	Audio Interface, DWA	SCF	AOUTLP/N, AOUTRP/N status
Power Down	L	-	-	OFF	OFF	Hi-Z
Standby (MCLK Stop)	H	Not Required	-	OFF	OFF	Hi-Z
Mute	H	Required	L	OFF	ON	VCML/R
Normal Operation	H	Required	H	ON	ON	Signal output

- means “Do not care”

9.8.1. Standby by stopping MCLK

The AK4498EX detects a clock stop and all circuits except MCLK stop detection circuit, bias generation circuit stops operation if MCLK is not input for 1μsec (min.) during operation (PDN pin = “H”). In this standby mode, the analog output goes floating state (Hi-Z). The AK4498EX returns to normal operation after starting to supply MCLK again.



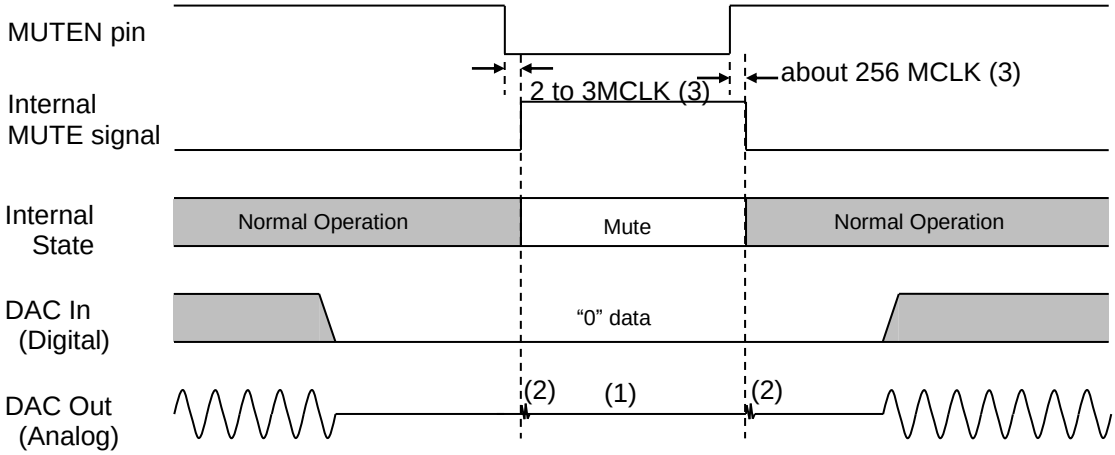
Notes:

(1) The AK4498EX detects MCLK stop and becomes standby state when MCLK edge is not detected for 1 μsec (min.) during operation.
(2) The analog output goes to floating state (Hi-z).
(3) Click noise can be reduced by inputting “0” data when stopping and resuming MCLK supply.
(4) Resume MCLK input to release the Standby state by MCLK. In this case, power up sequence by the PDN pin is not necessary.
(5) The analog output corresponding to the digital input has group delay of approximately 7MCLK cycles.

Figure 11. Standby by stopping MCLK

9.8.2. Mute Function

Audio Interface and DWA are reset by setting MUTEN pin to “L”. In this case, the analog output becomes VCML/R voltage. Figure 12 shows Mute sequence by MUTEN pin.



Notes:

(1) The analog output is VCML/R voltage when MUTEN pin = “L”.
(2) Click noise occurs at the edge of MUTEN pin. This noise is output even if “0” data is input.
(3) It takes 2 to 3 MCLK cycle until the internal MUTE signal is changed when changing MUTEN pin to “L” and it takes about 256 MCLK cycle when changing MUTEN pin to “H”.

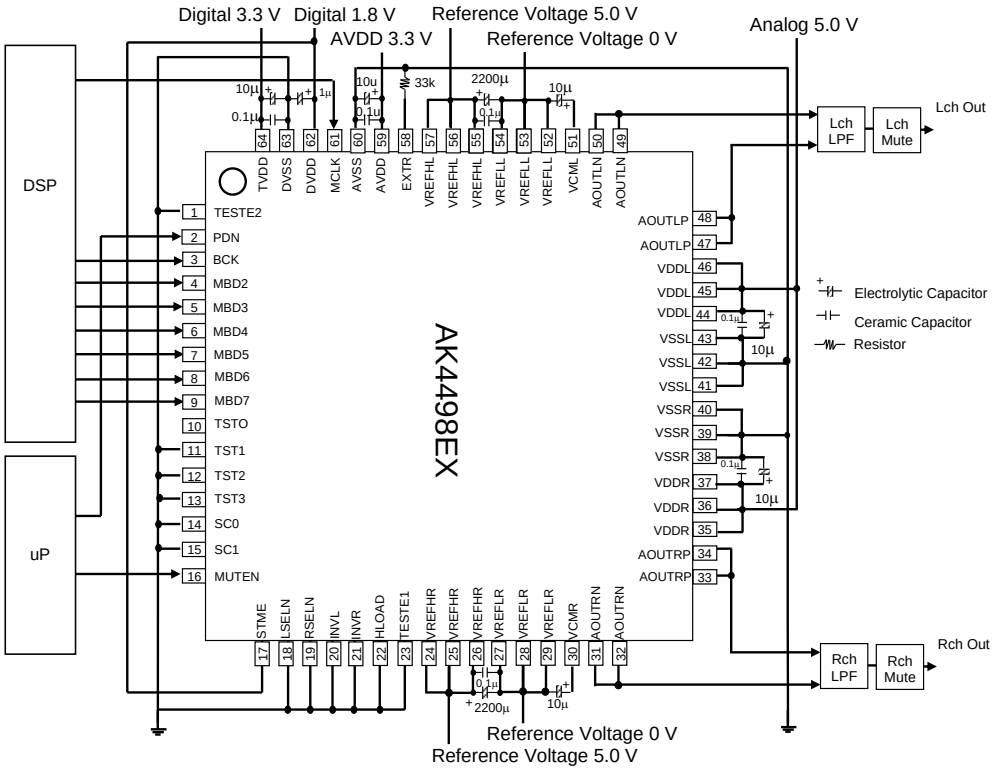
Figure 12. Mute function

9.9. Analog Output Heavy Load Drive

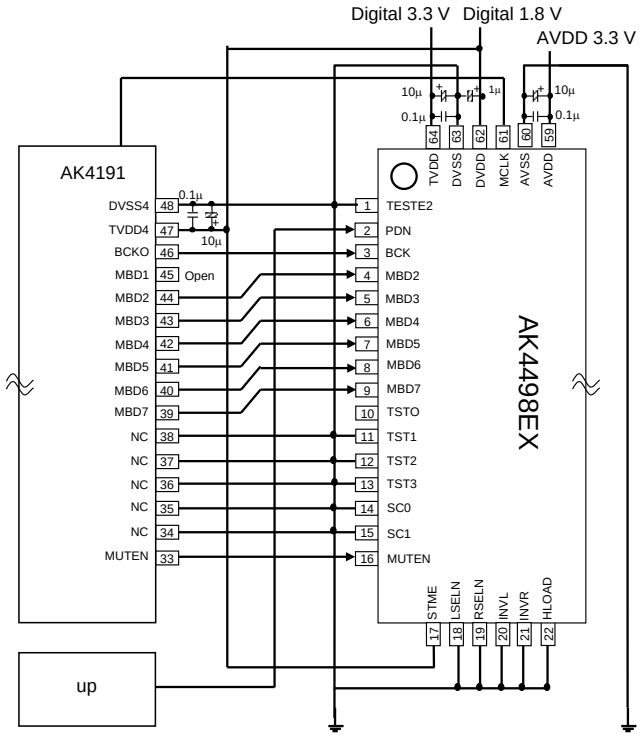
When HLOAD Pin = “H” at Pin Control mode, analog output pins AOUTLP/LN and AOUTRP/RN can drive 120ohm (min.) load resistance (referenced to ground), thus suppressing S/N ratio degradation due to thermal noise from external circuits. See Note 12, Figure 14 and Figure 15.

10. Recommended External Circuits

[1] Example of a system without using AK4191 (DSP + AK4498EX)



[2] Example of a system with using AK4191 (AK4191 + AK4498EX)



Notes:
- Power lines of AVDD, TVDD, VDDL and VDDR should be distributed separately from the point with low impedance of regulator etc.
- AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane. (Analog ground should have low impedance as a solid pattern. THD+N characteristics will degrade if there are impedances between each VSS.)
- It is recommended to connect a damping resistor if THD+N characteristics degrade by high frequency noise of MCLK.
- All input pins except pull-down pins should not be allowed to float.
- AK4498EX's MBD7-2 pins should be connected 1:1 to AK4191's MBD7-2 pins as shown in the figure above. When AK4498EX is used in combination with AK4191, AK4191's MBD1 pin should be open.

Figure 13. Typical Connection Diagram
(AVDD = TVDD = 3.3 V, VDDL/R = 5.0 V, DVDD = 1.8 V)

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD, TVDD, DVDD, VDDL and VDDR. Decoupling capacitors for high frequency should be placed as near as possible to the AK4498EX.
AVDD and VDDL/R are supplied from analog supply in system, and TVDD and DVDD are supplied from digital supply in system. Power lines of VDDL/R should be distributed separately from the point with low impedance of regulators or other parts.

AVSS, DVSS, VSSL and VSSR must be connected to the same analog ground plane.

2. Reference Voltage

The differential voltage between VREFHL and VREFLL, and VREFHR and VREFLR set the full-scale of the analog output range. The VREFHL/R pin is normally connected to the 5.0 V reference voltage, and the VREFLL/R pin is normally connected to the 0 V reference voltage. Connect a 0.1 μF ceramic capacitor and 2200 μF (min. value depends upon power supply quality) electrolytic capacitor between VREFHL and VREFLL, and VREFHR and VREFLR. Especially the ceramic capacitors should be connected as near as possible to the pin.
The VREFHL, VREFHR, VREFLL and VREFLR pins should avoid noises from other power supplies. Connect the VREFHL/R pin to the analog 5.0 V via a 10 Ω resistor, and the VREFLL/R pin to the analog ground via a 10 Ω resistor when it is difficult to obtain expected analog characteristics because of noises from other power supplies (A low-pass filter of fc = 3.6 Hz will be composed with the 2200 μF capacitor and a 10Ω resistor. It removes signal frequency noise from other power supply lines.) No load current may be drawn from the VCML/R pin since VCML/R is a common voltage of analog signals. All digital signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted coupling into the AK4498EX.

3. Analog Output

The analog outputs are full differential outputs. The differential outputs are summed externally, V_{AOUT} = (AOUT+) – (AOUT-) between AOUTLP/RP and AOUTLN/RN. When the input signal range via MBD7/6/5/4/3/2 pins is 0.56 × full scale and VREFHL/R – VREFLL/R = 5V, the output range is 2.8 Vpp (typ.) centered around VCML and VCMR voltages. In this case, the output range after summing will be 5.6 V (typ.). The bias voltage of the external summing circuit is supplied externally.

The input data format is 2's complement. The output voltage (V_{AOUT}) is at positive full-scale for 1FH (@6 bits) and at negative full-scale for 20H (@6 bits). The ideal V_{AOUT} is 0 V for 00H (@6 bits).
The internal switched-capacitor-filters attenuate the noise beyond the audio passband.
Figure 14 and Figure 15 show examples of external LPF circuit summing the differential outputs by a single op-amp. Figure 16 shows an example of external LPF with two op-amps and differential output circuits. Figure 17 shows an example of external LPF with two op-amps and the circuit when setting STME pin = “L”. A resistor that has 0.1 % or less absolute error must be used for external LPFs.

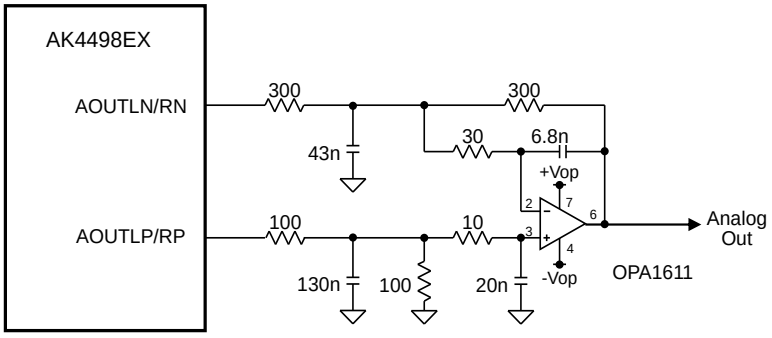


Figure 14. External LPF Circuit Example 1 when HLOAD PIN = “H” (fc = 98 kHz (Typ), Q = 0.667 (Typ))

Table 6. Frequency Response of External LPF Circuit Example 1

Gain (1 kHz, Typ)		0 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	–0.07 dB
	40 kHz	–0.32 dB
	80 kHz	–2.13 dB

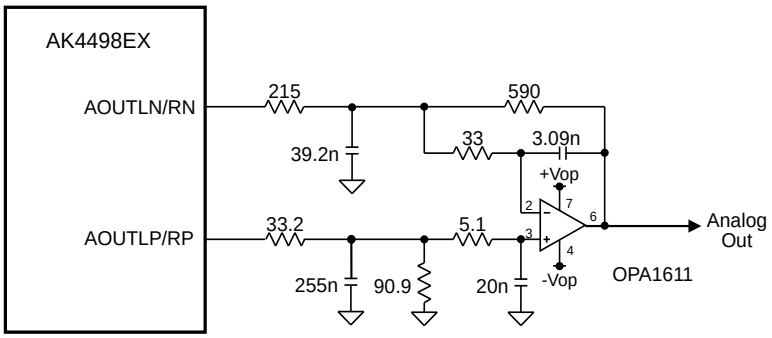


Figure 15. External LPF Circuit Example 2 when HLOAD PIN = “H” (fc = 104 kHz (Typ), Q = 0.693 (Typ))

Table 7. Frequency Response of External LPF Circuit Example 2

Gain (1 kHz, Typ)		+8.78 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	–0.02 dB
	40 kHz	–0.15 dB
	80 kHz	–1.46 dB

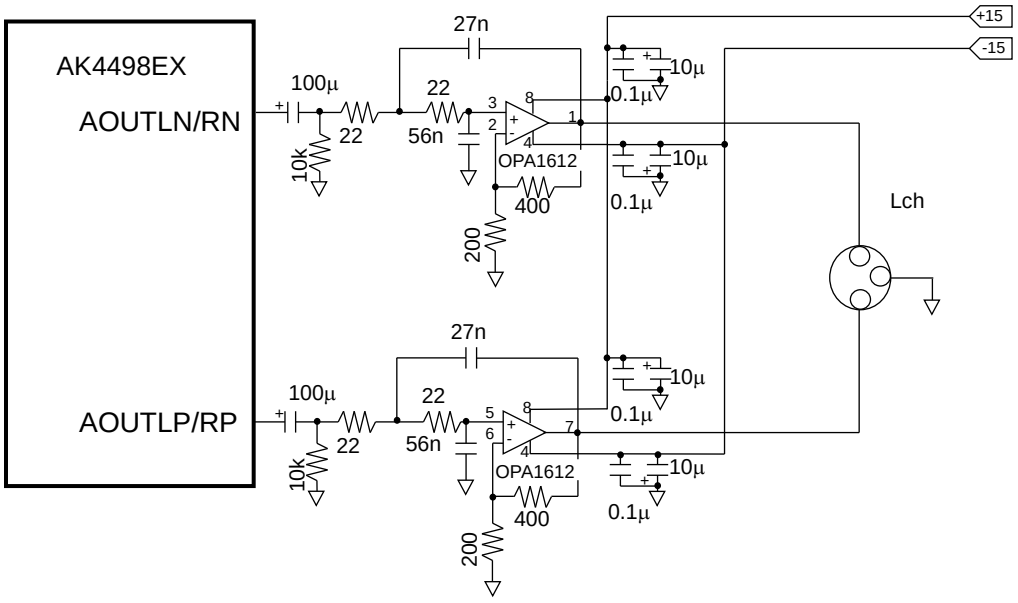


Figure 16. External LPF Circuit Example 3 (fc = 186 kHz (Typ), Q = 0.67 (Typ))

Table 8. Frequency Response of External LPF Circuit Example 3

Gain (1 kHz, Typ)		+9.54 dB
Frequency Response (ref:1 kHz, Typ)	20 kHz	–0.01 dB
	40 kHz	–0.06 dB
	80 kHz	–0.32 dB

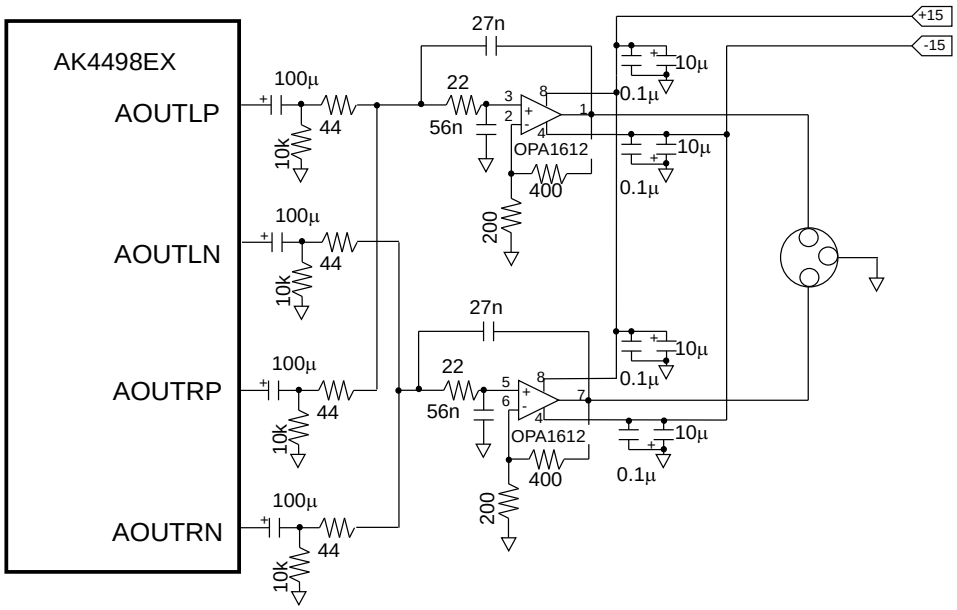
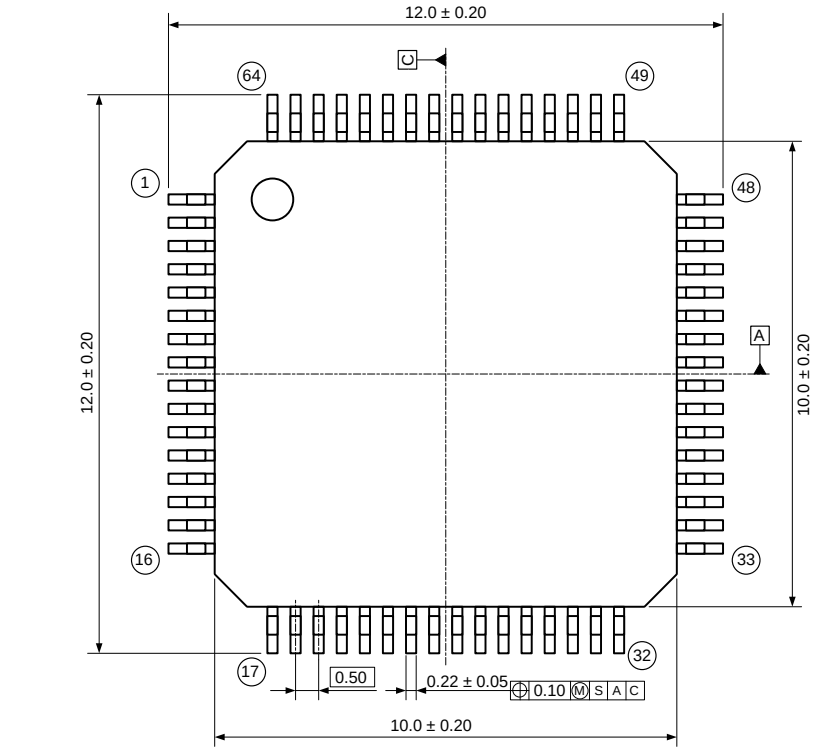
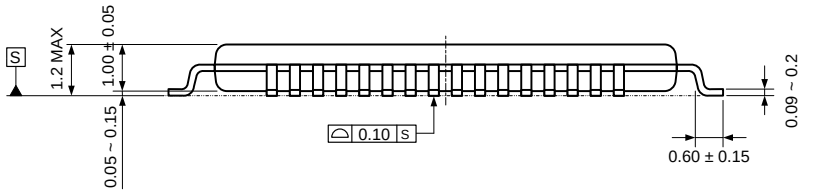


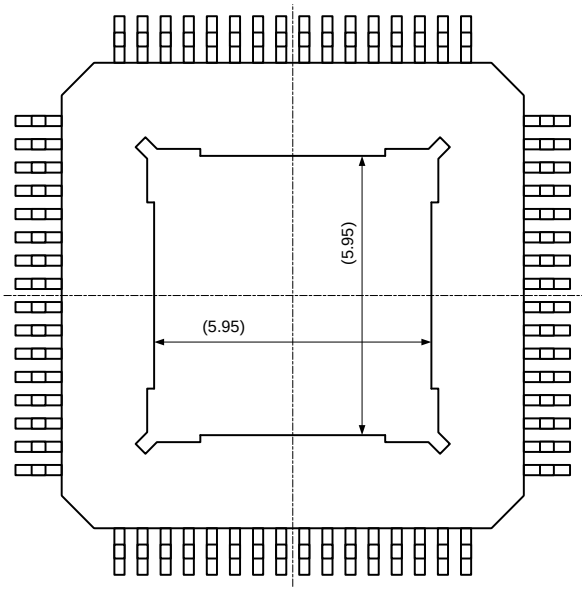
Figure 17. External LPF Circuit Example for mono mode (fc = 186 kHz (Typ), Q = 0.67 (Typ))

11. Package

11.1. Outline Dimensions (64-pin HTQFP10×10, Unit : mm)







11.2. Material & Terminal Finish

Package molding compound: Epoxy, Halogen (Br and Cl) free
Lead frame material: EFTEC-64T
Terminal Surface treatment: Solder (Pb free) plate

11.3. Marking

1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK4498EXVQ
4) Asahi Kasei Logo

12. Ordering Guide

AK4498EXVQ	−40 to +105°C	64-pin HTQFP (0.5 mm pitch)
AKD4498EX	Evaluation Board for AK4498EX	

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