Agilex™ 3 FPGAs and SoCs C-Series Product Table

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Version 2025.03.12

	Product Line	A3C025[1]	A3C050	A3C065	A3C100	A3C135
Resources	Specification Options[2]	Y, Z	Y, Z	Y, Z	W, Y, Z	W, Y, Z
	Logic elements (LEs)	25,075	47,200	65,490	100,300	135,110
	Adaptive logic modules (ALMs)	8,500	16,000	22,200	34,000	45,800
	ALM registers	34,000	64,000	88,800	136,000	183,200
	M20K memory blocks	65	123	169	262	353
	M20K memory size (Mb)	1.27	2.40	3.30	5.12	6.89
	MLAB memory count	450	800	1,050	2,000	2,300
	MLAB memory size (Mb)	0.27	0.49	0.64	1.22	1.40
	I/O PLL	2	2	2	4	4
	Fabric-feeding IOPLL[3]	5	5	5	8	8
	Variable-precision digital signal processing (DSP) blocks	34	65	88	138	184
	18 x 19 multipliers	68	130	176	276	368
	Peak INT8 (TOPS)	0.47	0.90	1.21	1.90	2.54
Maximum Available Device Resources	LVDS pairs at 1.25 Gbps	48	48	48	96	96
	LPDDR4 interfaces (x32)	0	1	1	2	2
	MIPI D-PHY interface	0	7	7	14	14
	Differential (RX or TX) pairs at 12.5 Gbps	0	0	0	4	4
	PCIe* 3.0 x4 instance	0	0	0	1	1
	High-speed I/O (HSIO)	96	96	96	192	192
	High-voltage I/O (HVIO)	160	160	160	200	200
	Secure Device Manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, and physical anti-tamper support				
	Hard processor system (HPS)	NA			Multi-core with 32-bit/64-bit dual-core Arm Cortex*-A55 processor up to 800 MHz with 32 KB I/D cache and 128 KB L2 cache, and up to 2 MB L3 cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, oscillator timer x2, SP timer x2, watchdog x5, and GPIO x2.	
	Transceiver	NA			PCIe hard IP up to PCIe 3.0 x4 endpoint (EP) and root port (RP) Transceiver channel count: up to 4 channels at 12.5 Gbps (NRZ) Ethernet IP: up to 4 x10 GbE hard IP (MAC, PCS, and FEC)	

Notes:
1. A3C025 does not support EMIF and MIPI.
2. Specification code definition:

Code	HPS	Crypto	EMIF, MIPI, PUF, SPDM Attestation
W	Yes	Yes	Yes
Y	No	No	Yes
Z	No	No	No

EMIF: External Memory Interface
MIPI: Mobile Industry Processor Interface
PUF: Physical Unclonable Function
SPDM: Security Protocal and Data Model

3. The fabric-feeding IOPLL count including system PLL at the transceiver bank. The system PLL can be repurposed for core fabric usage if not used for the transceiver.

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Product Line	A3C025[4]	A3C050	A3C065	A3C100	A3C135
Package Options[5] and I/O Pins					
Package Size, Ball Pitch	**HVIO/HSIO[6]/HPSIO/Transceiver**				
M12A (12 mm x 12 mm, 0.5 mm[7])	160/72/0/0	160/72/0/0	160/72/0/0		
M16A (16 mm x 16 mm, 0.5 mm[7])				40/192/48/4	40/192/48/4
B18A[8] (18 mm x 18 mm, variable[9, 10])	160/48/0/0	160/48/0/0	160/48/0/0	160/48/0/0	160/48/0/0
B18B (18 mm x 18 mm, variable[9, 10])	160/96/0/0	160/96/0/0	160/96/0/0		
B23C (23 mm x 23 mm, variable[9, 10])				200/144/48/4	200/144/48/4

Notes:
4. A3C025 does not support EMIF and MIPI.
5. For more information about the device migration path, please refer to Device Migration Guidelines: Agilex™ 3 FPGAs and SoCs.
6. The number of LVDS pairs is half of the HSIO count.
7. 0.5mm Micro Fineline BGA (MBGA).
8. B18A only supports specification Y & Z.
9. VPBGA packaging is compatible with Type III PCBs that use design rules equivalent to 0.8 mm ball pitch packages and standard plated through hole (PTH) vias.
10. The ball pitch is variable and it helps to ease signal routing. Please contact your local sales representative for more details about Variable Pitch BGA (VPBGA) technology.
11. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.