

REV	DATE	PAGES	DESCRIPTION
1.0	01/08/2025	ALL	INITIAL RELEASE
2.0	03/12/2025	ALL	FGI RELEASE
-	-	-	-

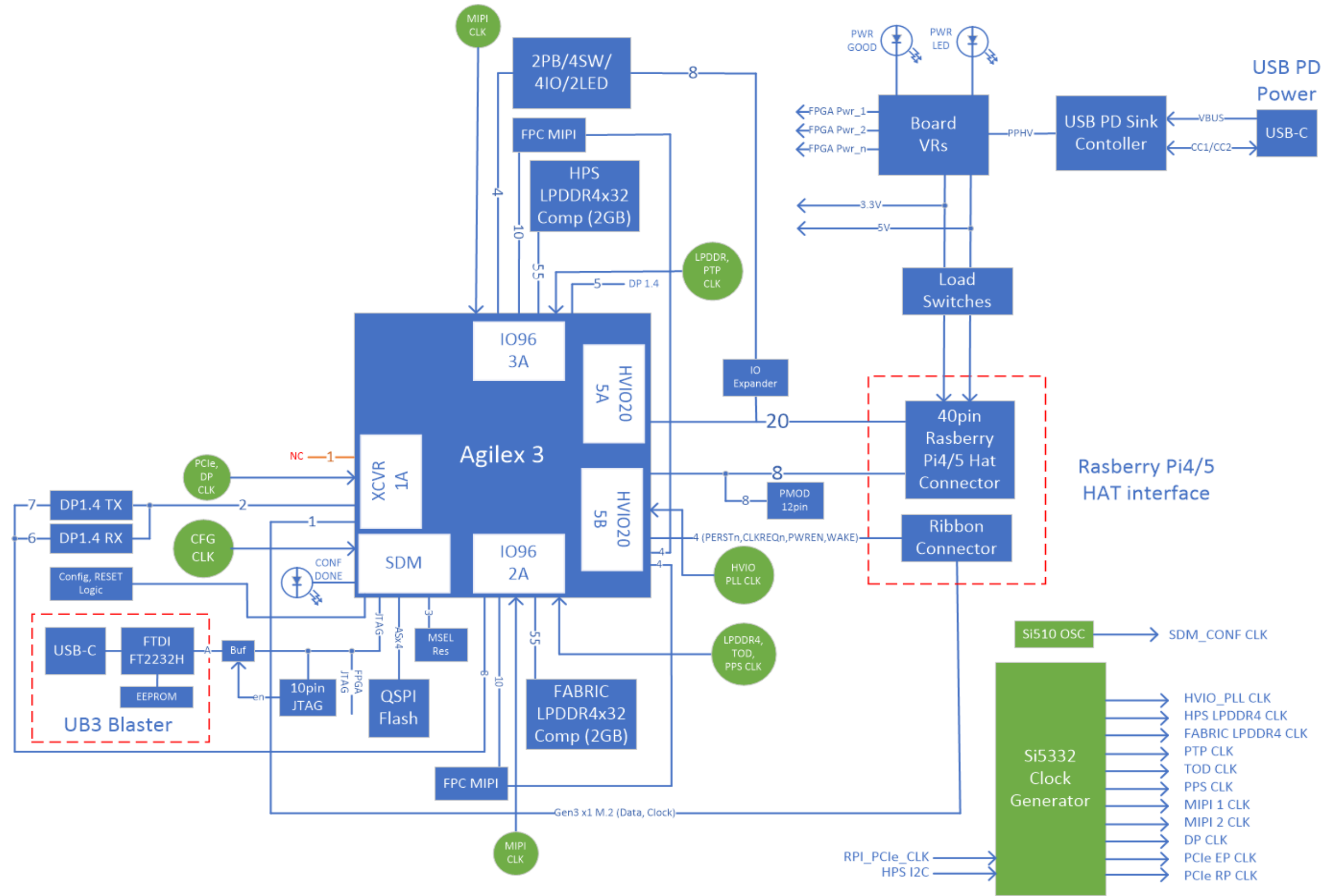
AGILEX .3 FPGA C-SERIES DEVELOPMENT KIT BOARD

	AGILEX .3 FPGA C-SERIES DEVELOPMENT KIT	AGILEX .3 FPGA AND SOC C-SERIES DEVELOPMENT KIT
MMID	99D62P	99D006
OPN	DK-A3Y135BM16AEA	DK-A3W135BM16AEA
DEVICE PN	A3CY135BM16AE6S	A3CW135BM16AE6S
DEVICE MMID	99D5C8	99D5C2
TA	N72223-002	N72225-002
PCBA	N72224-200	N72226-200
PB	N71086-200	N71086-200

Thu May 22 01:35:26 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 1 OF 65	

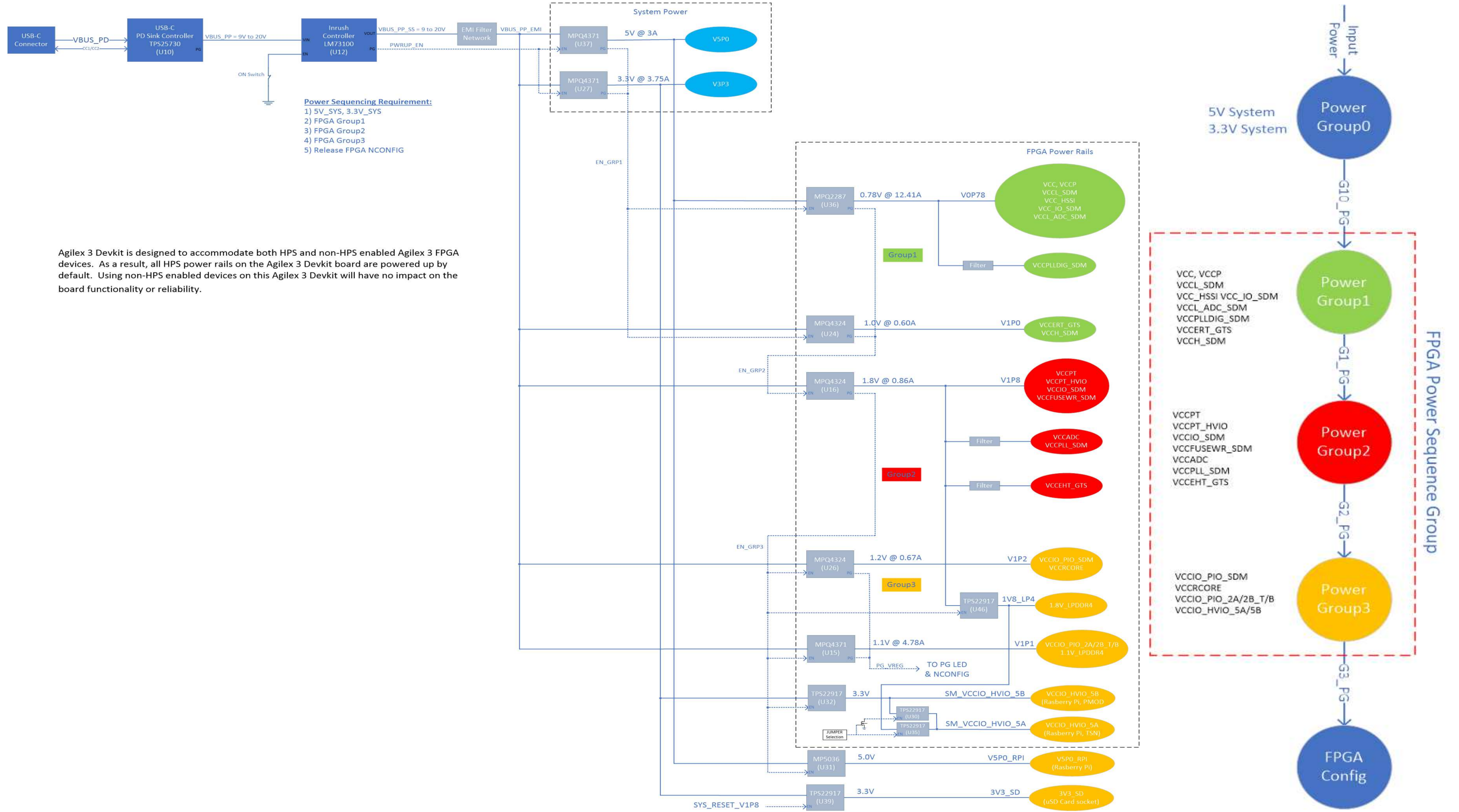
MAIN BLOCK DIAGRAM



Thu May 22 01:34:27 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE	CODE	DOCUMENT NUMBER	REV
		B	34649	305-PD-25-0242	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 3 OF 65	

POWER BLOCK DIAGRAM

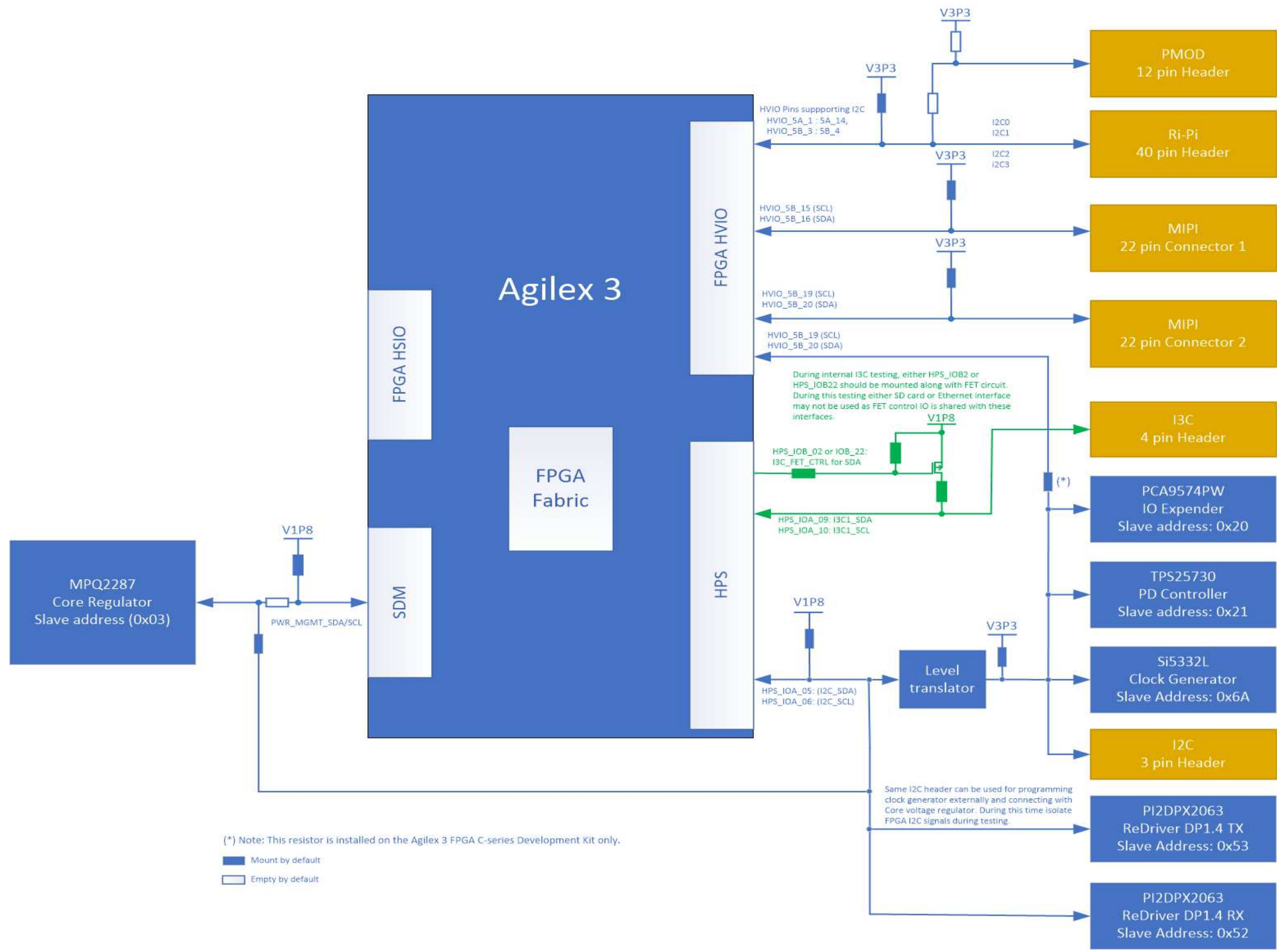


Agilex 3 Devkit is designed to accommodate both HPS and non-HPS enabled Agilex 3 FPGA devices. As a result, all HPS power rails on the Agilex 3 Devkit board are powered up by default. Using non-HPS enabled devices on this Agilex 3 Devkit will have no impact on the board functionality or reliability.

Thu May 22 01:27:52 2025

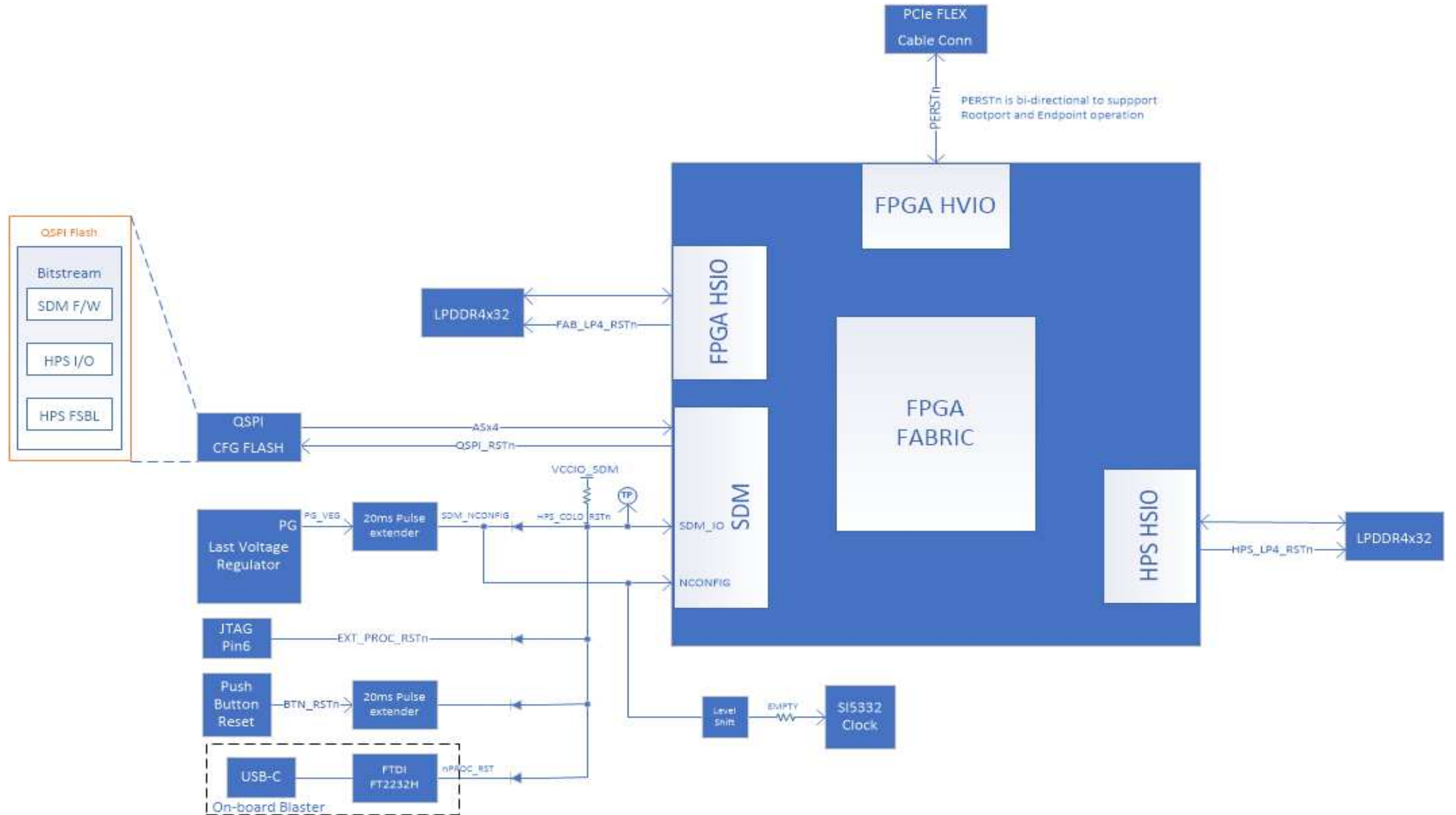
DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 4 OF 65	

I2C BLOCK DIAGRAM



Thu May 22 01:27:53 2025

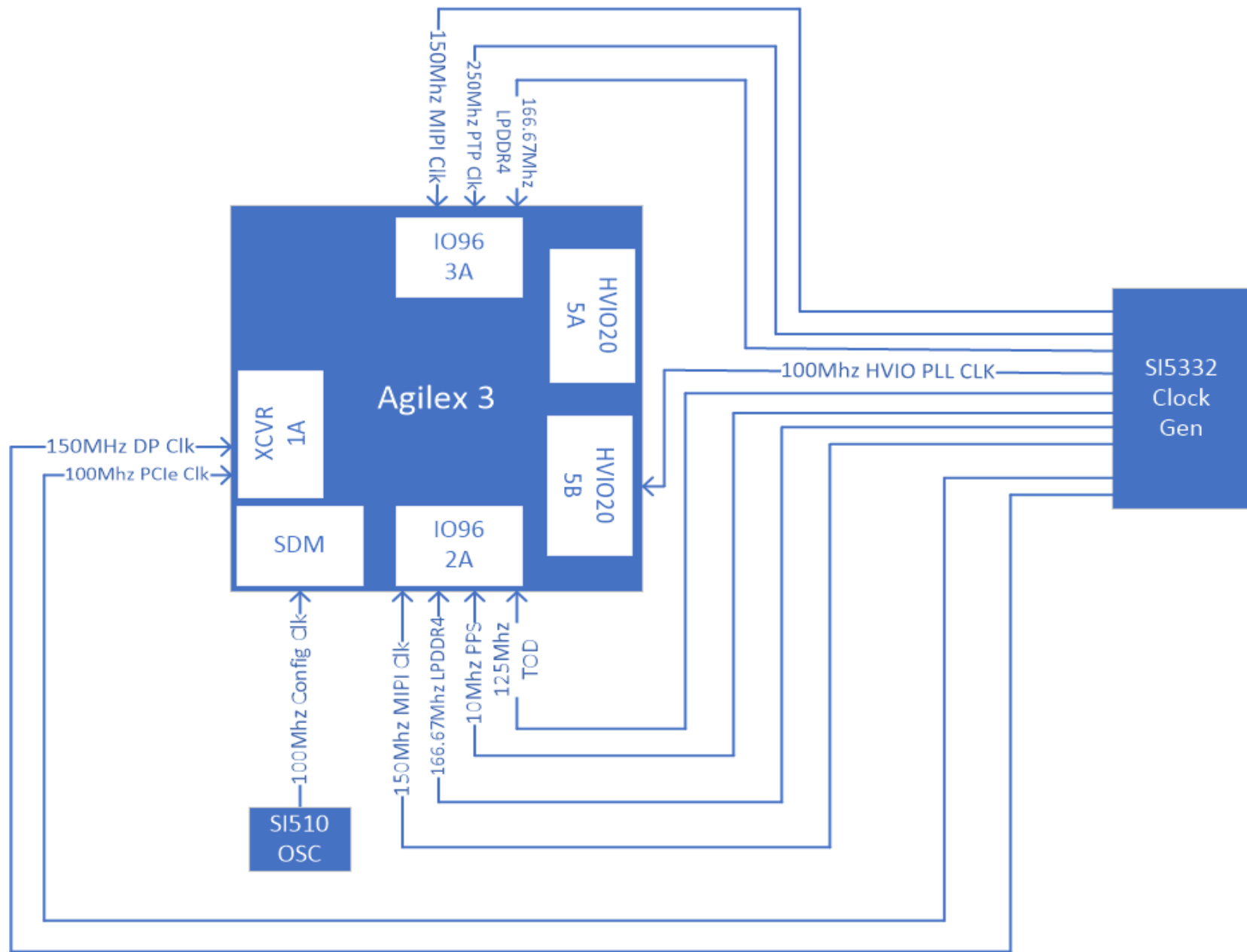
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SCALE:		DO NOT SCALE DRAWING		SHEET 5 OF 65	



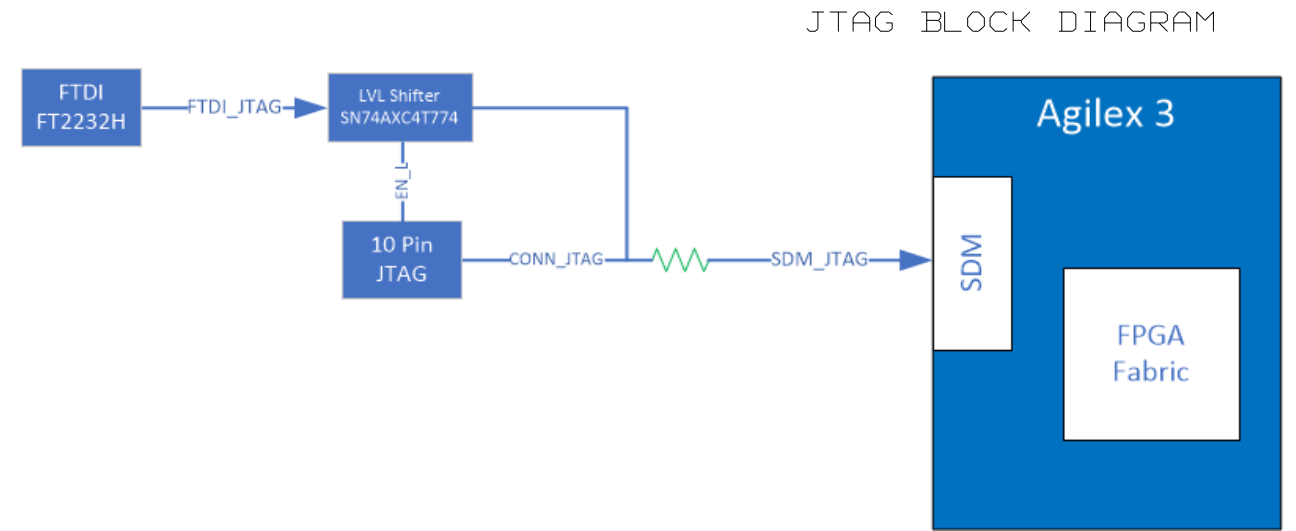
Thu May 22 01:27:53 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 6 OF 65	

CLOCK BLOCK DIAGRAM



CLOCK & JTAG BLOCK DIAGRAM



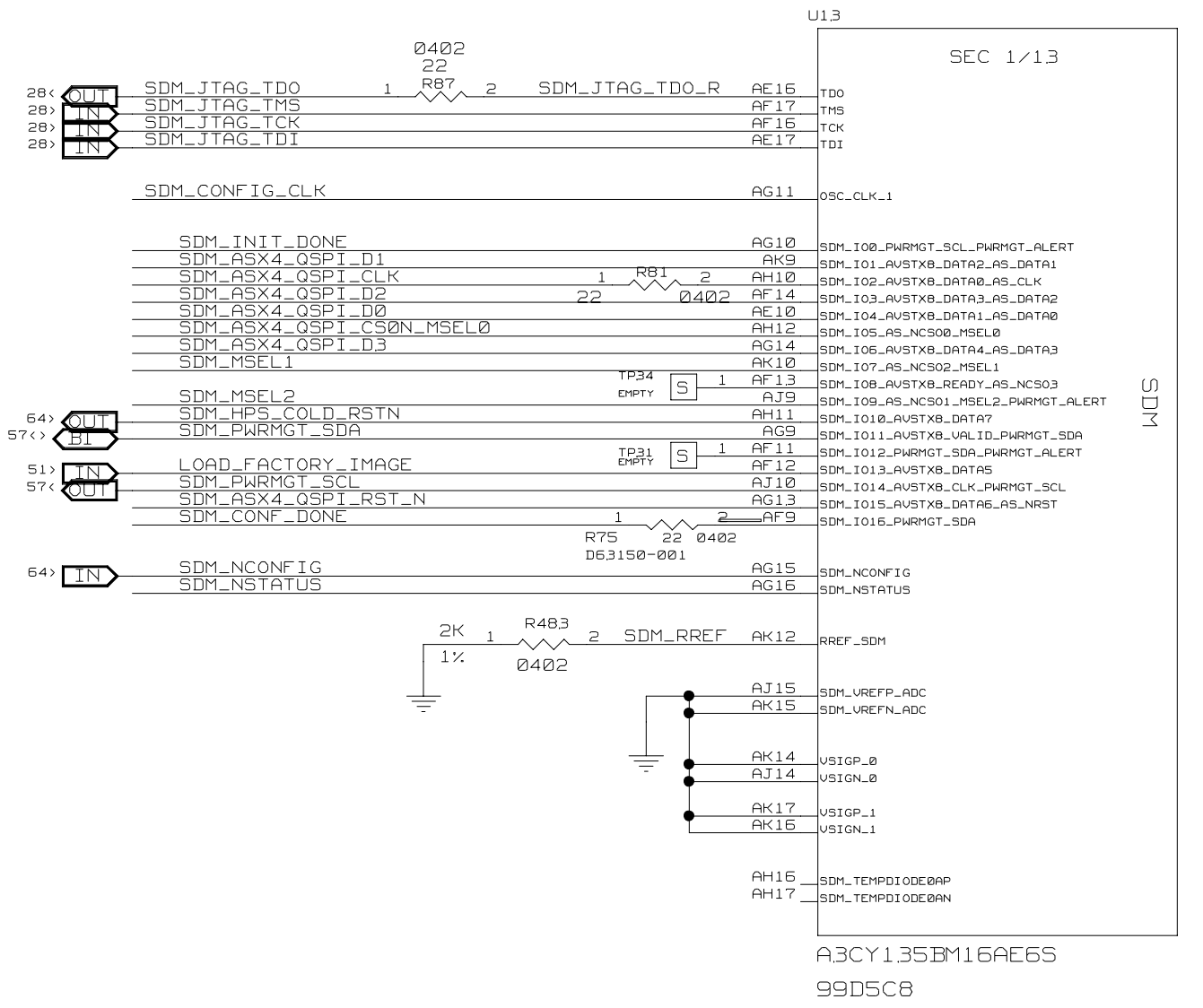
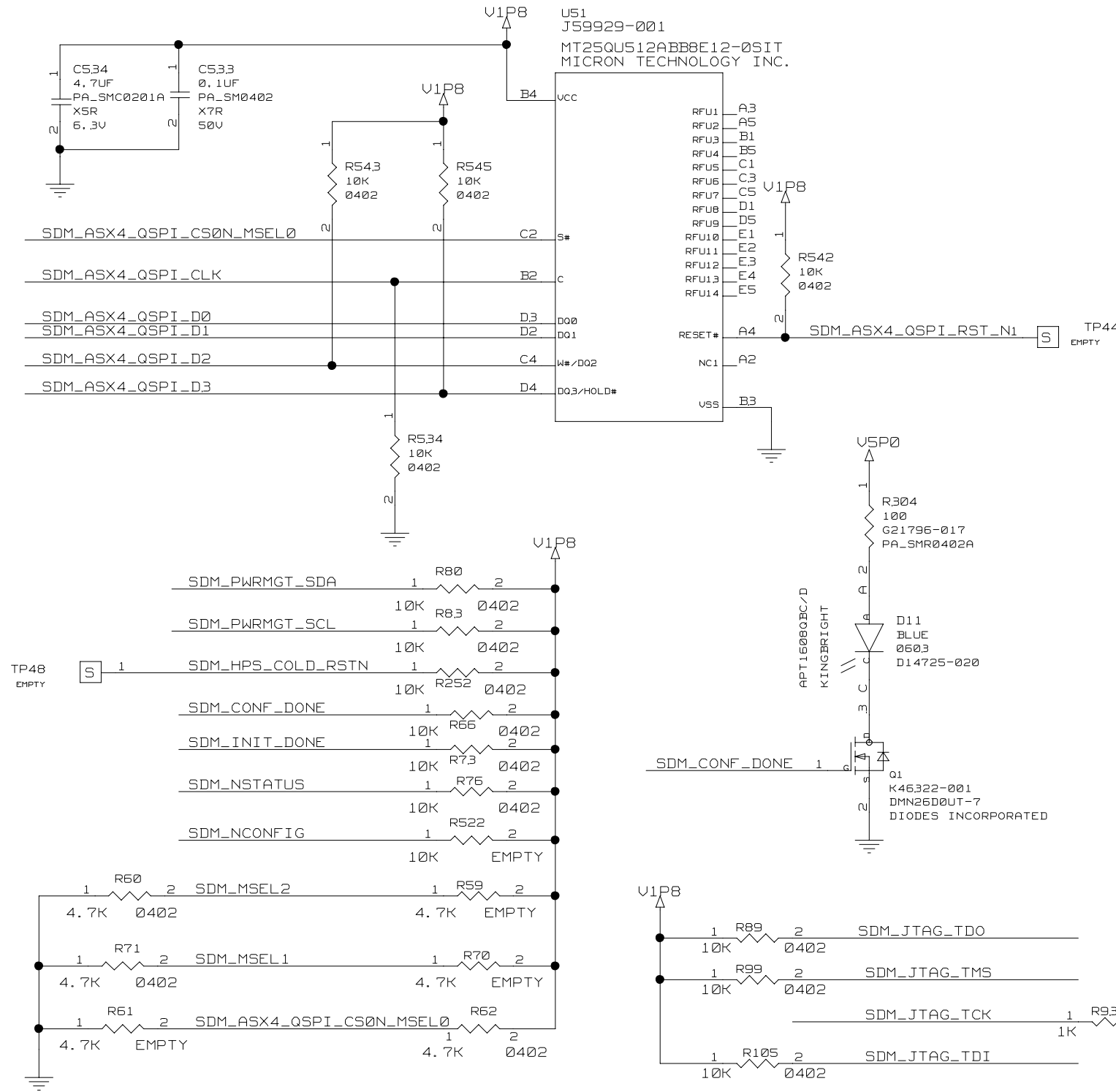
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DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 7 OF 65

QSPI FLASH



BANK VOLTAGE : 1.8V

CONFIG MODE	MSEL2	MSEL1	MSEL0
AS (NORMAL)	0	1	1
AS (FAST)	0	0	1

<- DEFAULT

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 8 OF 65

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SWIZZLING ON BANK 2A

FPGA 2A, FABRIC LPDDR4

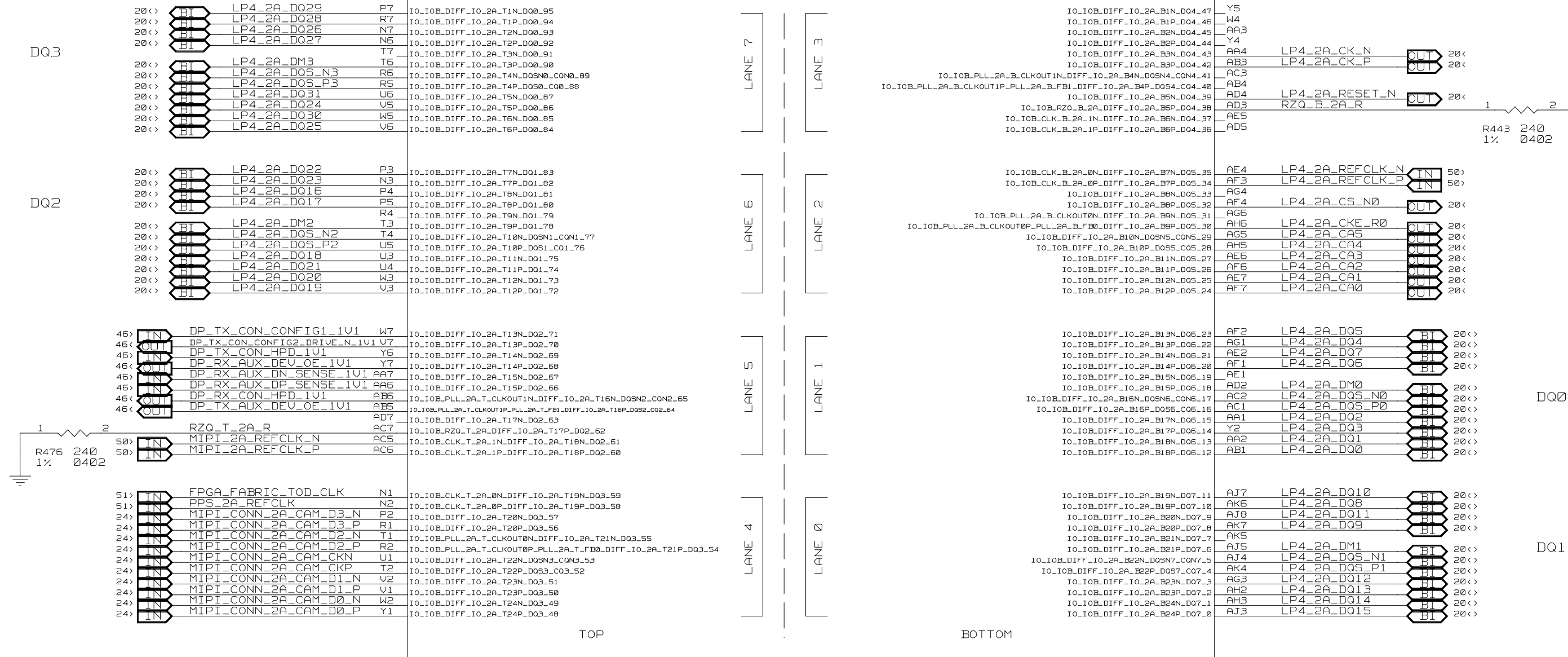
BYTE_SWIZZLE_CH0 = 1,0,X,X,X,X,2,3
 PIN_SWIZZLE_CH0_DQS0 = 5,4,7,6,2,3,1,0
 PIN_SWIZZLE_CH0_DQS1 = 10,8,11,9,12,13,14,15
 PIN_SWIZZLE_CH0_DQS2 = 22,23,16,17,18,21,20,19
 PIN_SWIZZLE_CH0_DQS3 = 29,28,26,27,31,24,30,25

U13

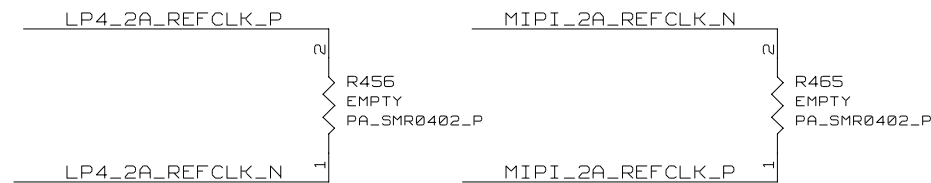
BANK VOLTAGE : 1.1V

SEC 3/13
 BANK 2A

BANK VOLTAGE : 1.1V



A3CY135BM16AE6S
 99D5C8



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DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 9 OF 65	

SWIZZLING ON BANK 3A

BYTE_SWIZZLE_CH0 = 3, 2, X, X, X, X, 1, 0
 PIN_SWIZZLE_CH0_DQS0 = 5, 6, 7, 4, 2, 3, 0, 1
 PIN_SWIZZLE_CH0_DQS1 = 12, 10, 11, 8, 13, 14, 15, 9
 PIN_SWIZZLE_CH0_DQS2 = 17, 22, 23, 16, 21, 20, 18, 19
 PIN_SWIZZLE_CH0_DQS3 = 29, 28, 31, 30, 25, 24, 27, 26

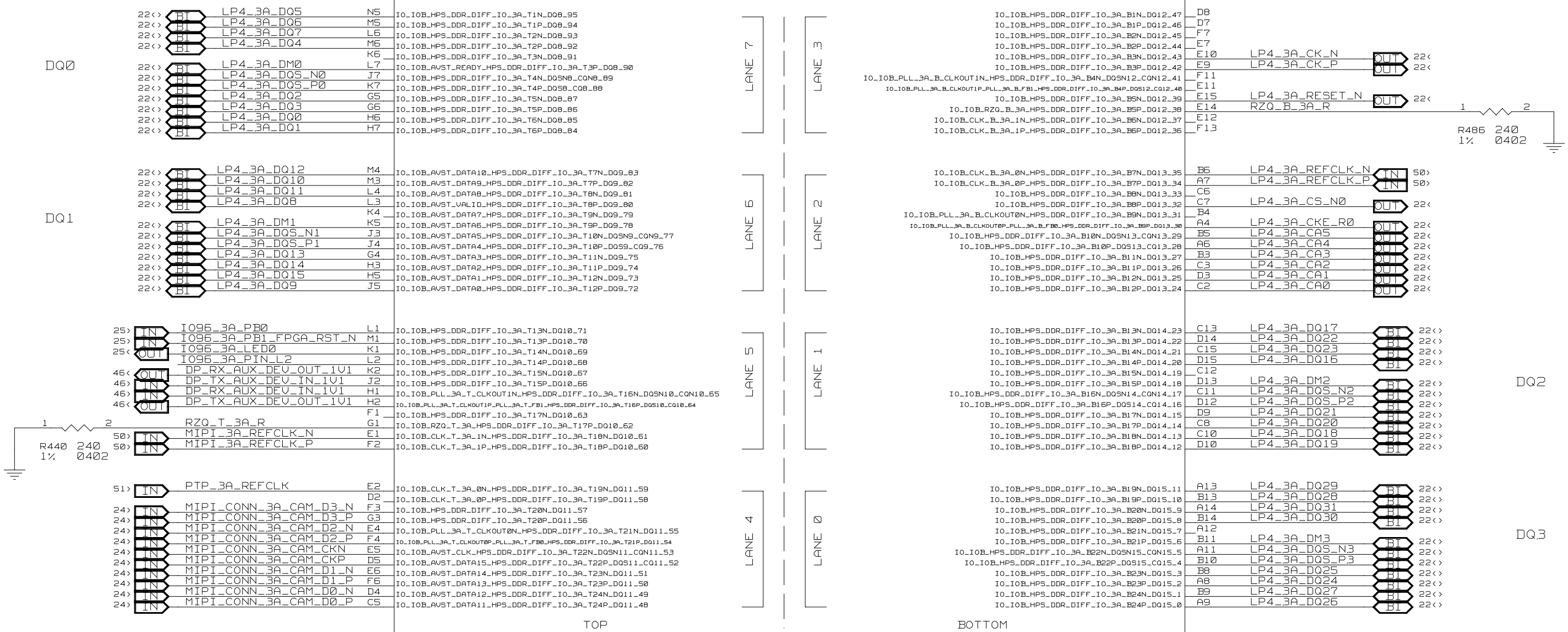
FPGA 3A, HPS LPDDR4

U13

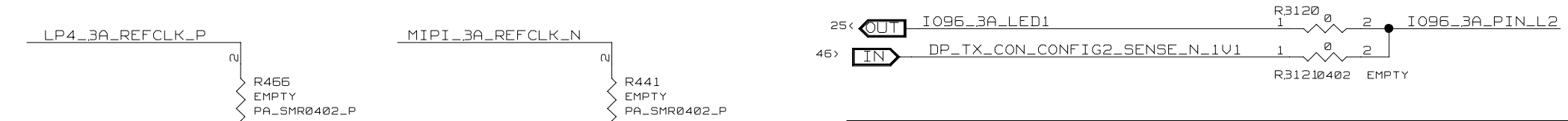
BANK VOLTAGE : 1.1V

SEC 4/13
BANK 3A

BANK VOLTAGE : 1.1V

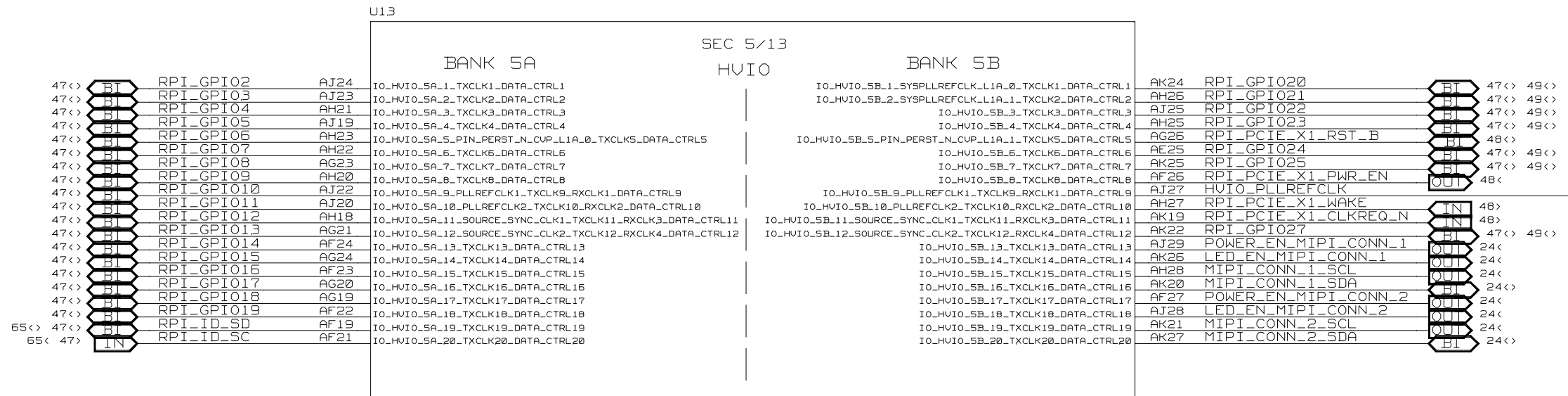


A3CY1.35BM16AE6S
99D5C8



Thu May 22 01:34:33 2025

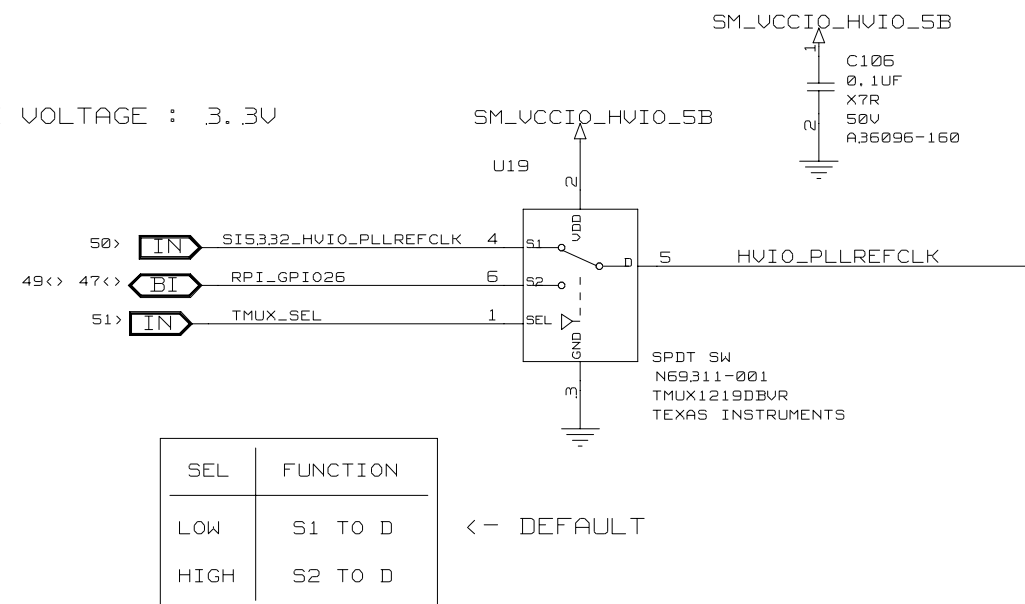
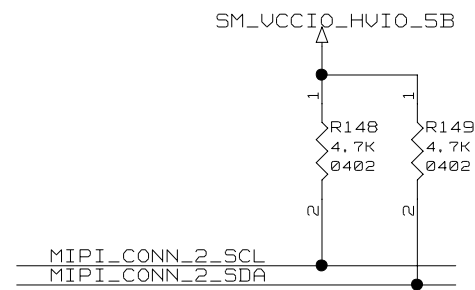
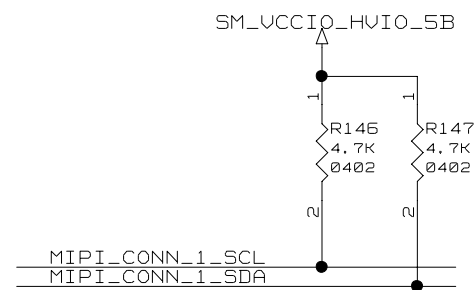
DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 10 OF 65	



A3CY1.35BM16AE6S
99D5C8

BANK VOLTAGE : 3.3V

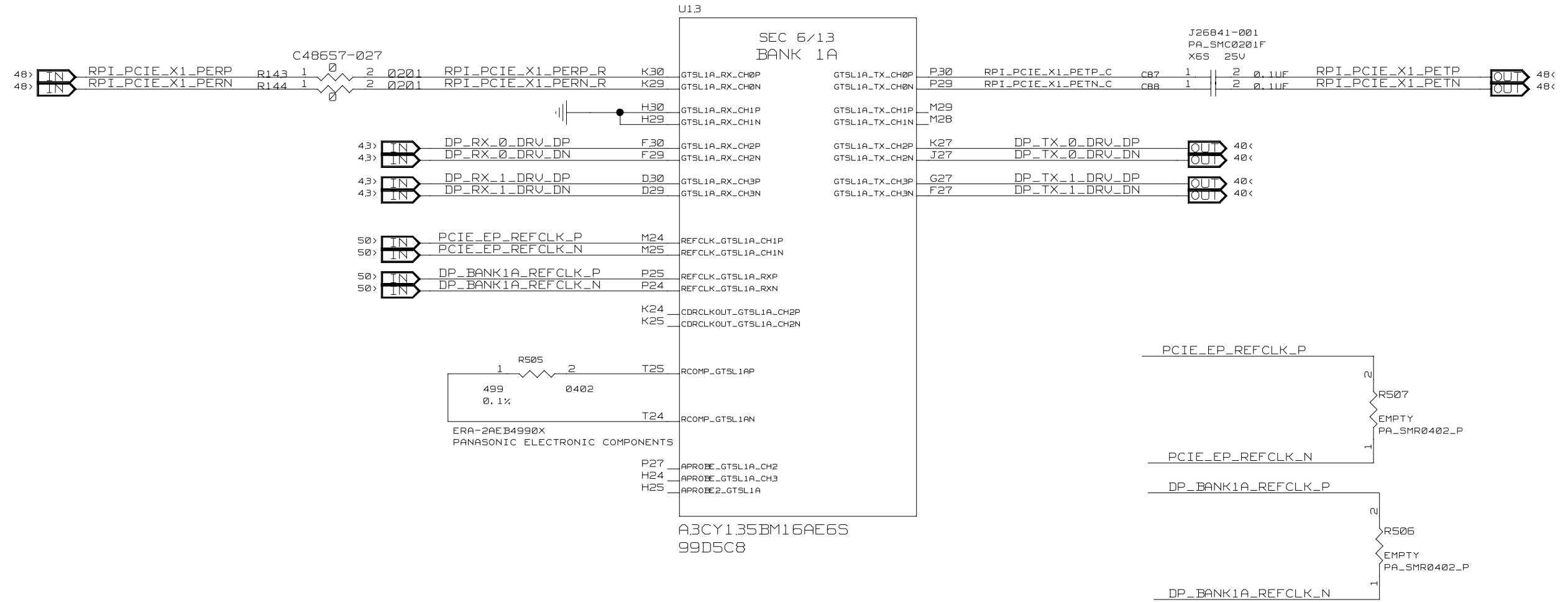
BANK VOLTAGE : 3.3V



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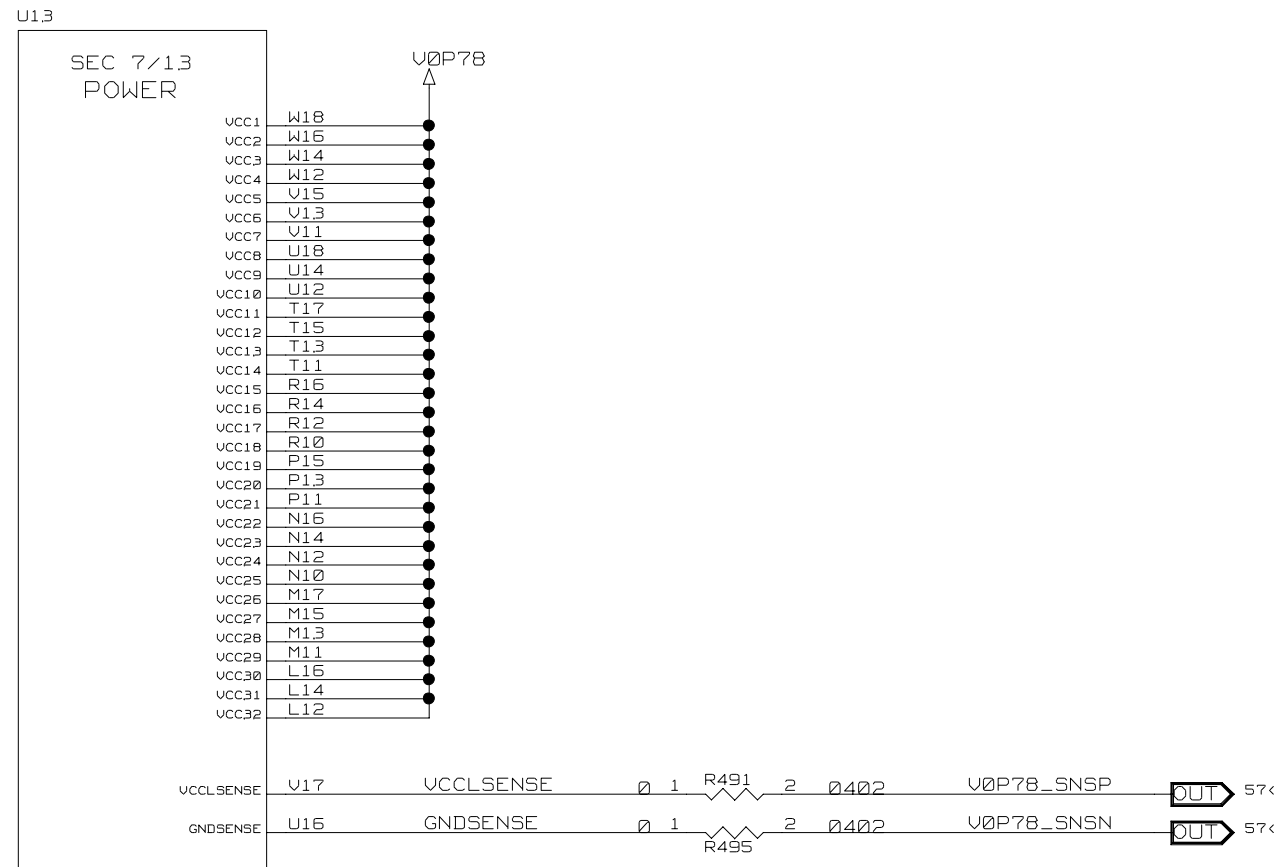
DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 11 OF 65

FPGA TRANSCEIVER

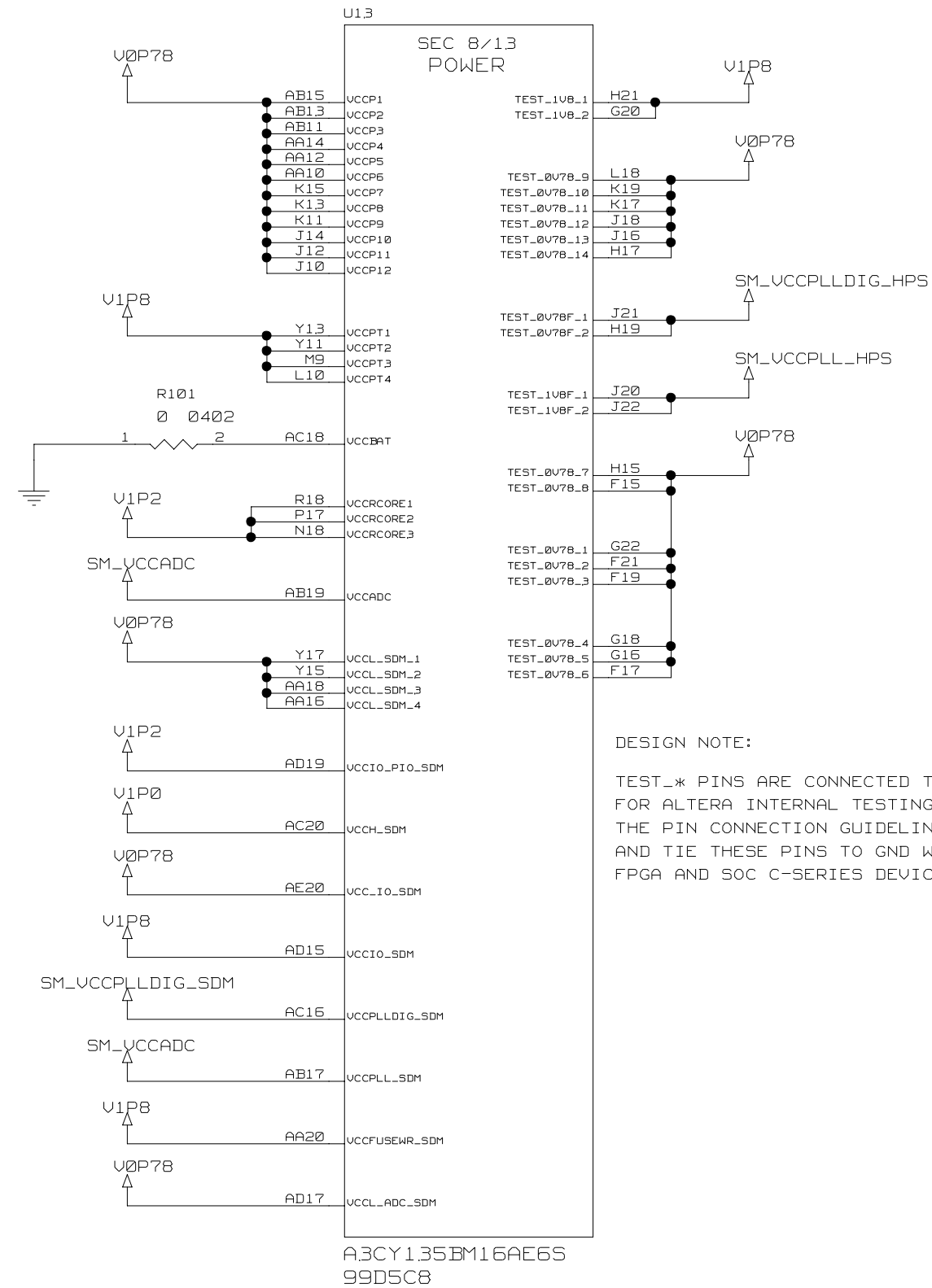


Thu May 22 01:34:33 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 13 OF 65	



A3CY135BM16AE6S
99D5C8



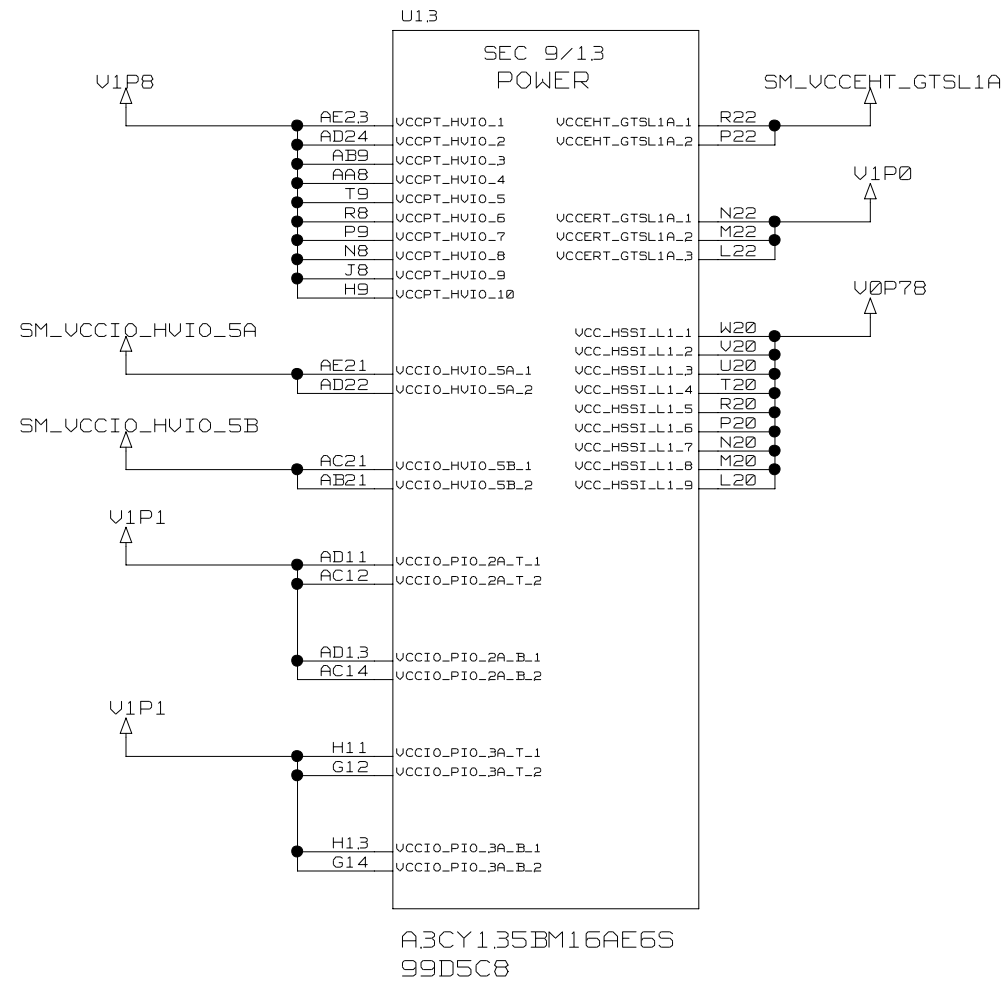
A3CY135BM16AE6S
99D5C8

DESIGN NOTE:

TEST_* PINS ARE CONNECTED TO POWER IN THIS SCHEMATIC FOR ALTERA INTERNAL TESTING ONLY. DESIGNERS MUST FOLLOW THE PIN CONNECTION GUIDELINES AND PIN-OUT DOCUMENTATION AND TIE THESE PINS TO GND WHEN DESIGNING FOR AGILEX 3 FPGA AND SOC C-SERIES DEVICES.

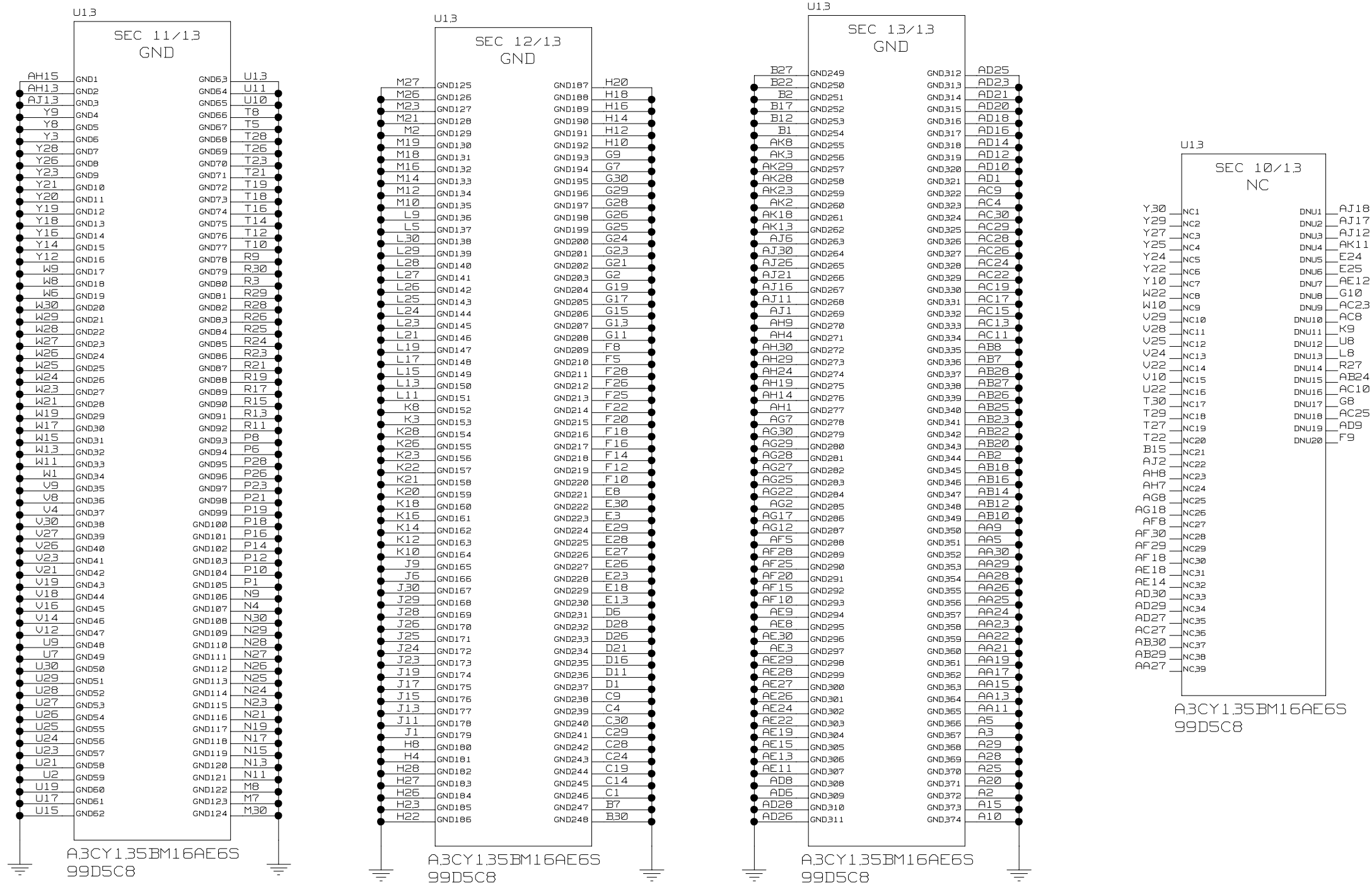
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DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 14 OF 65	



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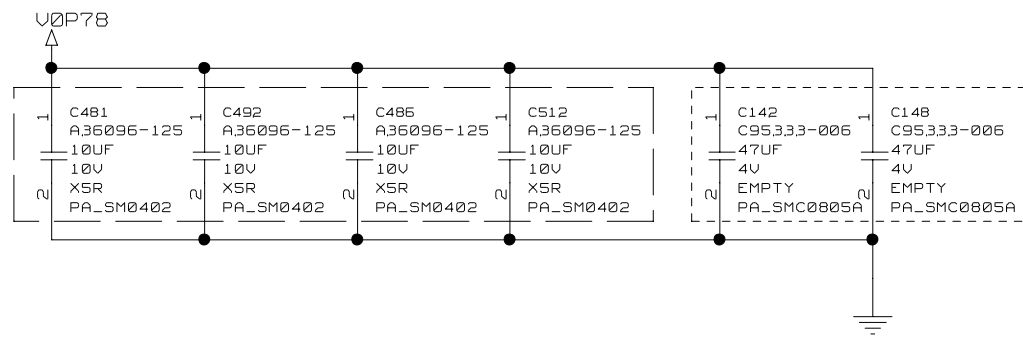
DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER .305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 15 OF 65	



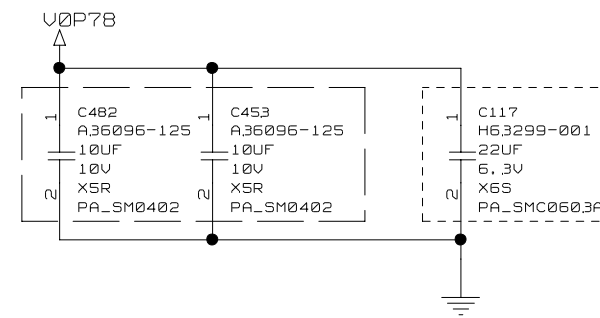
Thu May 22 01:34:34 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 16 OF 65	

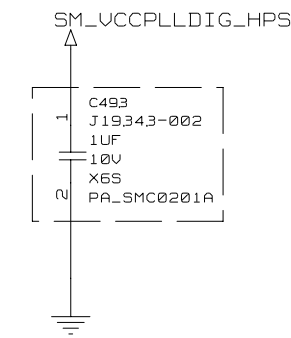
VCC, VCCP



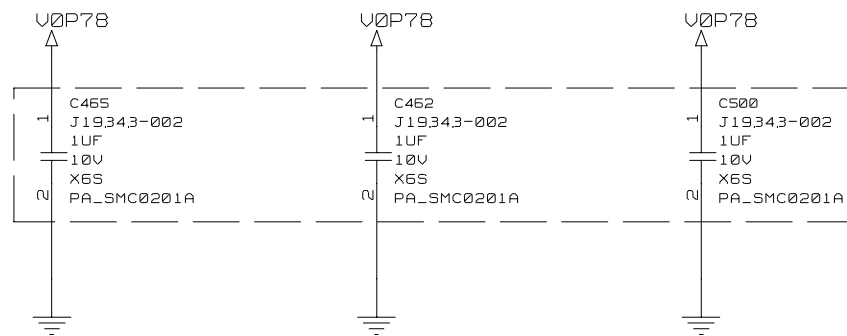
VCC_L HPS



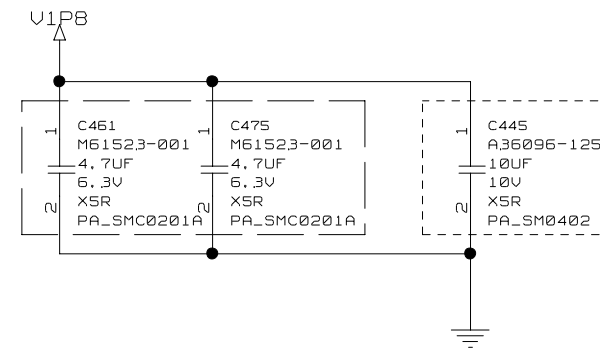
VCCPLLDIG HPS



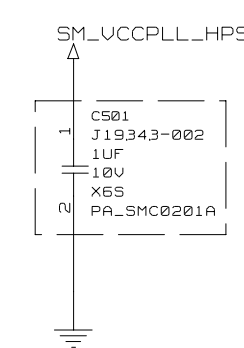
VCC_L HPS CORE



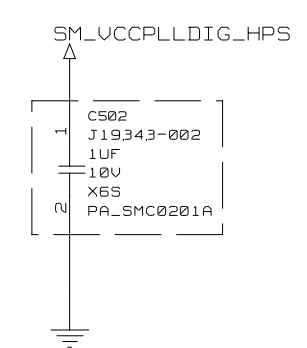
VCCPT



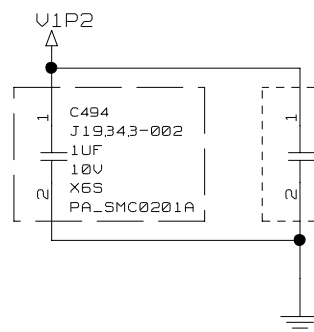
VCCPLL HPS



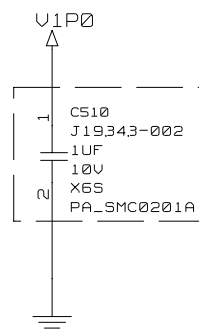
VCCPLLDIG HPS



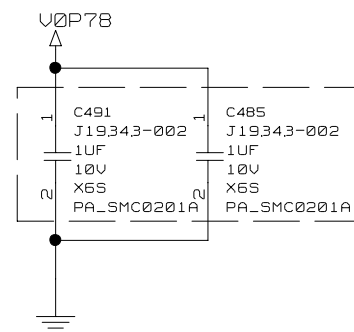
VCCRCORE



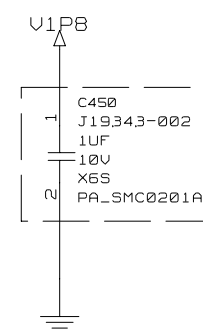
VCC_H SDM



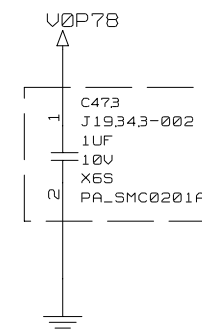
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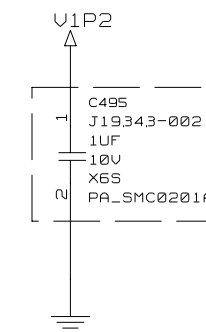
VCCIO HPS



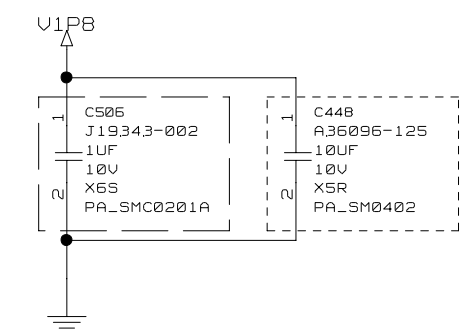
VCC IO SDM



VCCIO PIO SDM



VCCIO SDM

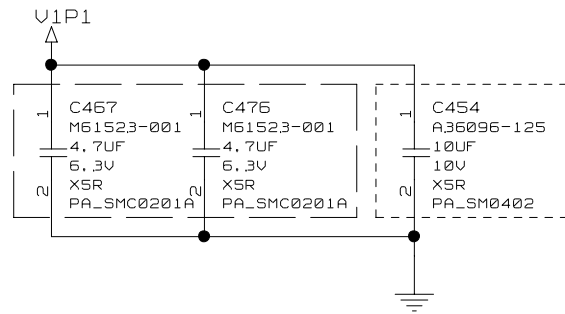


 BOTTOM CAPS
 PERIPHERAL CAPS

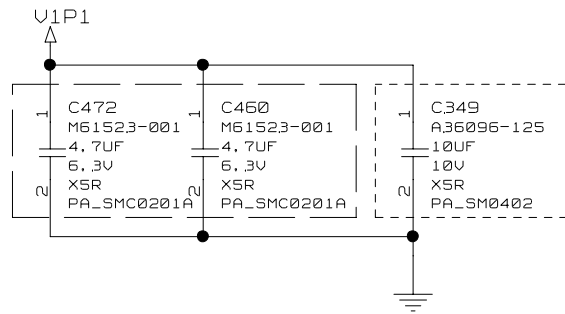
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DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 17 OF 65	

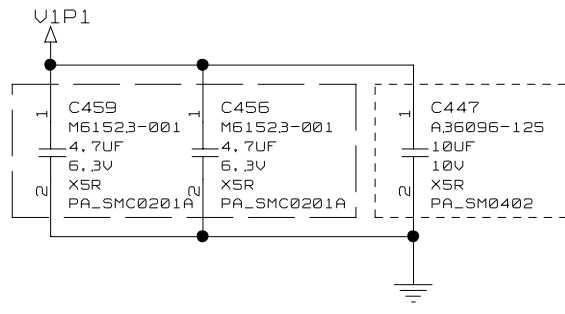
VCCIO PIO 2A T



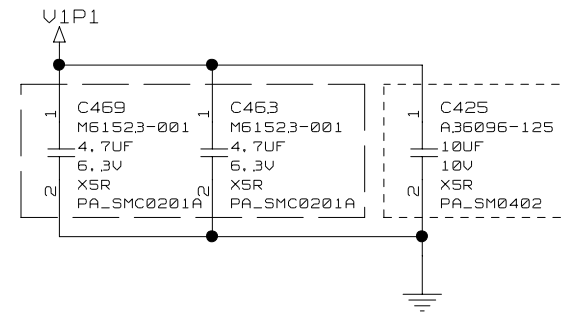
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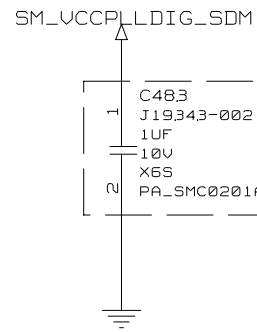
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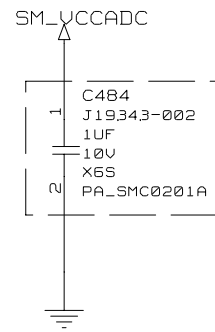
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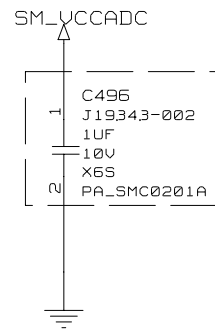
VCCPLLDIG SDM



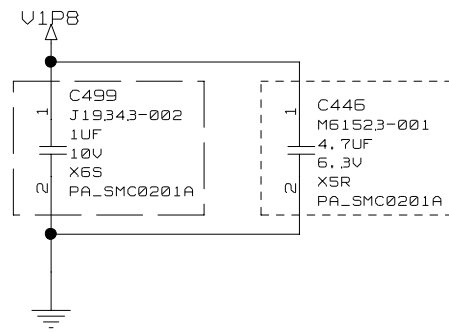
VCCADC



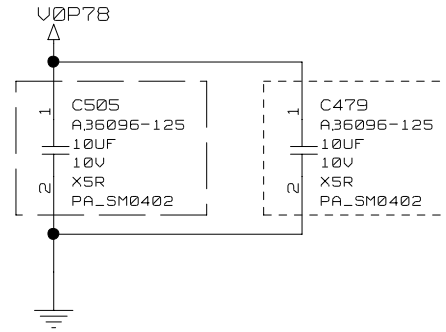
VCCPLL SDM



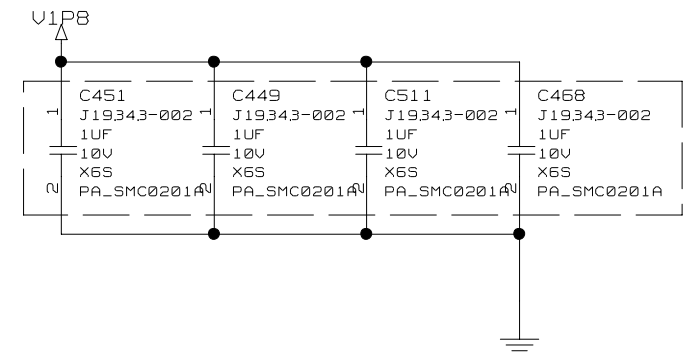
VCCFUSEWR SDM



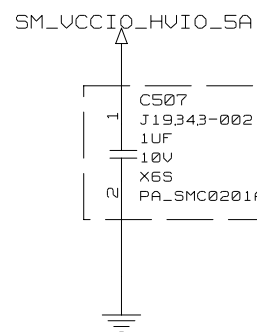
VCC HSSI



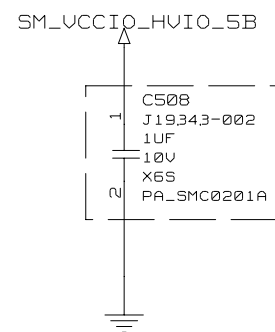
VCCPT HVIO



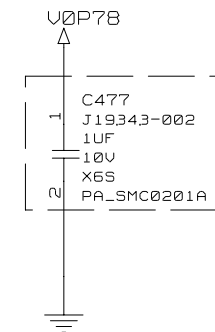
VCCIO HVIO 5A



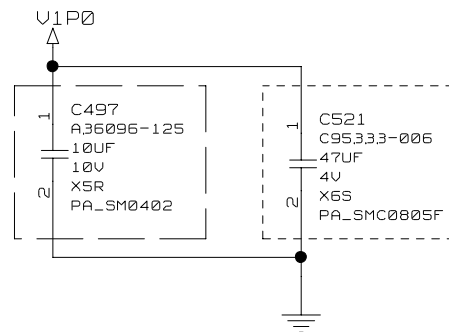
VCCIO HVIO 5B



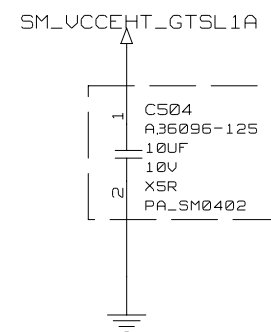
VCCL ADC SDM



VCCERT GTS



VCCEHT GTS



— — — — — BOTTOM CAPS

- - - - - PERIPHERAL CAPS

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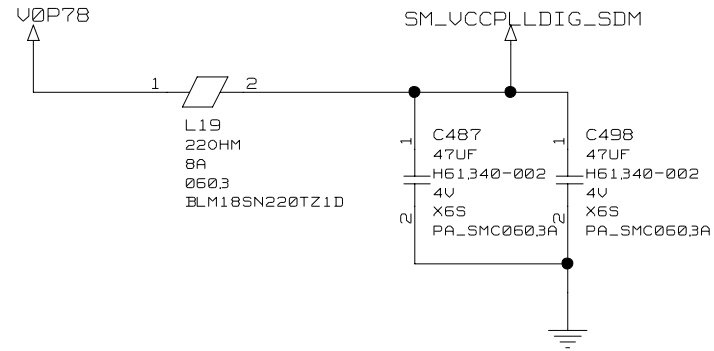
DEPARTMENT
PLATFORM HW DEVELOPMENT



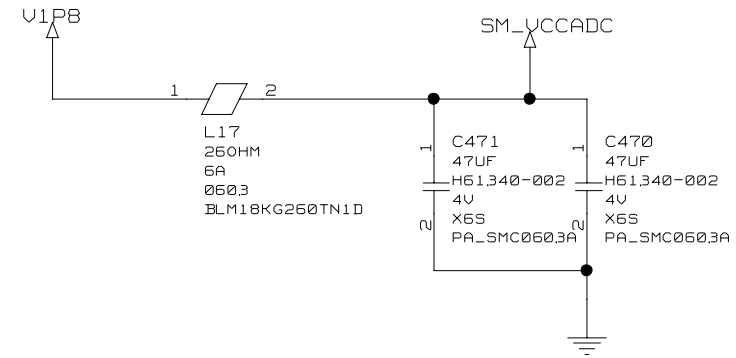
SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
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SCALE: DO NOT SCALE DRAWING SHEET 18 OF 65

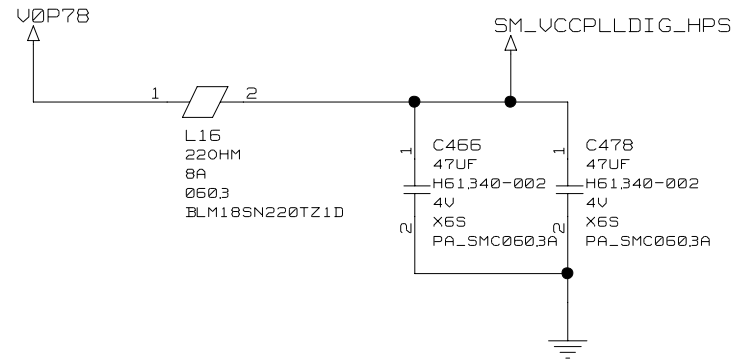
PERIPHERY CAPS



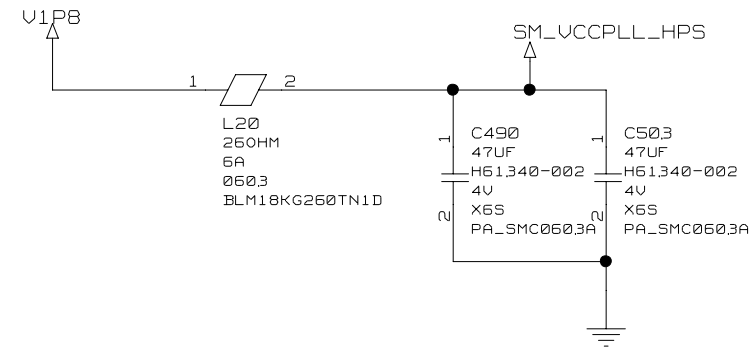
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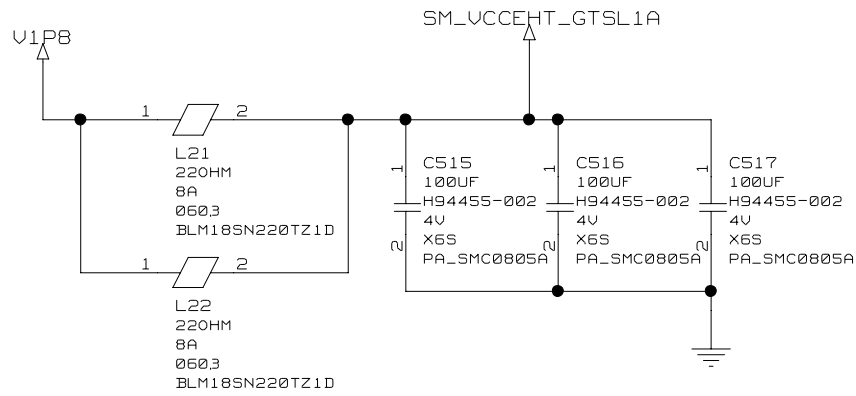
PERIPHERY CAPS



PERIPHERY CAPS



FILTER RECOMMENDATION



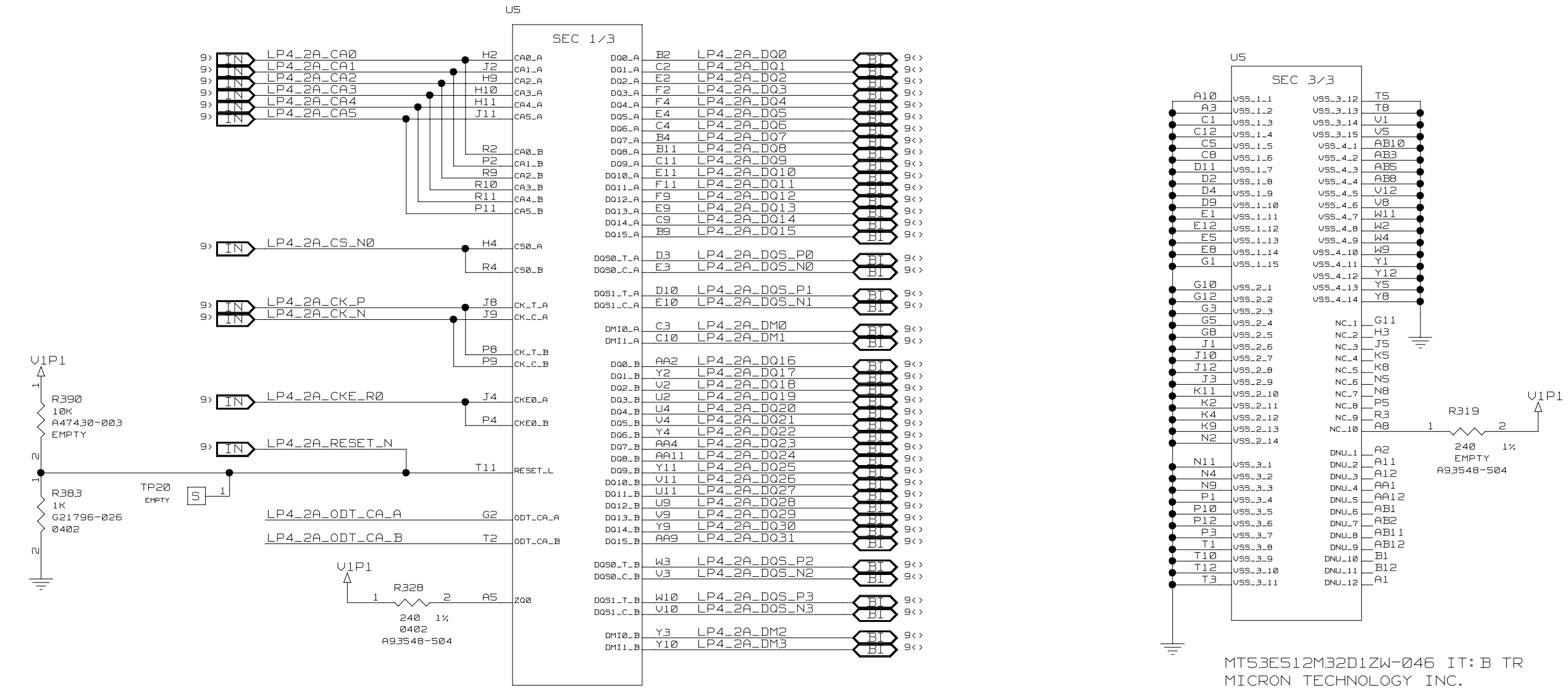
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DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 19 OF 65

FABRIC LPDDR4 (2A)

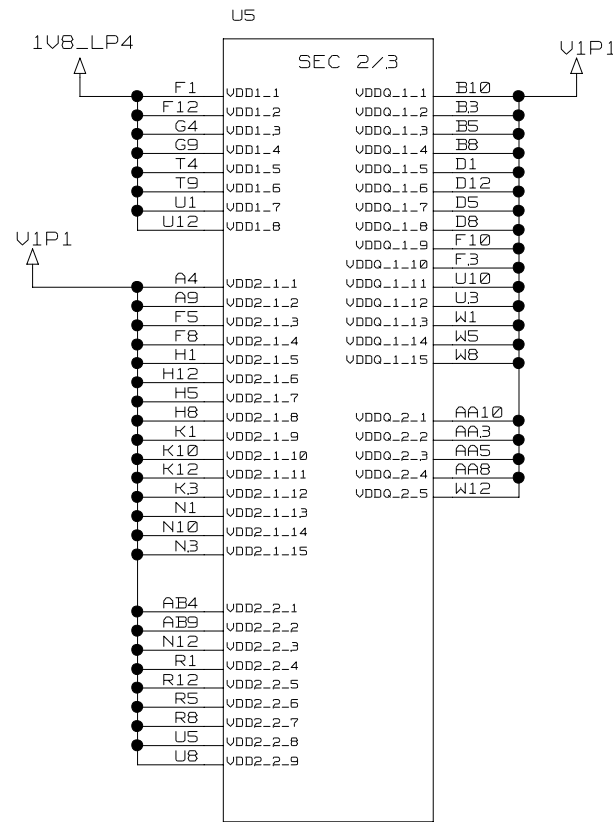


MT53E512M32D1ZW-046 IT:B TR
MICRON TECHNOLOGY INC.

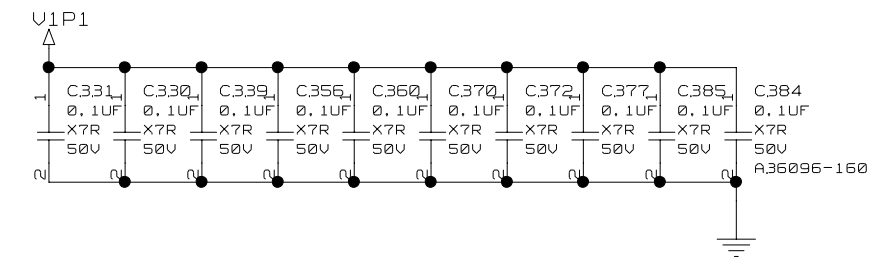
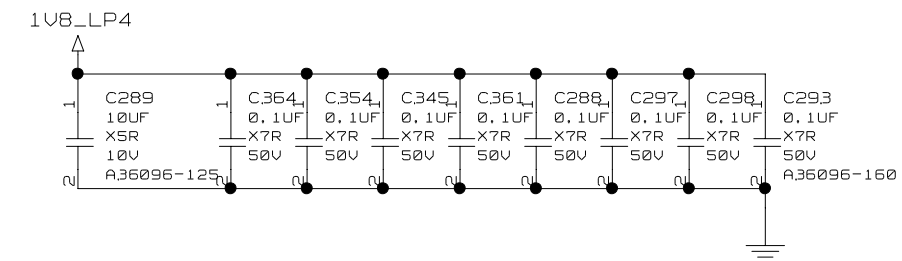
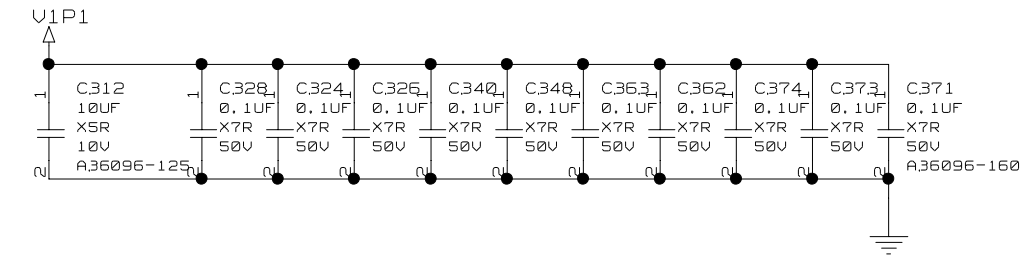
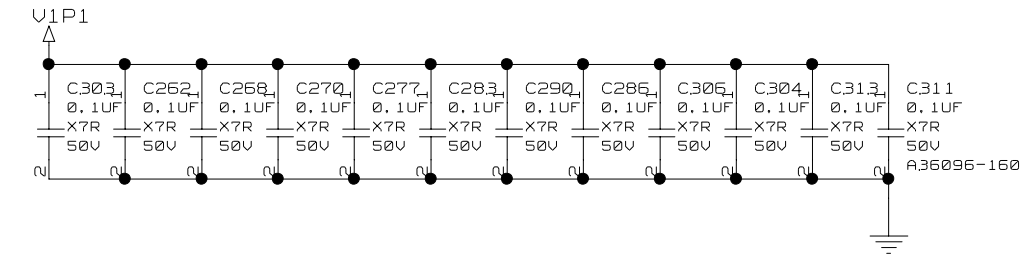
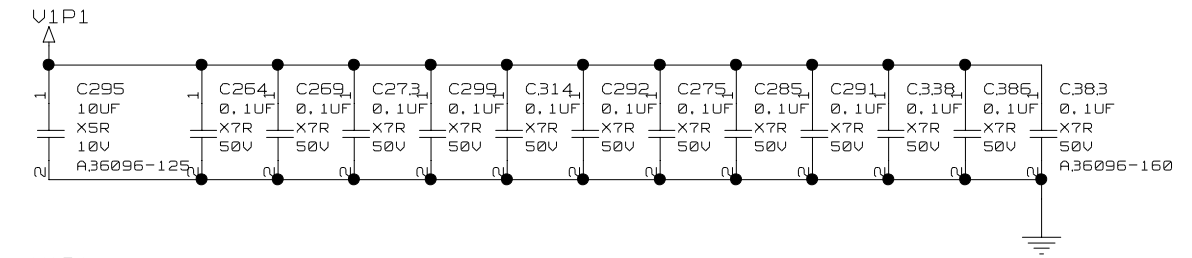
Thu May 22 01:34:34 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera™	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 20 OF 65	

FABRIC LPDDR4 (2A)

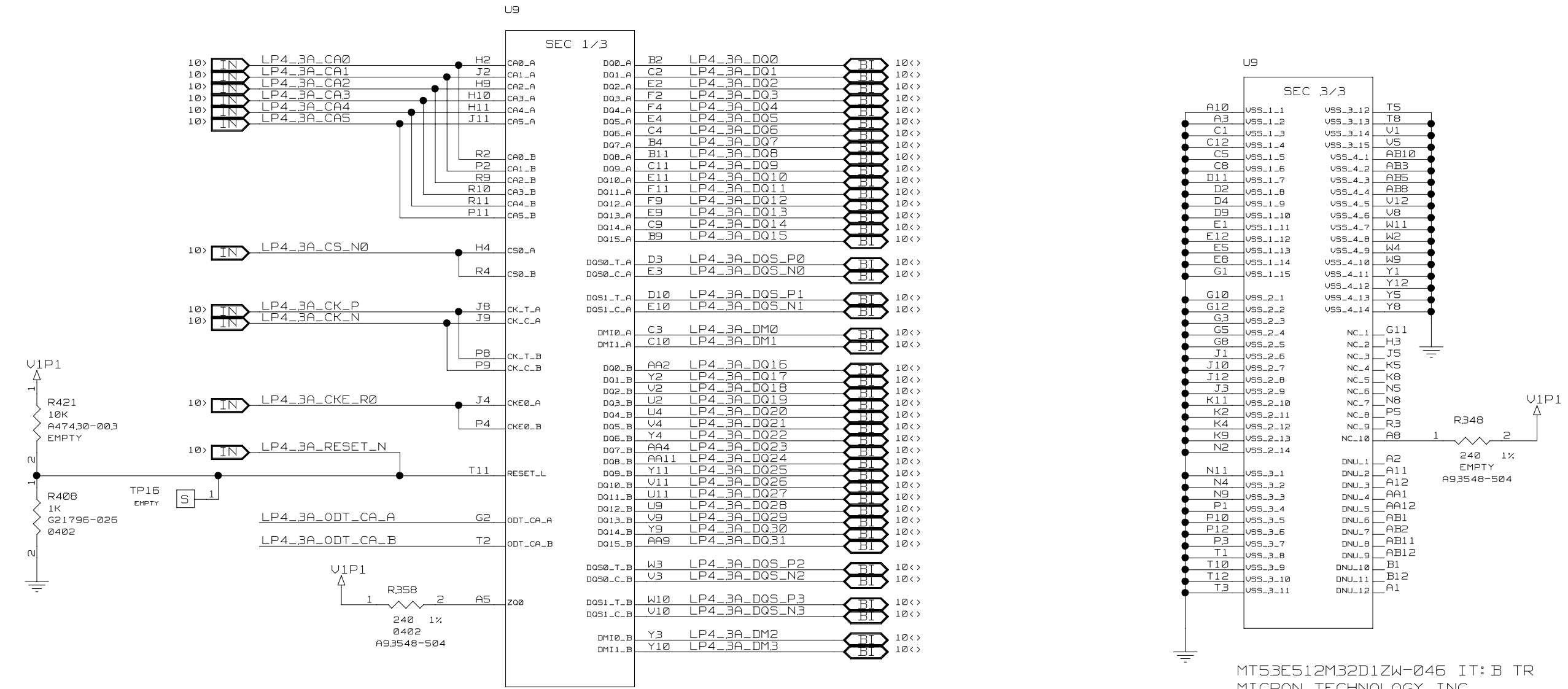


MT53E512M32D1ZW-046 IT: B TR
MICRON TECHNOLOGY INC.



Thu May 22 01:34:34 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 21 OF 65	

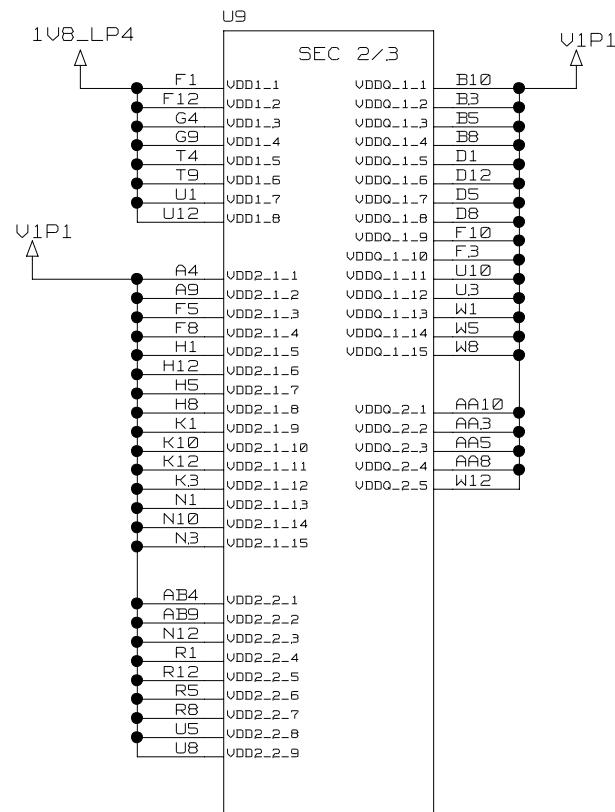


MT53E512M32D1ZW-046 IT: B TR
MICRON TECHNOLOGY INC.

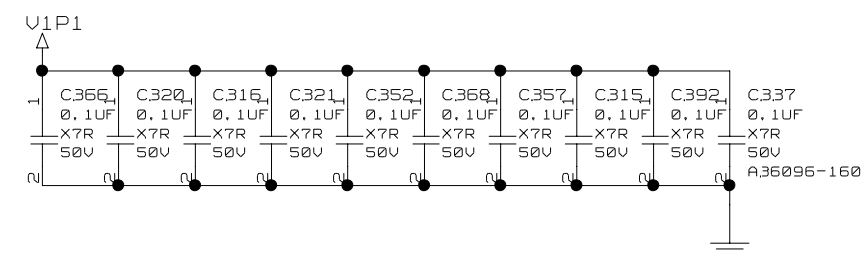
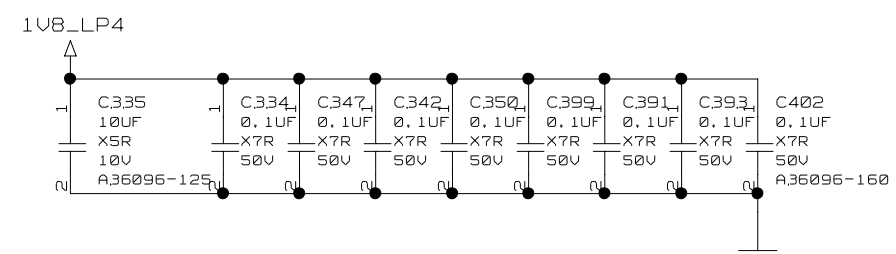
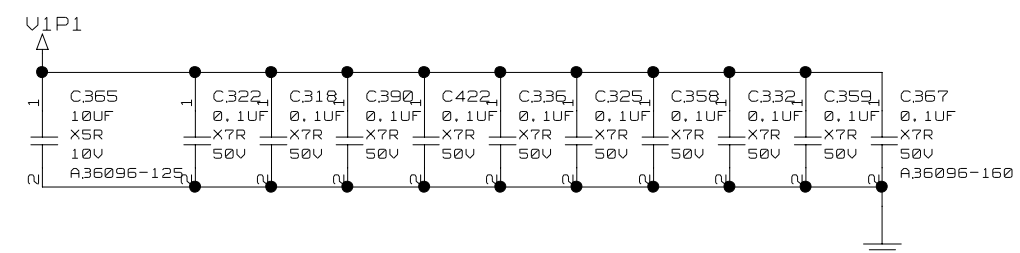
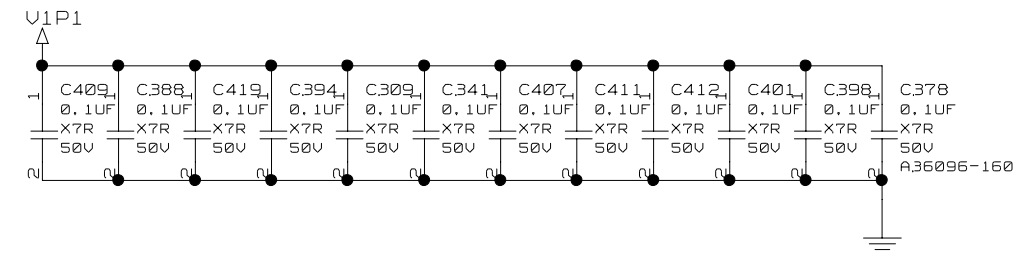
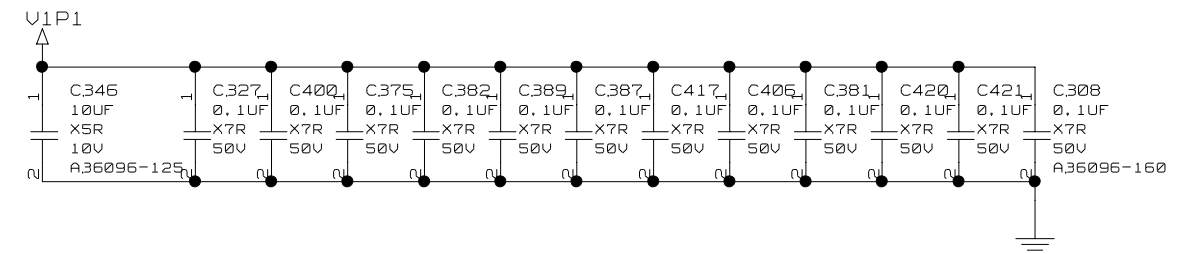
MT53E512M32D1ZW-046 IT: B TR
MICRON TECHNOLOGY INC.

Thu May 22 01:34:35 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE	CODE	DOCUMENT NUMBER	REV
		B	34649	.305-PD-25-0242	2.0
SCALE:		DO NOT SCALE DRAWING			SHEET 22 OF 65



MT53E512M32D1ZW-046 IT:B TR
MICRON TECHNOLOGY INC.



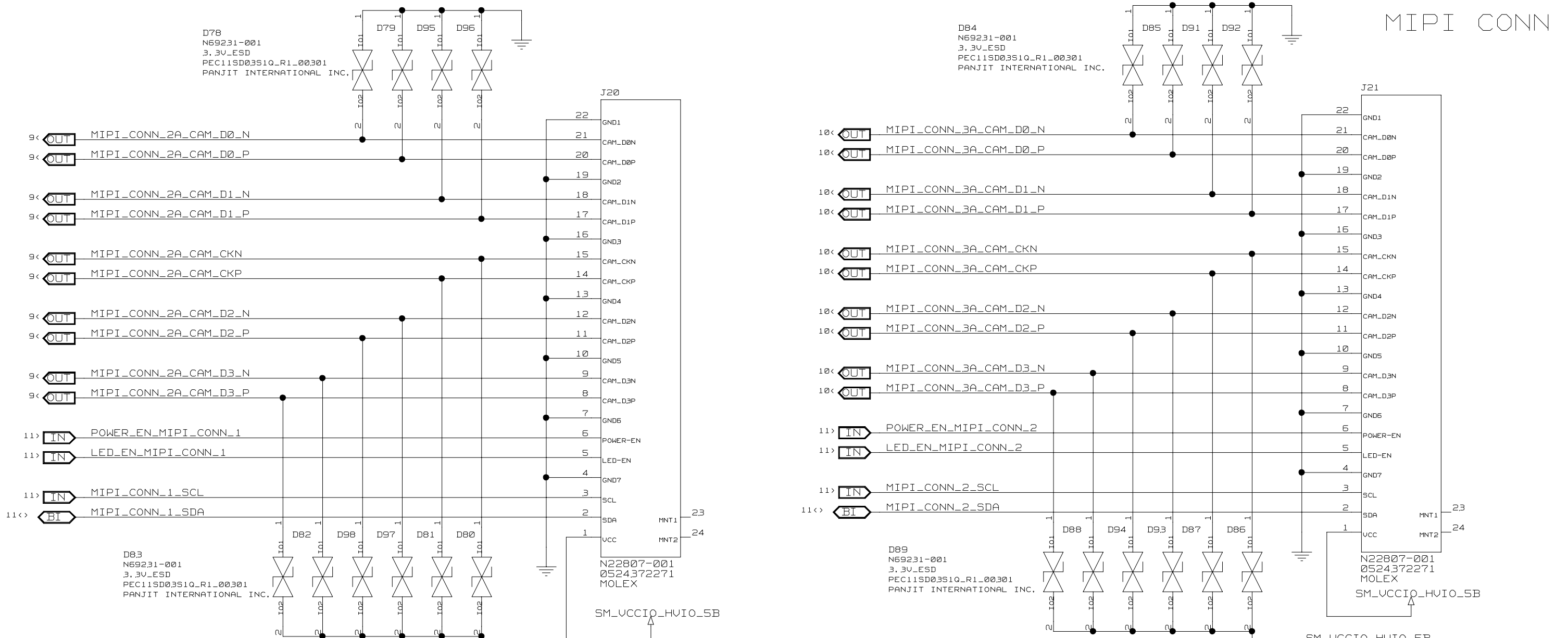
Thu May 22 01:34:35 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 23 OF 65

D78
N69231-001
3.3V_ESD
PEC11SD03S1Q_R1_00301
PANJIT INTERNATIONAL INC.

D84
N69231-001
3.3V_ESD
PEC11SD03S1Q_R1_00301
PANJIT INTERNATIONAL INC.

MIPI CONN

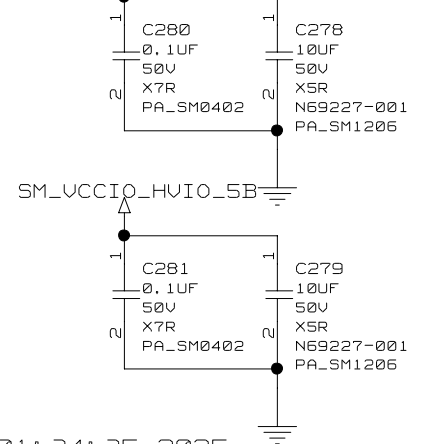
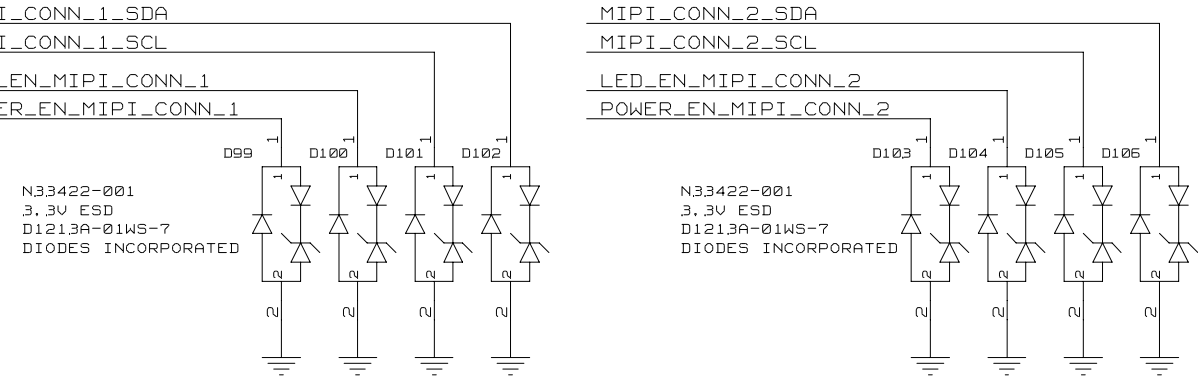
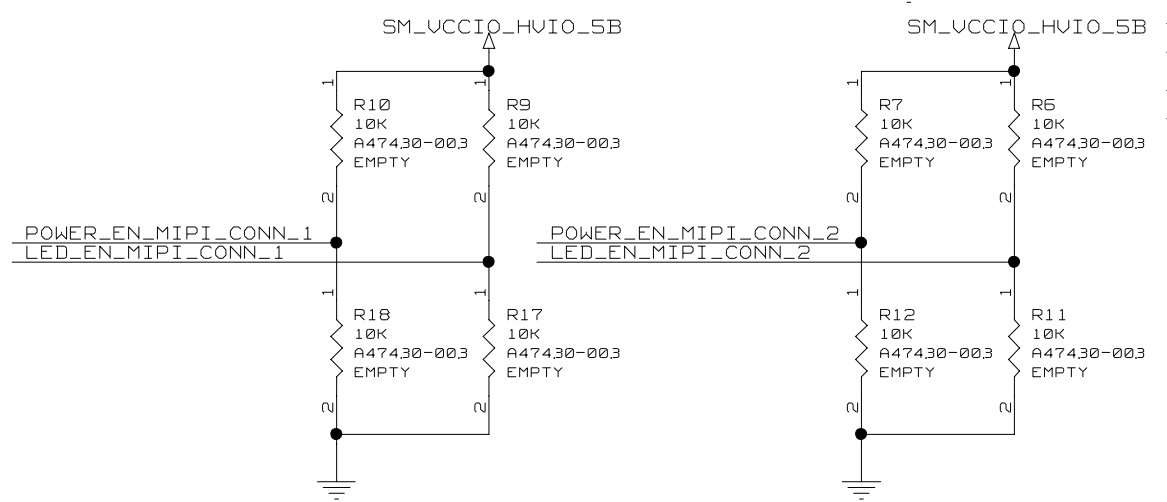


D83
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3.3V_ESD
PEC11SD03S1Q_R1_00301
PANJIT INTERNATIONAL INC.

D89
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3.3V_ESD
PEC11SD03S1Q_R1_00301
PANJIT INTERNATIONAL INC.

N22807-001
0524372271
MOLEX
SM_UCCIO_HVIO_5B

N22807-001
0524372271
MOLEX
SM_UCCIO_HVIO_5B



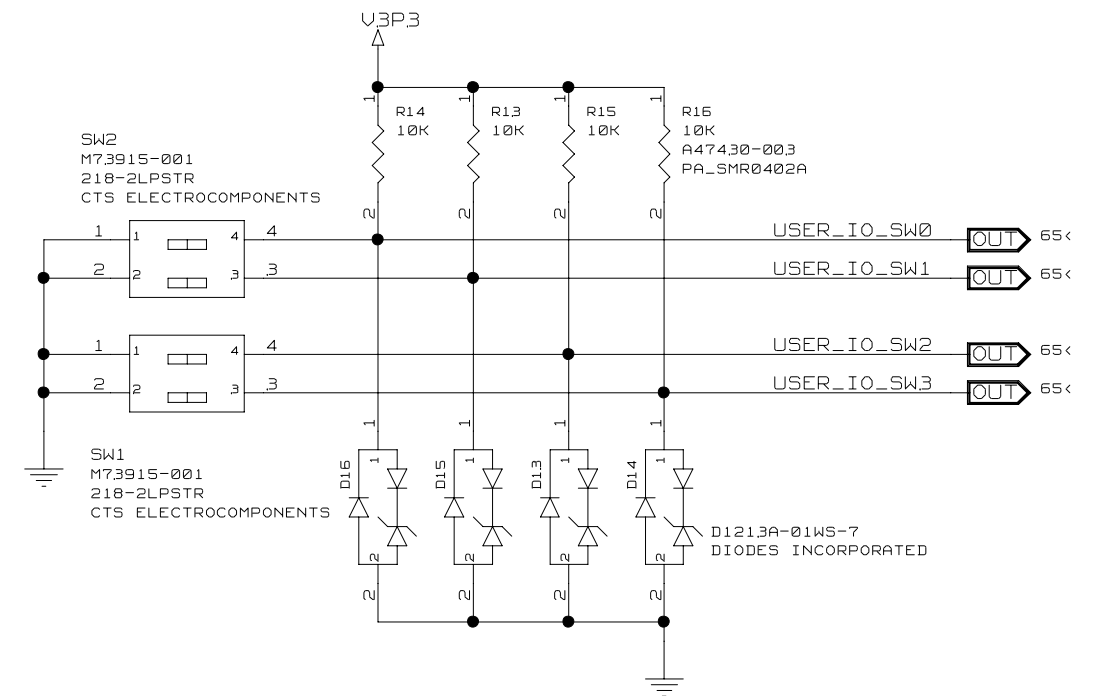
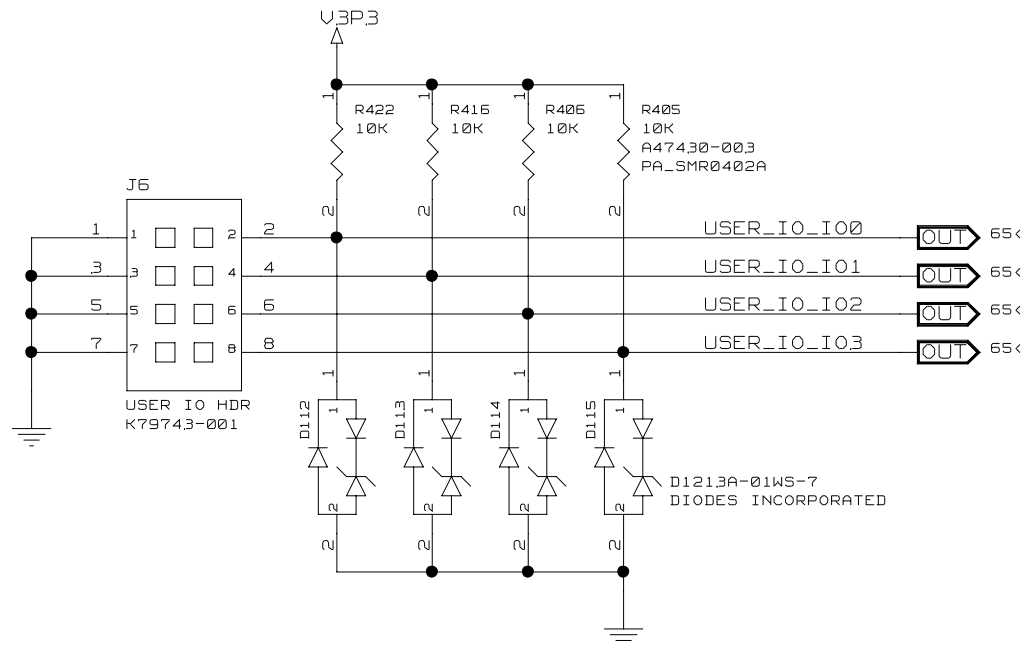
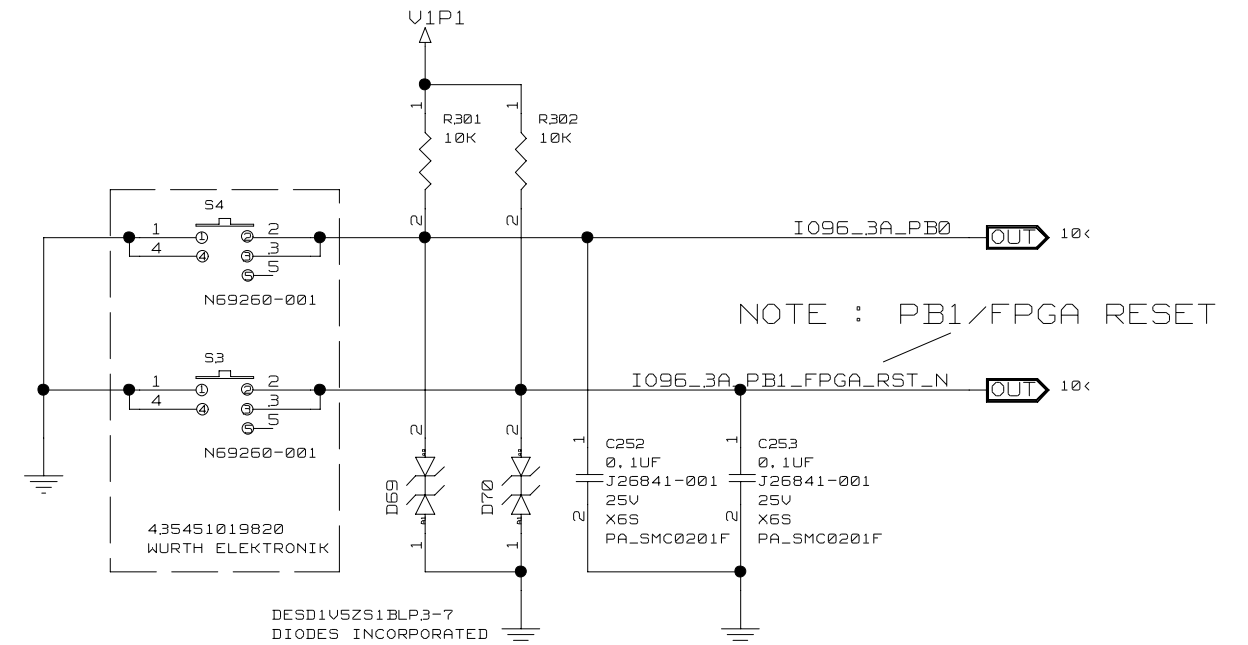
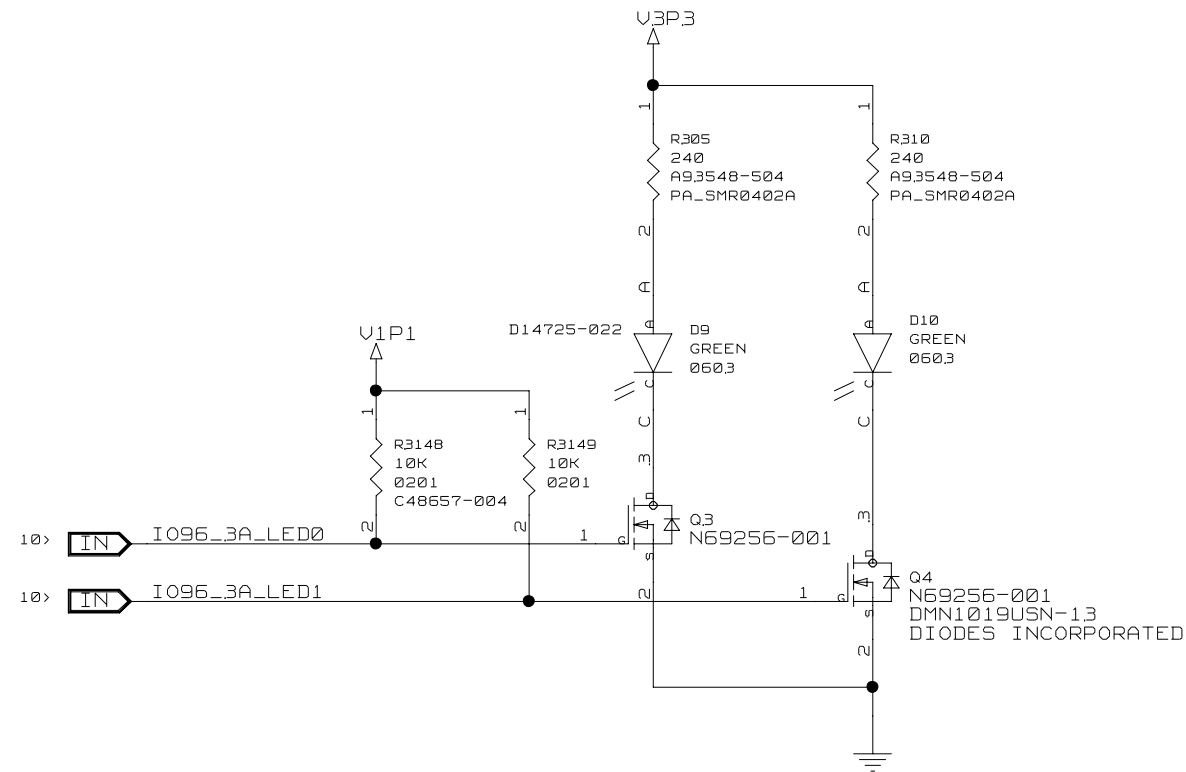
Thu May 22 01:34:35 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 24 OF 65

I096_3A USER IO



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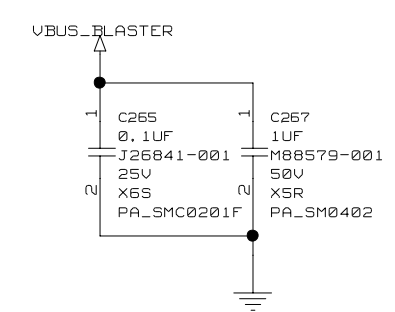
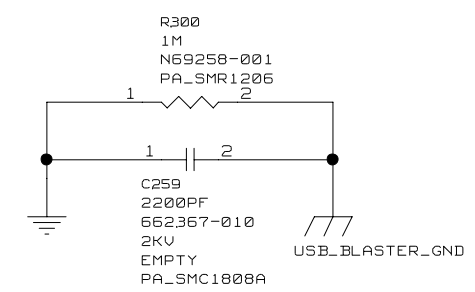
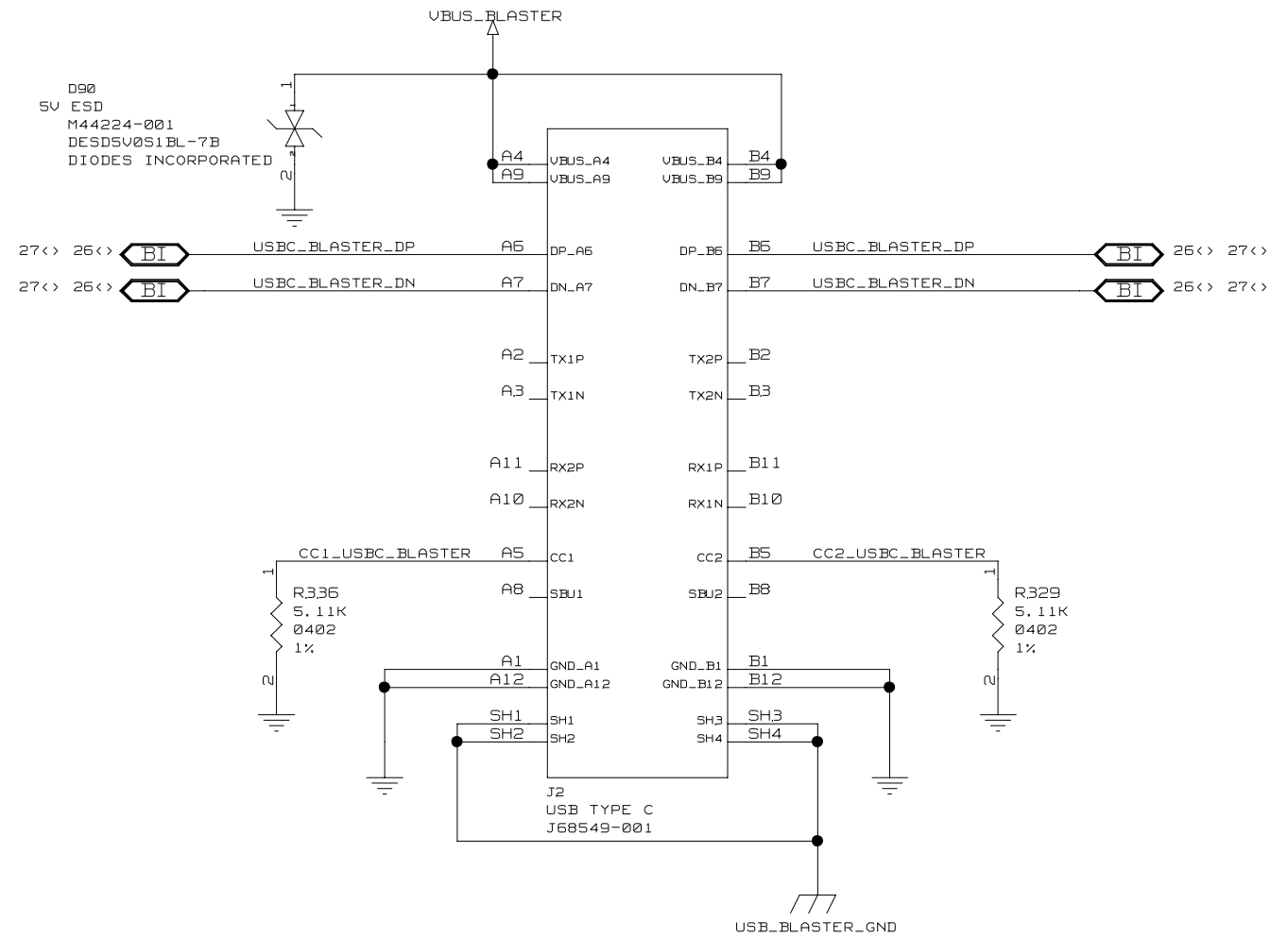
DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
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SCALE: DO NOT SCALE DRAWING SHEET 25 OF 65

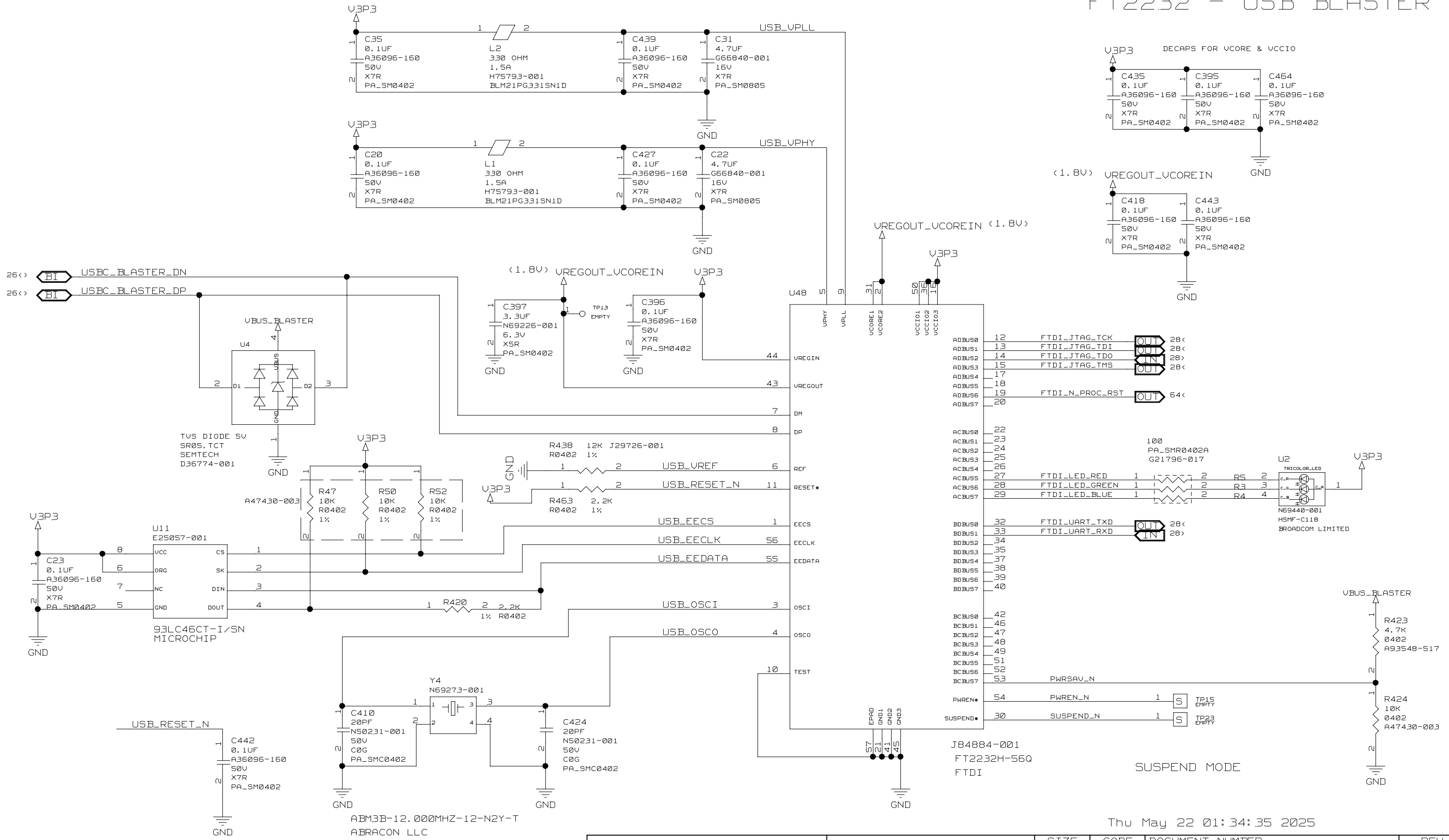
USB BLASTER



Thu May 22 01:34:35 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 26 OF 65	

FT2232 - USB BLASTER



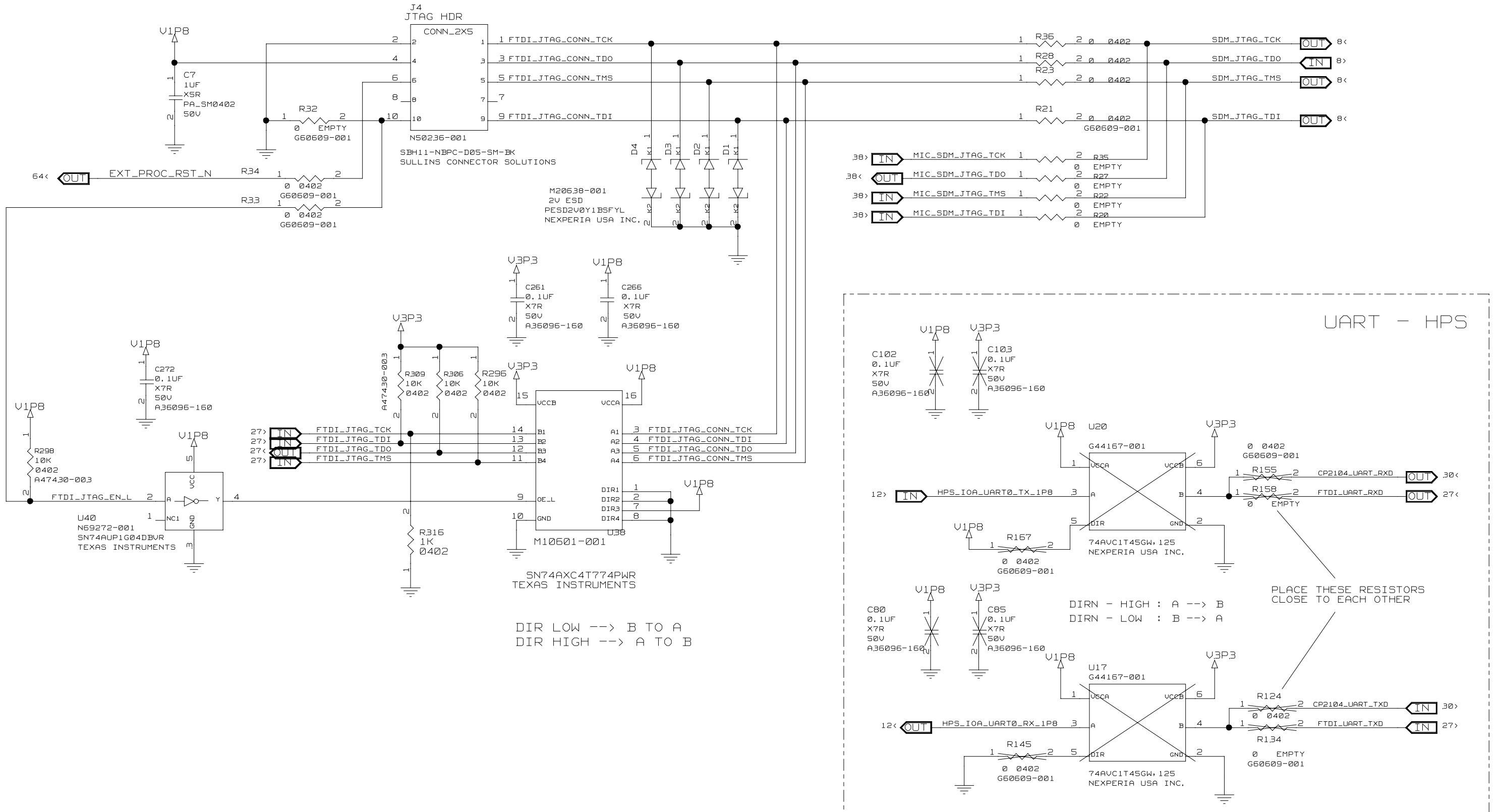
Thu May 22 01:34:35 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 27 OF 65

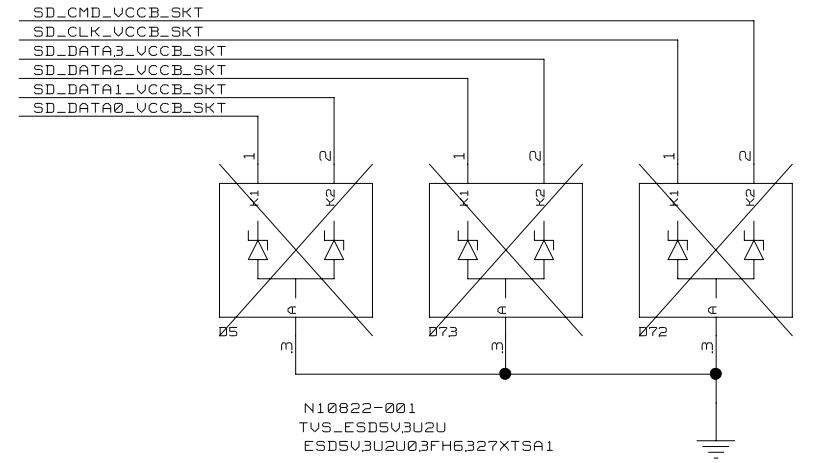
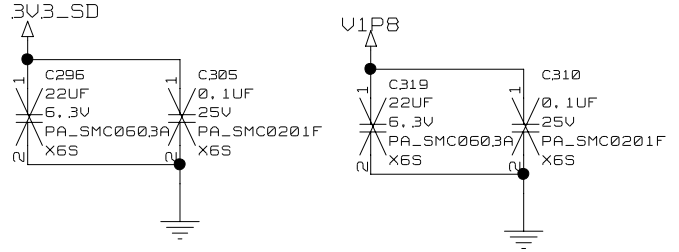
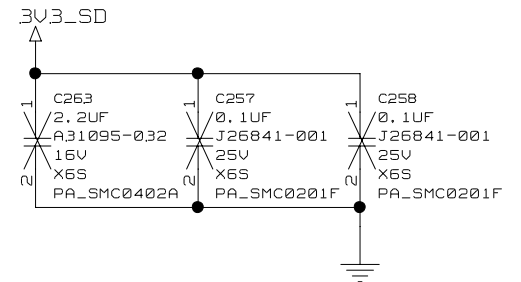
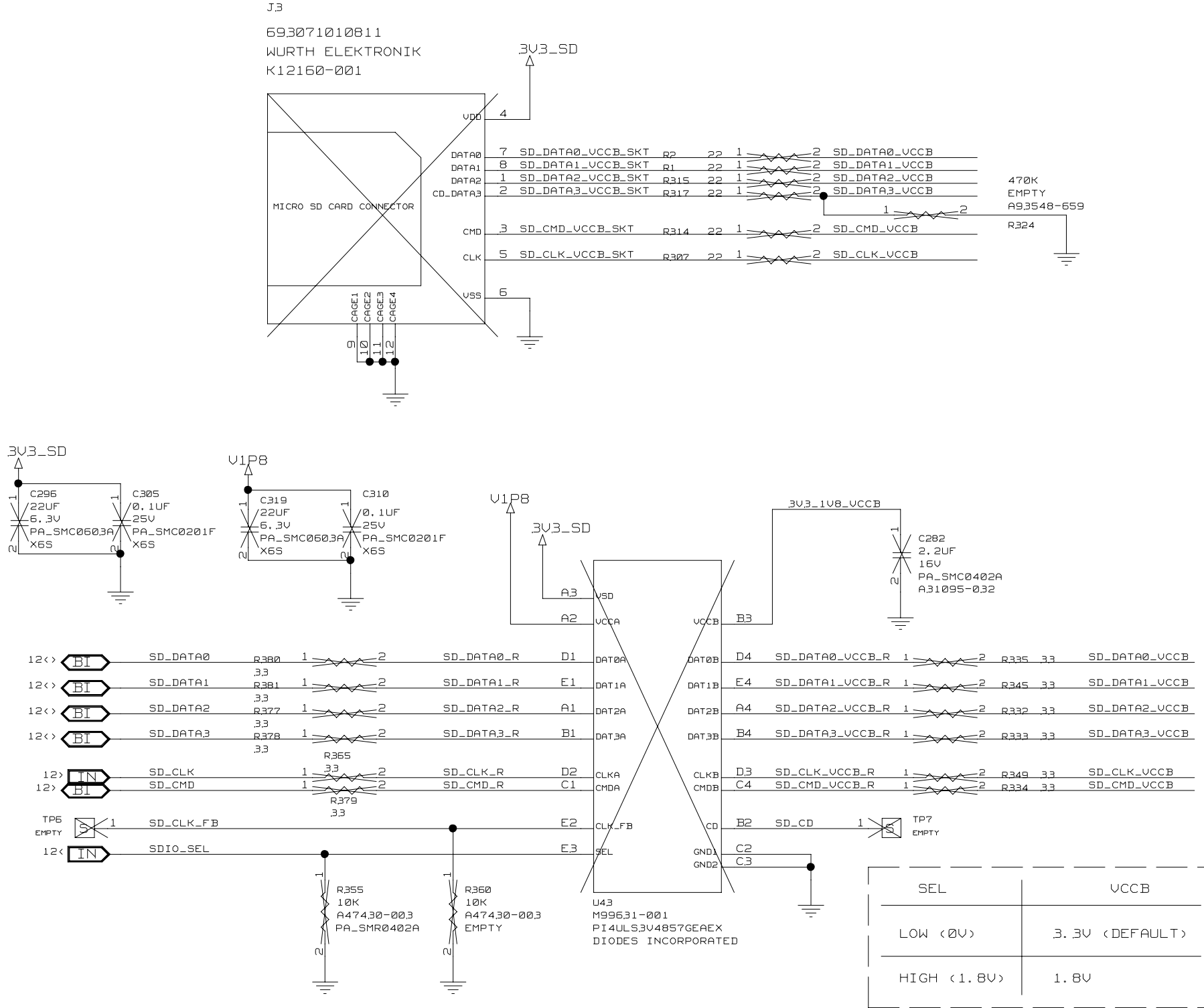
SDM JTAG HDR



Thu May 22 01:34:35 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE	CODE	DOCUMENT NUMBER	REV
		B	34649	305-PD-25-0242	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 28 OF 65	

MICRO SD CARD SOCKET

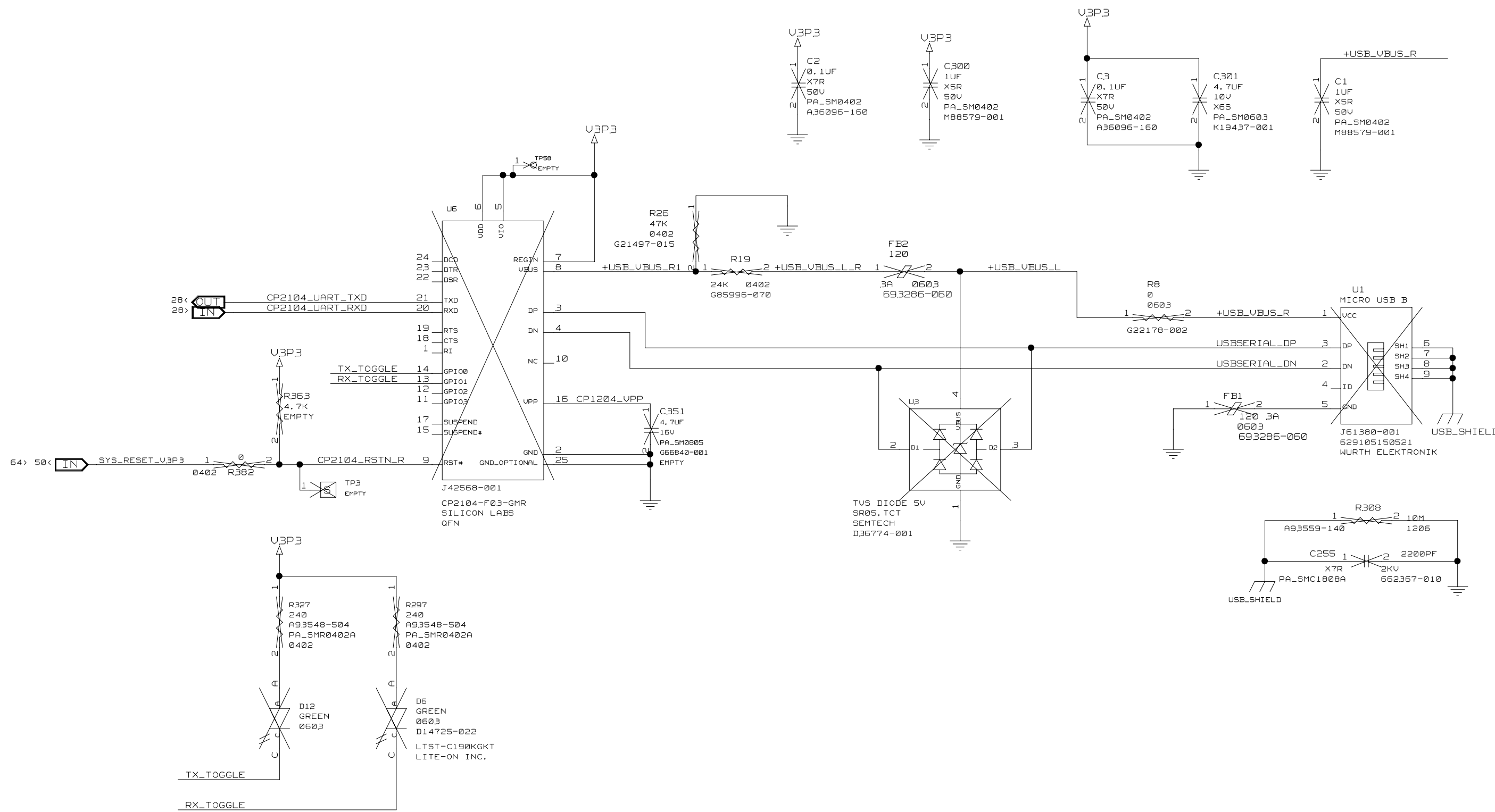


Thu May 22 01:34:35 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

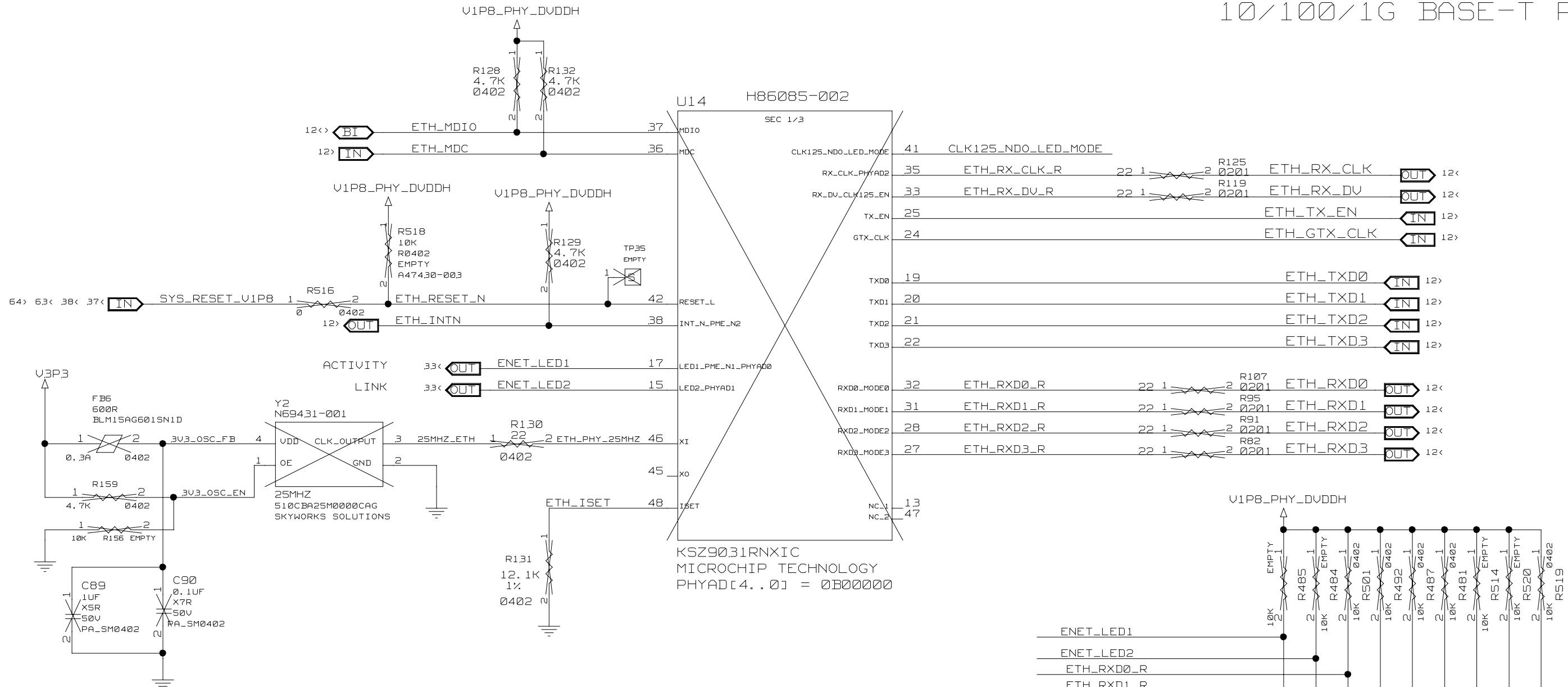


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 29 OF 65



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DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE	CODE	DOCUMENT NUMBER	REV
		B	34649	305-PD-25-0242	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 30 OF 65	



KSZ9031RNXIC
MICROCHIP TECHNOLOGY
PHYAD[4..0] = 0B00000

- ENET_LED1
- ENET_LED2
- ETH_RXD0_R
- ETH_RXD1_R
- ETH_RXD2_R
- ETH_RXD3_R
- ETH_RX_DV_R
- ETH_RX_CLK_R
- CLK125_NDO_LED_MODE

ETHERNET INTERFACE			
NAME	PIN	VALUE	DESCRIPTION
PHYAD2	35	0	ID = 0B00000
PHYAD1	15	0	
PHYAD0	17	0	
MODE3	27	1	"RGMII MODE - ADVERTISE ALL CAPABILITIES (10/100/1000 SPEED HALF-/FULL-DUPLEX), EXCEPT 1000BASE-T HALF-DUPLEX"
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
CLK125_EN	33	0	NO CLOCKOUTPUT FROM PIN41
LED_MODE	41	1	SINGLE LED MODE

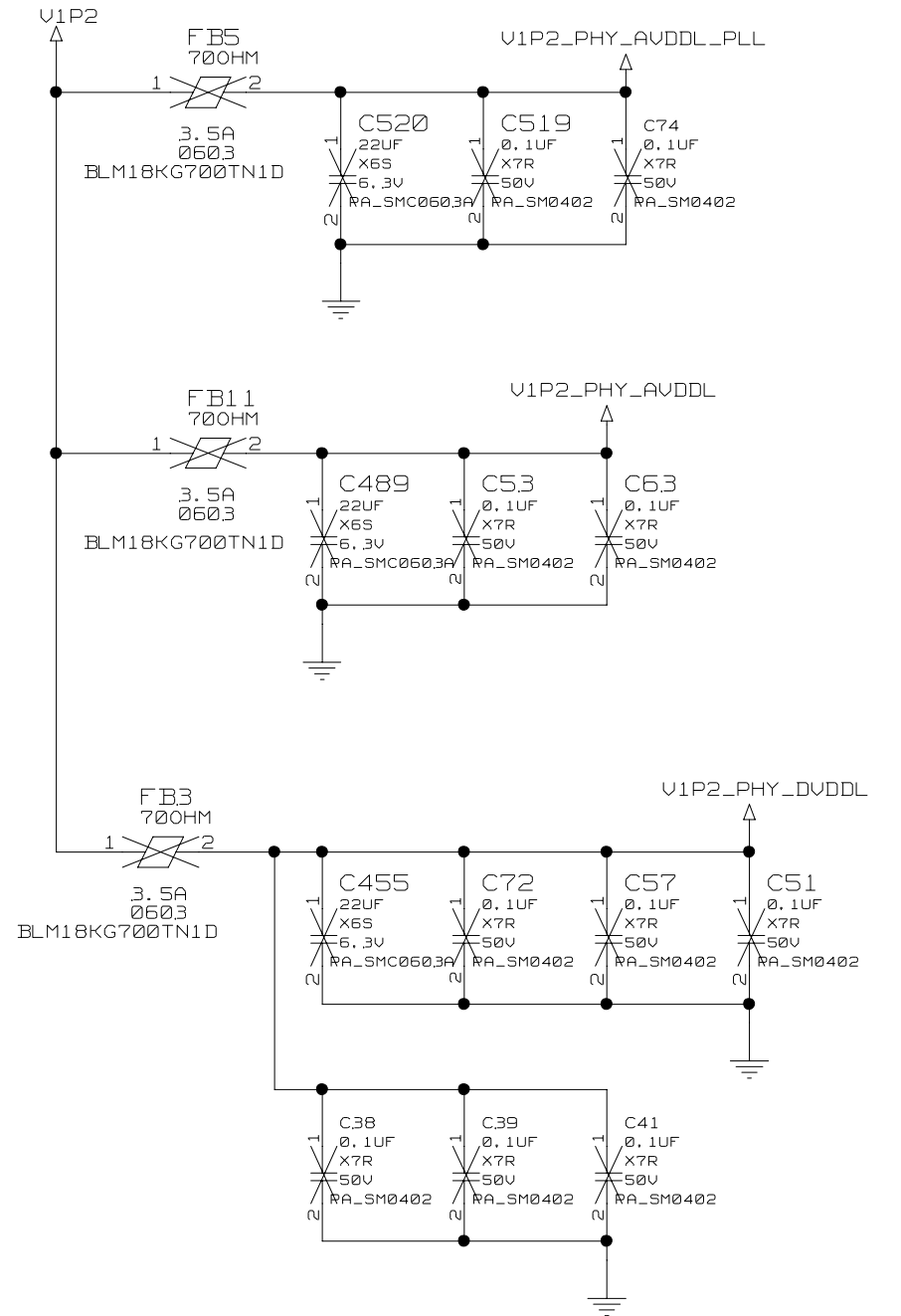
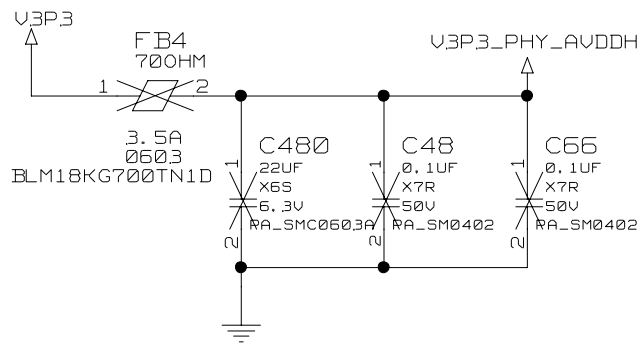
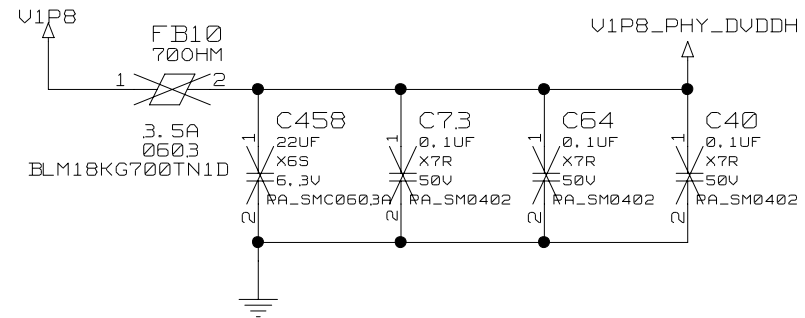
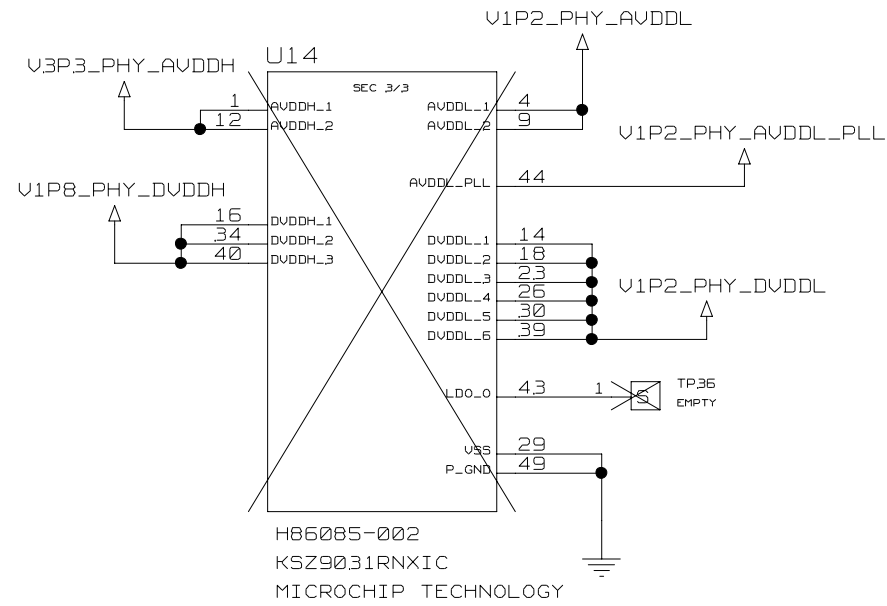
Thu May 22 01:34:36 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 31 OF 65

ETH PHY - POWER & DECAPS



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DEPARTMENT
PLATFORM HW DEVELOPMENT

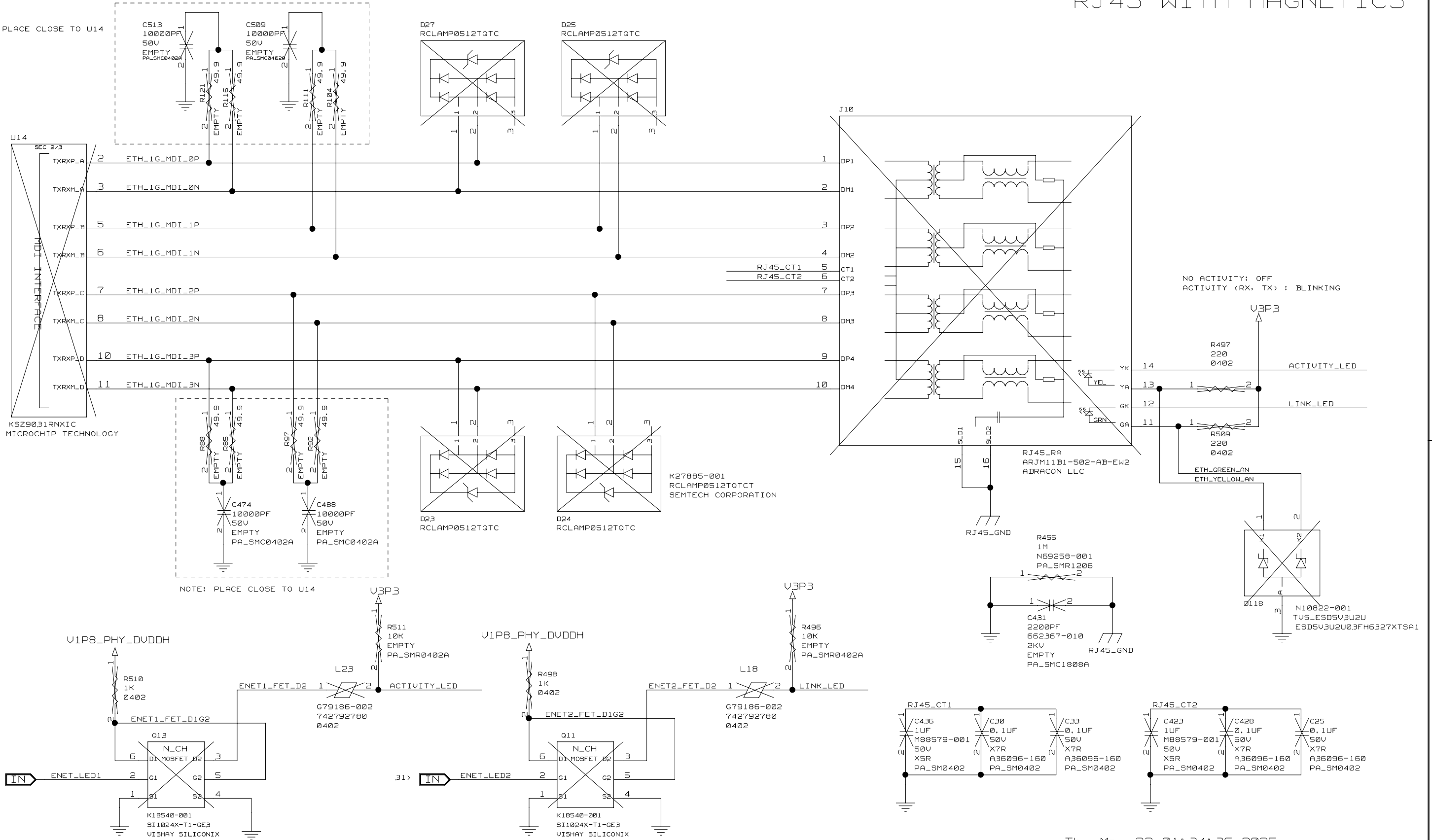


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
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SCALE: DO NOT SCALE DRAWING SHEET 32 OF 65

RJ45 WITH MAGNETICS

NOTE: PLACE CLOSE TO U14



NOTE: PLACE CLOSE TO U14

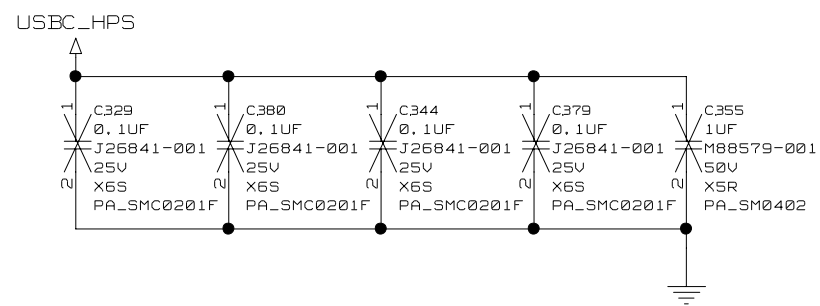
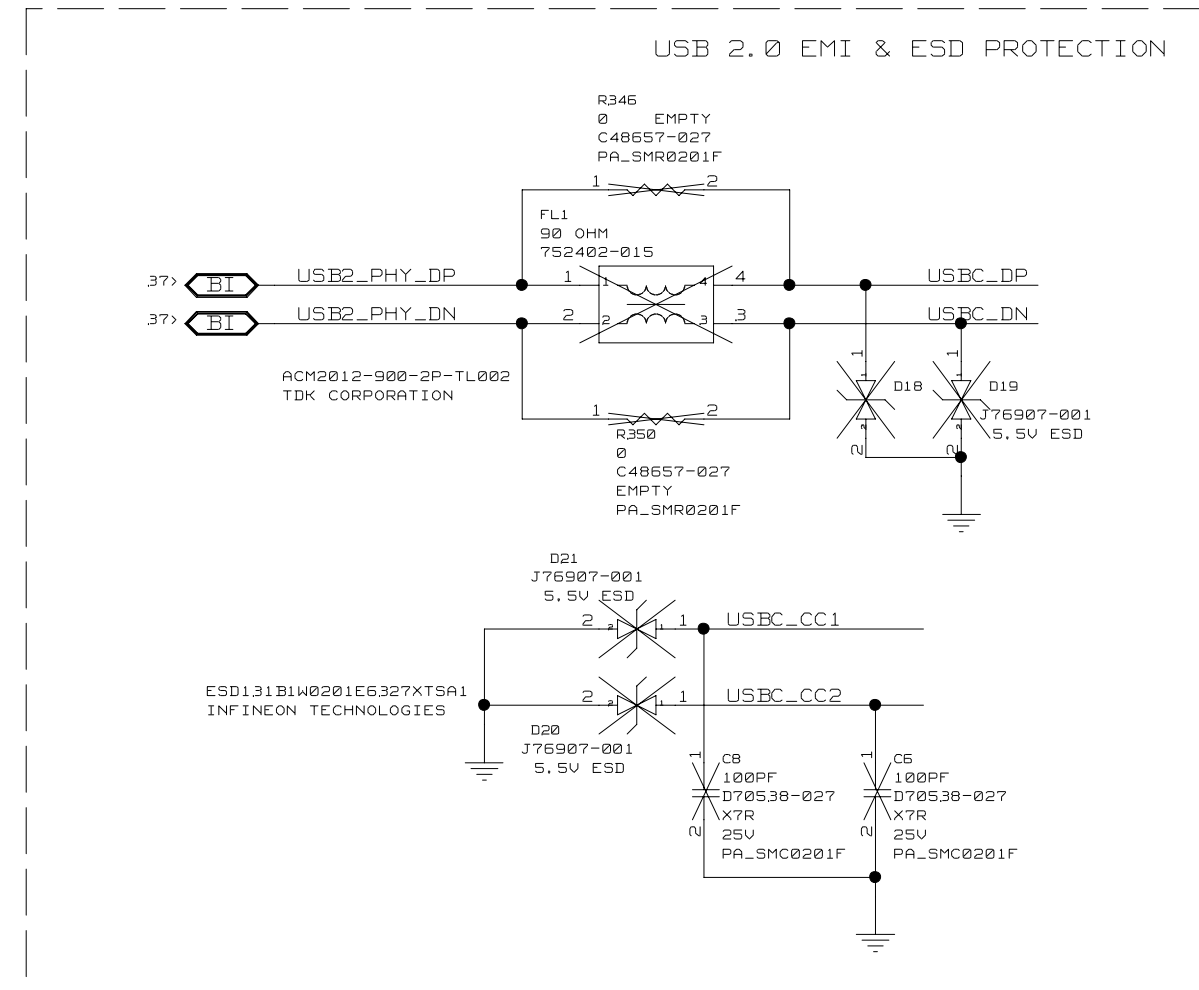
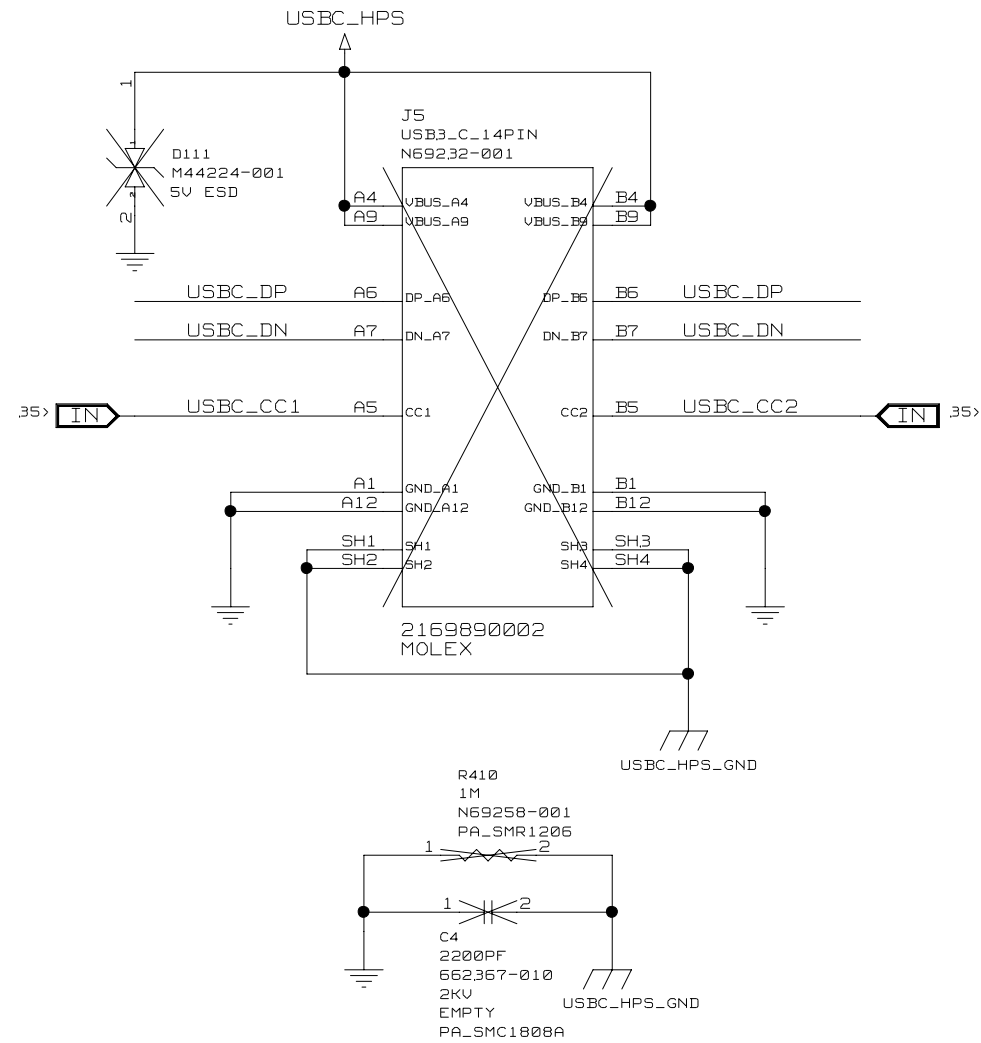
Thu May 22 01:34:36 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 33 OF 65

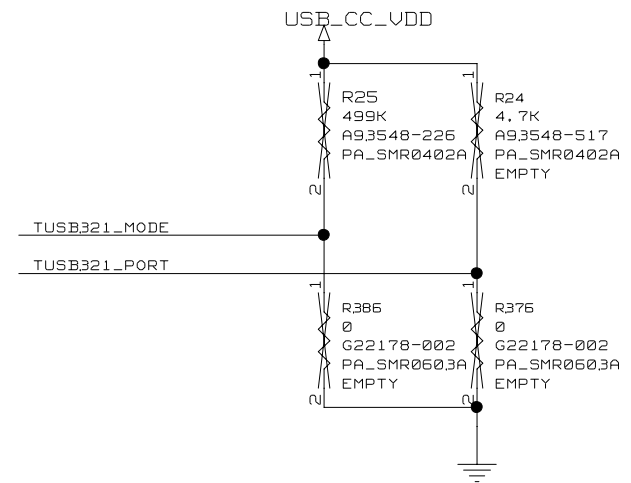
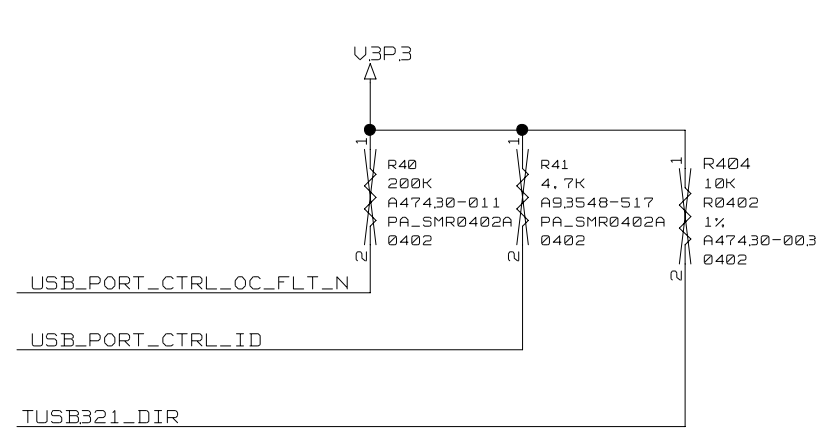
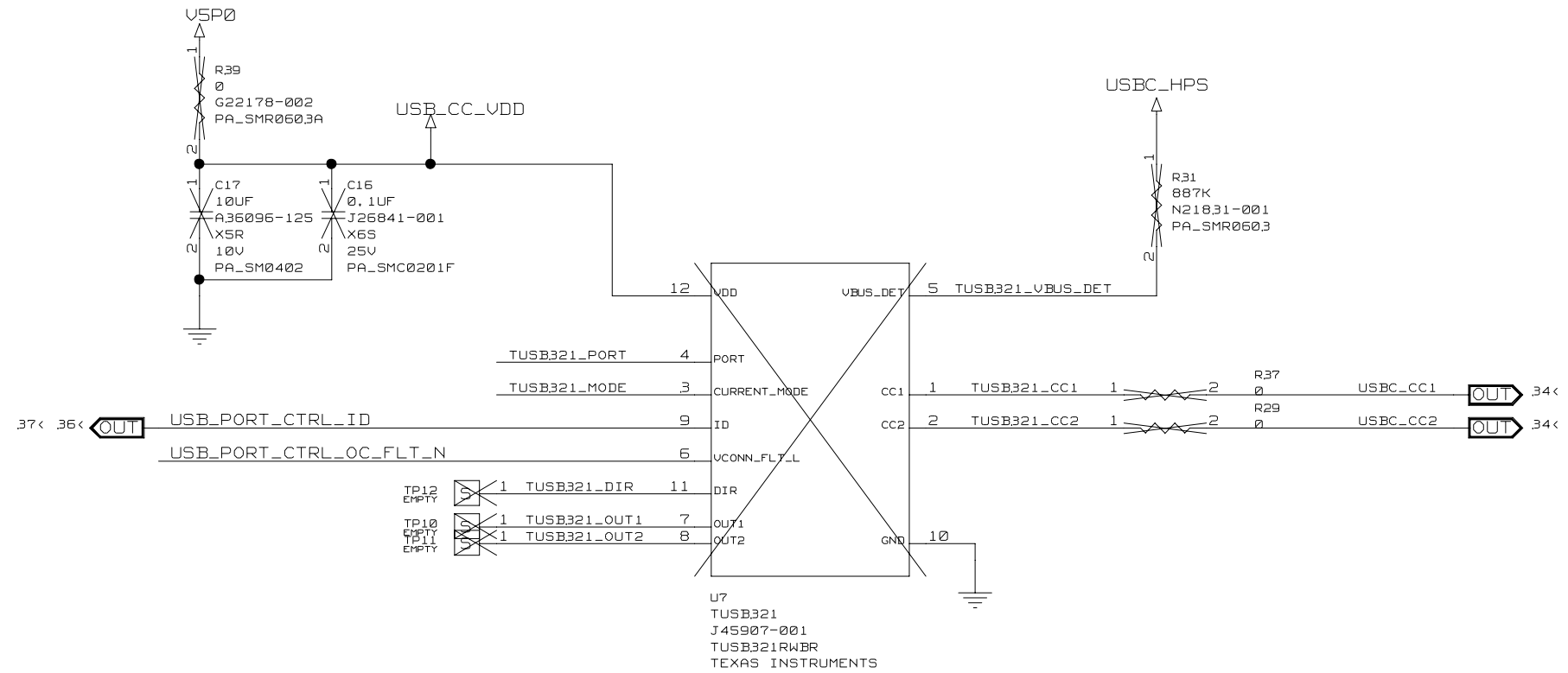
HPS USB TYPE C CONNECTION



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DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 34 OF 65	

HPS USB PORT CONTROLLER

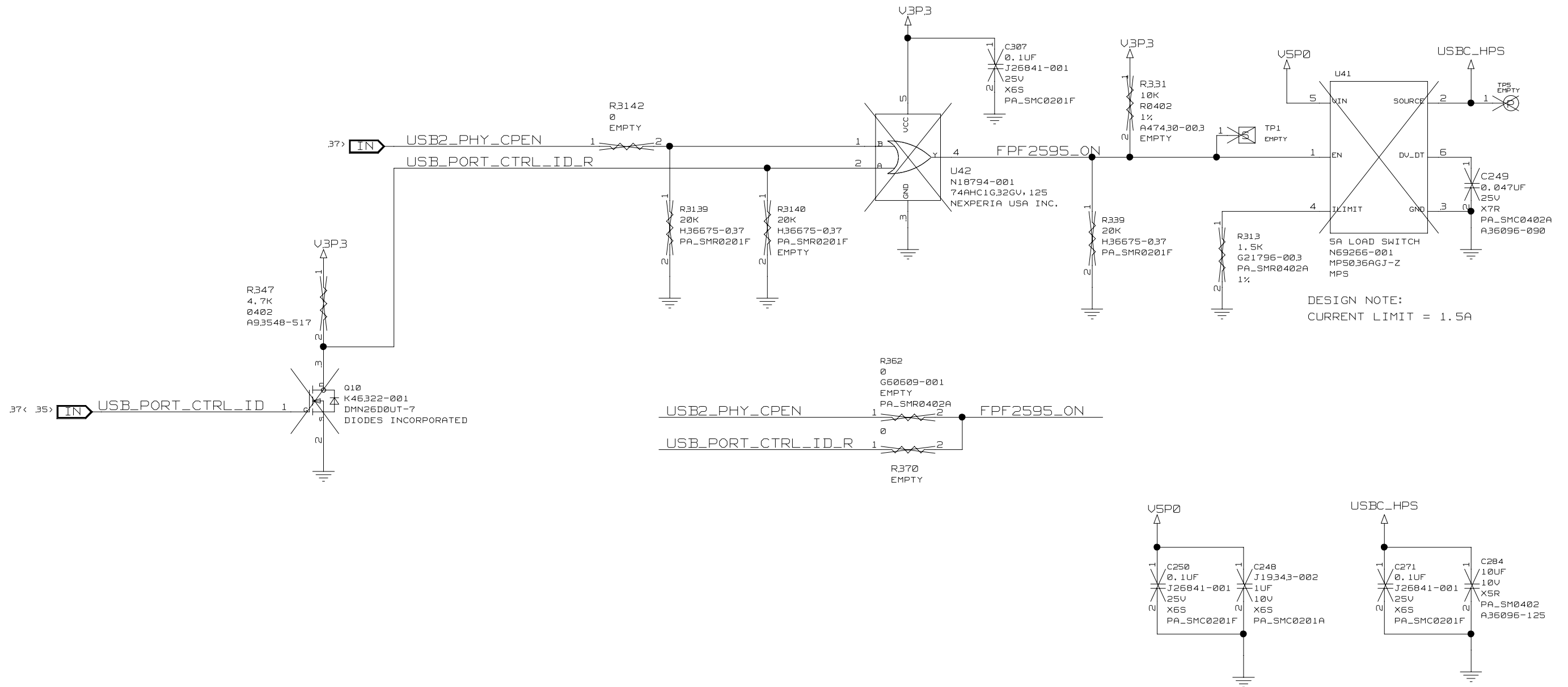


TUSB MANUAL ROLES CONFIG
 DESIGN NOTE :
 DRP MODE : DNI R376 AND DNI R24 <DEFAULT>
 HOST MODE : DNI R376 AND STUFF R24
 DEVICE MODE : STUFF R376 AND DNI R24

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DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 35 OF 65	

HPS USB POWER SWITCH



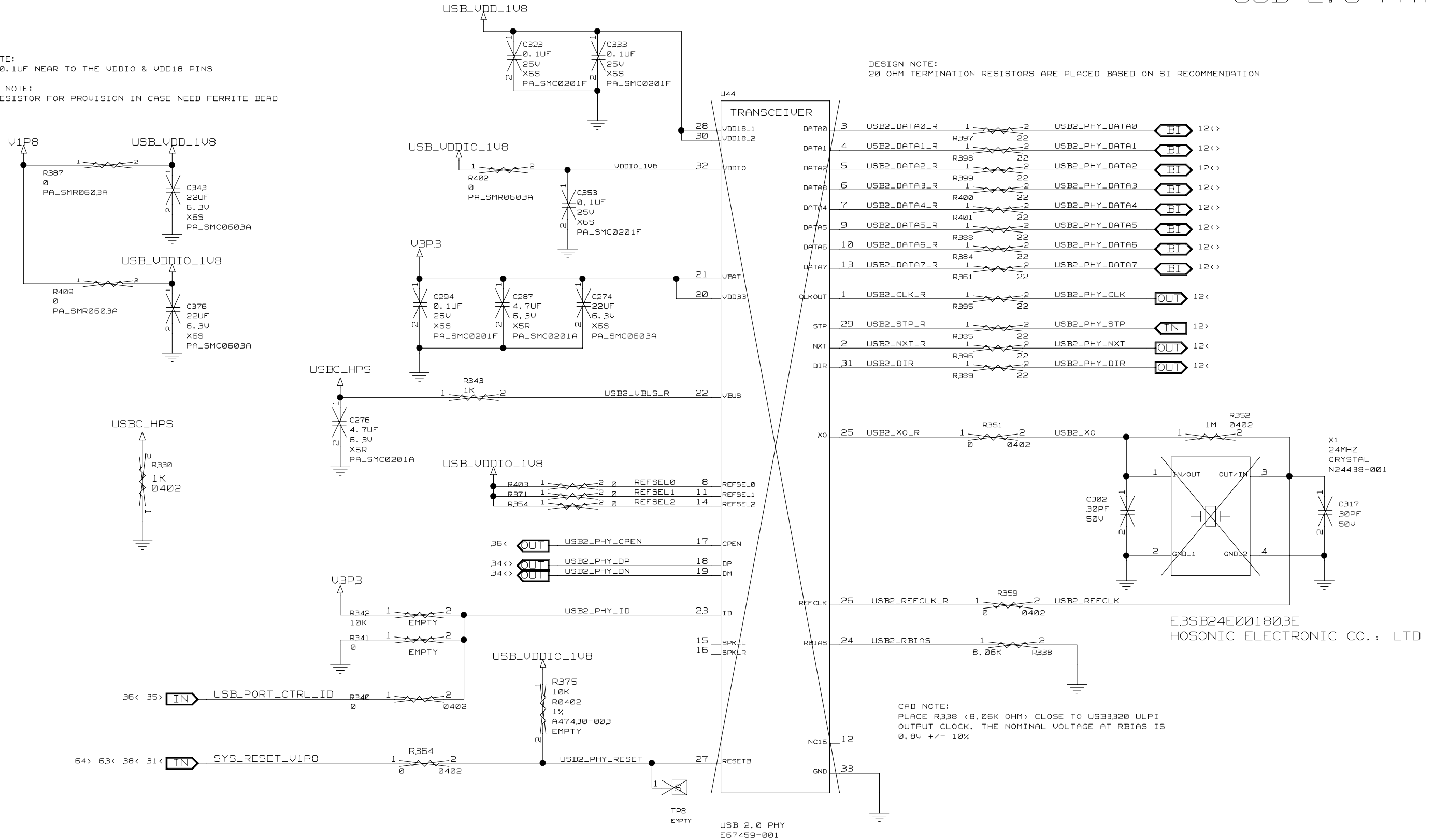
Thu May 22 01:34:36 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 36 OF 65	

CAD NOTE:
PLACE 0.1UF NEAR TO THE UDDIO & UDD18 PINS

DESIGN NOTE:
0OHM RESISTOR FOR PROVISION IN CASE NEED FERRITE BEAD

DESIGN NOTE:
20 OHM TERMINATION RESISTORS ARE PLACED BASED ON SI RECOMMENDATION



CAD NOTE:
PLACE R338 (8.06K OHM) CLOSE TO USB3320 ULP1
OUTPUT CLOCK. THE NOMINAL VOLTAGE AT RBIAIS IS
0.8V +/- 10%.

E.35B24E001803E
HOSONIC ELECTRONIC CO., LTD

USB 2.0 PHY
E67459-001

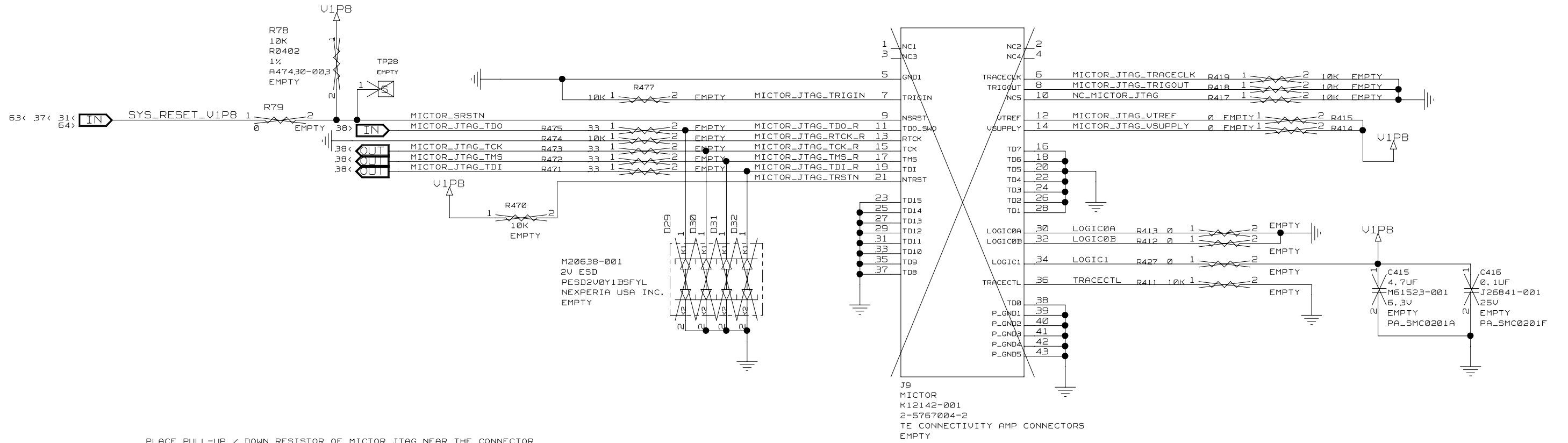
Thu May 22 01:34:37 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

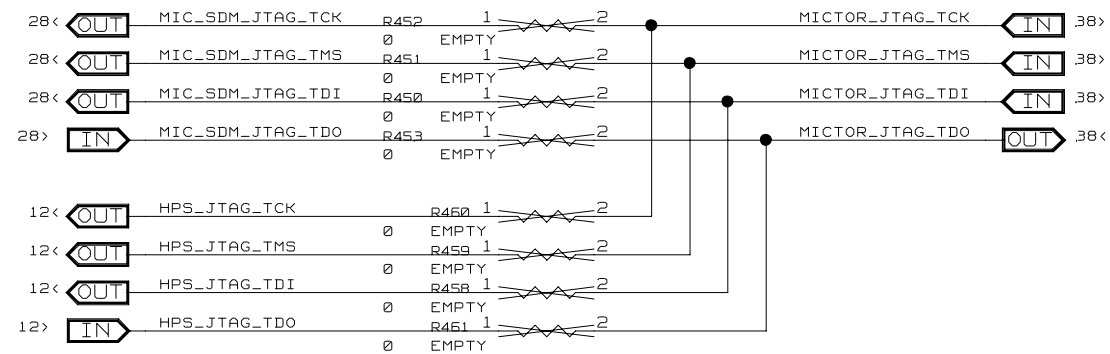
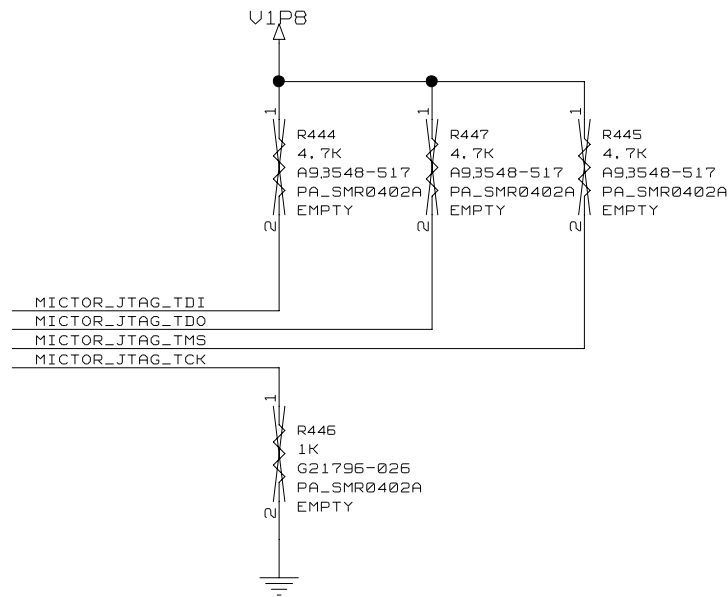


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 37 OF 65

MICTOR 38 JTAG HEADER



PLACE PULL-UP / DOWN RESISTOR OF MICTOR_JTAG NEAR THE CONNECTOR



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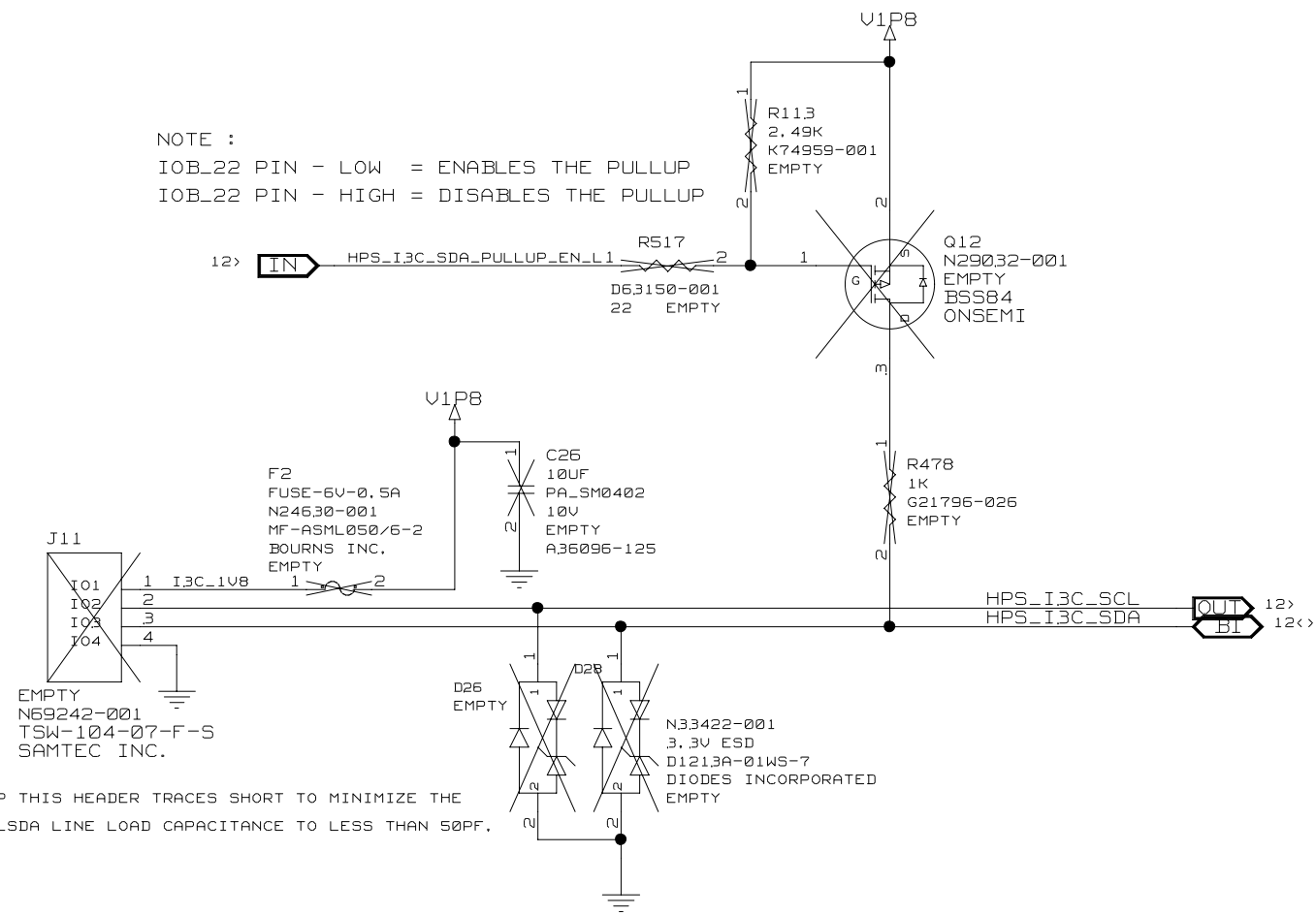
DEPARTMENT
PLATFORM HW DEVELOPMENT



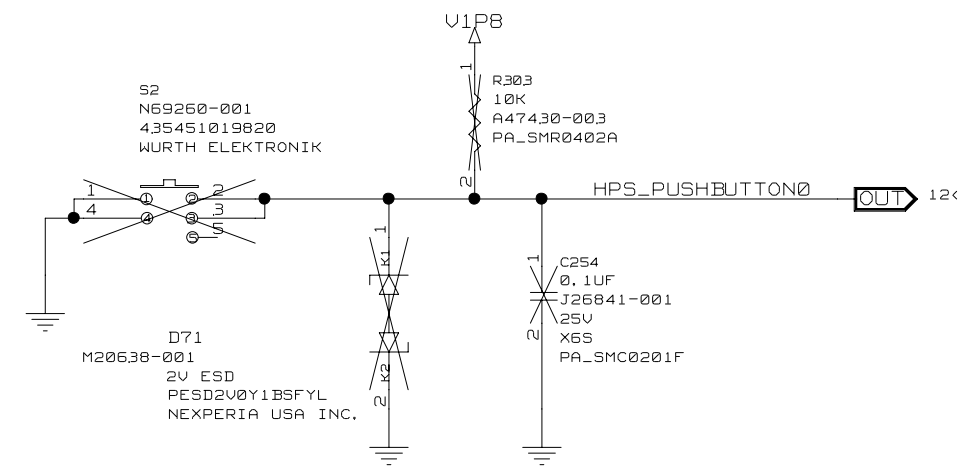
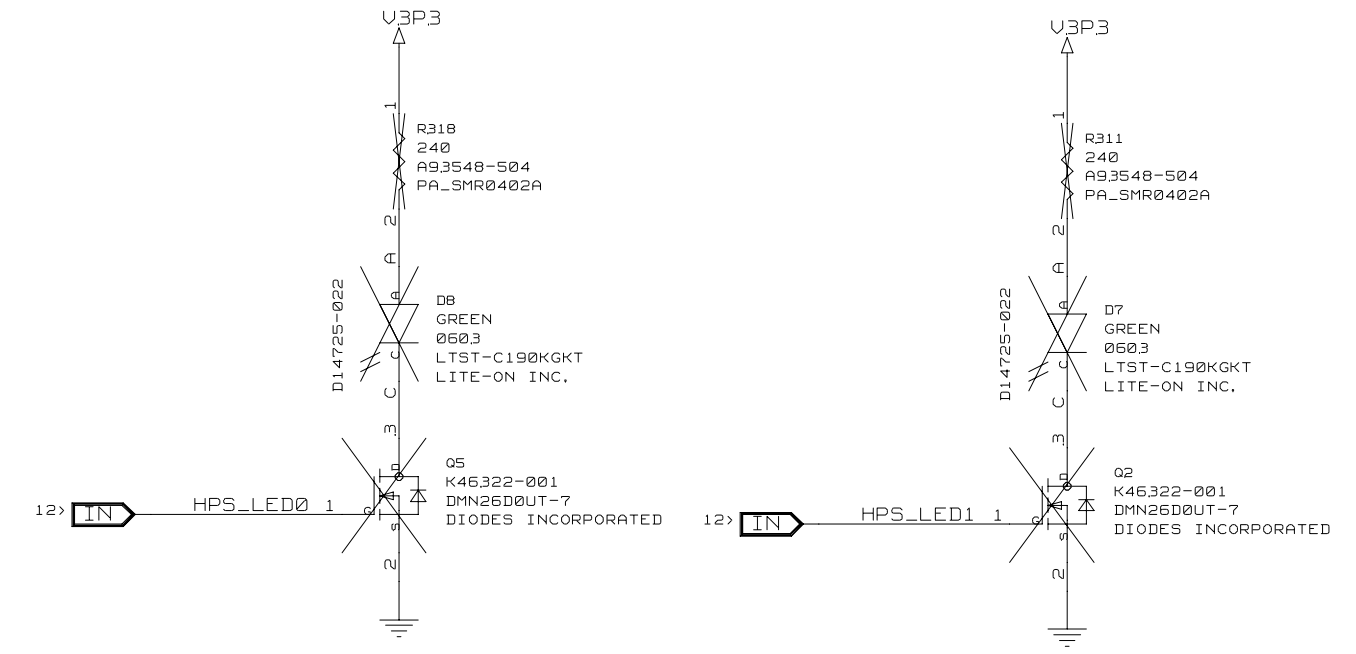
SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 38 OF 65

HPS USER IO

NOTE :
IOB_22 PIN - LOW = ENABLES THE PULLUP
IOB_22 PIN - HIGH = DISABLES THE PULLUP



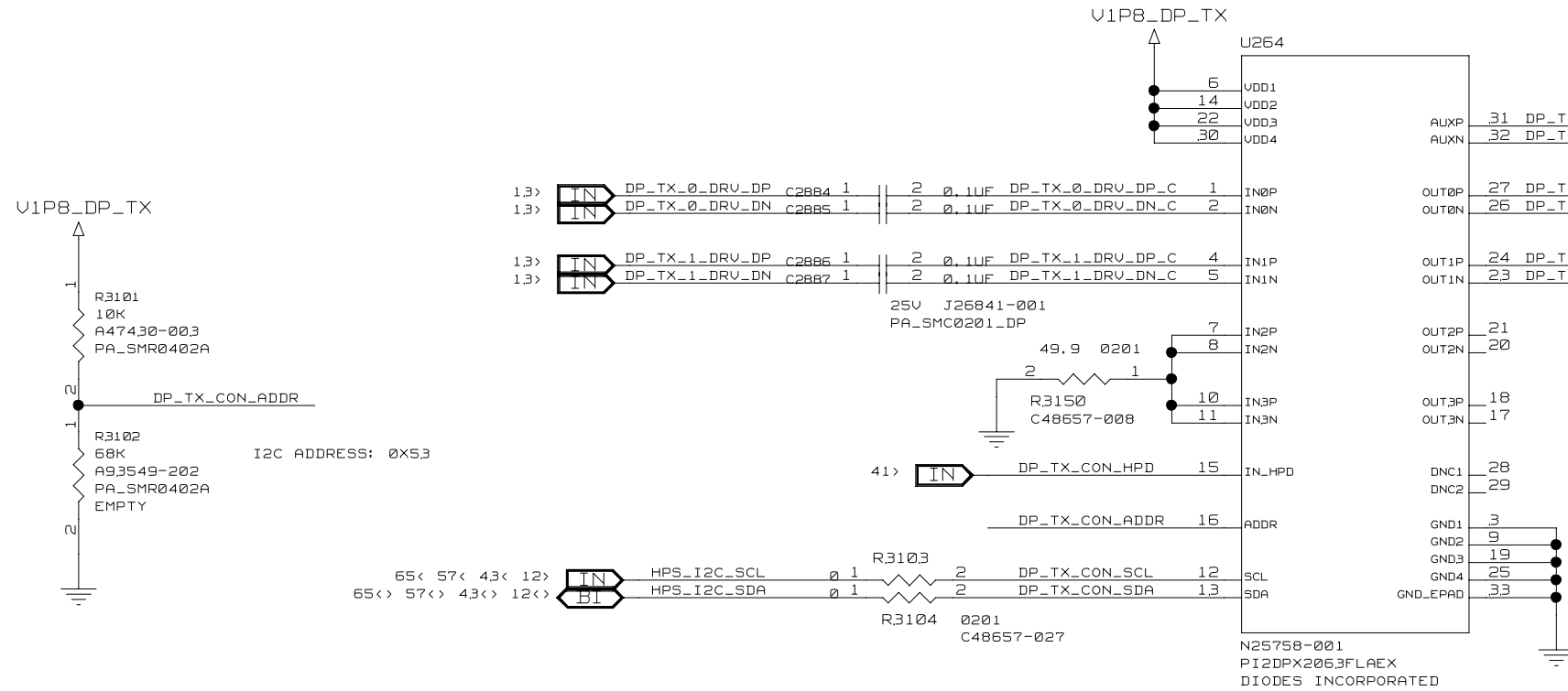
NOTE:KEEP THIS HEADER TRACES SHORT TO MINIMIZE THE I3C_SDA LINE LOAD CAPACITANCE TO LESS THAN 50PF.



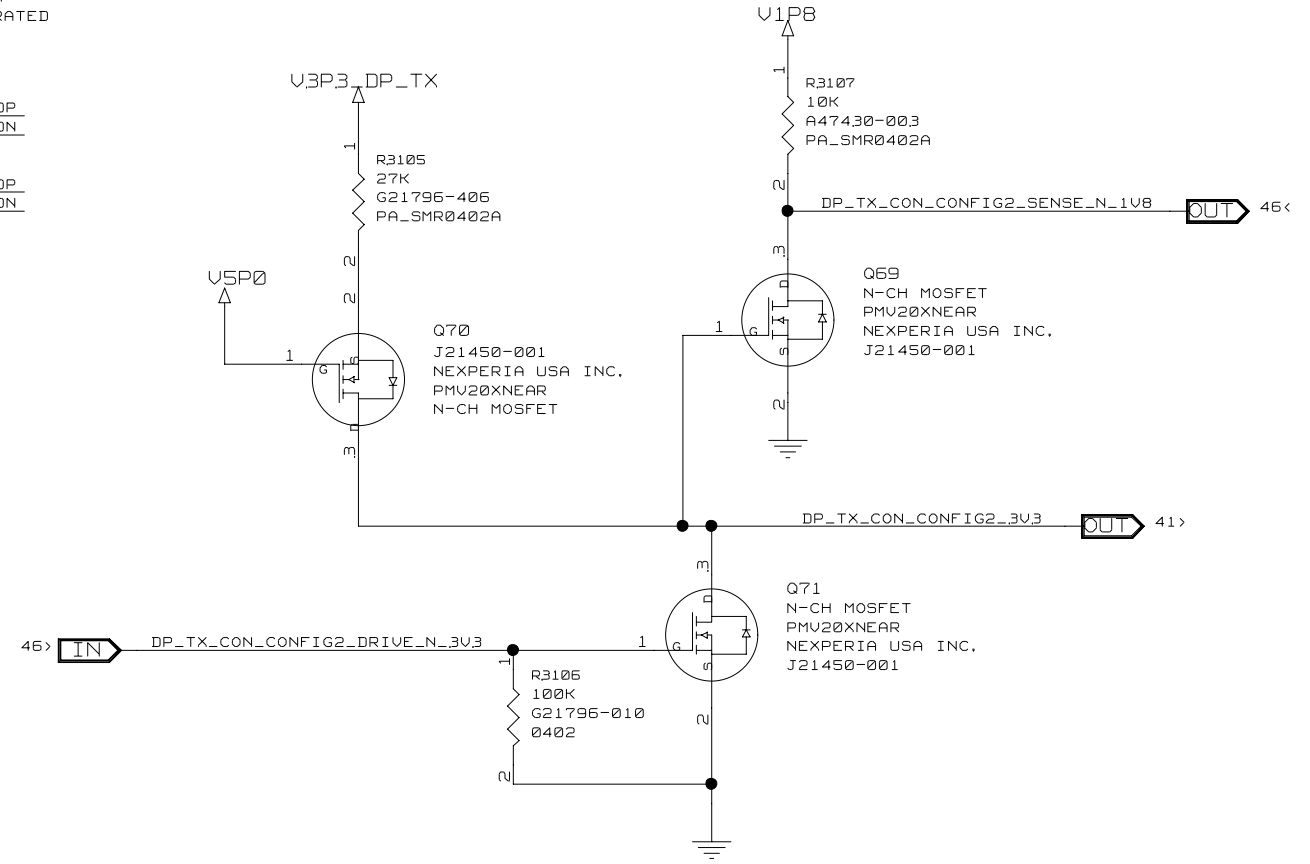
Thu May 22 01:34:37 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE: DO NOT SCALE DRAWING		SHEET 39 OF 65			

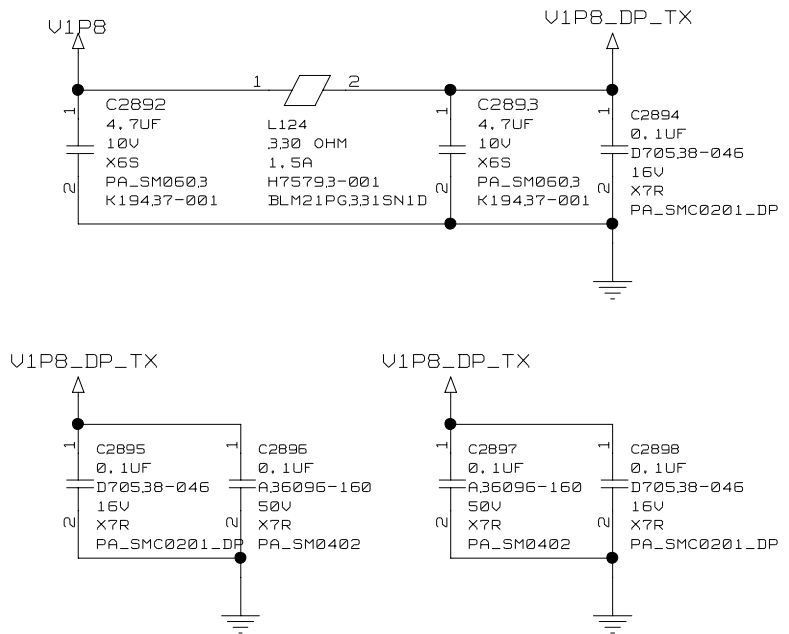
DP1.4 TX REDDRIVER



DP1.4 TX CEC SENSE/DRIVE



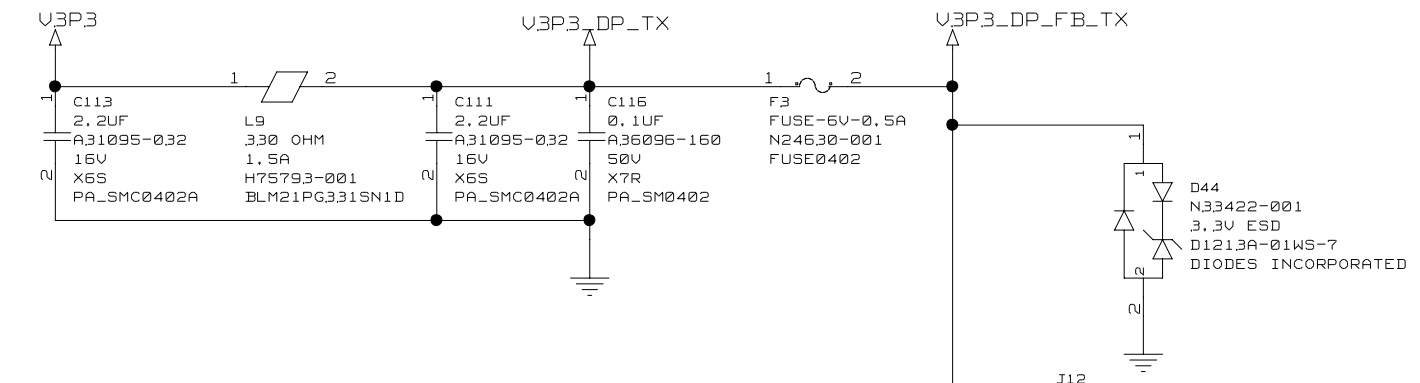
DP_TX_0_DRV_DP	R31221	2	0	EMPTY	DP_TX_0_DP	C2917	1	2	0.1UF	EMPTY	DP_TX_0_CON_DP
DP_TX_0_DRV_DN	R31231	2	0	EMPTY	DP_TX_0_DN	C2918	1	2	0.1UF	EMPTY	DP_TX_0_CON_DN
DP_TX_1_DRV_DP	R31241	2	0	EMPTY	DP_TX_1_DP	C2919	1	2	0.1UF	EMPTY	DP_TX_1_CON_DP
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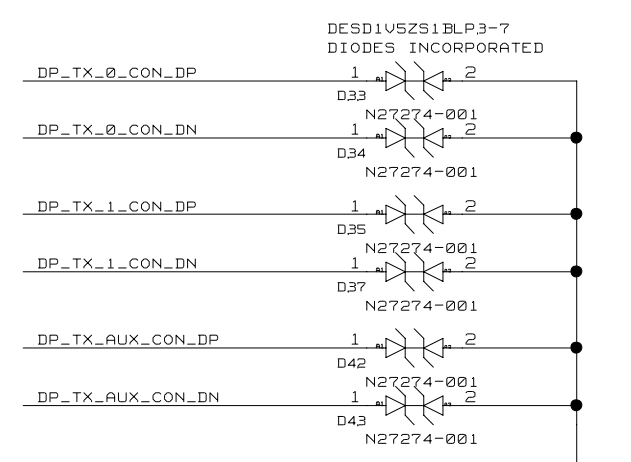
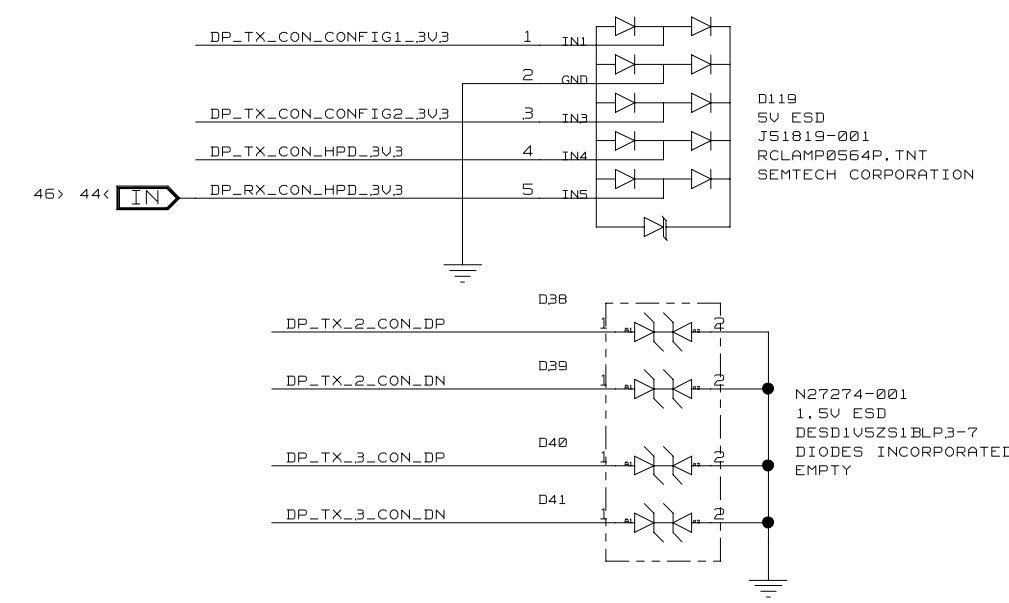
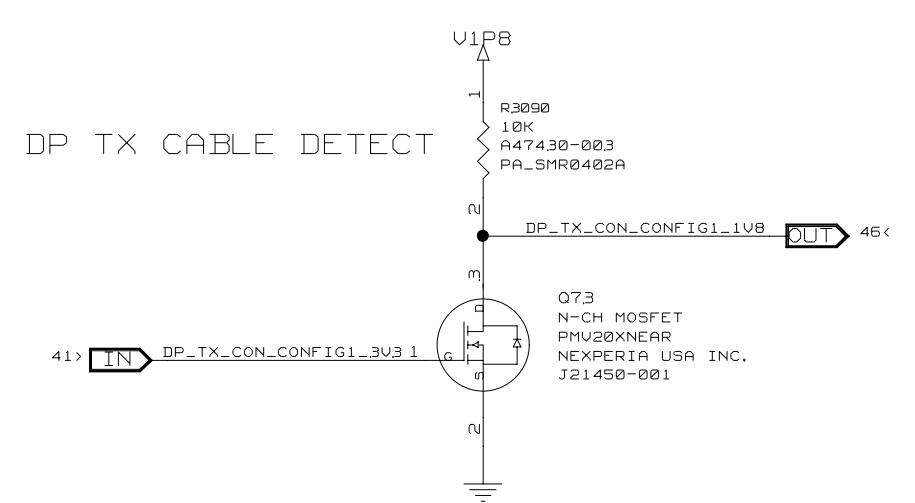
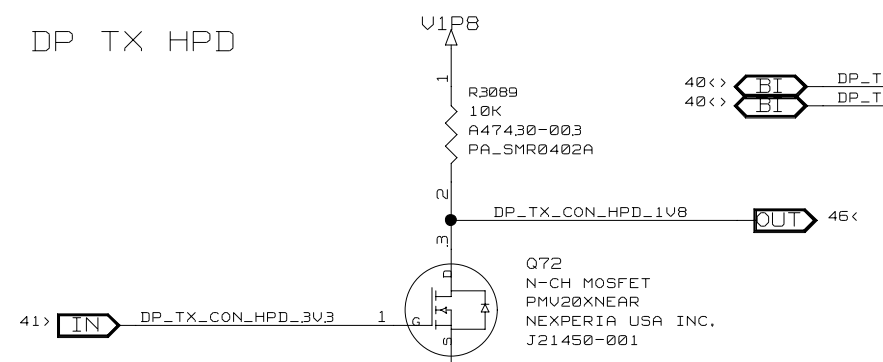
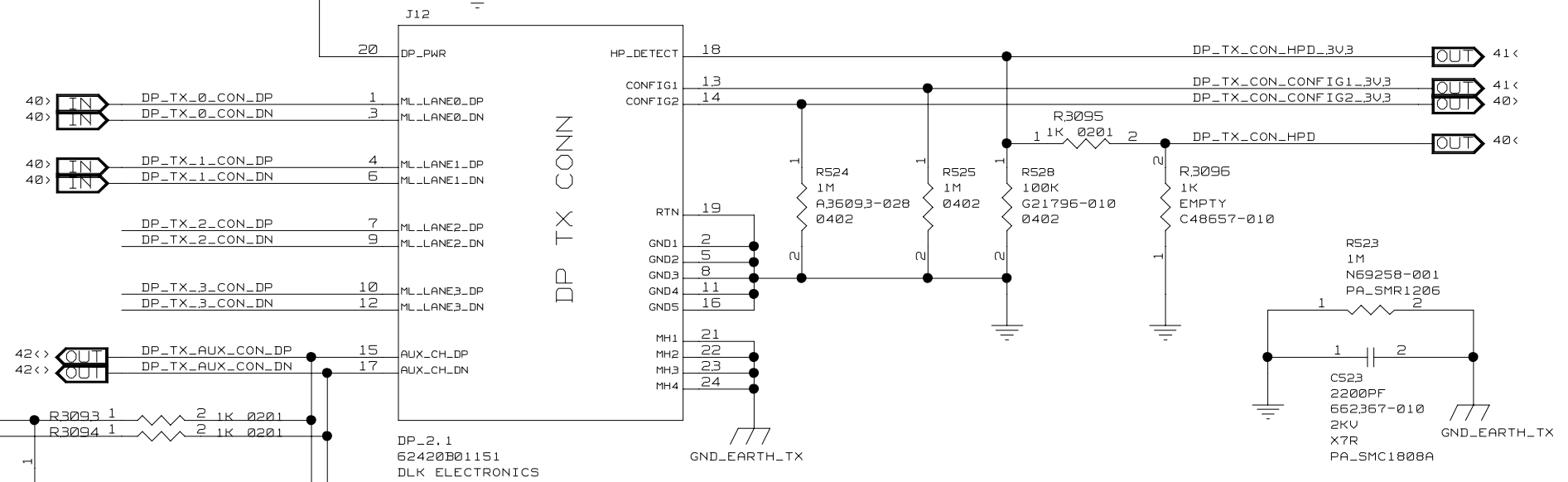
Thu May 22 01:34:37 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera™	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 40 OF 65	

DP1.4 TX CONNECTOR

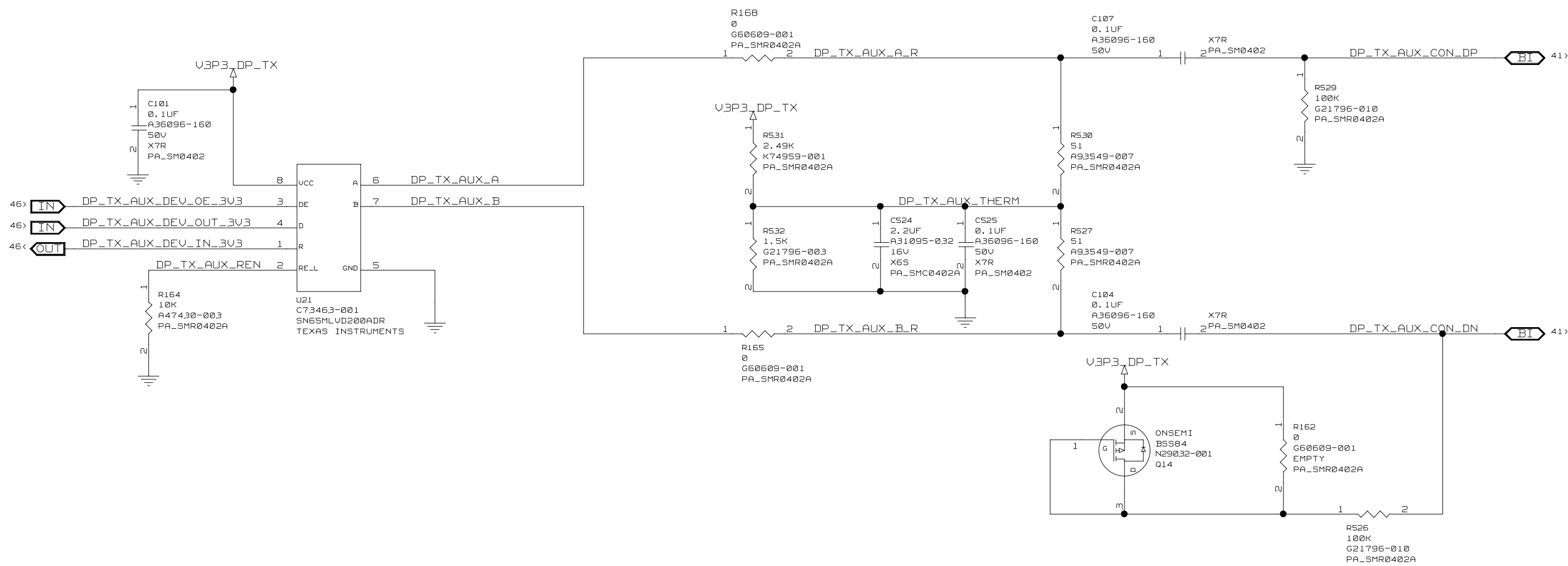


DESIGN NOTE:
USE STANDARD DP MATING CABLE WITH NO-POWER PIN WIRE



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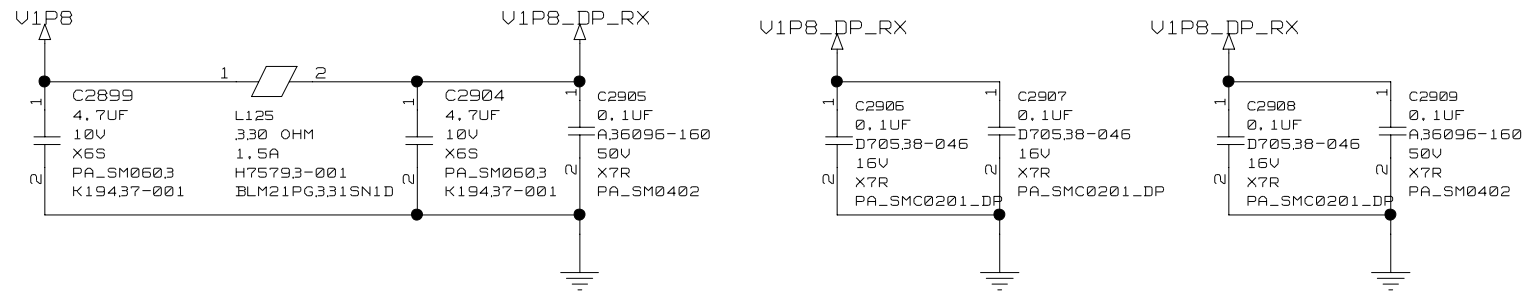
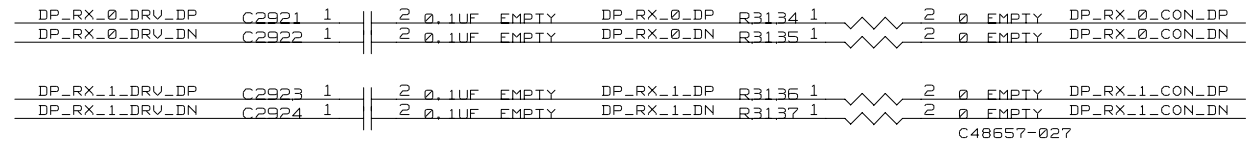
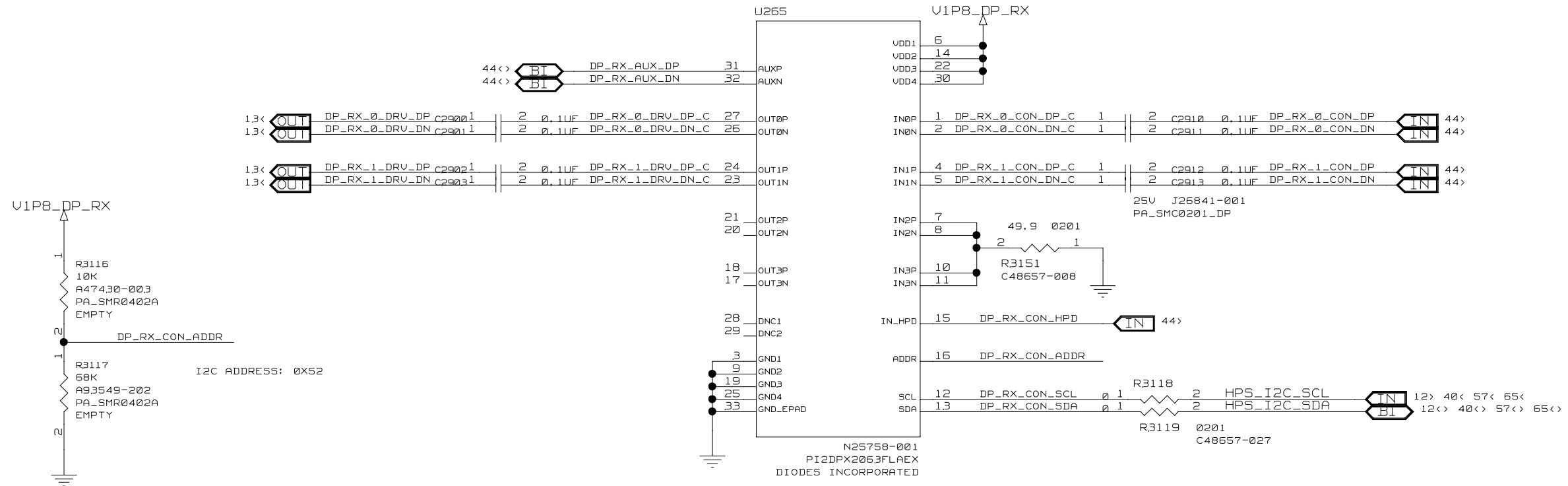
DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE	CODE	DOCUMENT NUMBER	REV
		B	34649	305-PD-25-0242	2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 41 OF 65	



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DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 42 OF 65	

DP1.4 RX REDRIVER



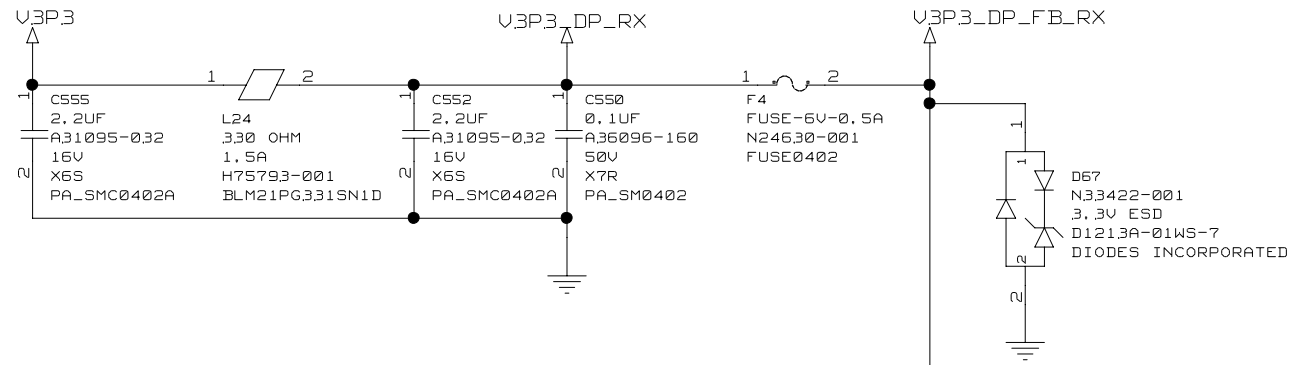
Thu May 22 01:34:37 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

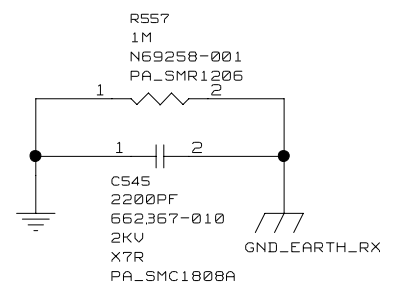
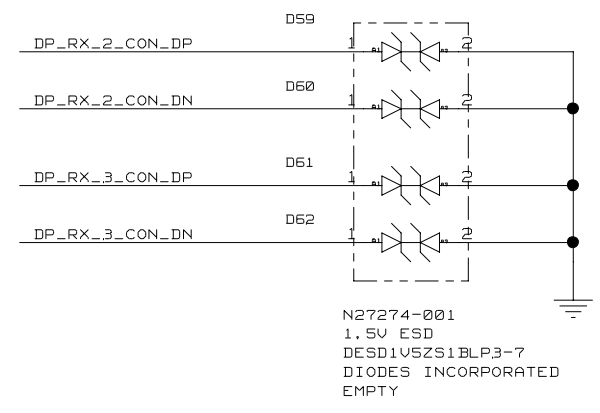
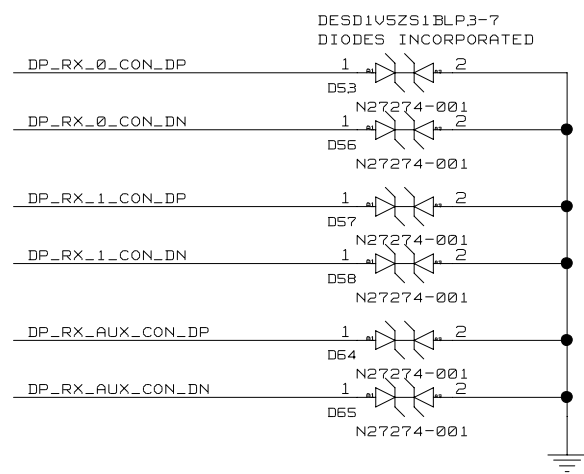
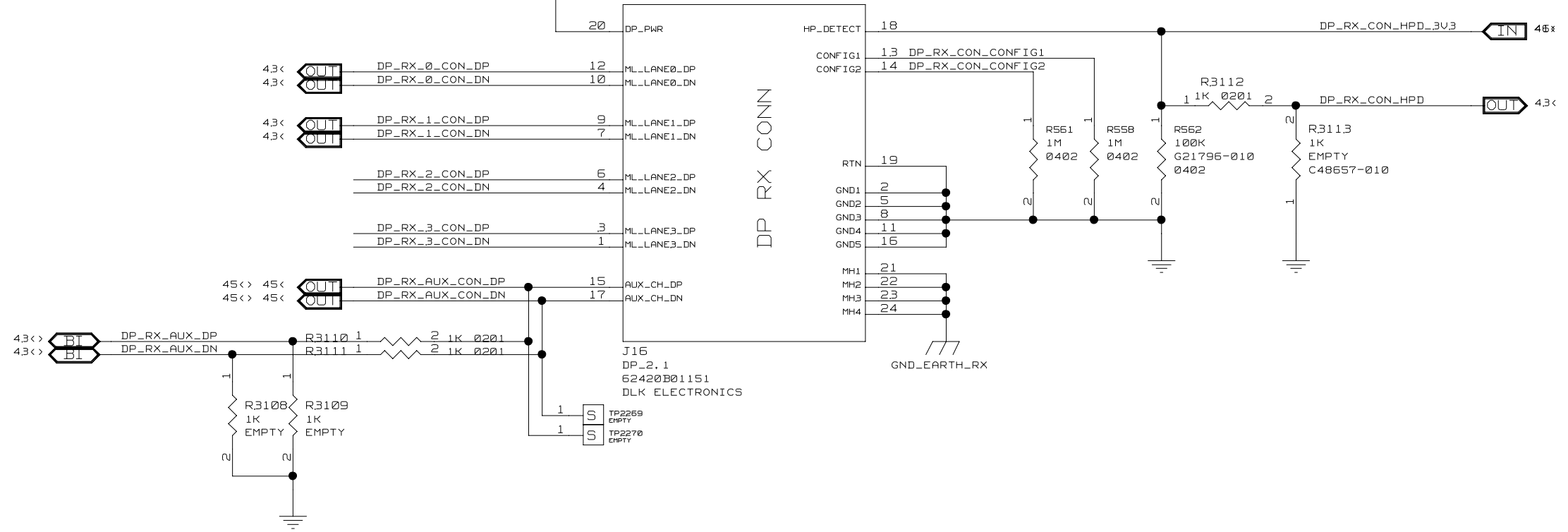


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 43 OF 65

DP1.4 RX CONNECTOR



DESIGN NOTE:
USE STANDARD DP MATING CABLE WITH NO-POWER PIN WIRE



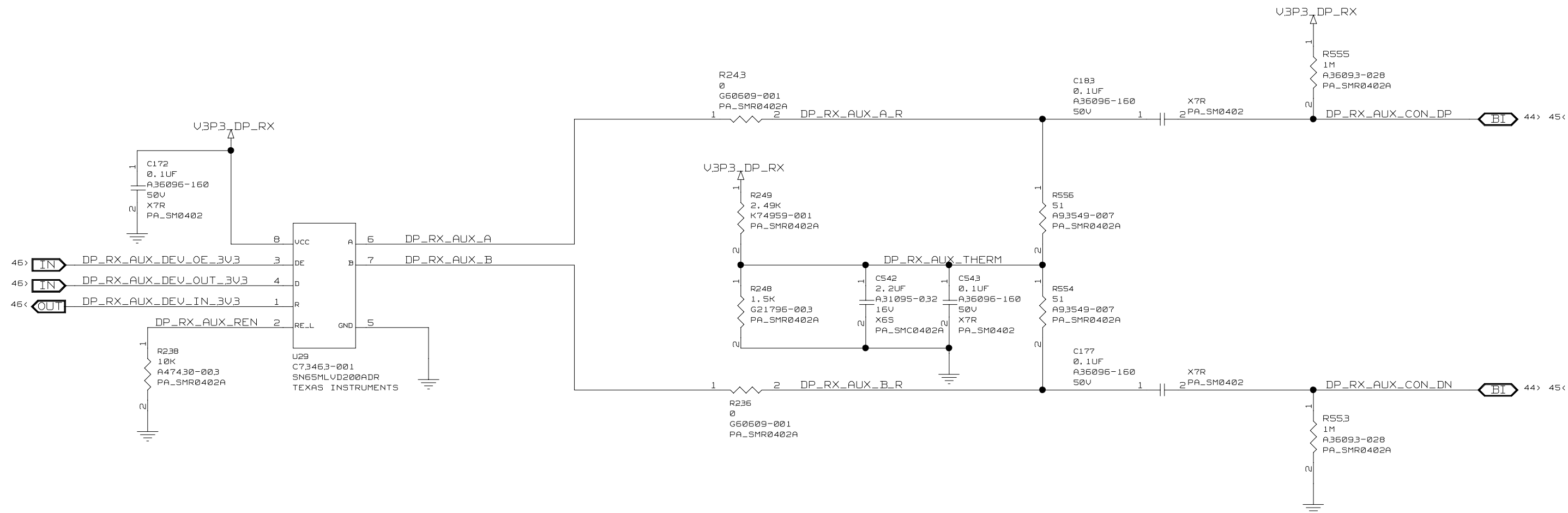
Thu May 22 01:34:38 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

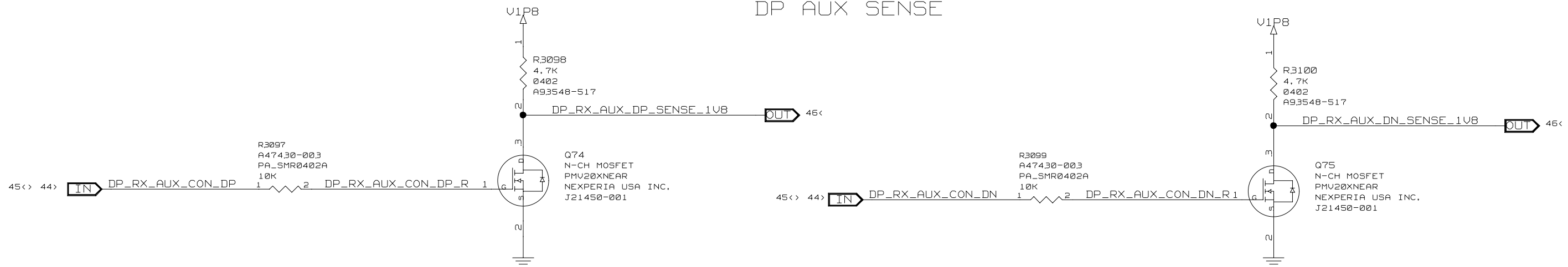


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:	DO NOT SCALE DRAWING		SHEET 44 OF 65

DP RX AUX



DP AUX SENSE



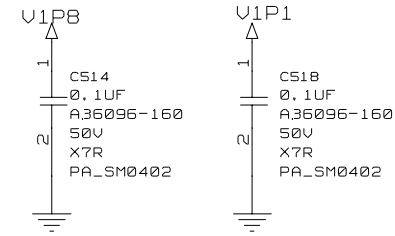
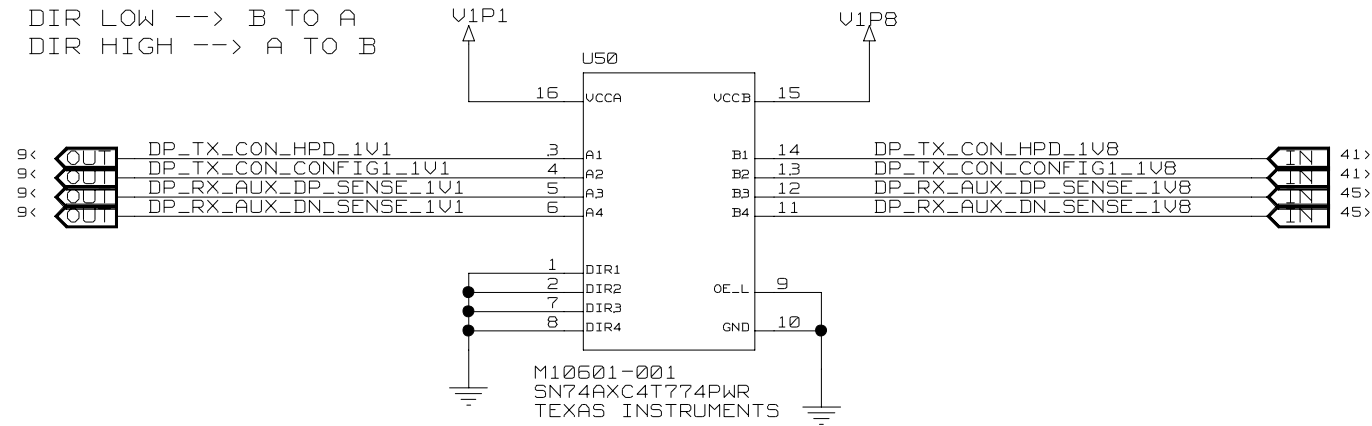
Thu May 22 01:34:38 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



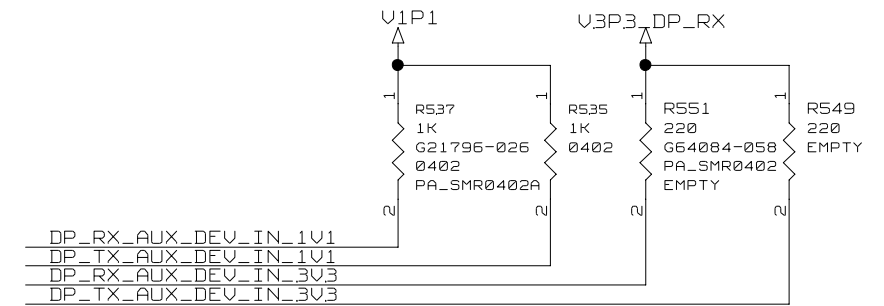
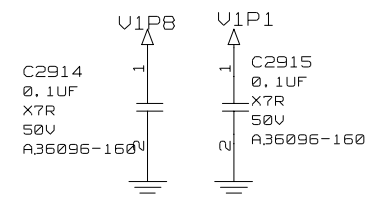
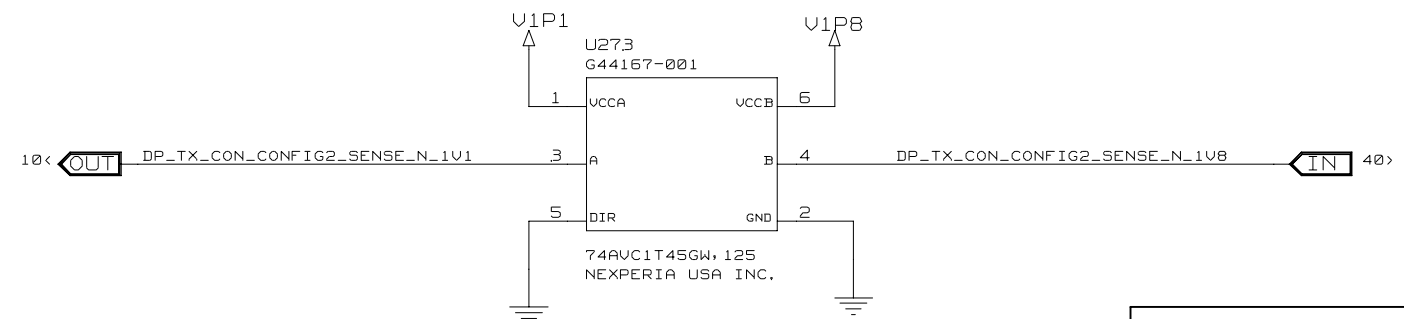
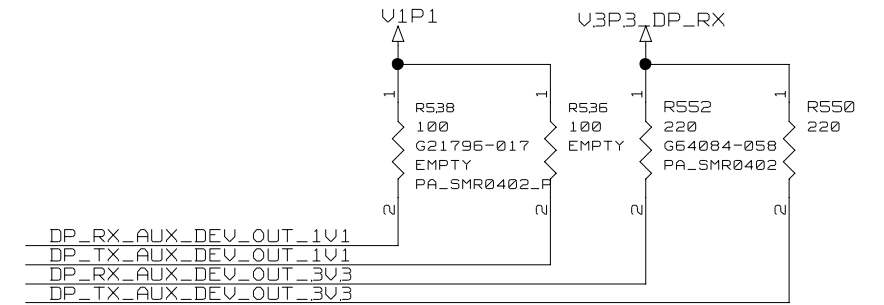
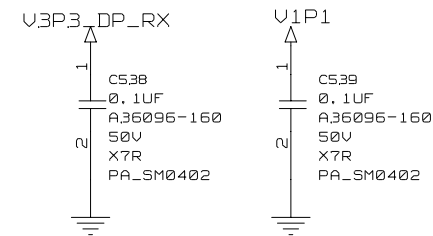
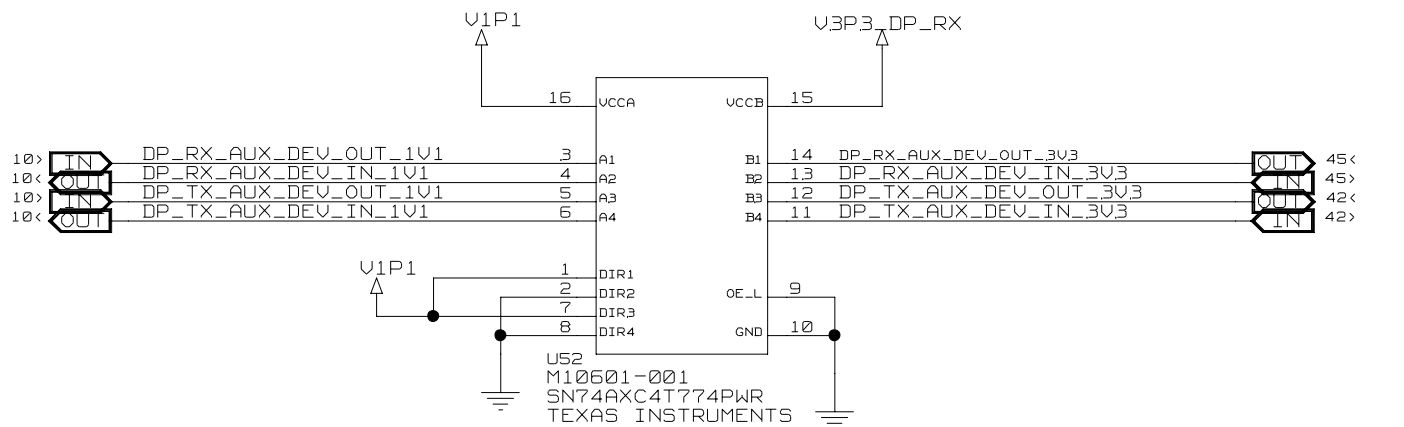
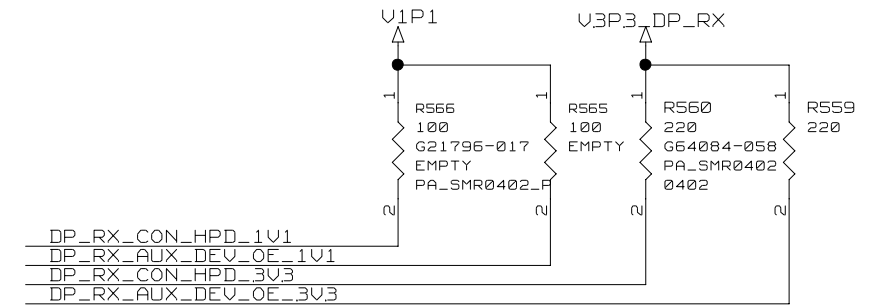
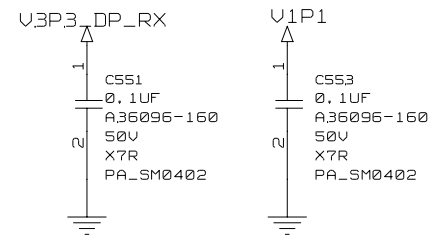
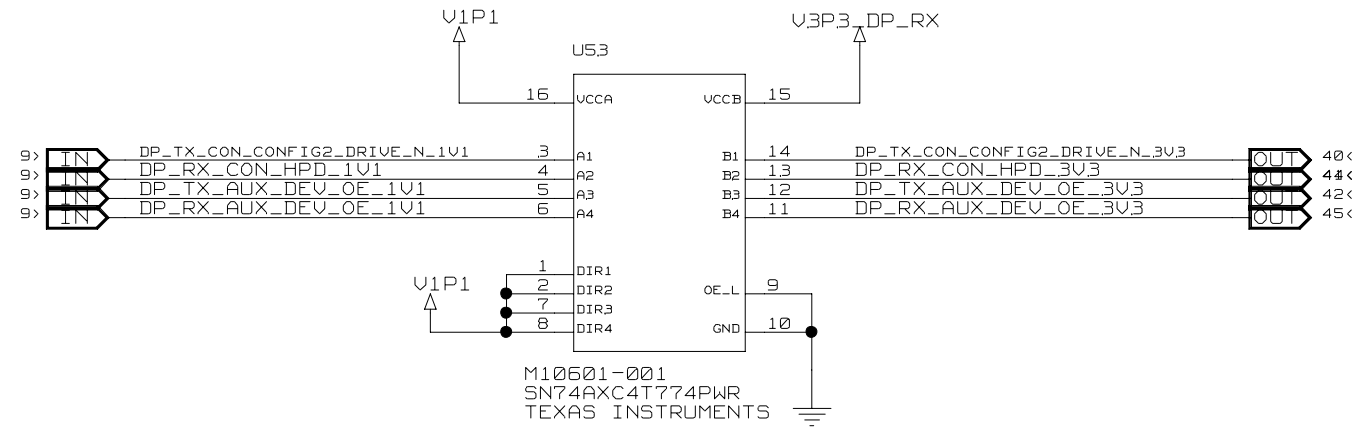
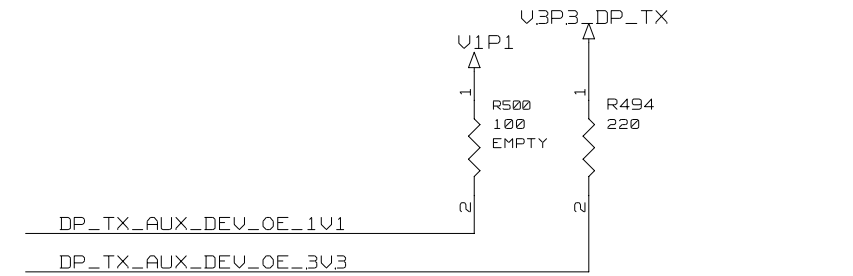
SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 45 OF 65

DIR LOW --> B TO A
DIR HIGH --> A TO B



DP - LEVEL SHIFTERS

FOR TX / RX CONTROLS



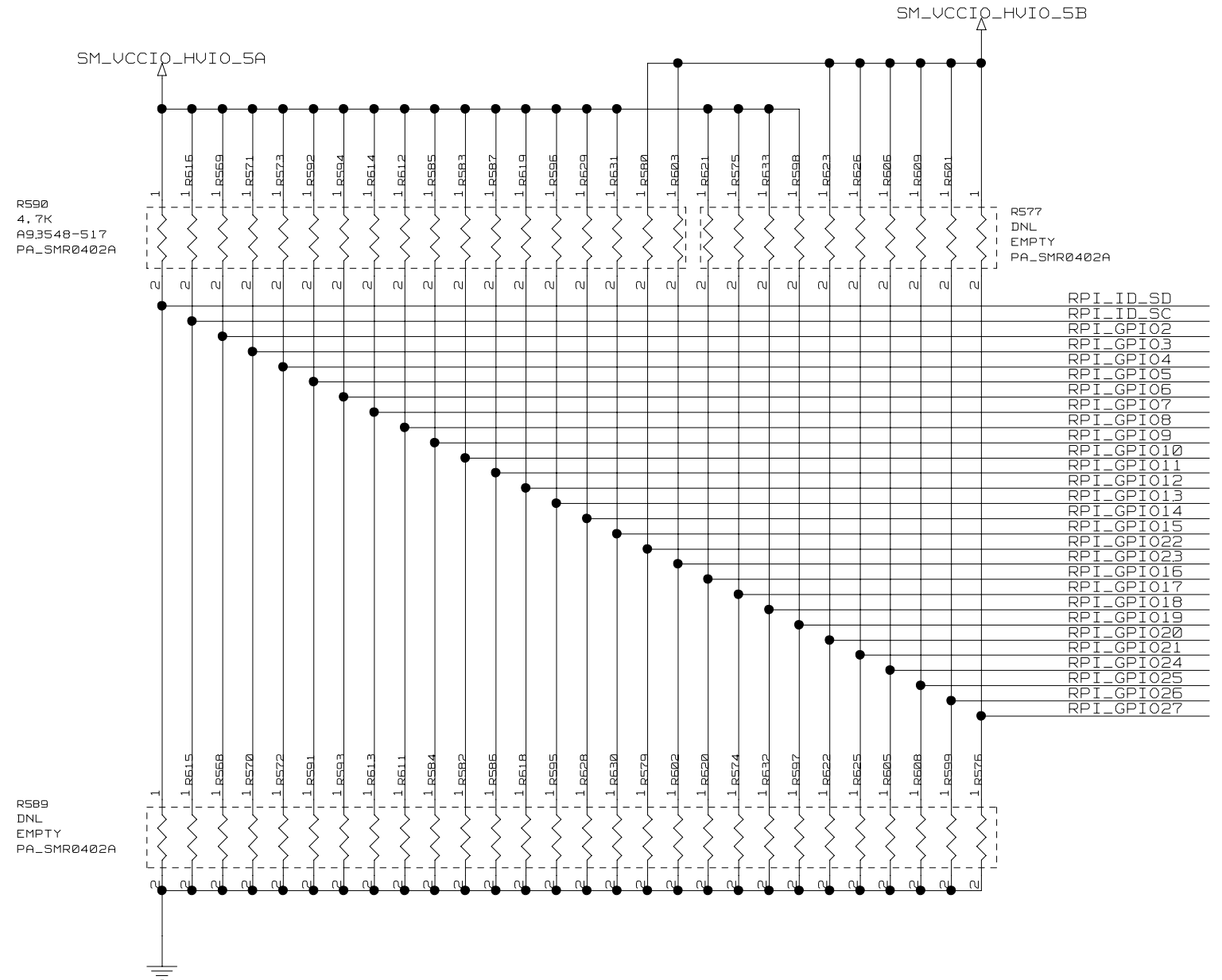
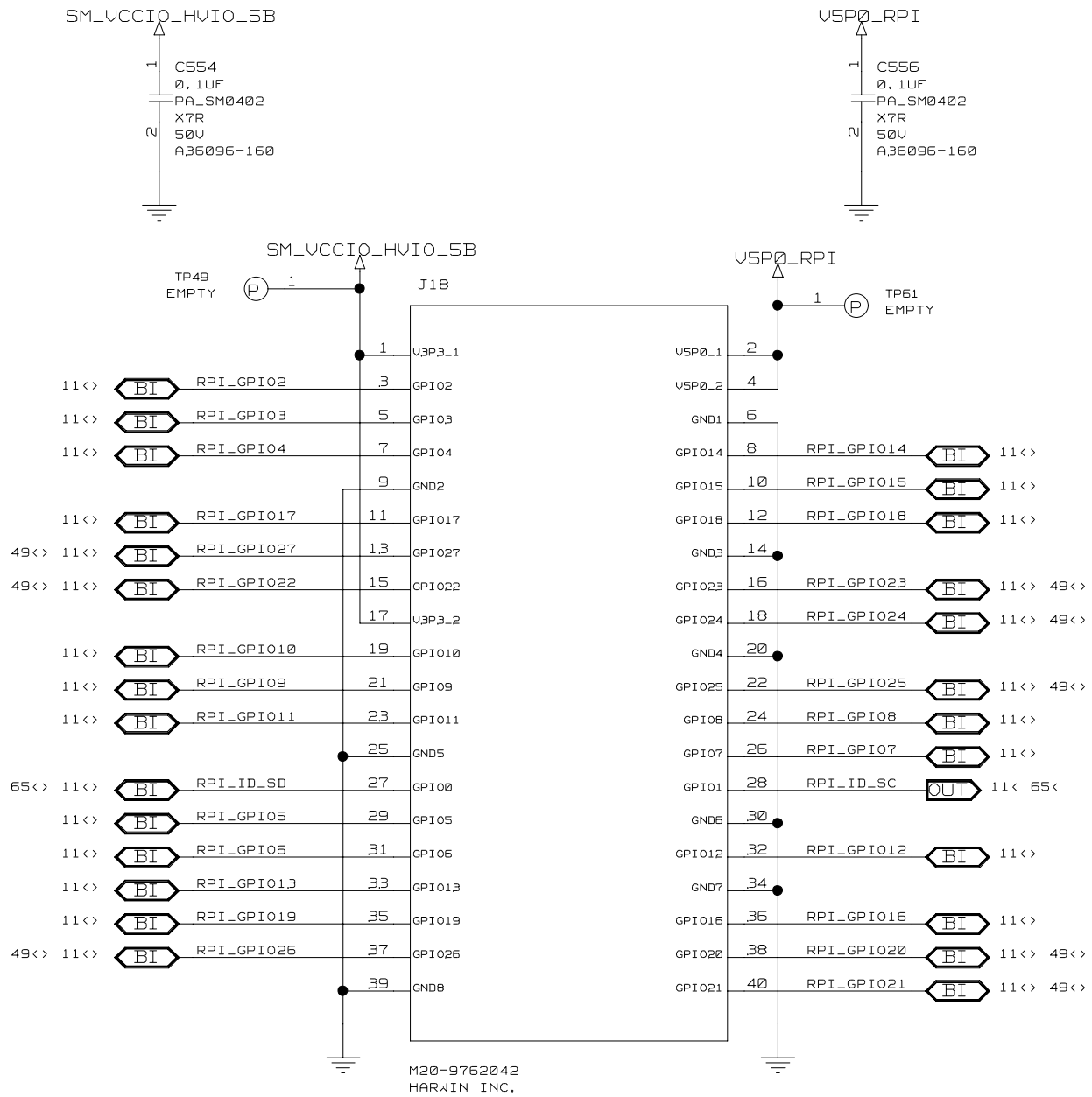
Thu May 22 01:34:38 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 46 OF 65

RASPBERRY PI4/5 HAT CONN



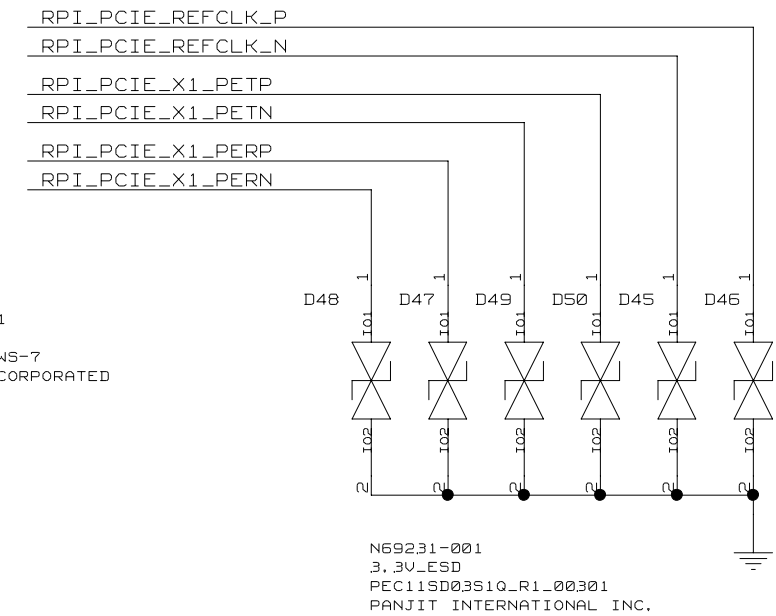
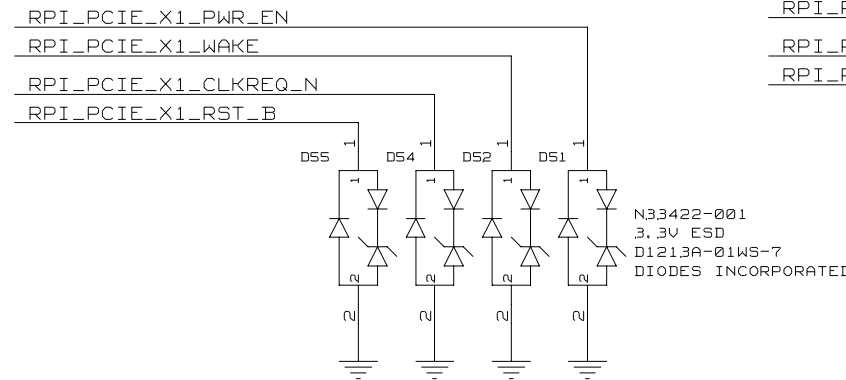
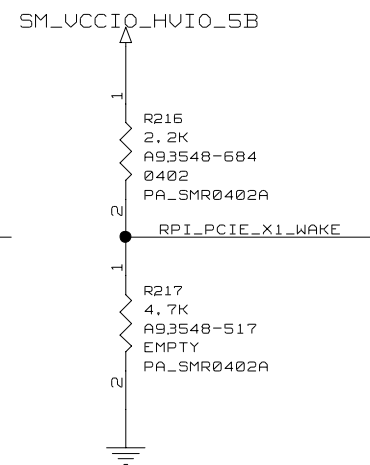
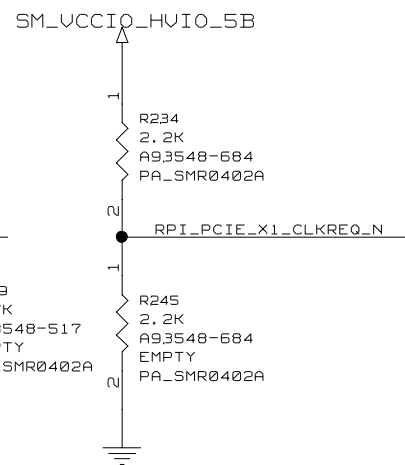
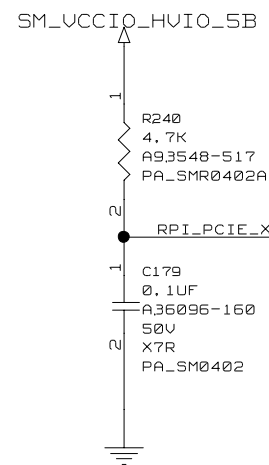
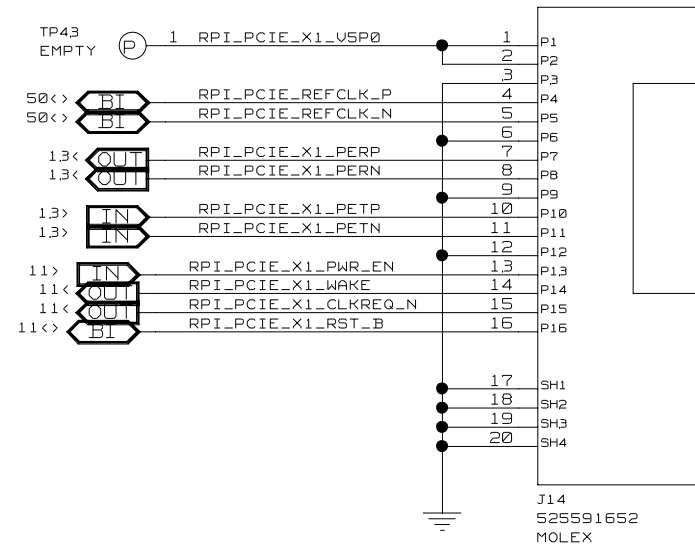
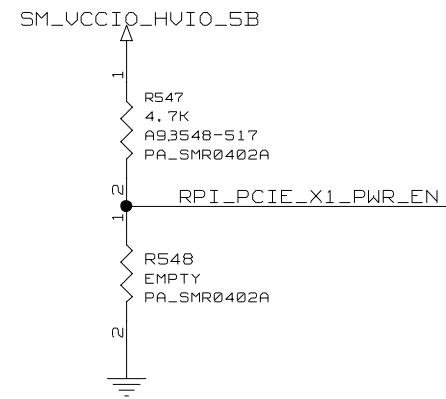
Thu May 22 01:34:38 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 47 OF 65

RASPBERRY PI PCIE CONN



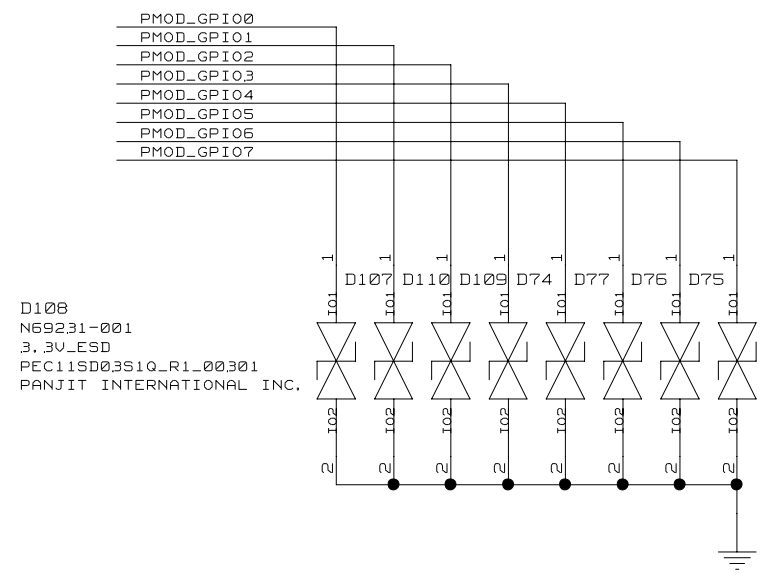
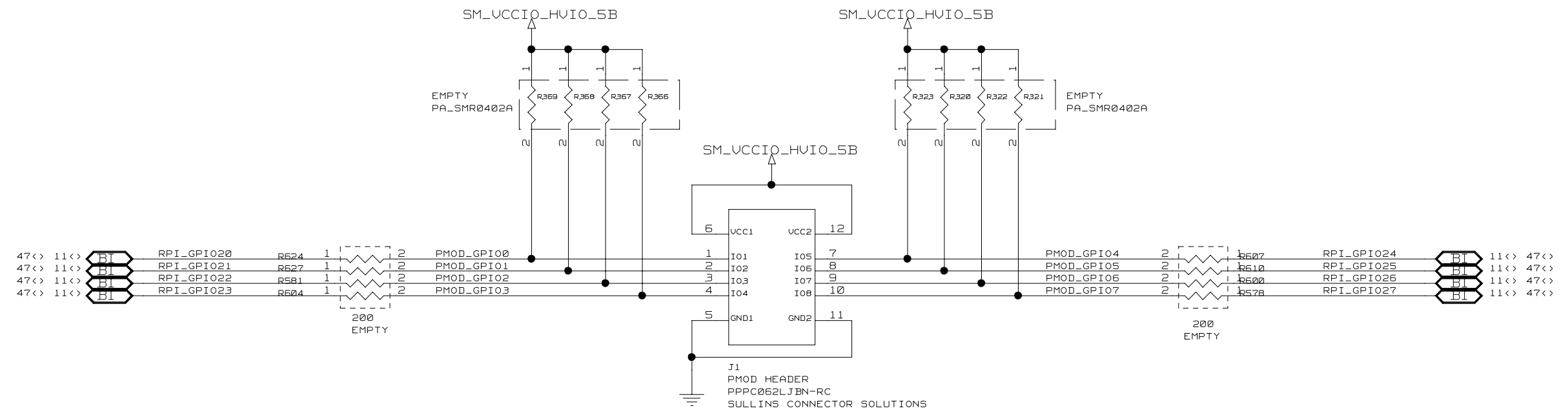
Thu May 22 01:34:38 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 48 OF 65

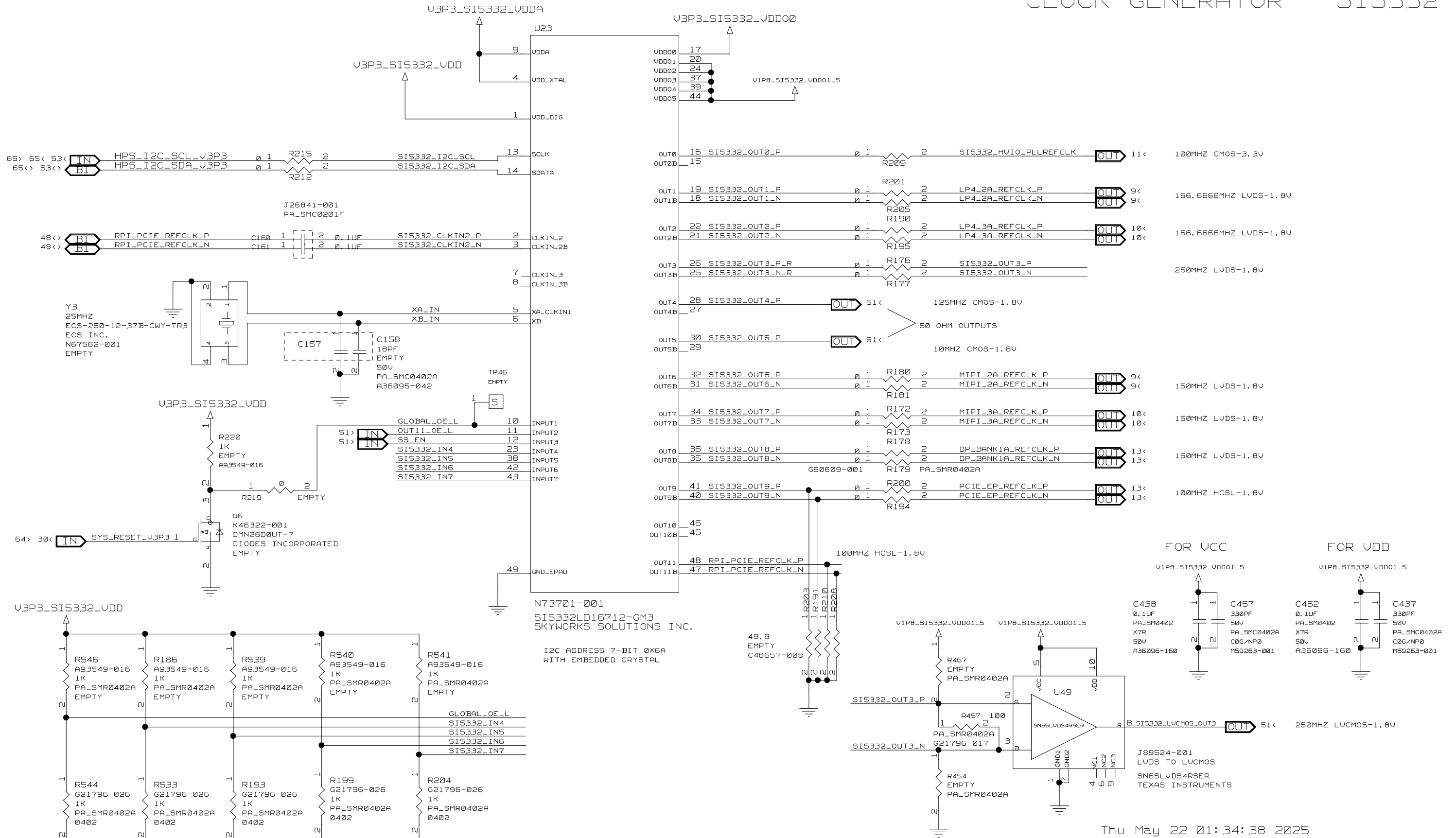
PMOD CONNECTOR



Thu May 22 01:34:38 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 49 OF 65

CLOCK GENERATOR - SI5332



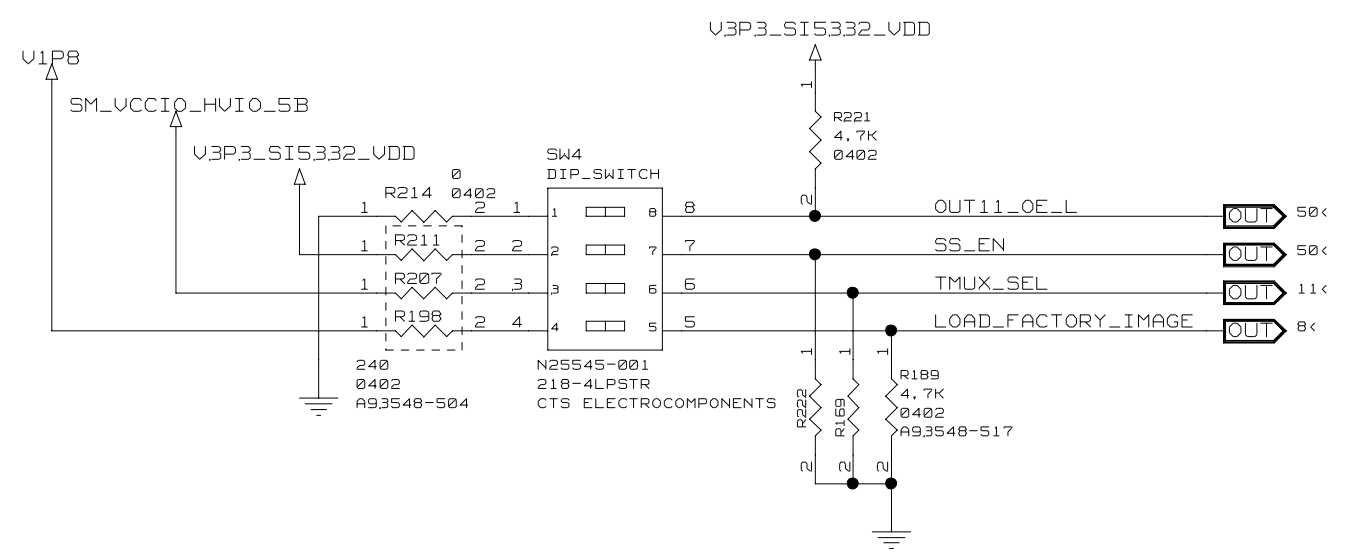
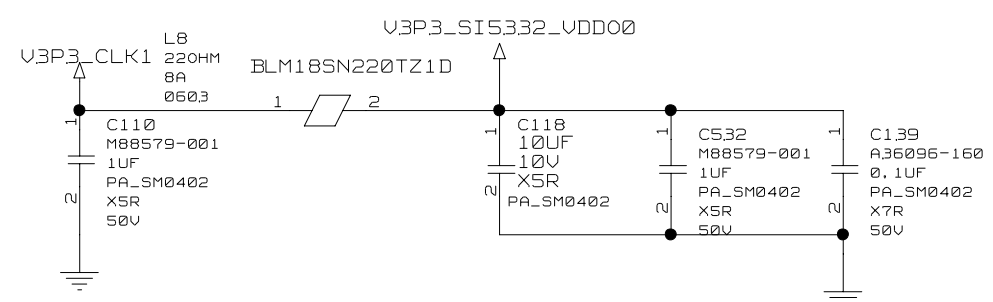
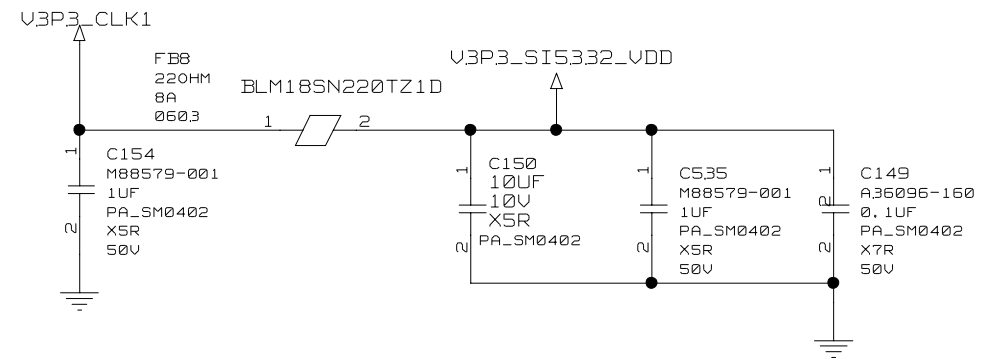
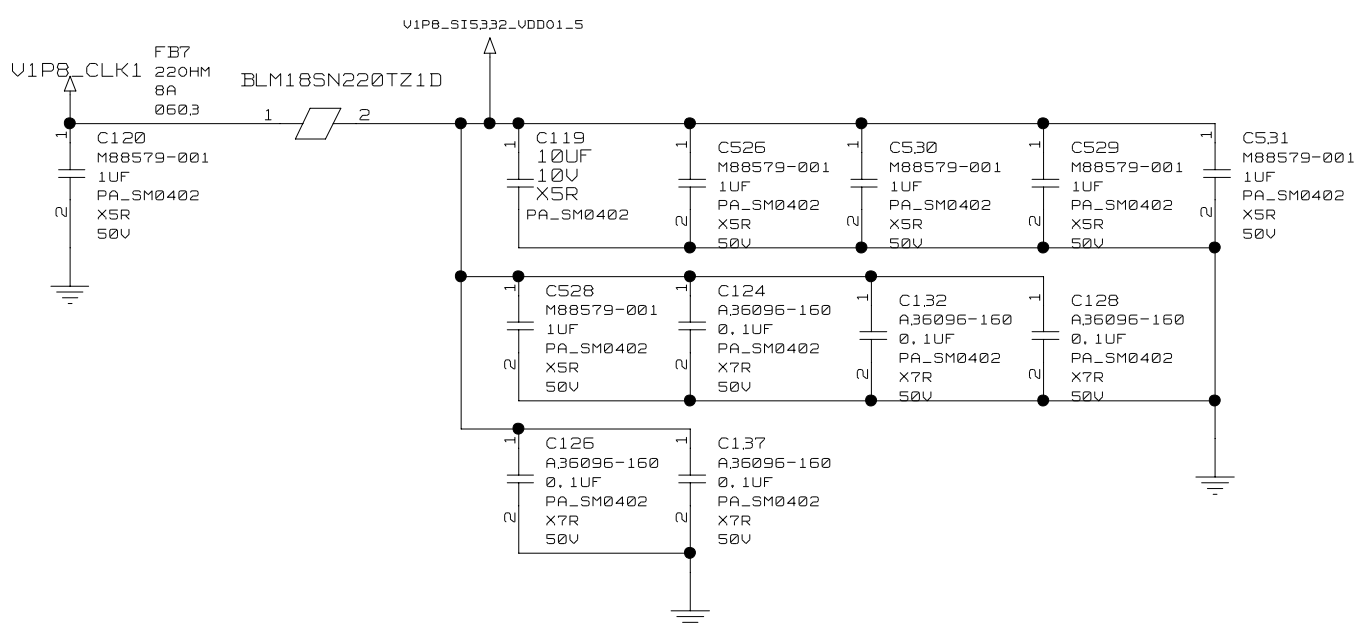
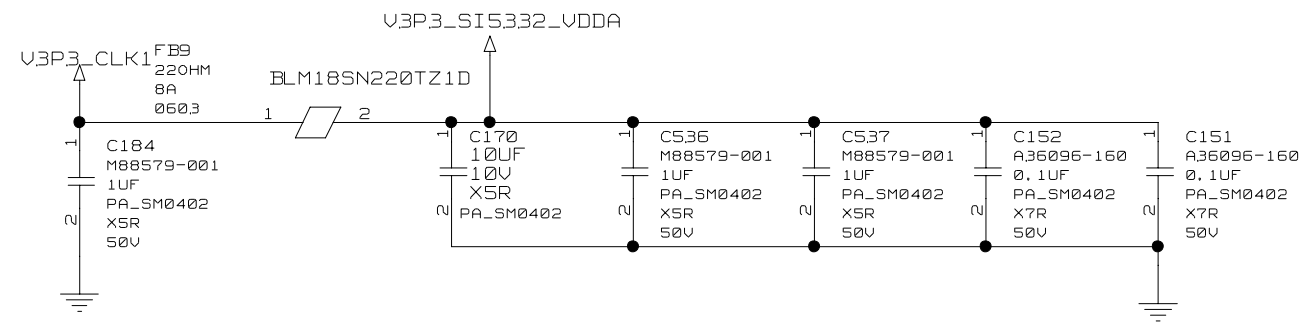
DEPARTMENT
PLATFORM HW DEVELOPMENT



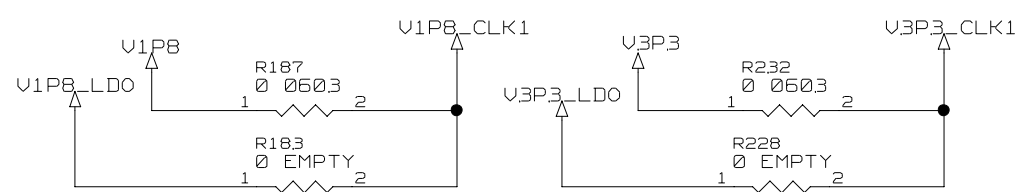
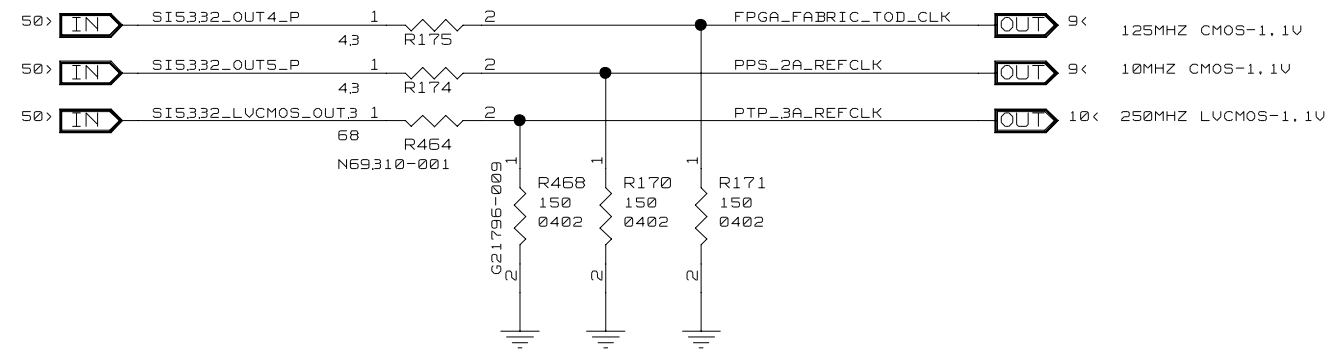
SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 50 OF 65

Thu May 22 01:34:38 2025

CLOCK GENERATOR - SI5332 DECAPS



SW4	ON	OFF	DEFAULT
POS1	OE11 = ENABLE, RP IS ACTIVE	OE11 = DISABLE, EP IS ACTIVE	OFF
POS2	SPREAD SPECTRUM = ENABLE	SPREAD SPECTRUM = DISABLE	OFF
POS3	RASPBERRY PI GPIO26	100MHZ HVIO PLL REFCLOCK	OFF
POS4	DEVICE TO LOAD FACTORY IMAGE	DEVICE TO LOAD APPLICATION IMAGE	OFF



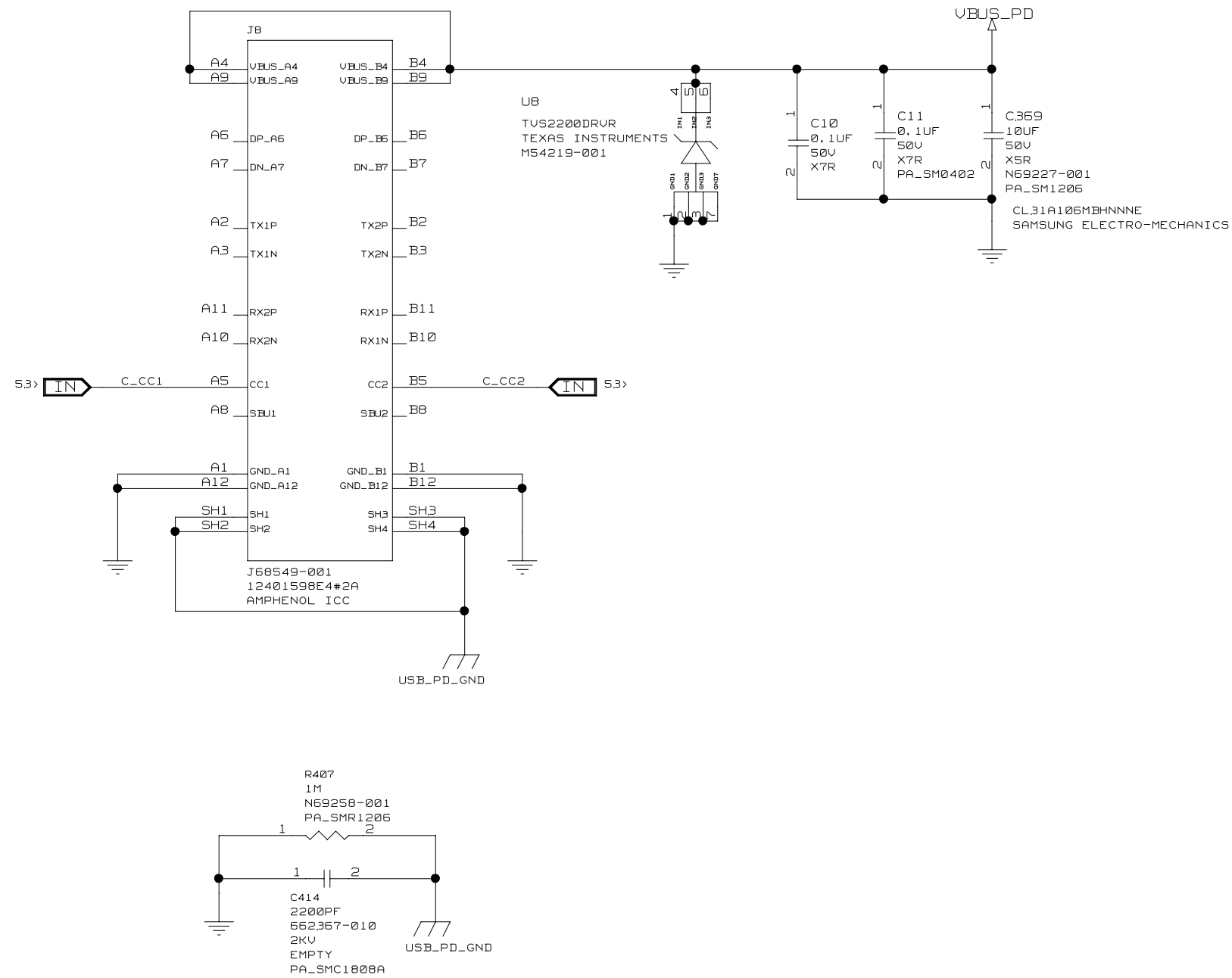
Thu May 22 01:34:39 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 51 OF 65

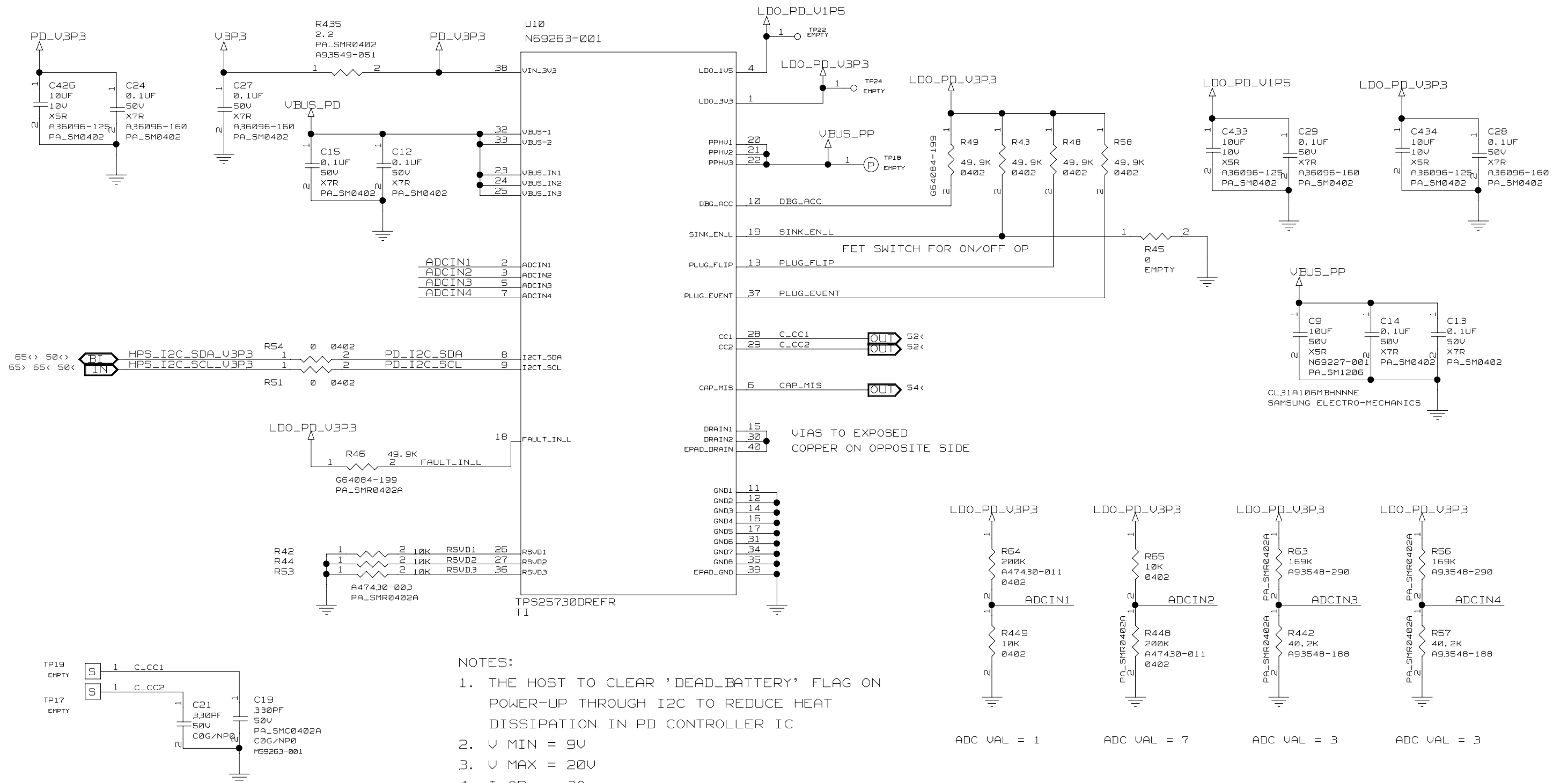
USB PD CONNECTOR



Thu May 22 01:34:39 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 52 OF 65	

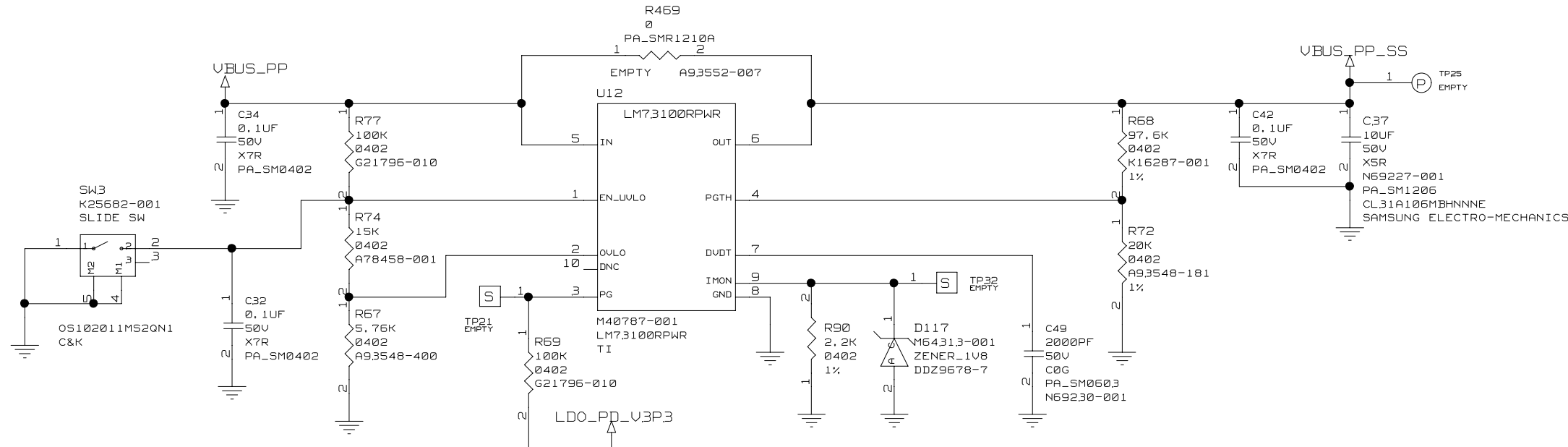
PD SINK CONTROLLER



Thu May 22 01:34:39 2025

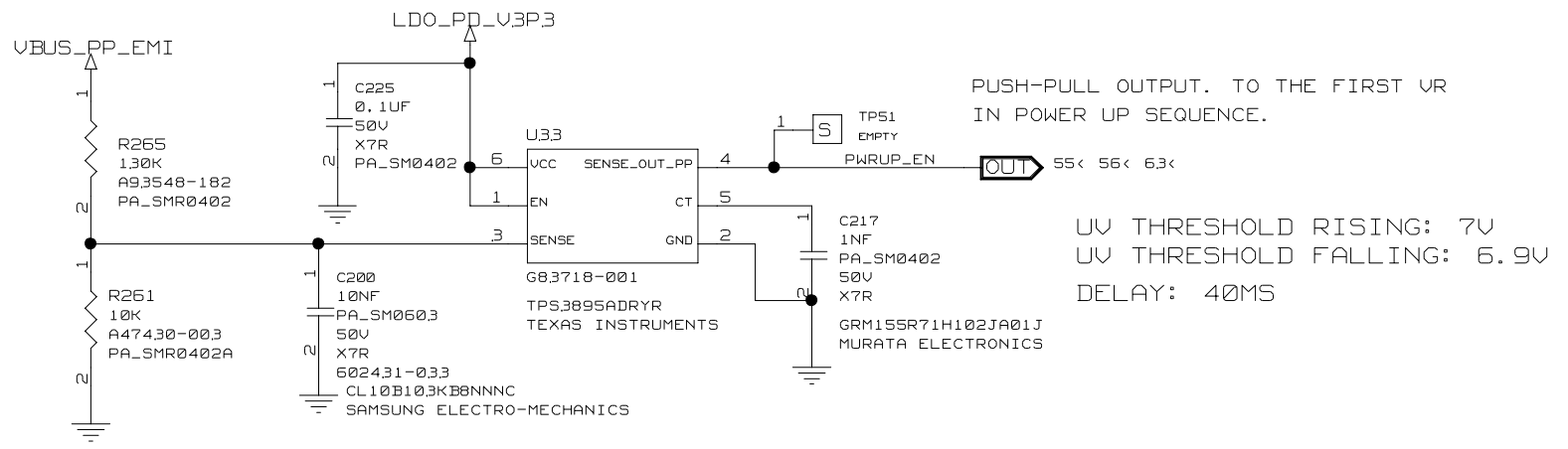
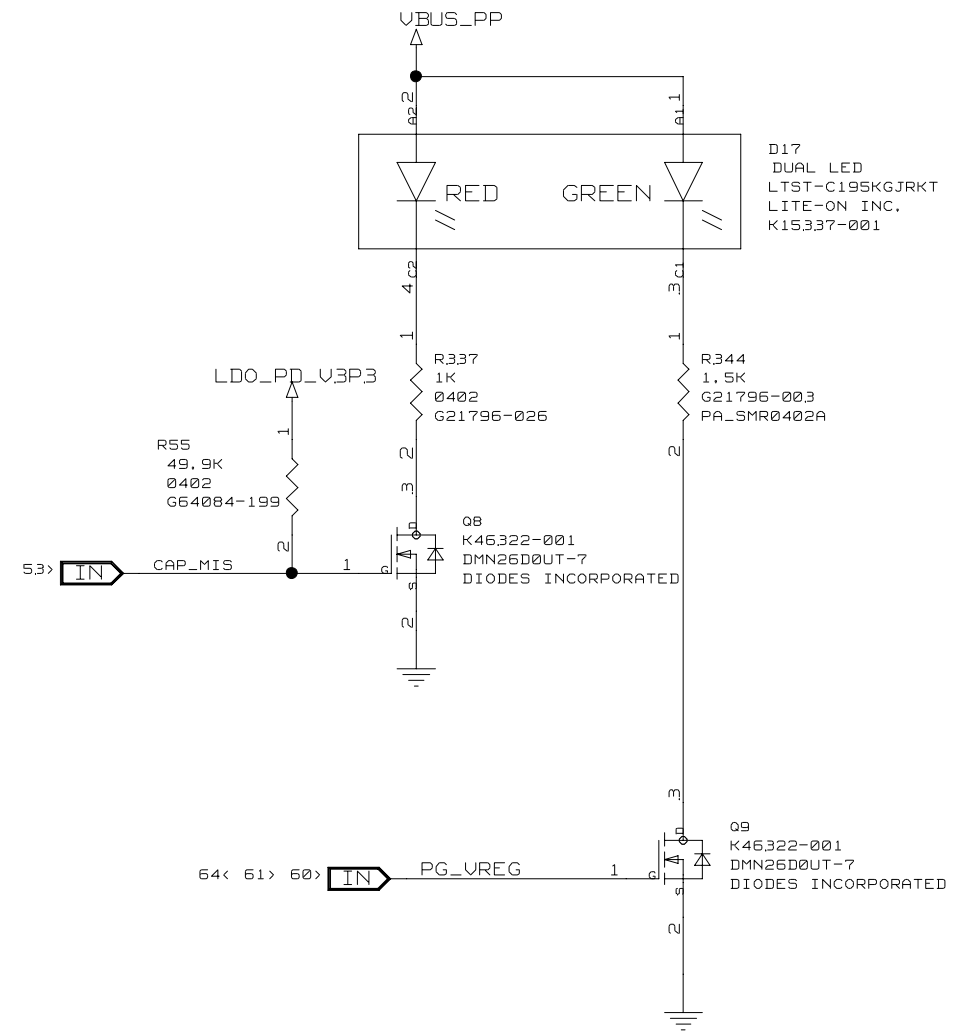
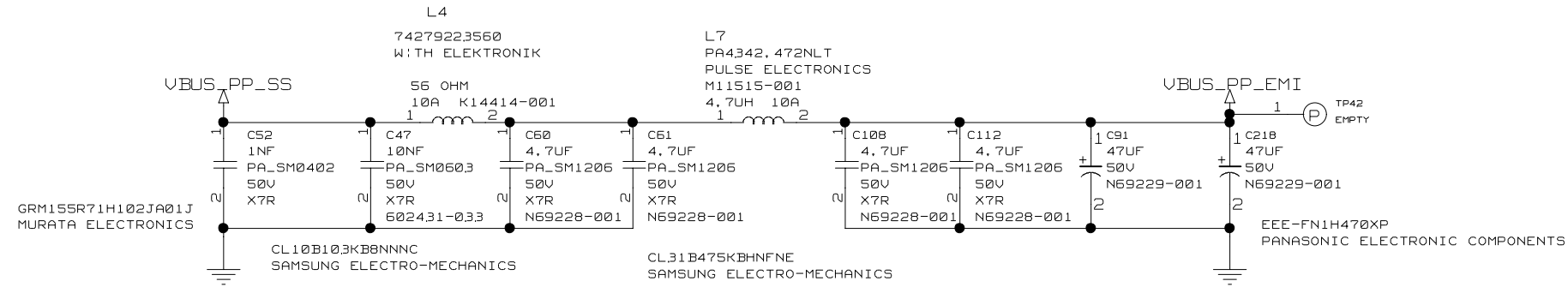
DEPARTMENT PLATFORM HW DEVELOPMENT	altera™	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 53 OF 65	

INRUSH PROTECTION, UVLO, EMI FILTER



I INRUSH MAX: 0.2A
 DV/DT: 1V/MS
 V PGOOD RISING: 7V
 V UV RISING: 7V
 V OV RISING: 25V

LED BLINKS ON USB PD SOURCE INSUFFICIENT CAPABILITIES



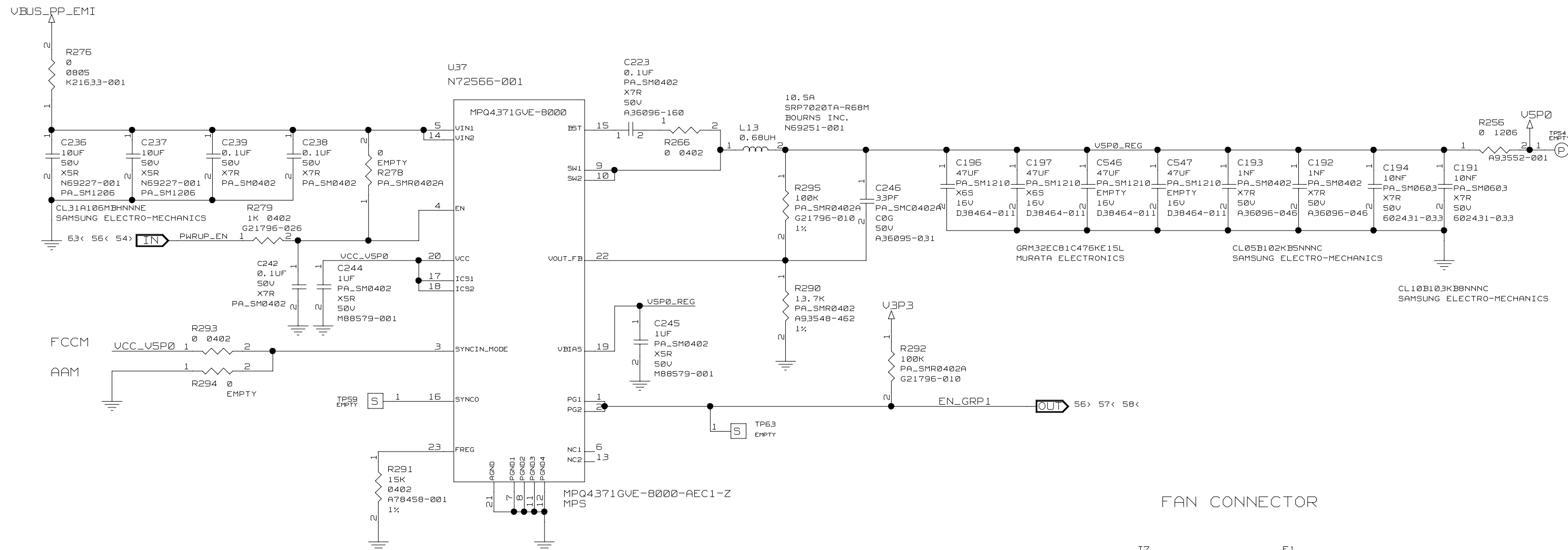
Thu May 22 01:34:39 2025

DEPARTMENT
 PLATFORM HW DEVELOPMENT

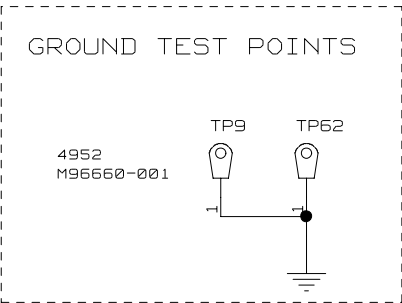


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:	DO NOT SCALE DRAWING		SHEET 54 OF 65

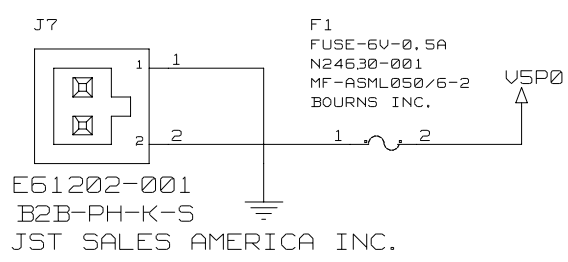
5V REGULATOR



V OUT: 5V
 F SW = 2.2MHZ
 I OUT OP: 6A
 I OUT RATED: 8A



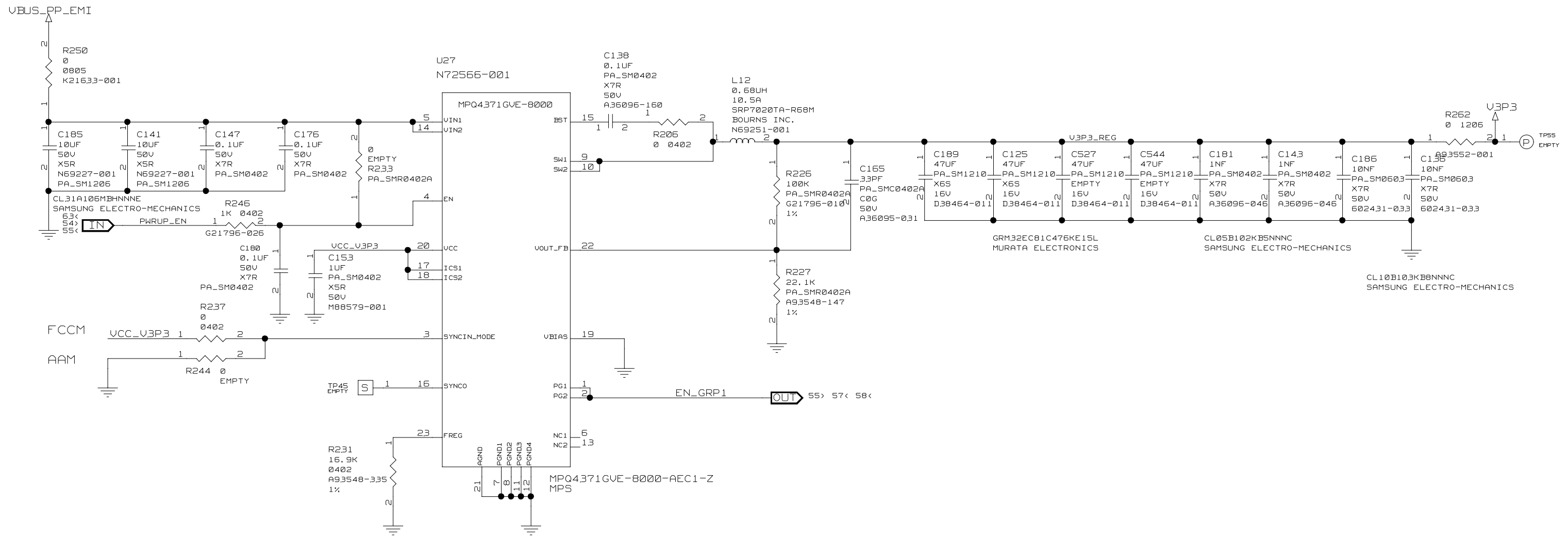
FAN CONNECTOR



Thu May 22 01:34:39 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera™	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 55 OF 65	

3.3V REGULATOR

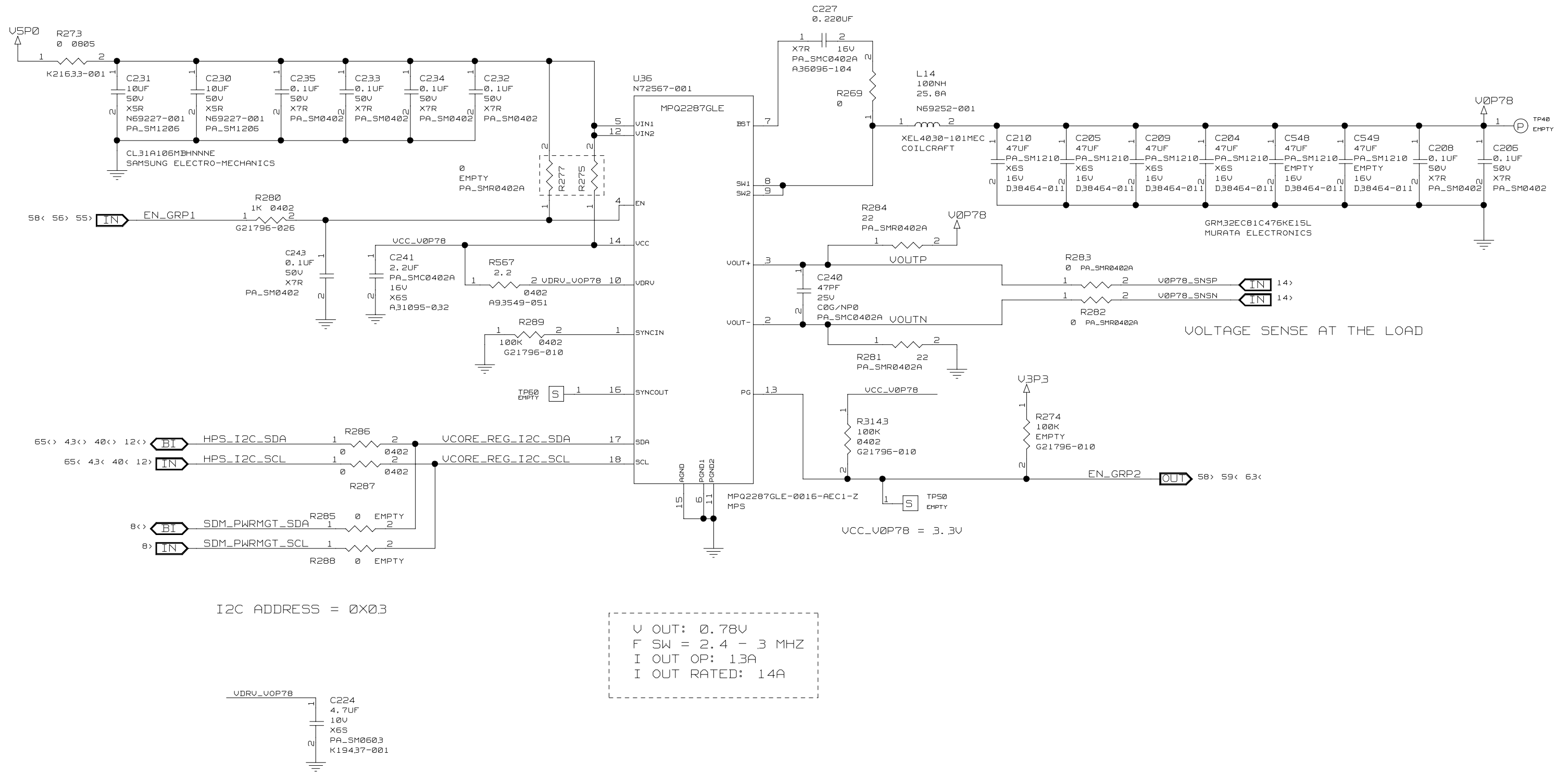


V OUT: 3.3V
 F SW = 2.0MHZ
 I OUT OP: 4A
 I OUT RATED: 8A

Thu May 22 01:34:39 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 56 OF 65

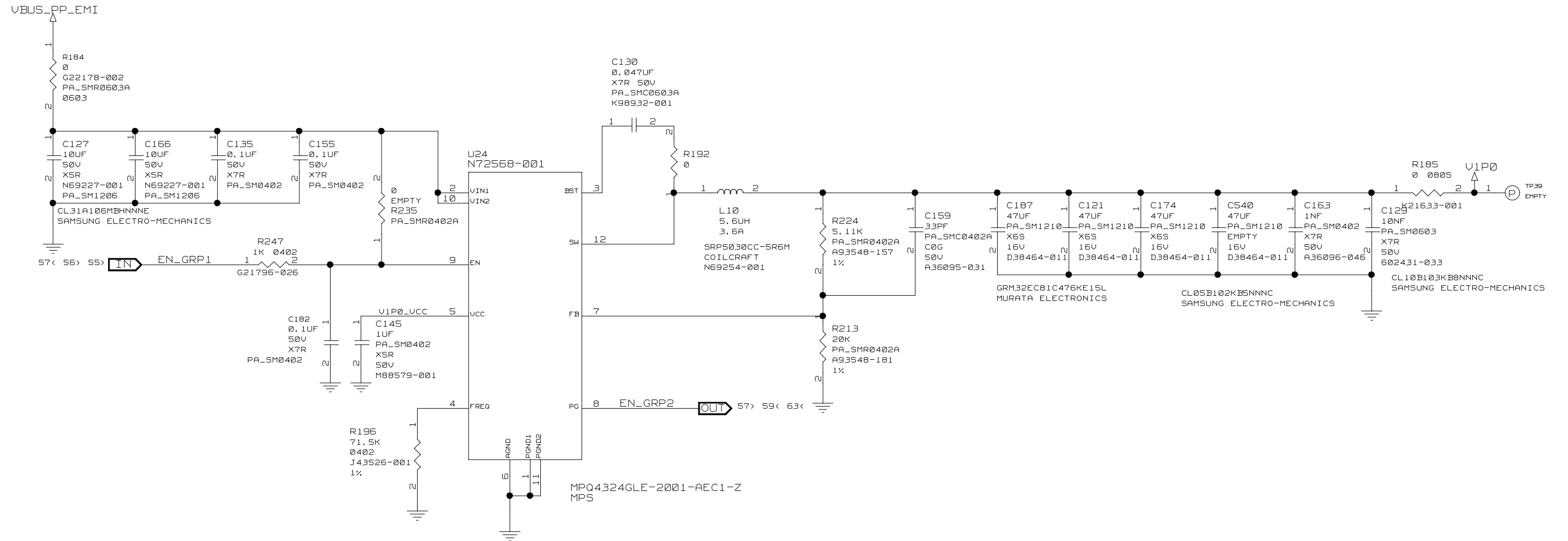
0.78V REGULATOR



Thu May 22 01:34:39 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 57 OF 65

1V REGULATOR

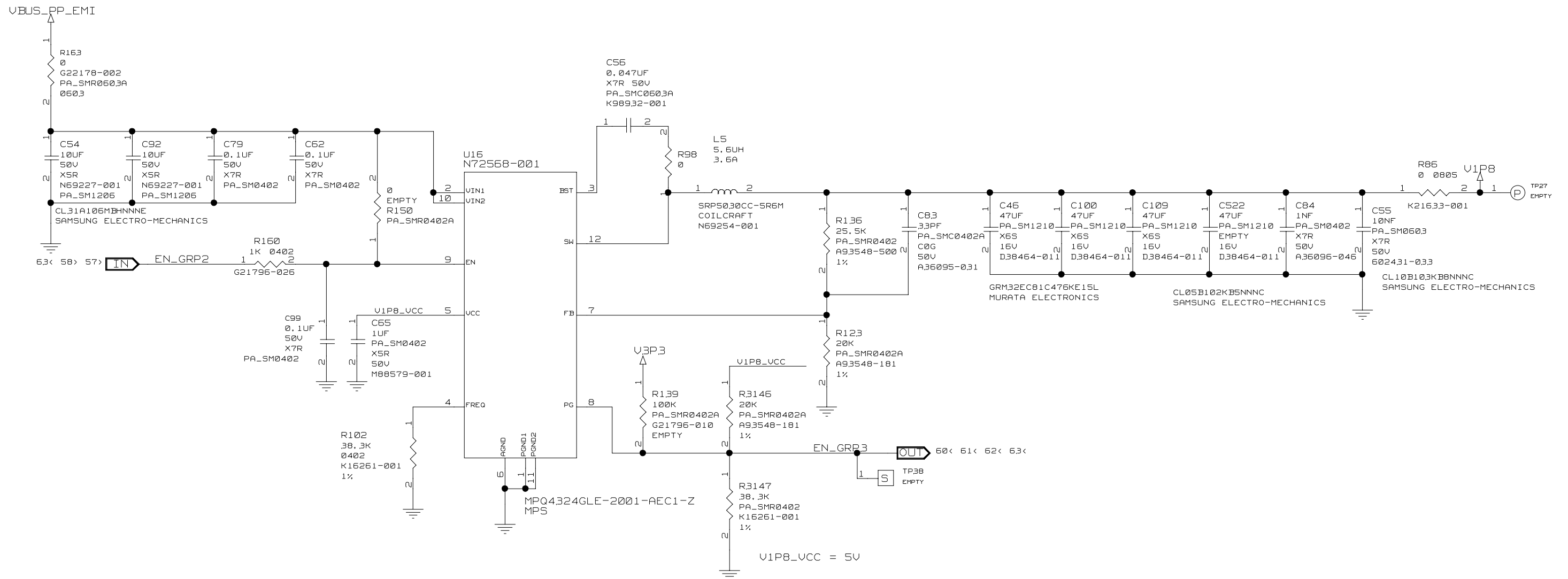


V OUT: 1.0V
 F SW = 0.5 MHz
 I OUT OP: 0.6A
 I OUT RATED: 2A

Thu May 22 01:34:40 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera™	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 58 OF 65	

1.8V REGULATOR

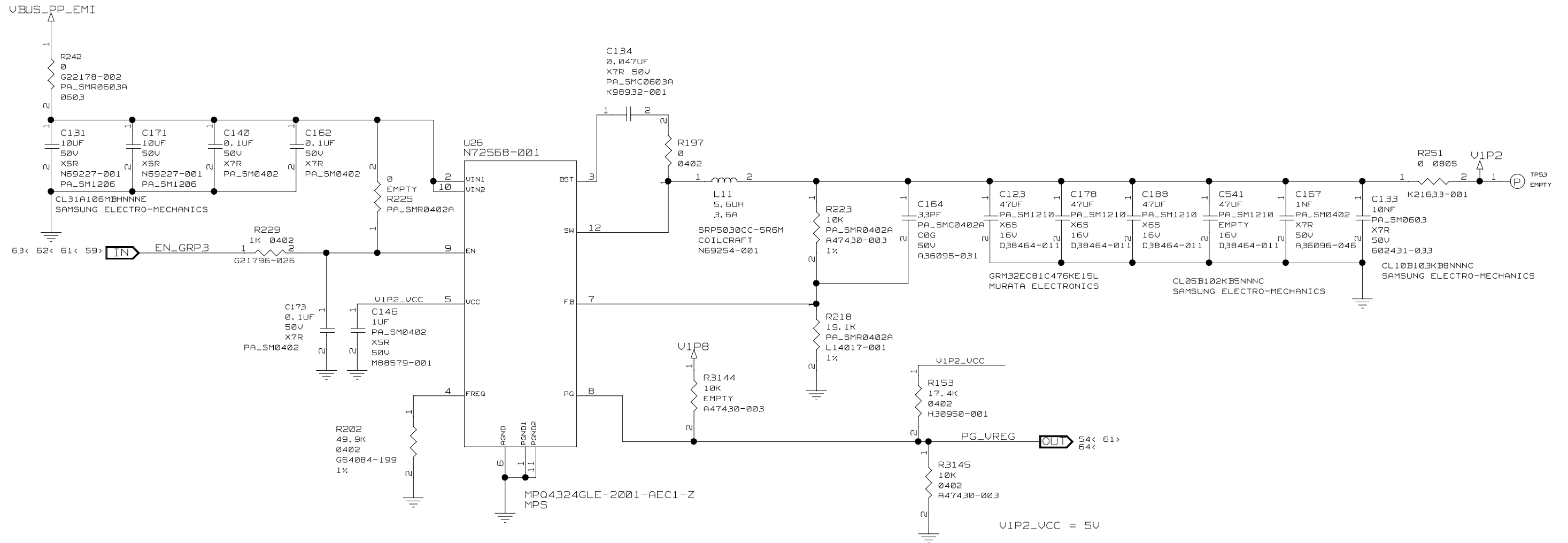


V OUT: 1.8V
 F SW = 900 KHZ
 I OUT OP: 0.86A
 I OUT RATED: 2A

Thu May 22 01:34:40 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 59 OF 65	

1.2V REGULATOR



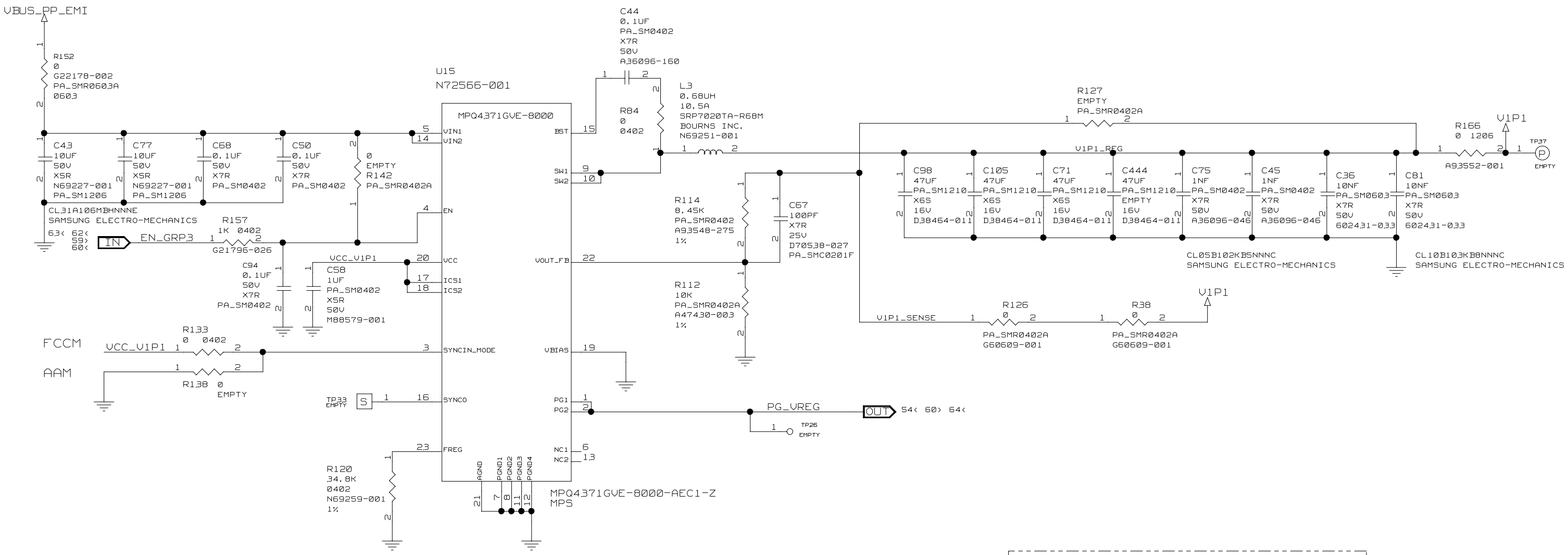
V OUT: 1.2V
 F SW = 700 KHZ
 I OUT OP: 0.67A
 I OUT RATED: 2A

V1P2_VCC = 5V

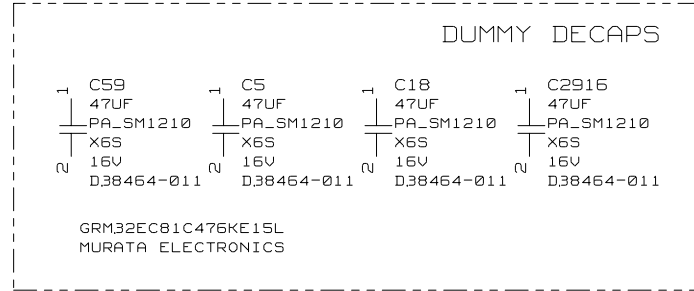
Thu May 22 01:34:40 2025

DEPARTMENT PLATFORM HW DEVELOPMENT		SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING		SHEET 60 OF 65	

1.1V REGULATOR



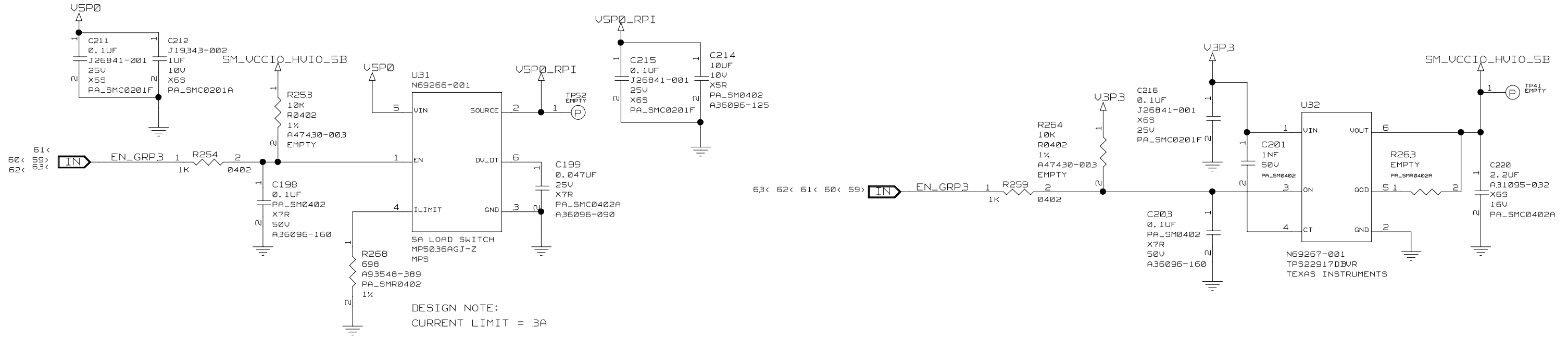
V OUT: 1.1V
 F SW = 1.0MHZ
 I OUT OP: 5A
 I OUT RATED: 6A



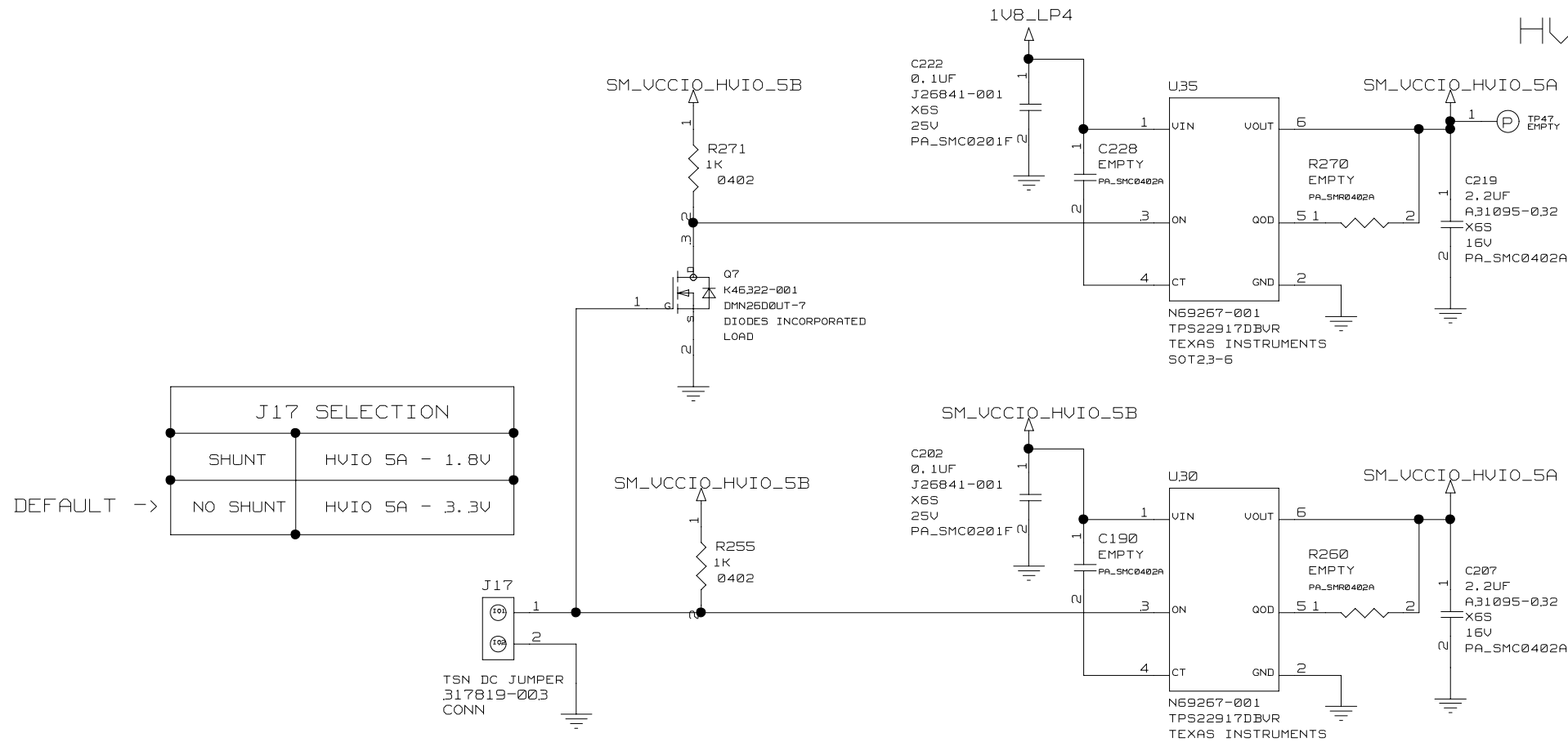
Thu May 22 01:34:40 2025

DEPARTMENT PLATFORM HW DEVELOPMENT	altera	SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
		SCALE:	DO NOT SCALE DRAWING		SHEET 61 OF 65

R-PI LOAD SWITCHES



HVIO 5A VOLTAGE SELECTION



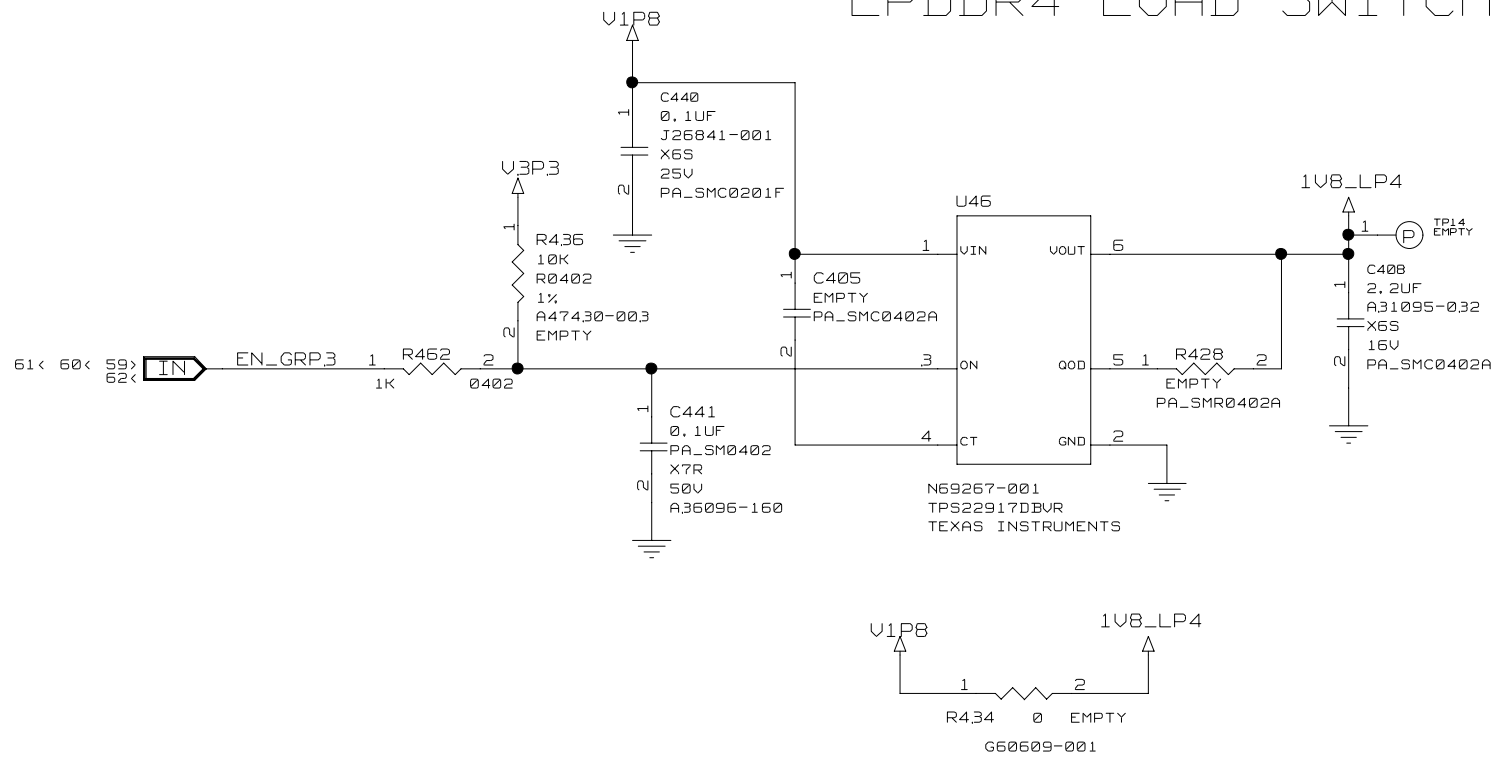
Thu May 22 01:34:40 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

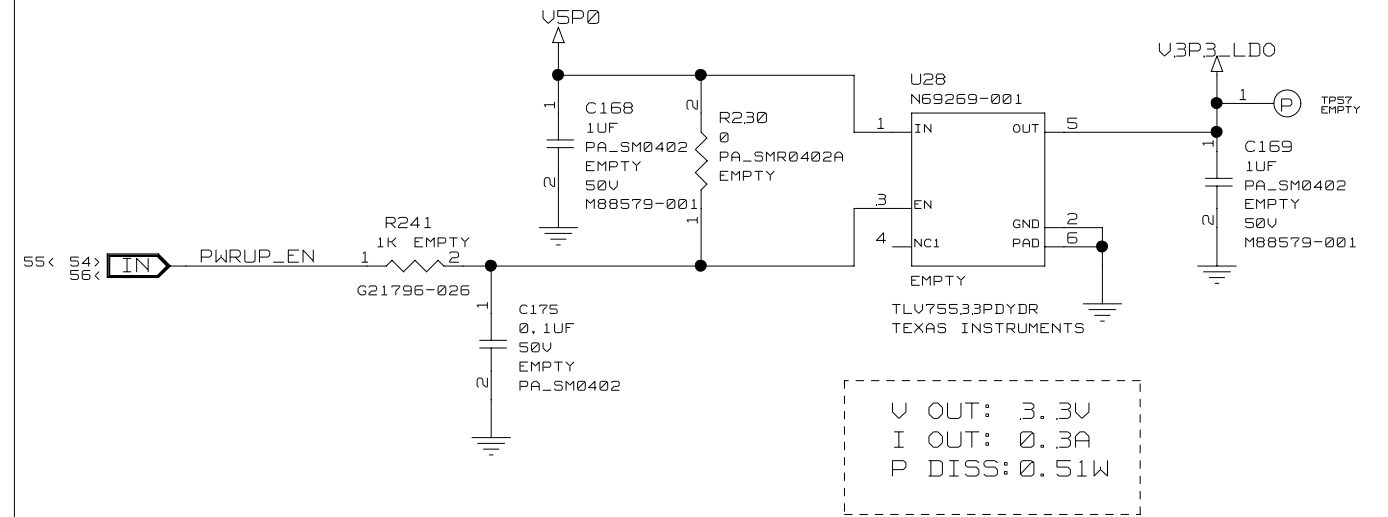


SIZE	CODE	DOCUMENT NUMBER	REV
B	34649	305-PD-25-0242	2.0
SCALE:	DO NOT SCALE DRAWING		SHEET 62 OF 65

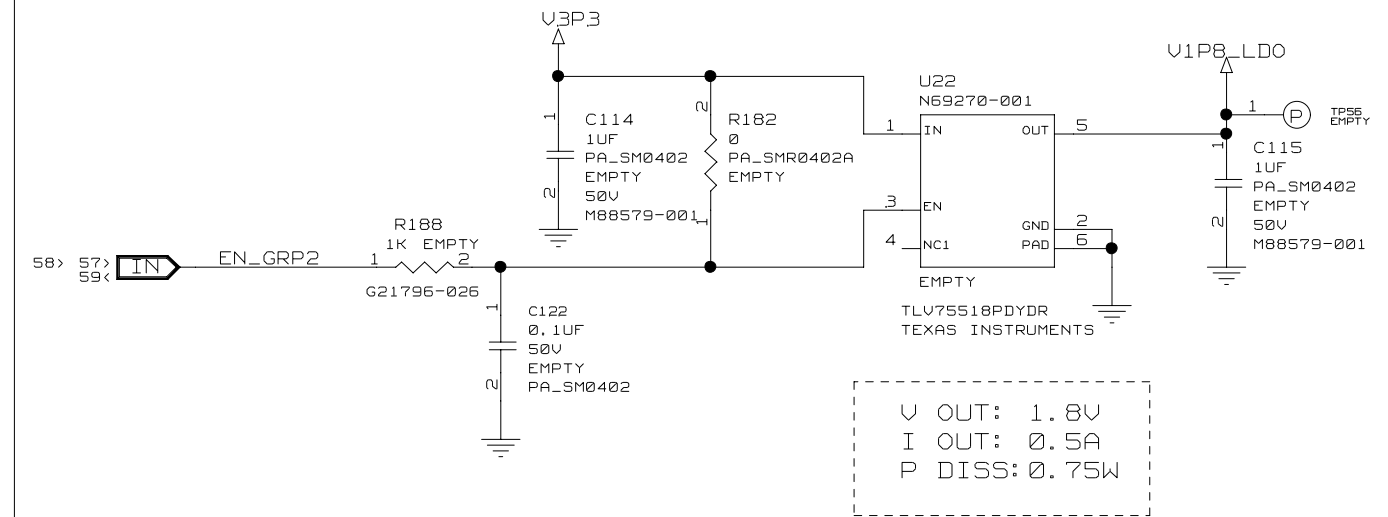
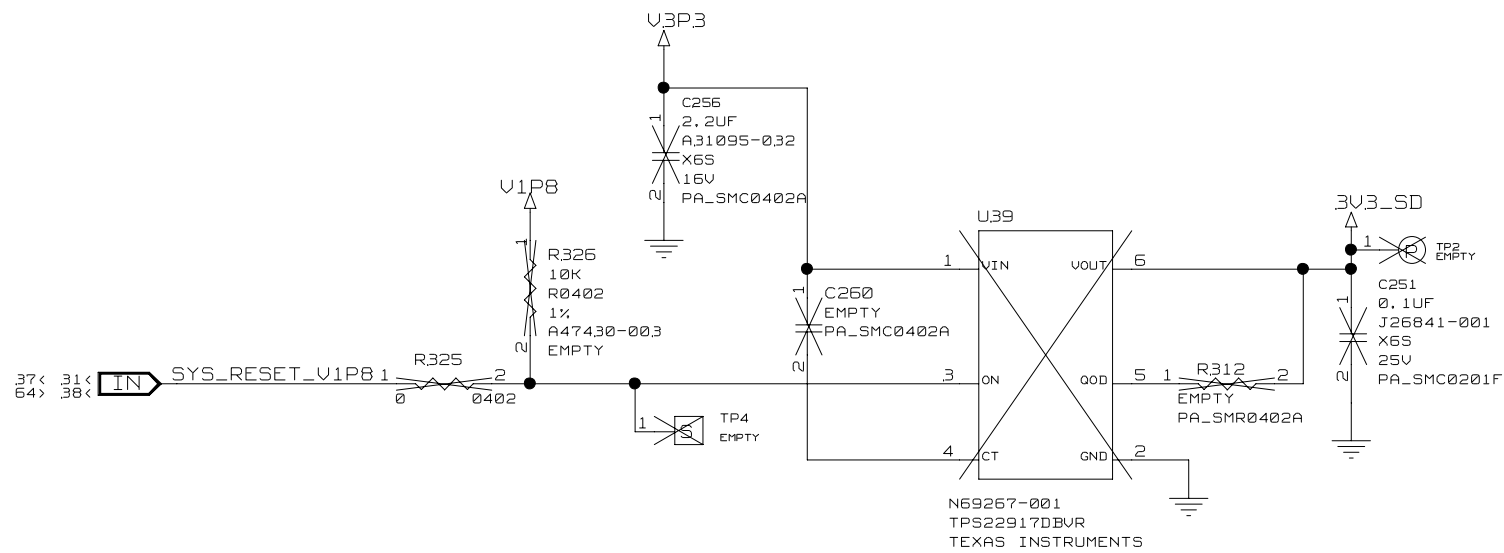
LPDDR4 LOAD SWITCH



CLOCK LDO REGULATORS



SD CARD LOAD SWITCH

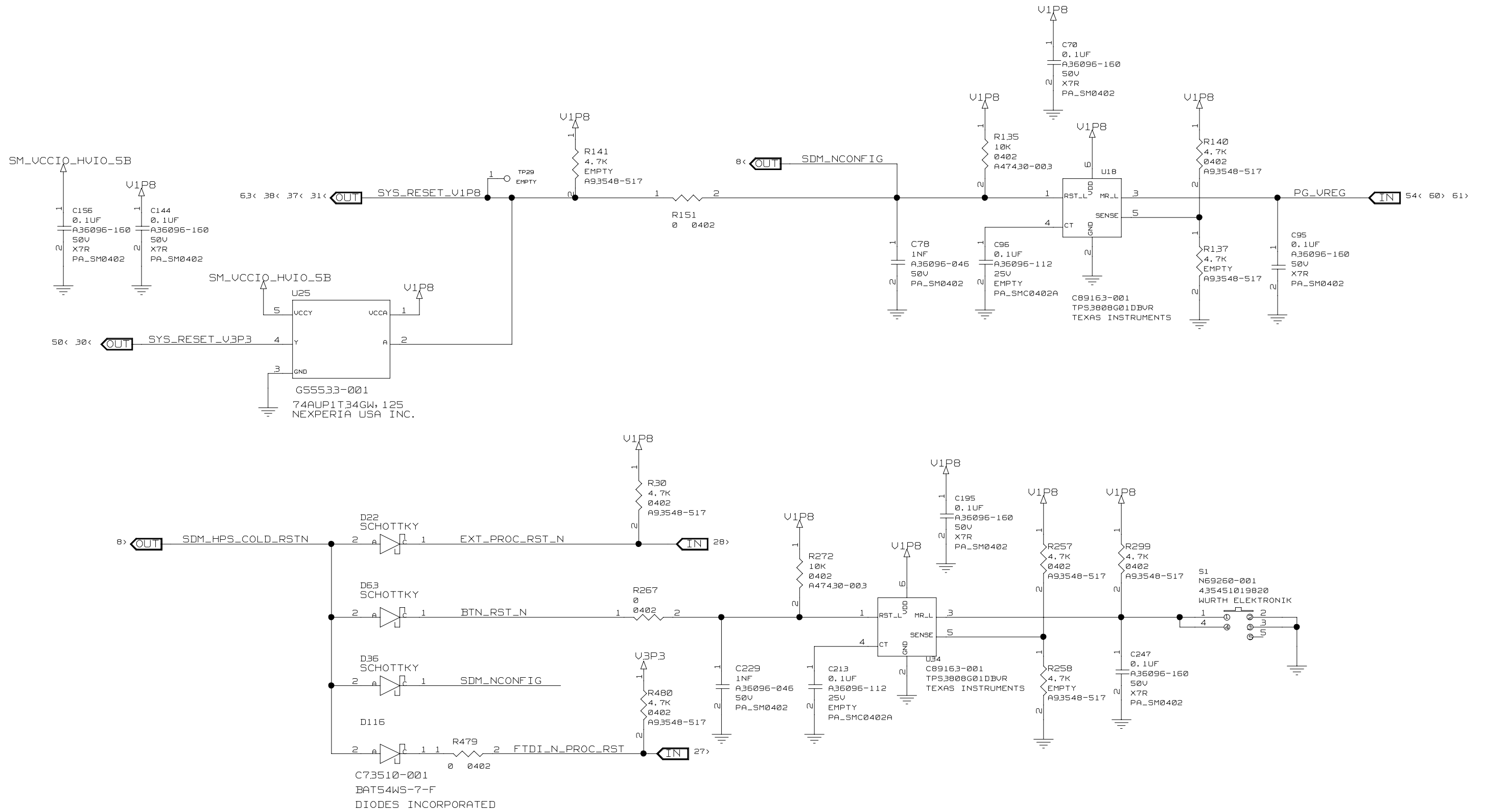


Thu May 22 01:34:40 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:		DO NOT SCALE DRAWING	SHEET 63 OF 65



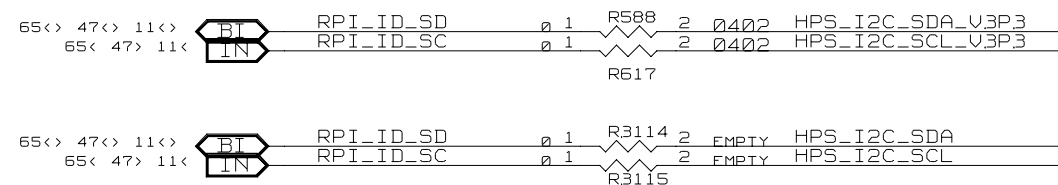
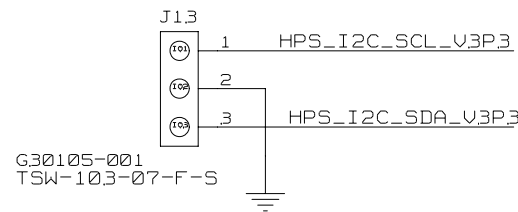
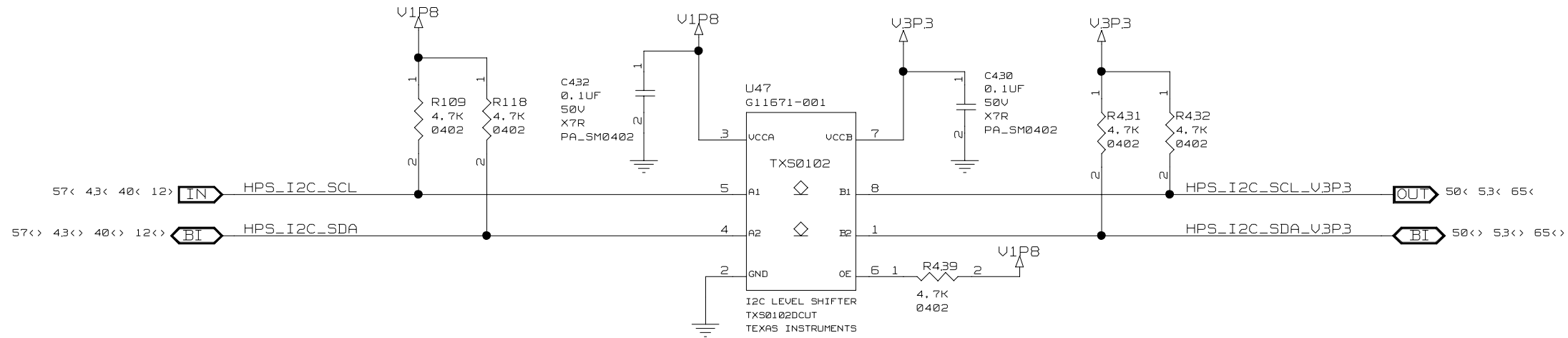
Thu May 22 01:34:40 2025

DEPARTMENT
PLATFORM HW DEVELOPMENT

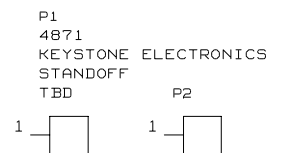
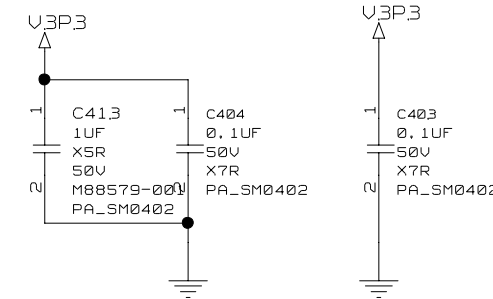
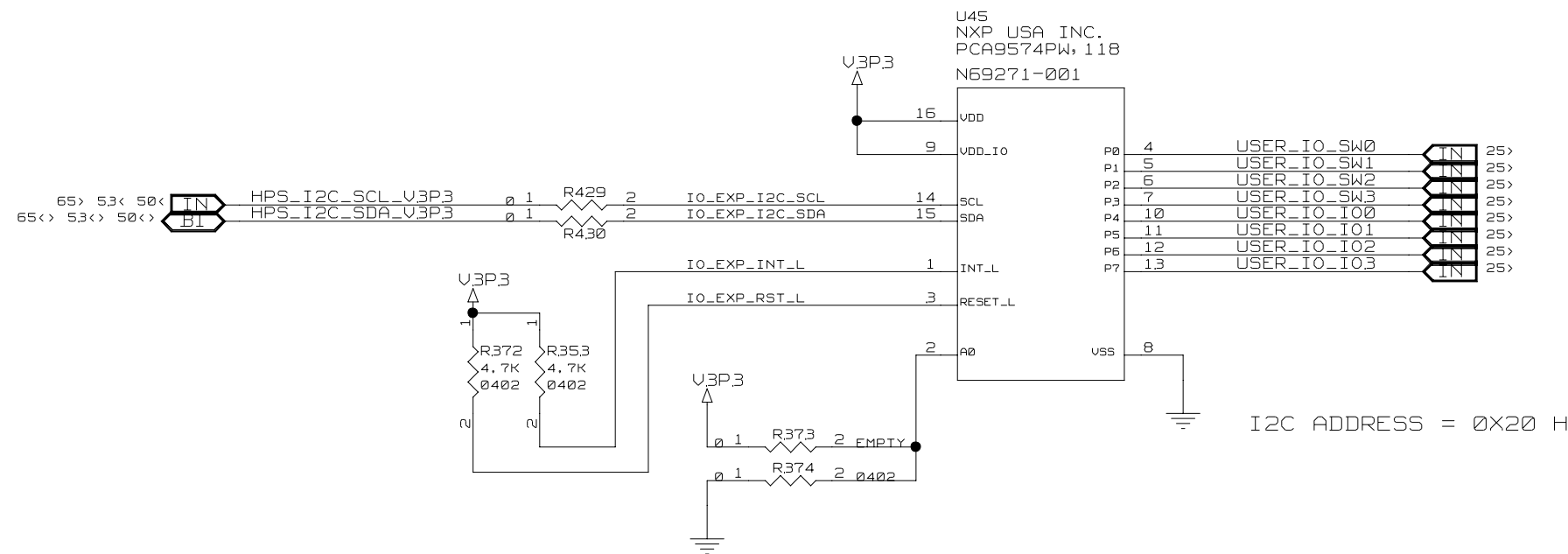


SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
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SCALE: DO NOT SCALE DRAWING SHEET 64 OF 65



NOTES FOR AGILEX 3 FPGA C-SERIES DEVELOPMENT KIT
 LOAD R588, R617 WHEN BANK 5A VOLTAGE IS SET TO 3.3V (DEFAULT)
 LOAD R3114, R3115 WHEN BANK 5A VOLTAGE IS SET TO 1.8V



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DEPARTMENT
 PLATFORM HW DEVELOPMENT



SIZE B	CODE 34649	DOCUMENT NUMBER 305-PD-25-0242	REV 2.0
SCALE:	DO NOT SCALE DRAWING		SHEET 65 OF 65