4.5V to 60V, 250mA Current-Limiter with OV, UV, and Reverse Protection

ADPL86610/ADPL86611/ADPL86612

General Description

The ADPL86610/ADPL86611/ADPL86612 are a series of adjustable overvoltage and overcurrent protection devices that are ideal to protect systems against positive and negative input voltage faults up to +60V and -65V, and feature low 1.42Ω (typ) R_{ON} FETs.

The adjustable input overvoltage protection range is 5.5V to 60V, and the adjustable input undervoltage protection range is 4.5V to 59V. The input Overvoltage-lockout (OVLO) and Undervoltage-lockout (UVLO) thresholds are set using external resistors. Additionally, the devices offer an internal input undervoltage threshold at 4.2V (typ).

The devices feature programmable current-limit protection up to 250mA; hence, controlling the inrush current at startup while charging large capacitors at the output. The current-limit threshold is programmed by connecting a resistor from the SETI pin to GND. When the device current reaches the programmed threshold, the device prevents further increases in current by modulating the Field-effect transistor (FET) resistance. The devices can be programmed to behave in three different ways under current-limit conditions: Autoretry, Continuous, or Latch-off modes. The voltage appearing on the SETI pin is proportional to the instantaneous current flowing through the device and is read by an Analog-to-digital converter (ADC).

ADPL86610 and ADPL86612 block current flowing in the reverse direction (i.e., from OUT to IN), whereas ADPL86611 allows current flow in the reverse direction. The devices feature thermal shutdown protection against excessive power dissipation.

The devices are available in a small, 10-pin (3mm x 3mm) TDFN-EP package. The devices operate over the -40°C to +125°C extended temperature range.

Benefits and Features

- Robust Protection Reduces System Downtime
  - Wide Input-Supply Range: +4.5V to +60V
  - Hot Plug-in Tolerant without Transient Voltage Suppressor (TVS) up to 35V Input Supply
  - Negative Input Tolerance to -65V
  - Low R_{ON} 1.42Ω (typ)
  - Reverse Current-Blocking Protection
  - Thermal Overload Protection
  - Extended -40°C to +125°C Temperature Range
  - ADPL86610 Enables OV, UV, and Reverse-Voltage Protection
  - ADPL86611 Enables OV and UV Protection
  - ADPL86612 Enables Reverse-Voltage Protection
- Flexible Design Options Enable Reuse and Less Requalification
  - Adjustable OVLO and UVLO Thresholds
  - Programmable Forward-Current Limit: 10mA to 20mA with ±6% Accuracy and 20mA to 250mA with ±5% Accuracy Over Full Temperature Range
  - Programmable Overcurrent Fault Response: Autoretry, Continuous, and Latch-Off Modes
  - Smooth Current Transitions
- Saves Board Space and Reduces External Bill of Materials (BOM) Count
  - 10-Pin, 3mm x 3mm, Thin Dual Flat No Leads (TDFN)-EP Package
  - Integrated FETs

Applications

- Sensor Systems
- Condition Monitoring
- Factory Sensors
- Process Instrumentation
- Weighing and Batching Systems
- Industrial Applications such as Programmable Logic Controller (PLC), Network-Control Modules, Battery-Operated Modules

Ordering Information ***appears at end of data sheet***.

19-102044; Rev 0; 10/25

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Typical Operating Circuits

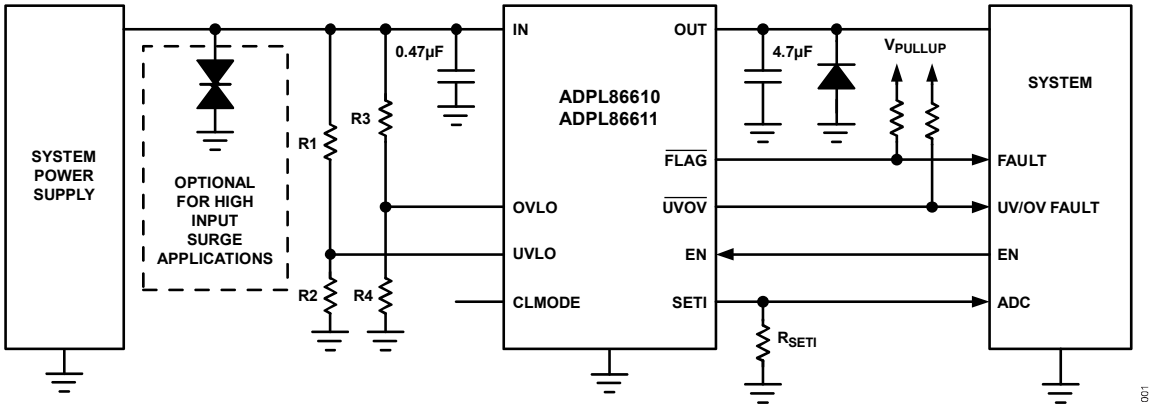


Figure 1. ADPL86610 and ADPL86611 Typical Operating Circuits

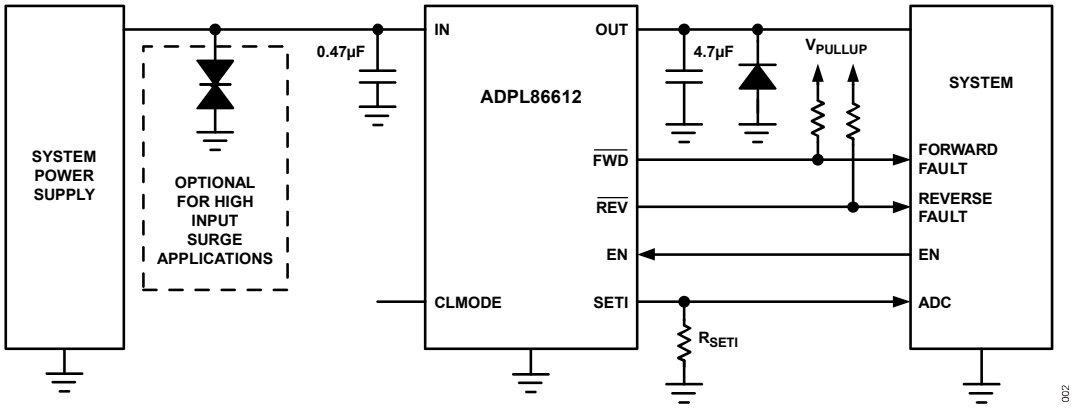


Figure 2. ADPL86612 Typical Operating Circuit

Absolute Maximum Ratings

IN to GND ..... -70V to +65V

IN to OUT ..... -65V to +65V

OUT to GND ..... -0.3V to +65V

UVLO, OVLO to GND ..... -0.3V to MAX(V_{IN}, V_{OUT}) + 0.3V

$\overline{UVOV}$, $\overline{FLAG}$, $\overline{FWD}$, $\overline{REV}$, EN, CLMODE to GND ..... -0.3V to +6.0V

IN Current (DC) 262.5mA

SETI to GND (*Note 1*) ..... -0.3V to +1.6V

Continuous Power Dissipation (10 pin TDFN-EP (T_A = +70°C, derate 24.4mW/°C above +70°C)) 1951.2mW

Extended Operating Temperature Range ..... -40°C to 125°C

Junction Temperature Range (*Note 2*) ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C°C

Note 1: SETI pin is internally clamped. Forcing more than 5mA current into the pin can damage the device.

Note 2: Junction temperature greater than +125°C degrades operating lifetimes.

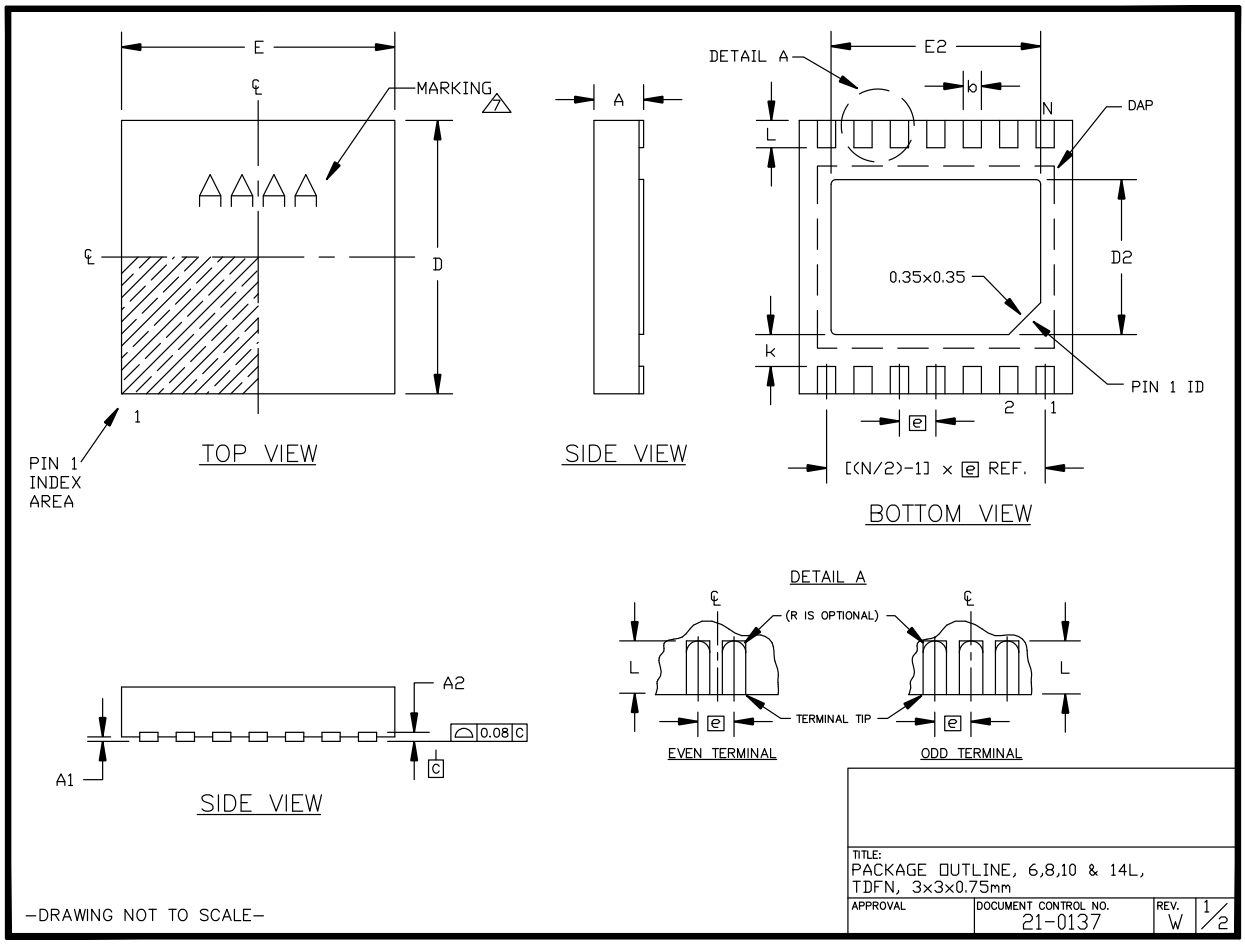
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10 TDFN	
Package Code	T1033+1C
Outline Number	*21-0137*
Land Pattern Number	*90-0003*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.


E
MARKING
D
1
PIN 1
INDEX
AREA
TOP VIEW
A
SIDE VIEW
DETAIL A
E2
b
N
DAP
L
D2
0.35x0.35
k
PIN 1 ID
2
1
e
[(N/2)-1] x e REF.
BOTTOM VIEW
A2
0.08 C
A1
C
SIDE VIEW
DETAIL A
(R IS OPTIONAL)
L
TERMINAL TIP
EVEN TERMINAL
ODD TERMINAL
TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, 3x3x0.75mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
W
1/2
-DRAWING NOT TO SCALE-

Electrical Characteristics

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.2kΩ.) (See *Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		4.5		60	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V, V_{IN} = 24V		25	60	µA
Shutdown Output Current	I_{OFF}	V_{EN} = 0V, V_{OUT} = 0V, V_{IN} = 24V	-2	<1	2	µA
Reverse Input Current	I_{IN_RVS}	V_{IN} = -60V, V_{OUT} = 0V	-85	-50		µA
Supply Current	I_{IN}	V_{IN} = 24V, V_{EN} = 5V		0.89	1.25	mA
Internal Undervoltage-Trip Level	V_{UVLO}	V_{IN} rising, V_{IN} = 24V	3.46	4.22	4.50	V
		V_{IN} falling, V_{IN} = 24V		3.5		
UVLO, OVLO Reference	V_{REF}	V_{IN} = 24V	1.45	1.50	1.55	V
UVLO, OVLO Threshold Hysteresis		V_{IN} = 24V		3.3		%
UVLO, OVLO Leakage Current	I_{LEAK}	V_{UVLO} = V_{OVLO} = 0 to 2V. (ADPL86610, ADPL86611 only), V_{IN} = 24V	-100		100	nA
OVLO Adjustment Range		(See *Note 4*), V_{IN} = 24V	5.5		60	V
UVLO Adjustment Range		(See *Note 4*), V_{IN} = 24V	4.5		59	V
Internal POR			3.0		4.3	V
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} =24V		1.42	2.7	Ω
Current-Limit Adjustment Range	I_{LIM}	(See *Note 5*)	10		250	mA
Current-Limit Accuracy		10mA < I_{LIM} < 20mA, V_{IN} = 24V	-6		+6	%
		20mA < I_{LIM} ≤ 250mA, V_{IN} = 24V	-5		+5	
$\overline{FLAG}$ Assertion Drop-Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V, I_{IN} = 10mA	370	470	570	mV
Reverse Current-Blocking Slow Threshold	V_{RIBS}	(V_{OUT} - V_{IN}). (ADPL86610, ADPL86612 only)	2	11	20	mV
Reverse Current-Blocking Debounce Blanking Time	t_{DEBRIB}	(ADPL86610, ADPL86612 only)	100	140	180	µs
Reverse Current-Blocking Powerup Blanking Time	t_{BLKRIB}	(ADPL86610, ADPL86612 only)	14.4	16.0	17.6	ms
Reverse Current-Blocking Fast Threshold	V_{RIBF}	(V_{OUT} -V_{IN}). (ADPL86610, ADPL86612 only)	70	105	140	mV
Reverse Current-Blocking Fast-Response Time	t_{RIB}	$I_{REVERSE}$ = 2.5A, (ADPL86610, ADPL86612 only) (See *Note 6*)		150	230	ns

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.2kΩ.) (See *Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse-Blocking Supply Current	I_{RBL}	Current into OUT when (V_{OUT} - V_{IN}) > 130mV. (ADPL86610, ADPL86612 only), V_{IN} = 24V		0.89	1.25	mA
SETI						
R_{SETI} x I_{LIM}	V_{RI}			1.5		V
Current-Mirror Output Ratio	C_{IRATIO}	10mA ≤ I_{OUT} ≤ 20mA	190	200	210	A/A
		20mA ≤ I_{OUT} ≤ 250mA	193	200	207	
Internal SETI Clamp		5mA into SETI	1.6		2.2	V
SETI Leakage Current		V_{SETI} = 1.6V	-0.1		0.1	µA
LOGIC INPUT						
EN Input-Logic High	V_{IH}	V_{IN} = 24V	1.4			V
EN Input-Logic Low	V_{IL}	V_{IN} = 24V			0.4	V
EN Pullup Voltage		EN pin unconnected. V_{IN} = 24V		1.3	2	V
EN Input Current		V_{EN} = 5.5V, V_{IN} = 24V		60	100	µA
EN Pullup Current		V_{EN} = 0.4V, V_{IN} = 24V	1.0	3.0	8.0	µA
CLMODE Input-Logic High		V_{IN} = 24V	2.0	3.8	4.9	V
CLMODE Input-Logic Low		V_{IN} = 24V	0.25	0.60	0.95	V
CLMODE Pullup Input Current		V_{IN} = 24V	8	10	12	µA
$\overline{FLAG}$, $\overline{UVOV}$, $\overline{FWD}$, $\overline{REV}$ OUTPUTs						
$\overline{FLAG}$, $\overline{UVOV}$, $\overline{FWD}$, $\overline{REV}$ Output-Logic Low Voltage		I_{SINK} = 1mA			0.4	V
$\overline{FLAG}$, $\overline{UVOV}$, $\overline{FWD}$, $\overline{REV}$ Output-Leakage Current		V_{IN} = $V_{\overline{FLAG}}$ = $V_{\overline{UVOV}}$ = $V_{\overline{FWD}}$ = $V_{\overline{REV}}$ = 5.5V. $\overline{FLAG}$, $\overline{UVOV}$, $\overline{FWD}$, and $\overline{REV}$ pins are deasserted			1	µA
TIMING CHARACTERISTICS						
Switch Turn-On Time	t_{ON_SWITCH}	V_{IN} = 24V, R_{LOAD} = 1kΩ, C_{LOAD} = 0pF, R_{SETI} = 1.2kΩ		230	450	µs
Overvoltage Switch Turn-Off Time	t_{OFF_OVP}	V_{OVLO} exceeds V_{REF} as a step; R_{LOAD} = 1kΩ		0.46	0.65	µs
Overvoltage Falling-Edge Debounce Time	t_{DEB_OVP}			20		µs
Overcurrent Protection Response Time	t_{OCP_RES}	I_{LIM} = 0.25A, C_{LOAD} = 0, I_{OUT} step from 0.125A to 0.375A. Time to regulate I_{OUT} to the current limit.		100		µs
IN Debounce Time	t_{DEB}	From V_{IN_UVLO} < V_{IN} < V_{IN_OVLO} and EN = High to V_{OUT} = 10% of V_{IN}. Elapses only at power-up.	14.4	16	17.6	ms

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.2kΩ.) (See *Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Smooth-Transition Time	t_{REF_RAMP}			100		µs
Current-Limit Blanking Time	t_{BLANK}		36	40	44	ms
Current-Limit Autoretry Time	t_{RETRY}	After blanking time from $I_{OUT} > I_{LIM}$ to $\overline{FLAG}$ deasserted (*Note 7*)	540	600	660	ms
THERMAL PROTECTION						
Thermal Shutdown	T_J			160		°C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			28		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design; not production tested.

Note 4: User-settable. See the *Overvoltage Lockout (OVLO)* and *Undervoltage Lockout (UVLO)* sections for instructions.

Note 5: The current limit can be set below 10mA with decreased accuracy.

Note 6: Guaranteed by design; not production tested.

Note 7: The ratio between autoretry time and blanking time is fixed and equal to 15.

Typical Operating Characteristics

(V_{IN} = +24V, C_{IN} = 0.47µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

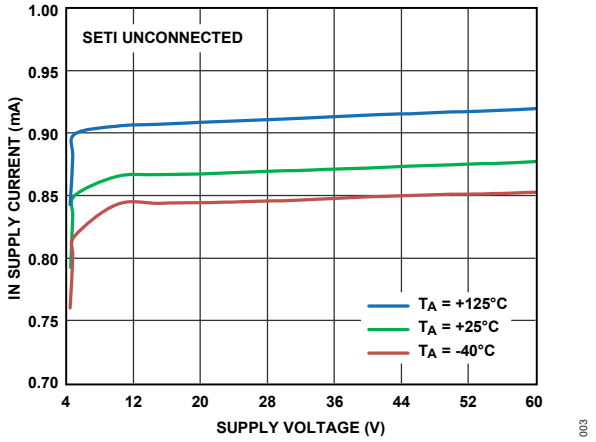


Figure 3. IN Supply Current vs. Supply Voltage

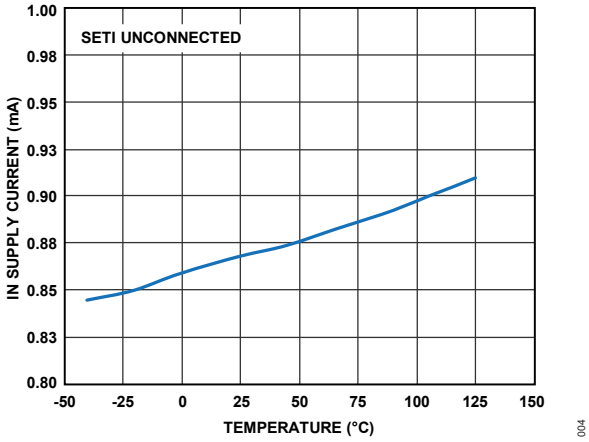


Figure 4. IN Supply Current vs. Temperature

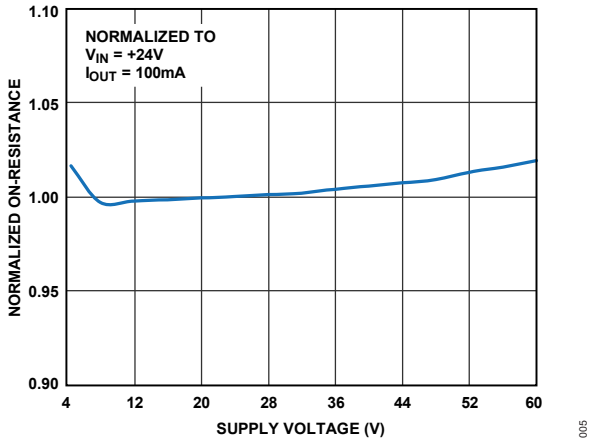


Figure 5. Normalized On-Resistance vs. Supply Voltage

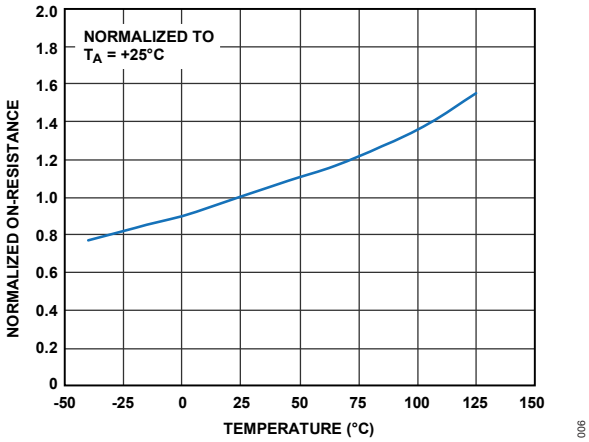


Figure 6. Normalized On-Resistance vs. Temperature

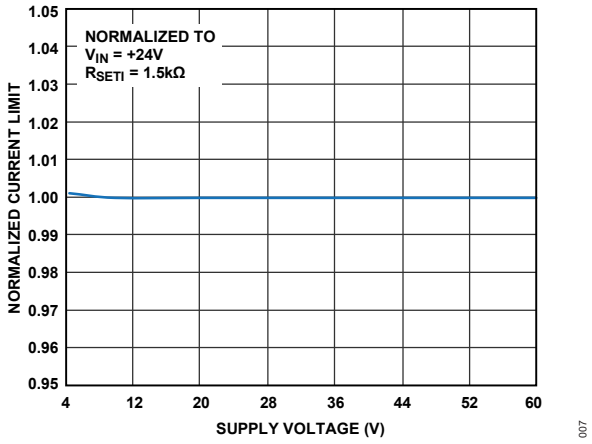


Figure 7. Normalized Current Limit vs. Supply Voltage

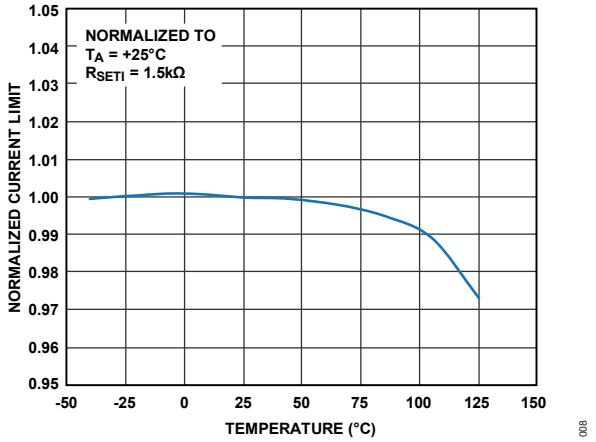


Figure 8. Normalized Current Limit vs. Temperature

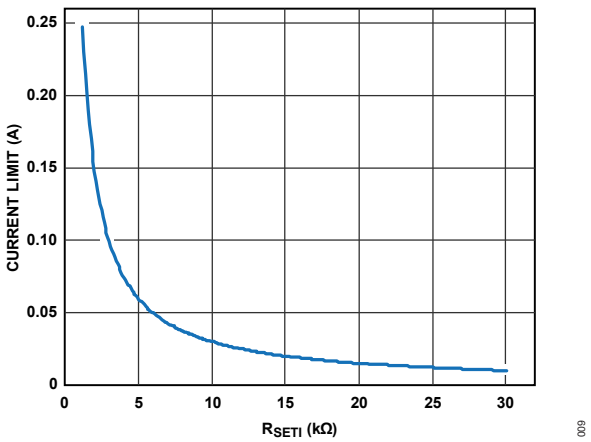


Figure 9. Current Limit vs. R_{SETI}

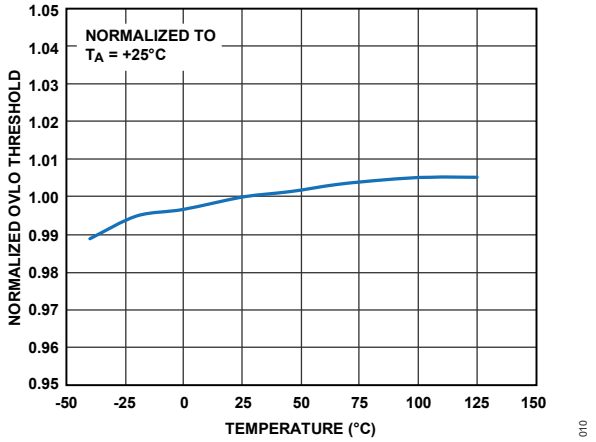


Figure 10. Normalized OVLO Threshold vs. Temperature

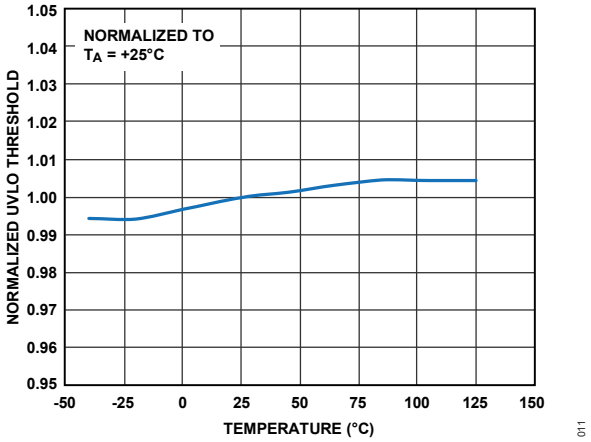


Figure 11. Normalized UVLO Threshold vs. Temperature

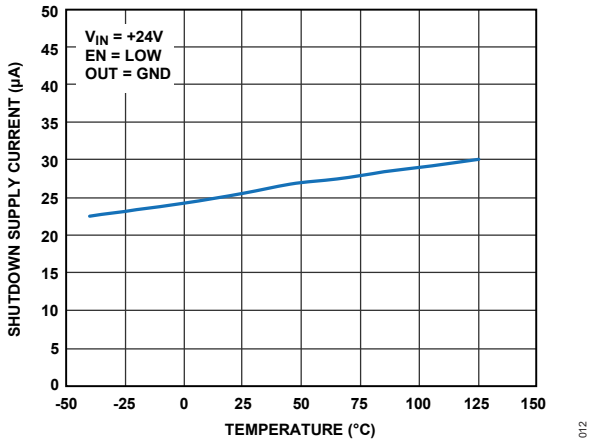


Figure 12. Shutdown Supply Current vs. Temperature

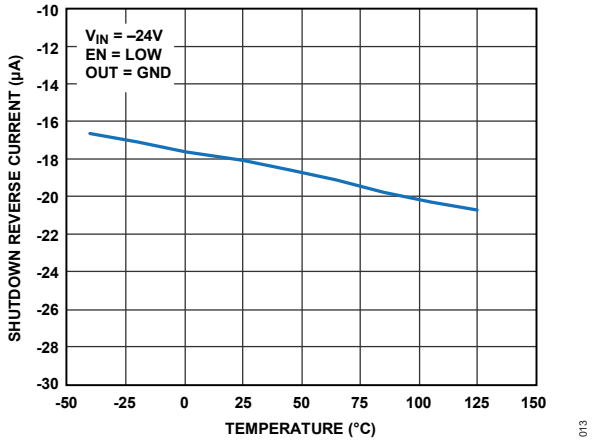


Figure 13. Shutdown Reverse Current vs. Temperature

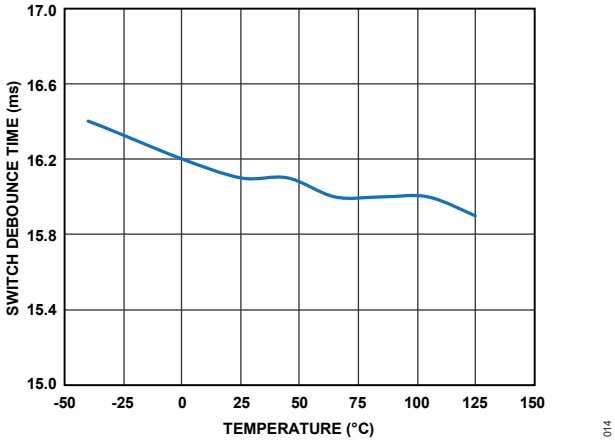


Figure 14. Switch Debounce Time vs. Temperature

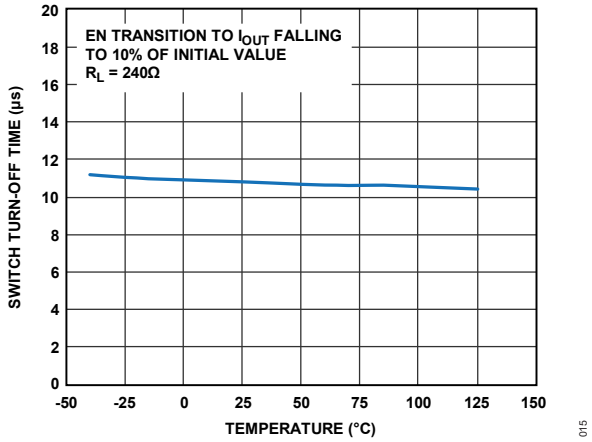


Figure 15. Switch Turn-Off Time vs. Temperature

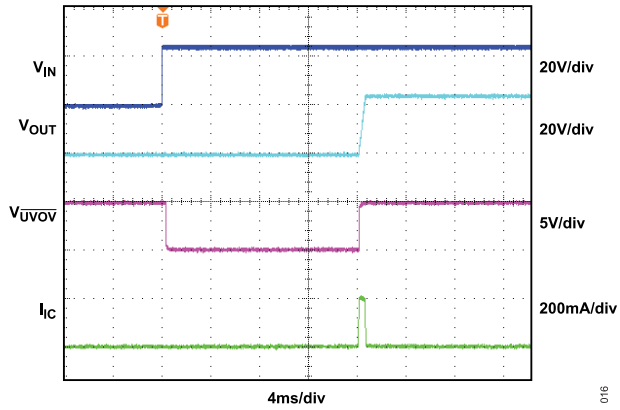


Figure 16. Power-Up Response

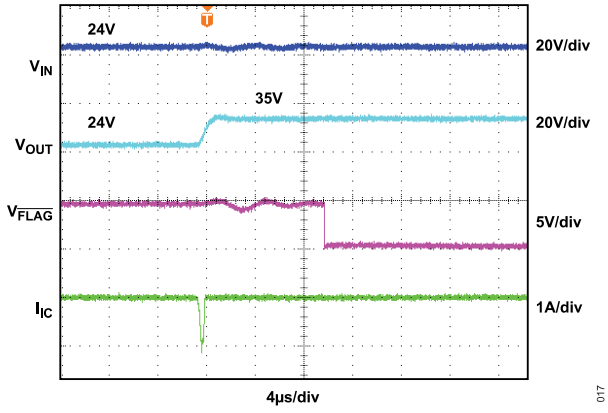


Figure 17. Reverse-Blocking Response

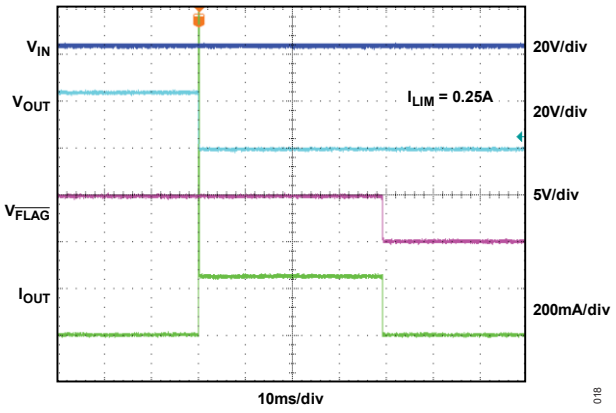


Figure 18. Output Short-Circuit Response

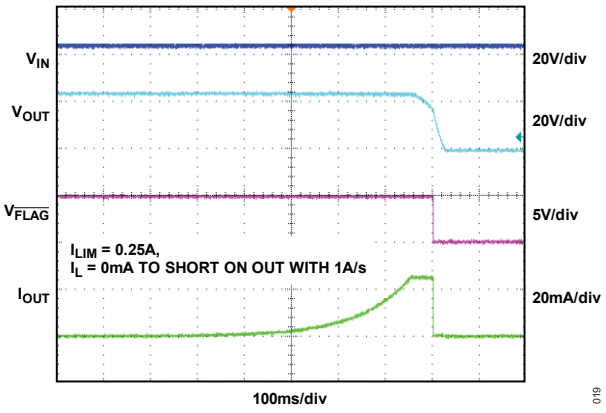


Figure 19. Current-Limit Response

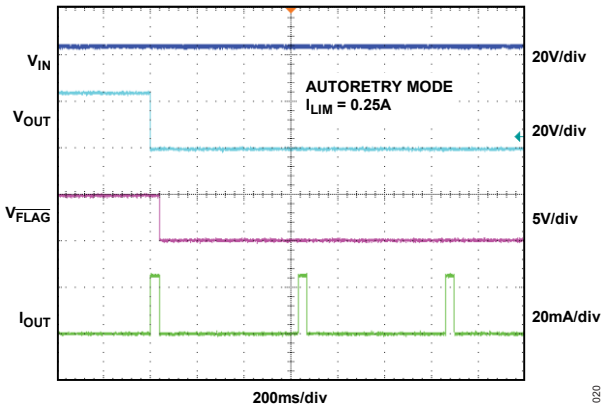


Figure 20. Autoretry Time (t_{RETRY})

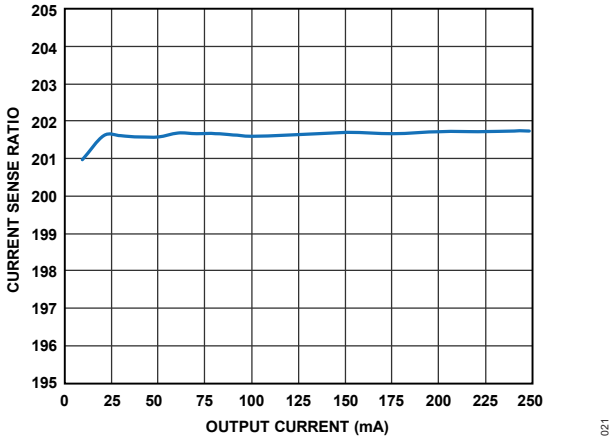


Figure 21. Current Sense Ratio vs. Output Current

Pin Configurations

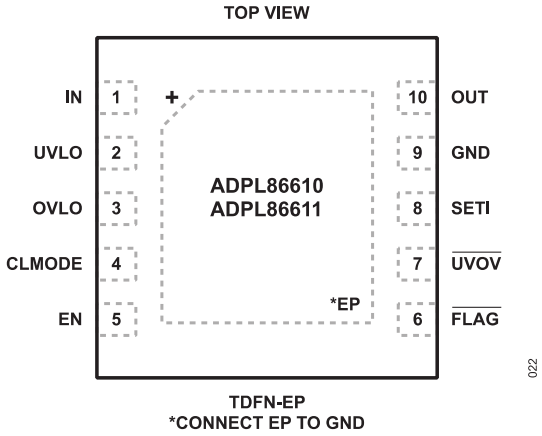


Figure 22. ADPL86610 and ADPL86611 Pin Configurations

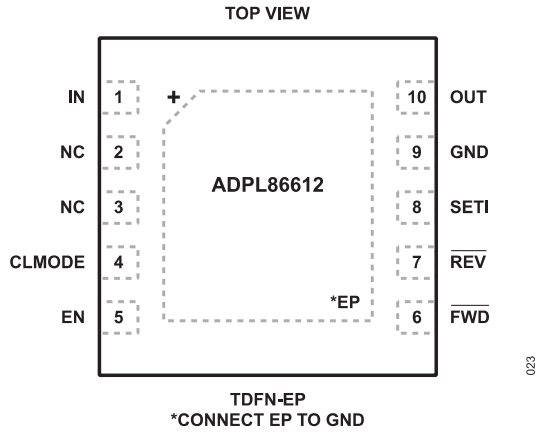


Figure 23. ADPL86612 Pin Configuration

Pin Descriptions

PIN		NAME	FUNCTION
ADPL86610 ADPL86611	ADPL86612		
1	1	IN	Input Pins. Connect a low-Equivalent series resistance (ESR) ceramic capacitor to GND. For Hot Plug-In applications, see the *Applications Information* section.
2	—	UVLO	UVLO Adjustment. Connect a resistive potential divider from IN to GND to set the UVLO threshold.
—	2-3	N.C	Not Connected. Leave unconnected.
3	—	OVLO	OVLO Adjustment. Connect a resistive potential divider from IN to GND to set the OVLO threshold.
4	4	CLMODE	Current-Limit Mode Selector. Connect CLMODE to GND for Continuous mode. Connect a 150kΩ resistor between CLMODE and GND for Latch-off mode. Leave CLMODE unconnected for Autoretry mode.
5	5	EN	Active-High Enable Input. Internally pulled up to 1.8V.
6	—	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when: • Overcurrent duration exceeds the blanking time. • Reverse current is detected (ADPL86610 only). • Thermal shutdown is active. • R_{SETI} is less than 1kΩ (max).
—	6	$\overline{FWD}$	Open-Drain, Fault Indicator Output. $\overline{FWD}$ goes low when: • Overcurrent duration exceeds the blanking time. • Thermal shutdown is active. • R_{SETI} is less than 1kΩ (max).
7	—	$\overline{UVOV}$	Open-Drain, Fault Indicator Output. $\overline{UVOV}$ goes low when: • Input voltage falls below the UVLO threshold. • Input voltage rises above the OVLO threshold.
—	7	$\overline{REV}$	Open-Drain, Fault Indicator Output. $\overline{REV}$ goes low when reverse current is detected.
8	8	SETI	Overcurrent Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set the overcurrent limit. See the *Setting Current-Limit Threshold* section.
9	9	GND	Ground.
10	10	OUT	Output Pins. For a long output cable or inductive load, see the *Applications Information* section.
—	—	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for the best thermal performance. Refer to the *ADPL86610 EV kit*, *ADPL86611 EV kit*, and *ADPL86612 EV kit* user guides for a reference layout design.

Functional Diagrams

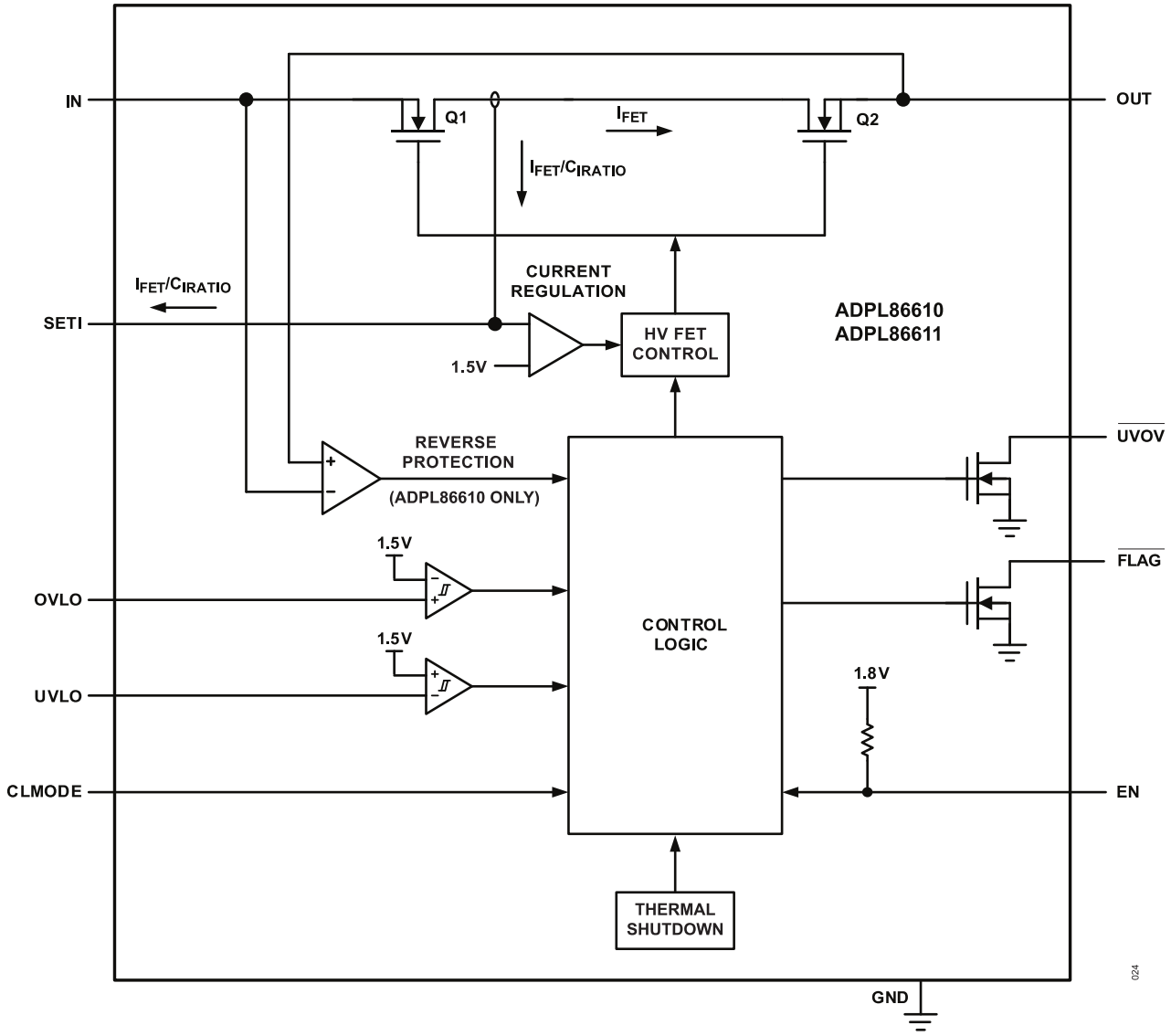


Figure 24. ADPL86610 and ADPL86611 Functional Diagrams

Functional Diagrams (continued)

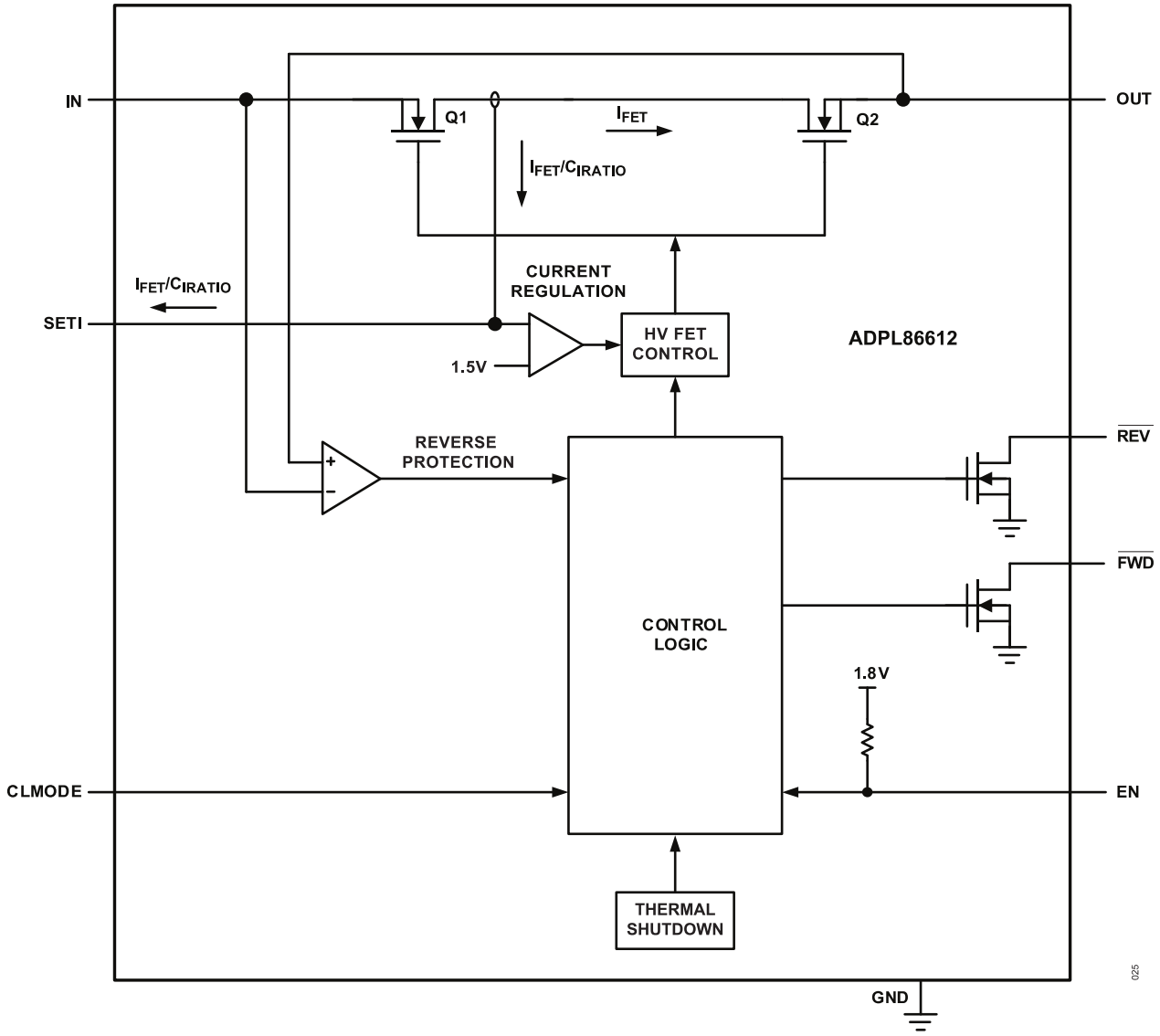


Figure 25. ADPL86612 Functional Diagram

Detailed Description

The ADPL86610/ADPL86611/ADPL86612 overvoltage- and overcurrent-protection devices offer adjustable protection boundaries for systems against input positive and negative faults up to +60V and -65V, and output load current up to 250mA. The devices feature two internal MOSFETs connected in series with a low cumulative R_{ON} of 1.42Ω (typ). The devices block out negative input voltages completely. Input undervoltage protection can be programmed between 4.5V and 59V, while the overvoltage protection can be independently programmed between 5.5V and 60V. Additionally, the devices have an internal default undervoltage lockout set at 4.2V (typ).

The devices are enabled or disabled through the EN pin by a master supervisory system, hence offering a switch operation to turn on or turn off power delivery to the connected load. The current through the devices is limited by setting a current limit, which is programmed by a resistor connected from SETI to GND.

The current limit can be programmed between 10mA to 250mA. When the device current reaches or exceeds the set current limit, the on-resistance of the internal FETs is modulated to limit the current to the set limits. The devices offer three different behavioral models when under current limited operations: Autoretry, Continuous, and Latch-Off modes. The SETI pin also presents a voltage with reference to GND, which under normal operation is proportional to the device current. The voltage appearing on the SETI pin is read by an ADC on the monitoring system for recording instantaneous device current. To avoid oscillation, do not connect more than 10pF to the SETI pin.

The devices offer communication signals to indicate different operational and fault signals. ADPL86610 and ADPL86611 offer $\overline{FLAG}$ and $\overline{UVOV}$ signals, while ADPL86612 offers $\overline{FWD}$ and $\overline{REV}$ signals. All communication signal pins are open-drain in nature and require external pull-up resistors to the appropriate system interface voltage. ADPL86610 and ADPL86612 block reverse current flow (from OUT to IN) while ADPL86611 allows reverse current flow.

All three devices offer internal thermal shutdown protection against excessive power dissipation.

Undervoltage Lockout (UVLO)

ADPL86610 and ADPL86611 have a UVLO adjustment range from 4.5V to 59V. Connect an external resistive potential divider to the UVLO pin as shown in the *Typical Operating Circuits* to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. The recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{REF} \times \left[1 + \frac{R1}{R2}\right]$$

where V_{REF} = 1.5V.

All three devices have an input UVLO threshold set at 4.2V (typ). ADPL86612 has no UVLO pin to adjust the UVLO threshold voltage externally.

Overvoltage Lockout (OVLO)

ADPL86610 and ADPL86611 devices have an OVLO adjustment range from 5.5V to 60V. Connect an external resistive potential divider to the OVLO pin as shown in the *Typical Operating Circuits* to adjust the OVLO threshold voltage. Use the following equation to adjust the OVLO threshold. The recommended value of R3 is 2.2MΩ.

$$V_{UVLO} = V_{REF} \times \left[1 + \frac{R3}{R4}\right]$$

where V_{REF} = 1.5V.

The ADPL86612 does not offer the overvoltage protection feature.

The OVLO reference voltage (V_{REF}) is set at 1.5V. If the voltage at the OVLO pin exceeds V_{REF} for a time equal to the overvoltage switch turn-off time (t_{OFF_OVP}), the switch is turned off and UVOV is asserted. When the OVLO condition is removed, the device takes the overvoltage falling-edge debounce time (t_{DEB_OVP}) to start the switch turn-on process. The switch turns back on after the switch turn-on time (t_{ON_SWITCH}) and UVOV is deasserted. *Figure 26* depicts typical behavior in overvoltage conditions.

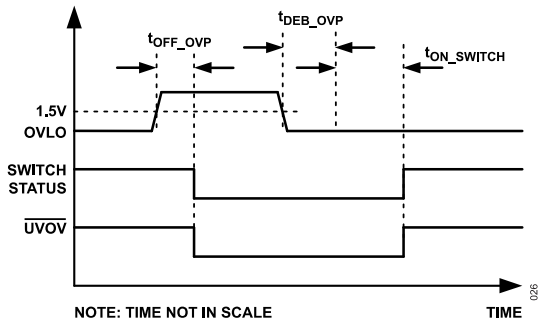


Figure 26. Overvoltage-Fault Timing Diagram

Input Debounce Protection

The devices feature input debounce protection. The devices start operation (turn on the internal FETs) only if the input voltage is higher than the UVLO threshold for a period greater than the debounce time (t_{DEB}). The t_{DEB} elapses only at power-up of the devices. This feature is intended for applications where the EN signal is present when the power supply ramps up. *Figure 27* depicts a typical debounce timing diagram.

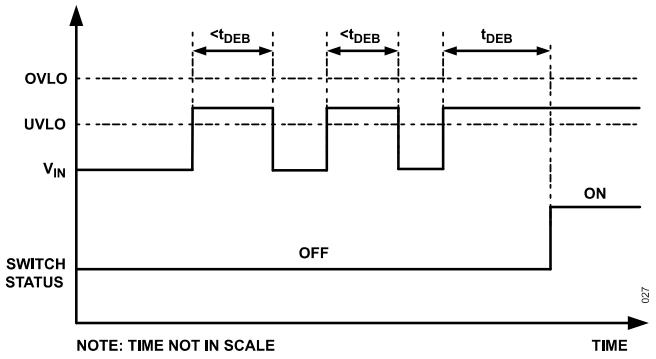


Figure 27. Debounce Timing Diagram

Enable

The devices are enabled or disabled through the EN pin by driving it above or below the EN threshold voltage. Hence the devices can be used to turn on or off power delivery to connected loads using the EN pin. The Input debounce protection is present when the devices turn on by driving the EN pin.

Setting Current-Limit Threshold

Connect a resistor between SETI and GND to program the current-limit threshold in the devices. Use the following equation to calculate the current-limit setting resistor:

$$R_{SETI}\,(k\Omega) = \frac{300}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current limit in mA.

Do not use a R_{SETI} lower than 1.2kΩ. *Table 1* shows current-limit thresholds for different resistor values.

Table 1. Current-Limit Threshold vs. SETI-Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT (mA)
30	10
12	25
6	50
3	100
2	150
1.5	200
1.2	250

The devices feature a read-out of the current flowing into the IN pin. A current mirror, with a ratio of C_{IRATIO}, is implemented, using a current-sense auto-zero operational amplifier. The mirrored current flows out through the SETI pin, into the external current-limit resistor. The voltage on the SETI pin provides information about the IN current with the following relationship:

$$I_{IN-OUT}(A) = \frac{V_{SETI}(V)}{R_{SETI}(k\Omega)}$$

If SETI is left unconnected, V_{SETI} ≥ 1.5V. The current regulator does not allow any current to flow. During startup, this causes the switches to remain off and $\overline{FLAG}$ (or $\overline{FWD}$) to assert after t_{BLANK} elapses. During startup, 270µA current is forced to flow through R_{SETI}. If the voltage at SETI is below 150mV, the switches remain off, and $\overline{FLAG}$ (or $\overline{FWD}$) asserts.

Current-Limit Type Select

The CLMODE pin is used to program the overcurrent response of the devices in one of the following three modes:

Autoretry mode (CLMODE pin is left unconnected), Continuous mode (CLMODE pin is connected to GND), Latch-off mode (a 150kΩ resistor is connected between CLMODE and GND).

Autoretry Current Limit

In autoretry current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts if the overcurrent condition is present for t_{BLANK}. The timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed. A retry time delay (t_{RETRY}) starts immediately after t_{BLANK} has elapsed. During the t_{RETRY} time, the switch remains off. Once the t_{RETRY} has elapsed, the switch is turned back on again. If the fault still exists, the cycle is repeated, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin remains asserted. If the overcurrent condition is resolved, the switch stays on.

The autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is on during the t_{BLANK} time, the supply current is held at the current limit. During the t_{RETRY} time, there is no current through the switch. Thus, the output current is much less than the programmed current limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK}}{t_{RETRY} + t_{BLANK}}\right]$$

With a 40ms (typ) t_{BLANK} and 600ms (typ) t_{RETRY}, the duty cycle is 6.25%, resulting in a 93.75% power reduction when compared to the switch being on the entire time. *Figure 28* depicts typical behavior in the autoretry current-limit mode.

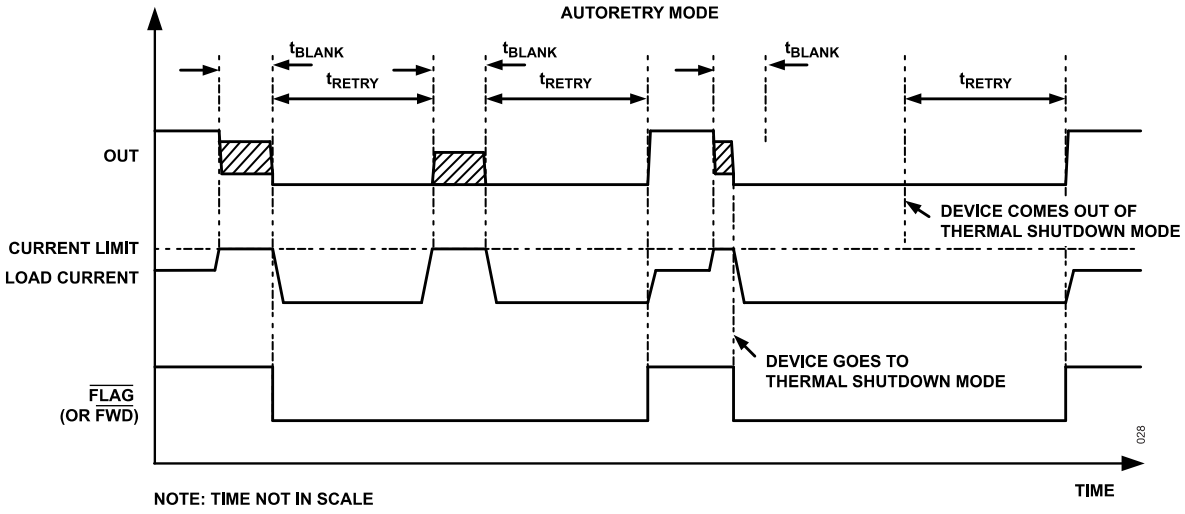


Figure 28. Autoretry Fault-Timing Diagram

Continuous Current Limit

In continuous current-limit mode, when the current through the device reaches the current limit threshold, the device limits the output current to the programmed current limit. The $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts if an overcurrent condition is present for t_{BLANK} and deasserts when the overload condition is removed. *Figure 29* depicts typical behavior in the continuous current-limit mode.

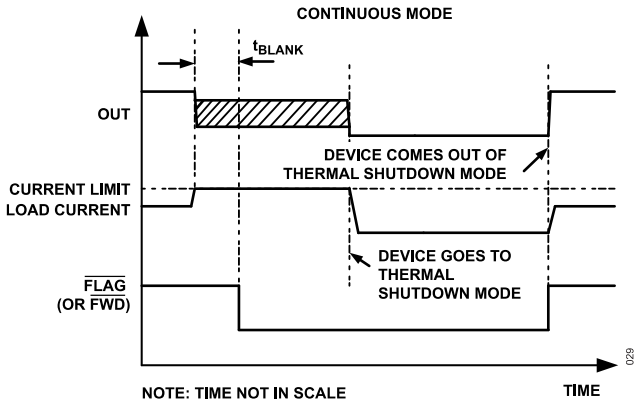


Figure 29. Continuous Fault-Timing Diagram

Latch-Off Current Limit

In latch-off current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts if an overcurrent condition is present for t_{BLANK}. The timer resets when the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond t_{BLANK}. To reset the switch, either toggle the control logic (EN) or cycle the input voltage. *Figure 30* depicts typical behavior in latch-off current-limit mode.

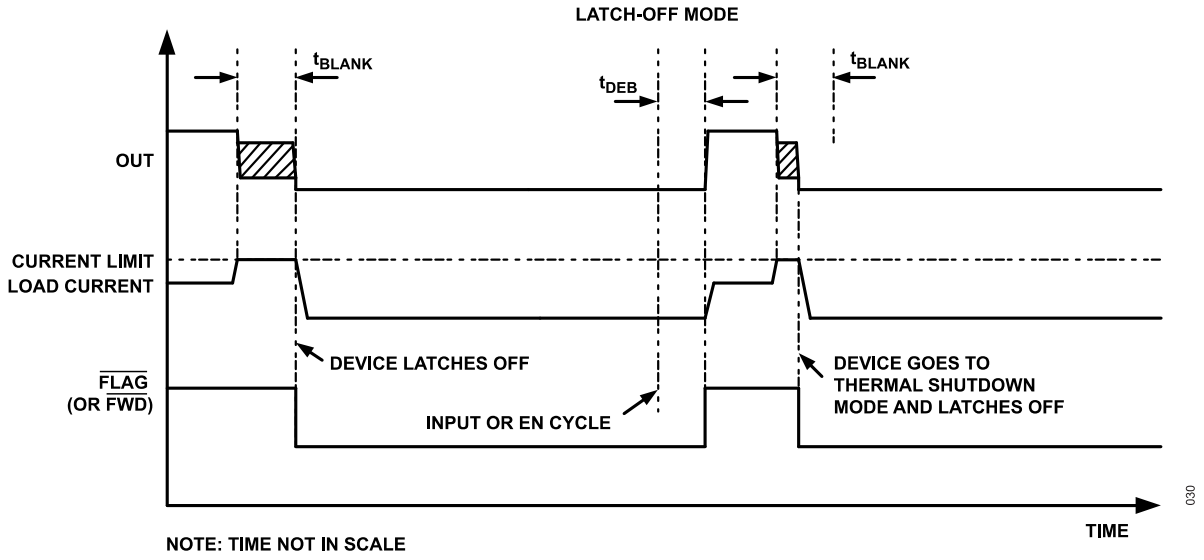


Figure 30. Latch-Off Fault-Timing Diagram

Reverse Current Protection

In ADPL86610 and ADPL86612, the reverse current-protection feature is enabled, and it prevents reverse current flow from OUT to IN pins. In ADPL86611, the reverse current-protection feature is disabled, which allows reverse current flow from the OUT to IN pins. This feature is useful in applications with inductive loads.

In ADPL86610 and ADPL86612 devices, two different reverse-current features are implemented. A slow reverse-current condition is detected if (V_{IN} - V_{OUT}) < V_{RIBS} is present for reverse current-blocking debounce blanking time (t_{DEBRIB}). Only the input NFET (Q1) is turned off, and the $\overline{FLAG}$ (or $\overline{REV}$) pin is asserted while the output NFET (Q2) is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, Q1 is turned back on, and the $\overline{FLAG}$ (or $\overline{REV}$) pin is deasserted. Q1 takes t_{Q1_ON} (~100µs) time to turn on. *Figure 31* depicts typical behavior in slow reverse current conditions.

A fast reverse-current condition is detected if (V_{IN} - V_{OUT}) < V_{RIBF} is present for reverse current blocking fast response time (t_{RIB}). Only the input NFET (Q1) is turned off, and the $\overline{FLAG}$ (or $\overline{REV}$) pin is asserted while the output NFET (Q2) is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, Q1 is turned back on, and the $\overline{FLAG}$ (or $\overline{REV}$) pin is deasserted. Q1 takes t_{Q1_ON} (~100µs) time to turn on. *Figure 32* depicts typical behavior in a fast reverse-current condition.

The device contains two reverse-current thresholds with slow (< 140µs) and fast (< 150ns) response time for reverse protection. The threshold values for slow reverse are 11mV (typ), whereas for fast reverse, it is 105mV (typ). This feature results in robust operation in a noisy environment, while still delivering fast protection for severe faults, such as input short-circuit or hot plug-in at the OUT pins.

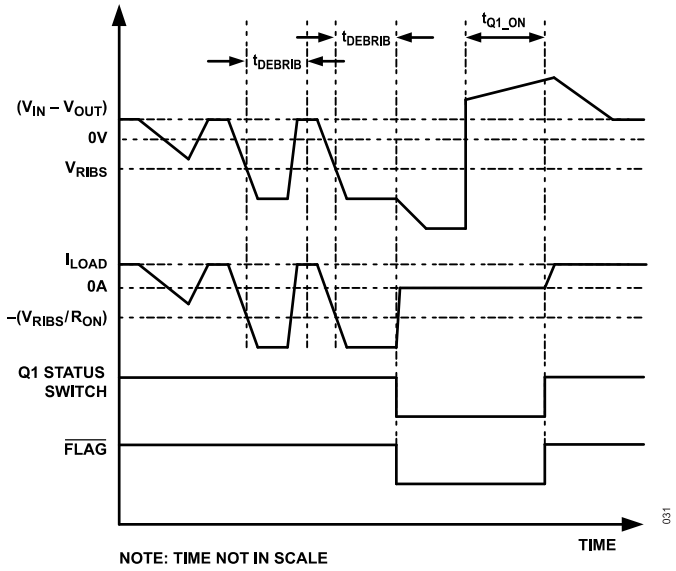


Figure 31. Slow Reverse-Current Fault-Timing Diagram

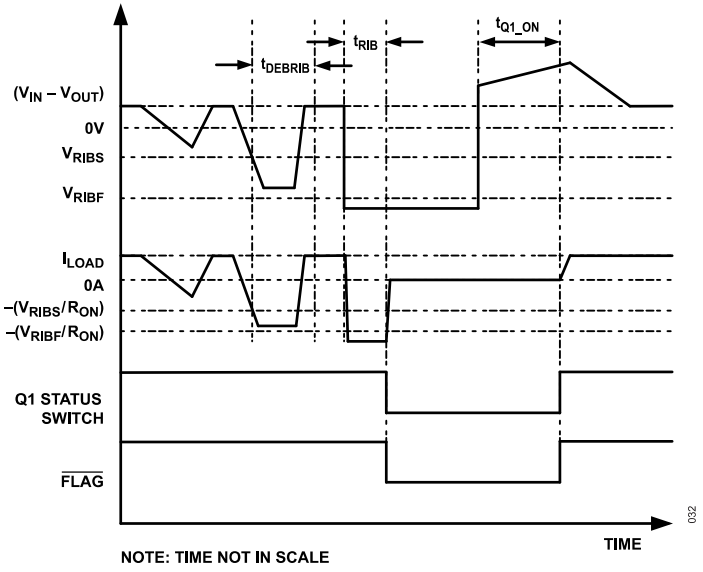


Figure 32. Fast Reverse-Current Fault-Timing Diagram

Fault Output

ADPL86610 and ADPL86611 devices have two open-drain fault outputs, $\overline{FLAG}$ and $\overline{UVOV}$. They require external pull-up resistors to a DC supply. The $\overline{FLAG}$ pin goes low when any of the following conditions occur:

- Overcurrent duration exceeds blanking time.
- Reverse current is detected (ADPL86610 only).
- Thermal shutdown is active.
- R_{SETI} is less than 1kΩ (max).

The other fault output $\overline{UVOV}$ goes low, when the input voltage falls below the UVLO threshold or rises above the OVLO threshold. Note that the UVLO fault has a debounce time of 16ms. This fault is removed 16ms after the input voltage has crossed the UVLO threshold. This debounce also elapses only at power-up. As a consequence, the $\overline{UVOV}$ pin fault signal is always asserted at power-up for at least 16ms.

The ADPL86612 device has two open-drain fault outputs, $\overline{FWD}$ and $\overline{REV}$. They require external pull-up resistors to a DC supply. FWD goes low when any of the following conditions occur:

- Overcurrent duration exceeds the blanking time.
- Thermal shutdown is active.
- R_{SETI} is less than 1kΩ (max).

$\overline{REV}$ goes low when reverse current is detected.

Thermal Shutdown Protection

The devices have a thermal shutdown feature to protect against overheating. The devices turn off, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts when the junction temperature exceeds +160°C (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools down by 28°C (typ), except when in latchoff mode, the devices remain latched off.

The thermal limit behaves similarly to the current limit. In autoretry mode, the thermal limit works with the autoretry timer. When the junction temperature falls below the falling thermal-shutdown threshold, devices turn on after the retry time. In latch-off mode, the devices latch off until power or EN is cycled. In continuous mode, the devices only disable while the temperature is over the limit. There is no blanking time for thermal protection. *Figure 28*, *Figure 29*, and *Figure 30* depict typical behavior under different current limit modes.

Applications Information

IN Capacitor

A 0.47µF capacitor from the IN pin to GND is recomended to hold input voltage during sudden load-current changes.

Hot Plug-In at IN Terminal

In many system powering applications, an input-filtering capacitor is required to lower radiated emission and enhance Electrostatic discharge (ESD) capability. In hot plug-in applications, parasitic cable inductance, along with the input capacitor, causes overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to a maximum of 60V shall be placed close to the input terminal for enhanced protection. The maximum tolerated slew rate at the IN pins is 100V/µs.

Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The ADPL86610 and ADPL86612 devices detect reverse current entering at the OUT pin and flowing out of the IN pin and turn off the internal FETs. The magnitude of the reverse current depends on the inductance of the input circuitry and any capacitor installed near the IN pins.

The devices can be damaged in case V_{IN} goes so negative that (V_{OUT} - V_{IN}) > 60V.

OUT Capacitor

The maximum capacitive load (C_{MAX}) that can be connected is a function of the current-limit setting (I_{LIM} in mA), the blanking time (t_{BLANK} in ms), and the input voltage. C_{MAX} is calculated using the following relationship:

$$C_{MAX(\mu F)} = \frac{I_{LIM}(mA) \times t_{BLANK(TYP)}(ms)}{V_{IN}(V)}$$

For example, for V_{IN} = 24V, $t_{BLANK(TYP)}$ = 40ms, and I_{LIM} = 250mA, C_{MAX} is 416µF.

Output capacitor values in excess of C_{MAX} can trigger false overcurrent conditions. Note that the above expression assumes no load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current, resulting in a longer charging period; hence, the possibility of a false overcurrent condition.

Hot Plug-In at OUT Terminal

In some applications, there might be a possibility of applying an external voltage at the OUT terminal of the devices with or without the presence of an input voltage. During these conditions, devices detect any reverse current entering at the OUT pin and flowing out of the IN pin and turn off the internal FETs. Parasitic cable inductance, along with input and output capacitors, causes overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the absolute maximum ratings. The maximum tolerated slew rate at OUT pins is 100V/µs.

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a Schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small, and the package temperature change is minimal. Power dissipation under steady-state normal operation is calculated as:

$$P_{(SS)} = I^2_{OUT} \times R_{ON}$$

See the *Electrical Characteristics* table and *Typical Operating Characteristics* for R_{ON} values at various operating temperatures.

If the output is continuously shorted to ground at the maximum supply voltage, the switches with the autoretry option do not cause thermal shutdown detection to trip. Power dissipation in the devices operating in autoretry mode is calculated using the following equation:

$$P_{(MAX)} = \frac{V_{IN(MAX)} \times I_{OUT(MAX)} \times t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

Attention must be given to continuous current-limit mode when the power dissipation during a fault condition can cause the device to reach the thermal-shutdown threshold. Thermal vias from the exposed pad to ground plane are highly recommended to increase the system thermal capacitance while reducing the thermal resistance to the ambient.

ESD Protection

The devices are specified for ±15kV (HBM) ESD on IN when IN is bypassed to ground with a 0.47µF, low-ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) (typ) ESD on IN. All the pins have a ±2kV (HBM) typical ESD protection. *Figure 33* shows the HBM, and *Figure 34* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

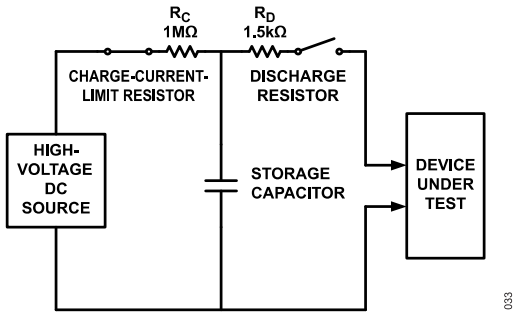


Figure 33. Human Body ESD Test Model

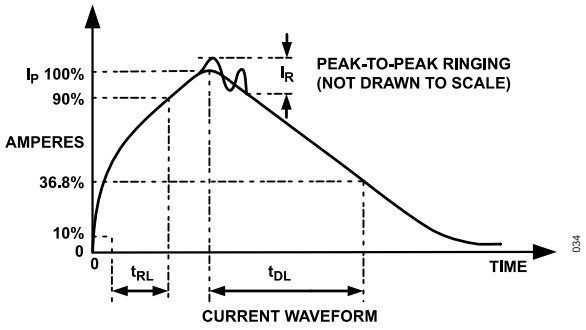


Figure 34. Human Body Current Waveform

Ordering Information

PART	TEMP RANGE	PIN PACKAGE	FEATURE DIFFERENCES
ADPL86610ATB+T	-40°C to +125°C	10 TDFN-EP*	OV, UV, Reverse Voltage Protection
ADPL86611ATB+T	-40°C to +125°C	10 TDFN-EP*	OV, UV
ADPL86612ATB+T	-40°C to +125°C	10 TDFN-EP*	Reverse Voltage Protection

+Denotes a lead (Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

**EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—