AD9081-FMCA-EBZ/AD9082-FMCA-EBZ User Guide
UG-1829

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Preliminary Technical Data

Evaluating the AD9081 or AD9082 Mixed-Signal Front-End RF Transceiver

FEATURES

- Fully functional evaluation boards for the AD9081 and AD9082
- PC software for control with ACE software
- On-board clocking provided by the HMC7044 manages device and FPGA clocking
- Option to switch to external direct clocking

EVALUATION KIT CONTENTS

- AD9081-FMCA-EBZ/AD9082-FMCA-EBZ evaluation board
- Subminiature push on female (SMP-F) to Subminiature Version A female (SMA-F) cables
- MicroSD card (AD-FMC-SDCARD)

ADDITIONAL HARDWARE NEEDED

- ADS9-V2EBZ FPGA-based data capture board
- Signal generator for analog input
- Spectrum analyzer (to measure DAC output)
- SMA cable
- SMA female to female adapter (optional)
- Ethernet to USB adapter (optional)
- PC with USB port and Ethernet port
- Windows® 7 or newer operating system

SOFTWARE NEEDED

- Analysis, control, evaluate (ACE) software
- DPGDownloaderLite software (included in ACE installation)
- WinSCP (or similar Telnet software)

DOCUMENTS NEEDED

- AD9081/AD9082 data sheet
- ADS9-V2EBZ user guide
- ACE documentation
- Serial Control Interface Standard (Rev 1.0)
- AN-835

EVALUATION BOARD PHOTOGRAPHS

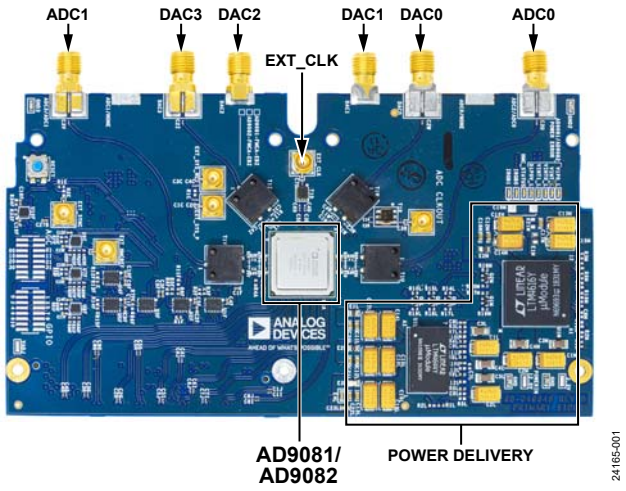


Figure 1. AD9082-FMCA-EBZ Top Image

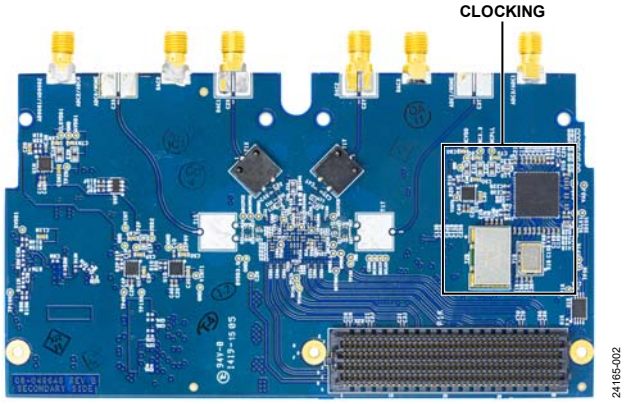


Figure 2. AD9082-FMCA-EBZ Bottom Image

GENERAL DESCRIPTION

This user guide describes the AD9081-FMCA-EBZ and AD9082-FMCA-EBZ evaluation boards, which provide all of the support circuitry required to operate the AD9081 and AD9082 in their various modes and configurations. The application software used to interface with the devices is also described. The AD9081-FMCA-EBZ and AD9082-FMCA-EBZ evaluation boards connect to the Analog Devices, Inc., ADS9-V2EBZ for evaluation with the ACE software. The boards can also interface to commercially available field-programmable gate array (FPGA) development boards from Xilinx® or Intel®. Information on how to use these platforms to evaluate the AD9081 or AD9082 is available in the Using the AD-FMC-SDCARD section.

The ACE software allows the user to set up the AD9081 or AD9082 in various modes, and capture analog-to-digital converter (ADC) data for analysis. The DPGDownloaderLite software generates and transmits vectors to the DACs, which can then be sent to a spectrum analyzer for further analysis.

For more details, see the AD9081 and AD9082 data sheets, which must be consulted in conjunction with this user guide when using the evaluation boards.

TABLE OF CONTENTS

EVALUATION BOARD OVERVIEW

BOARD MODELS

The AD9081 and AD9082 have different board models. They are all listed in Table 1.

Certain early revisions of the boards shipped with a 122.88 MHz on-board crystal oscillator. The ACE plugin is designed to detect the board and make it function appropriately.

EVALUATION BOARD CONNECTION OVERVIEW

Figure 3 shows the basic hardware setup required to evaluate the AD9081 or AD9082 (AD9082-FMCA-EBZ shown as an example). This setup uses the on-board clock to manage the clocks for the AD9082 as well as the FPGA for proper functioning of the transceivers.

Table 1. Board Variants and Their EEPROM Designators

Board Model Number	On-Board Crystal Oscillator	EEPROM Label
AD9081-FMCA-EBZ	100 MHz	AD9081-FMCA-EBZ-A2
AD9082-FMCA-EBZ	100 MHz	AD9082-FMCA-EBZ-A2

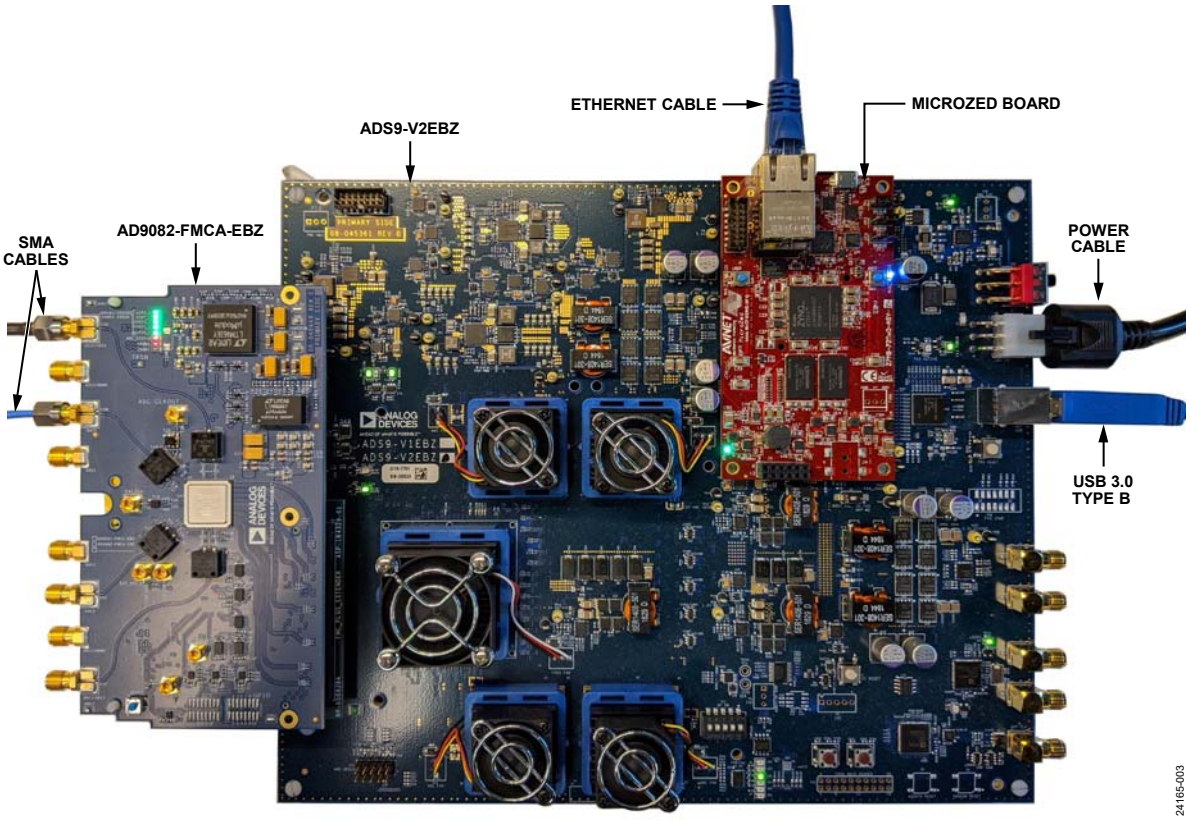


Figure 3. Bench Setup for Evaluation of the AD9081 or AD9082

EVALUATION BOARD SOFTWARE

ACE AND DPGDownloaderLite

Download and run the ACE installer from the ACE web page at www.analog.com/ace. Check all options under the **High Speed DAC Components** section to install DPGDownloaderLite, which replaces the legacy DPGDownloader (see Figure 4).

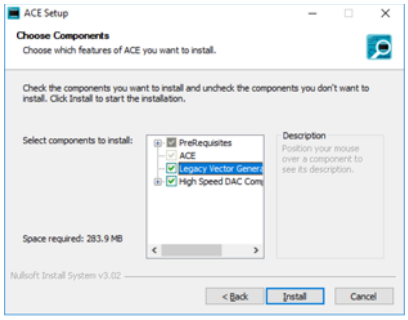


Figure 4. ACE Installation Including DPGDownloaderLite

After the ACE software is installed, the user must install the plugin for the specific evaluation board. There are two options for installing the plugin, as described in the following sections.

Plugin Installation from ACE

Installing plugins can be performed using the **Plug-in Marketplace** feature in the ACE software as described in this section. Plugins can be downloaded from the ACE software page by searching for the relevant device number within the ACE software.

To install a plugin from ACE, follow these steps:

1. From the **Start** menu, click **All Programs** > **Analog Devices** > **ACE** to open the main ACE software window.
2. In the left pane, click **Plug-in Marketplace**. The **Manage Plug-ins** window opens, as shown in Figure 5.

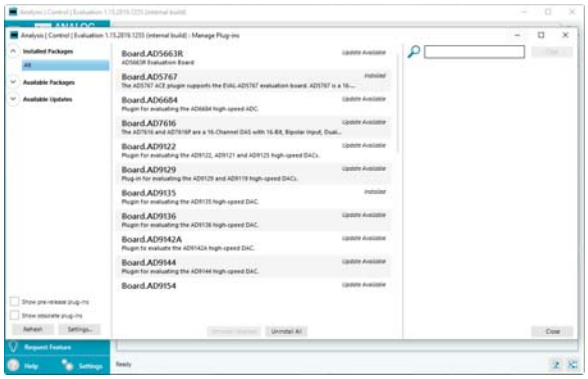


*Figure 5. ACE **Manage Plug-ins** Window*

3. Click the **Available Packages** dropdown menu on the left side of the software window.
4. Enter the device model number (**AD9081** or **AD9082**) in the search bar on the right side of the window to search for the device that is intended for evaluation and find the appropriate board plugin.
5. Select the required plugin that supports the AD9081 or AD9082, and click **Install Selected**.
6. Click **Close**.

Plugin Installation from the Web

To install the plugin from the web, follow these steps:

1. Ensure that the ACE software is installed.
2. From the ACE software page on the Analog Devices, Inc., website (www.analog.com/ace), navigate to the **ACE Evaluation Board Plug-ins** section and search for the device to evaluate.
3. Click the appropriate board plugin, as shown in Figure 6. The board plugin automatically downloads to the PC. When the download is complete, locate the downloaded file. Note that if the browser used for the plugin download is Internet Explorer, the file extension of the plugin file is **.zip**. If this occurs, right click the file and rename the file extension to **.acezip**.
4. Double click the **.acezip** file to automatically install the plugin.
5. The plugin installation process open the ACE software. Close ACE after plugin installation completes.

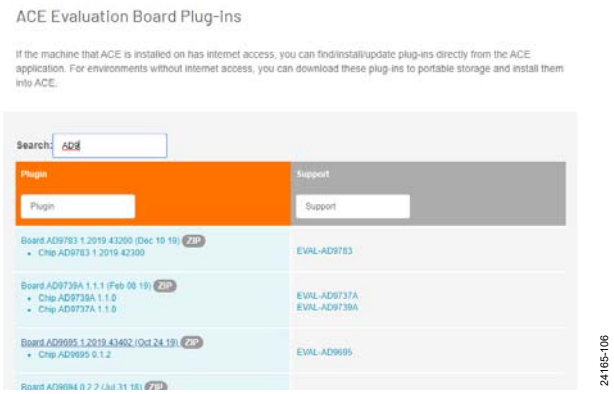


*Figure 6. **ACE Evaluation Board Plug-ins** Web Installation*

INTRODUCTION TO THE AD9081 OR AD9082 PLUGIN

The AD9081 or AD9082 plugin allows the user to evaluate the AD9081 or AD9082 chip via the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ evaluation board. First, ensure the board is connected with all proper hardware as shown in Figure 3. Next, ensure that the ADS9-V2EBZ board is powered on before opening ACE. When the user opens the ACE software, the plugin appears in the **Attached Hardware** section (see Figure 7).

Board View

Double clicking the board icon in the **Attached Hardware** section in ACE opens the **AD9081-FMCA-EBZ-A2** or **AD9082-FMCA-EBZ-A2** board view.

The board view tab enables the user to quickly set up the AD9081 or AD9082. Figure 8 shows the **QUICK CONFIGURATION** pane within the **AD9082-FMCA-EBZ-A2** board view.

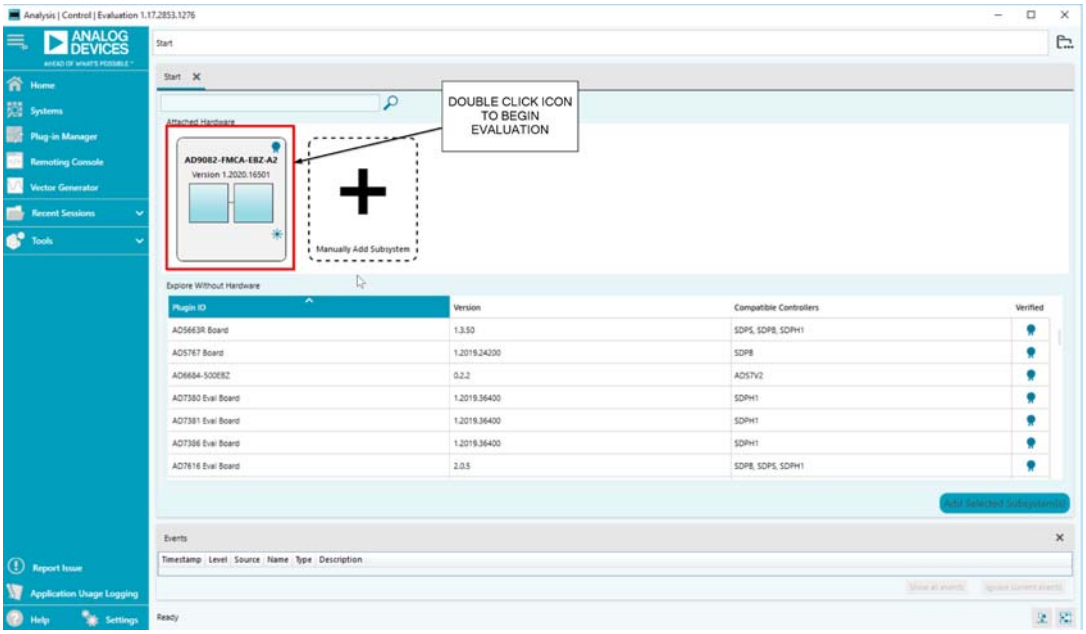


*Figure 7. ACE Initial Window Showing **Attached Hardware***

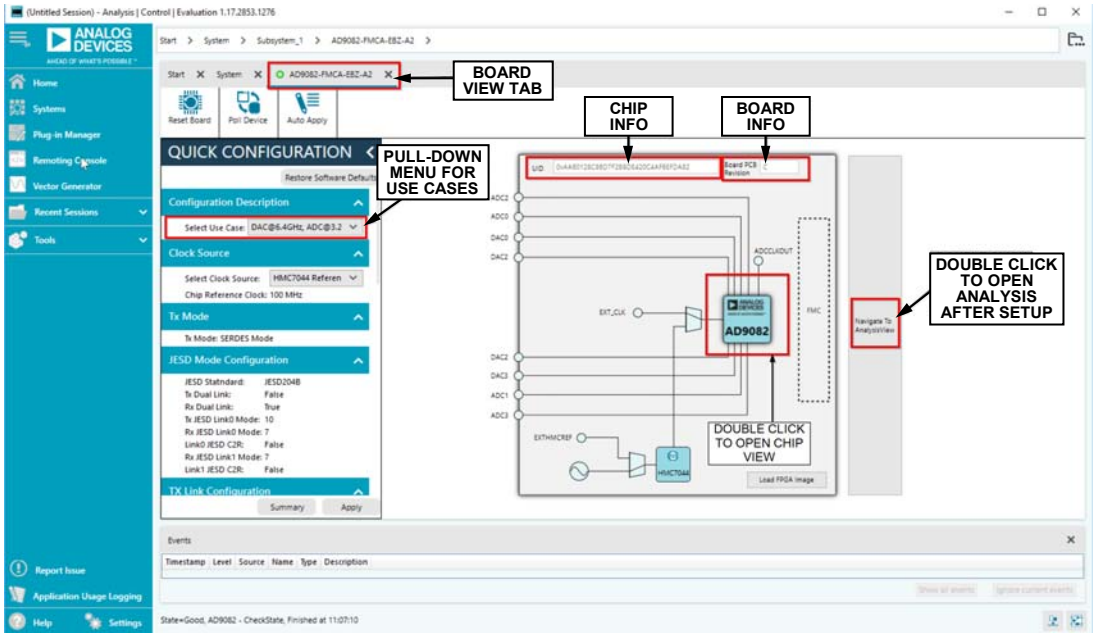


*Figure 8. **AD9082-FMCA-EBZ-A2** Board View Tab Detail*

Chip View

Double clicking the **AD9081** or **AD9082** icon in the board view opens the chip view. The chip view enables the user to customize the AD9081 or AD9082 beyond the functions available in the board view. Use the **QUICK CONFIGURATION** pane in the chip view if using a direct external clock. Figure 9 shows the details of the chip view for the **AD9082** as an example.

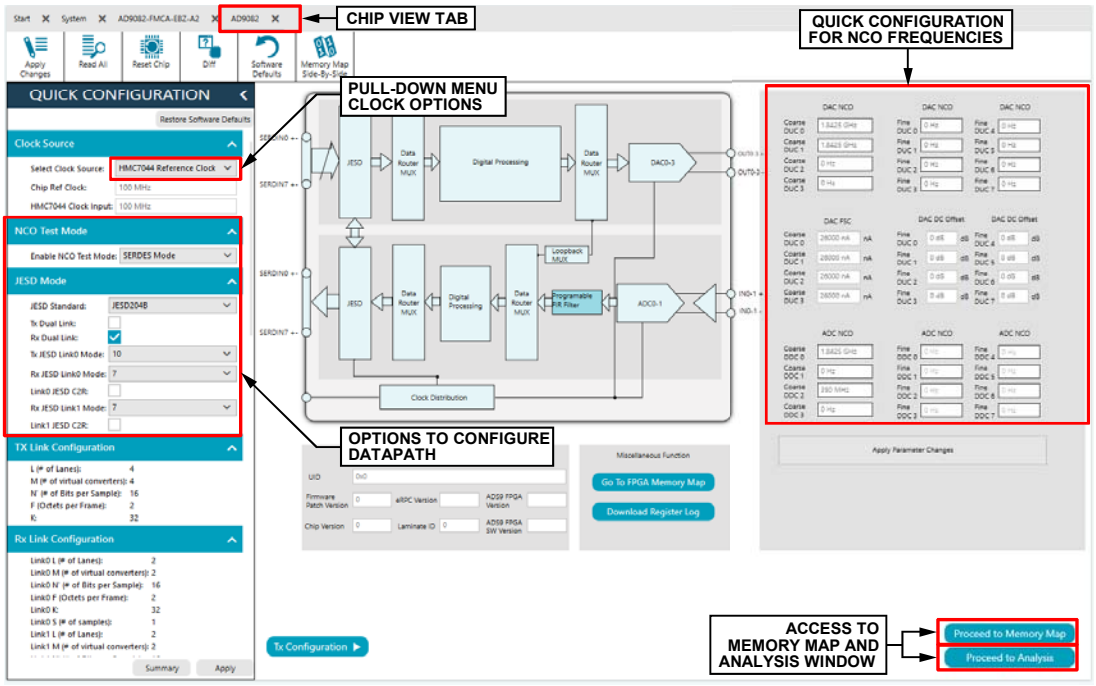


*Figure 9. **AD9082** Chip View Tab Detail*

SET UP MICROZED CONNECTION

Before performing the evaluation of the AD9081 or AD9082, the Ethernet interface to the MicroZed™ board must be set up by configuring the network interface between the PC and the MicroZed board.

MICROSD CARD FOR THE MICROZED BOARD

To ensure proper connection between the microSD card and the MicroZed board, follow these steps:

1. Locate the microSD card labeled HSX from the contents of ADS9-V2EBZ packaging.
2. Connect the microSD card to the MicroZed board (the contacts of the microSD card are face up). See Figure 10 for more details.

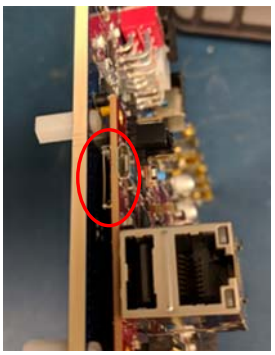


Figure 10. MicroSD Card Slot in MicroZed Board

3. As a precaution, ensure that the MicroZed board is seated properly on the ADS9-V2EBZ, as shown in Figure 3. Only a visual inspection is needed.

MODE JUMPER CONNECTIONS FOR THE MICOZED BOARD

Ensure that the mode jumpers on the MicroZed board are connected as shown in Figure 11.

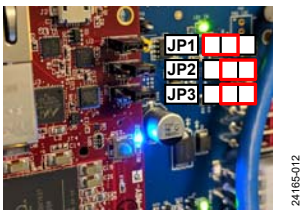


Figure 11. Mode Jumper Connections for MicroZed Board

The boot mode jumpers (JP1 to JP3) shown in Figure 11 allow the MicroZed board to boot the image from the microSD card.

CONFIGURE THE NETWORK INTERFACE TO THE MICROZED BOARD

To configure the network interface to the MicroZed board, follow these steps:

1. Ensure that the connections to ADS9-V2EBZ are as shown in Figure 3. It is not necessary to connect the AD9082-FMCA-EBZ evaluation board.
2. One end of the Ethernet cable can be connected directly to the PC Ethernet port or to a USB to Ethernet adapter, with the other end connected to the MicroZed board.
3. Power on the ADS9-V2EBZ board. Allow up to 10 sec for the MicroZed board to boot up.
4. Open the local area connection settings. On Windows 7: **Start Menu > Control Panel > Network and Sharing Center > Change adapter settings**. On Windows 10: **Start Menu > Settings > Network & Internet > Change adapter options**.
5. If the **Local Area Connection** icon does not appear in the **Network Connections** window, unplug the Ethernet connection from the MicroZed board and then reconnect it.

6. Double click the **Local Area Connection** icon that appears (Figure 12 shows **Local Area Connection 3** as an example).
7. Click **Properties**.
8. Select **Internet Protocol Version 4 (TCP/IPv4)**.
9. Click **Properties**.
10. Enter **192.168.0.1** in the **IP address** field.
11. Ensure the **Subnet mask** field shows **255.255.255.0**.
12. Click **OK**.

CHECKING THE CONNECTION TO THE MICROZED BOARD

To check the connection to the MicroZED board, follow these steps:

1. Power cycle the ADS9-V2EBZ. Wait about 10 sec for the MicroZed to boot up.
2. Open a telnet software like WinSCP or Tera Term.
3. Initiate a secure shell (SSH) connection to 192.168.0.1, which is the IP address to the embedded remote procedure call (eRPC) server in the MicroZed board.
4. Login with username: **root** and password: **analog**.
5. When the login is complete, the contents of the root folder display in the telnet software, which confirms the Ethernet connection.

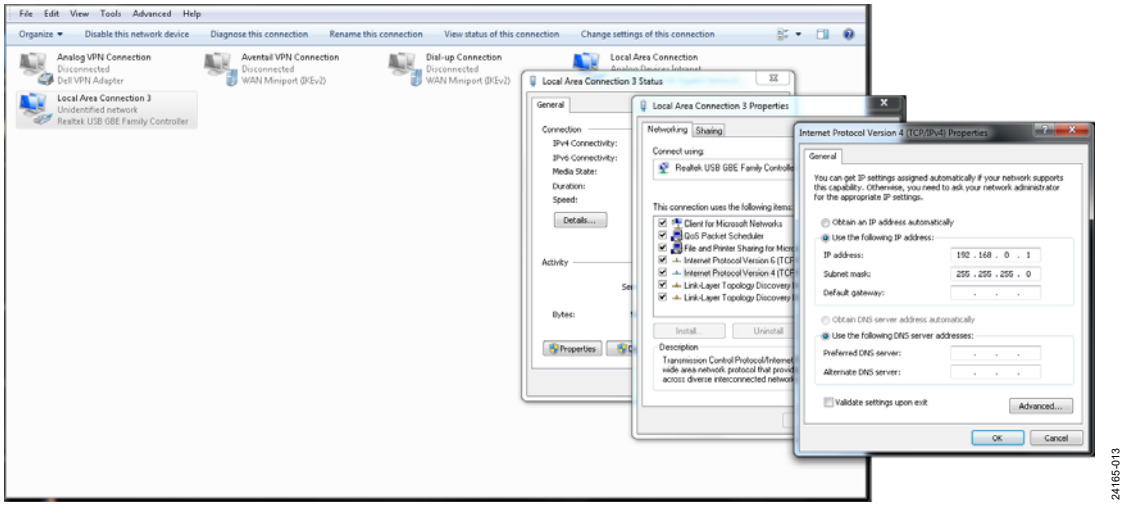


Figure 12. Internet Protocol Settings

EVALUATION BOARD HARDWARE SETUP

DETERMINE THE CLOCK SOURCE

Determine whether the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ evaluation board is set to the external clock or on-board HMC7044 clock by checking the C3D, C4D, C5D, and C6D capacitors on the board. By default, the HMC7044 clock is enabled (C3D and C5D are placed, and C4D and C6D are do not insert (DNI)). If using a direct external clock, the user can remove Capacitors C3D and C5D, and place Capacitors C4D and C6D. The capacitors are 0.1 µF, Size 0201 (imperial) or Size 0603 (metric).

DEFAULT CLOCKING SCHEME FOR AD9082-FMCA-EBZ/AD9081-FMCA-EBZ

The default clocking scheme for the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ evaluation board uses the on-chip PLL within the AD9081 or AD9082. The HMC7044 provides the reference input to the AD9081 or AD9082. The evaluation board provides all necessary clocks for conducting a quick evaluation of the device, including auxiliary clocks needed by the FPGA in the ADS9-V2EBZ board to set up the JESD204B or JESD204C link. The clocking scheme is shown in Figure 14.

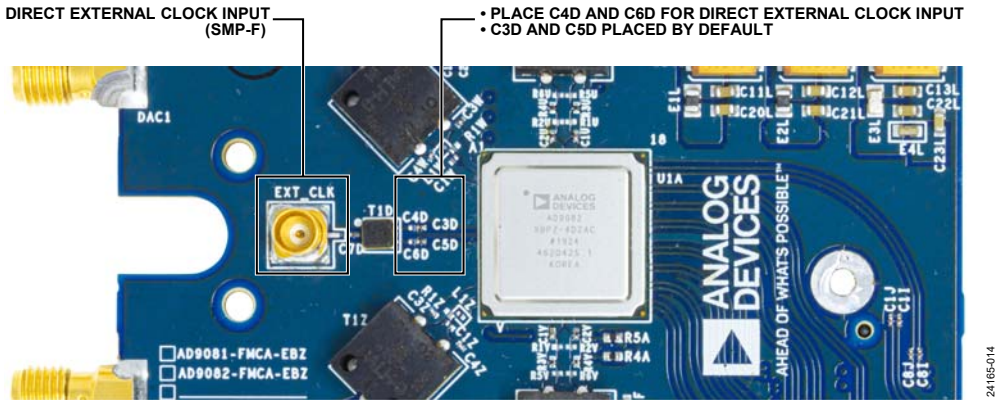


Figure 13. Capacitor Position for Direct External vs. On-Board HMC7044 Clocking

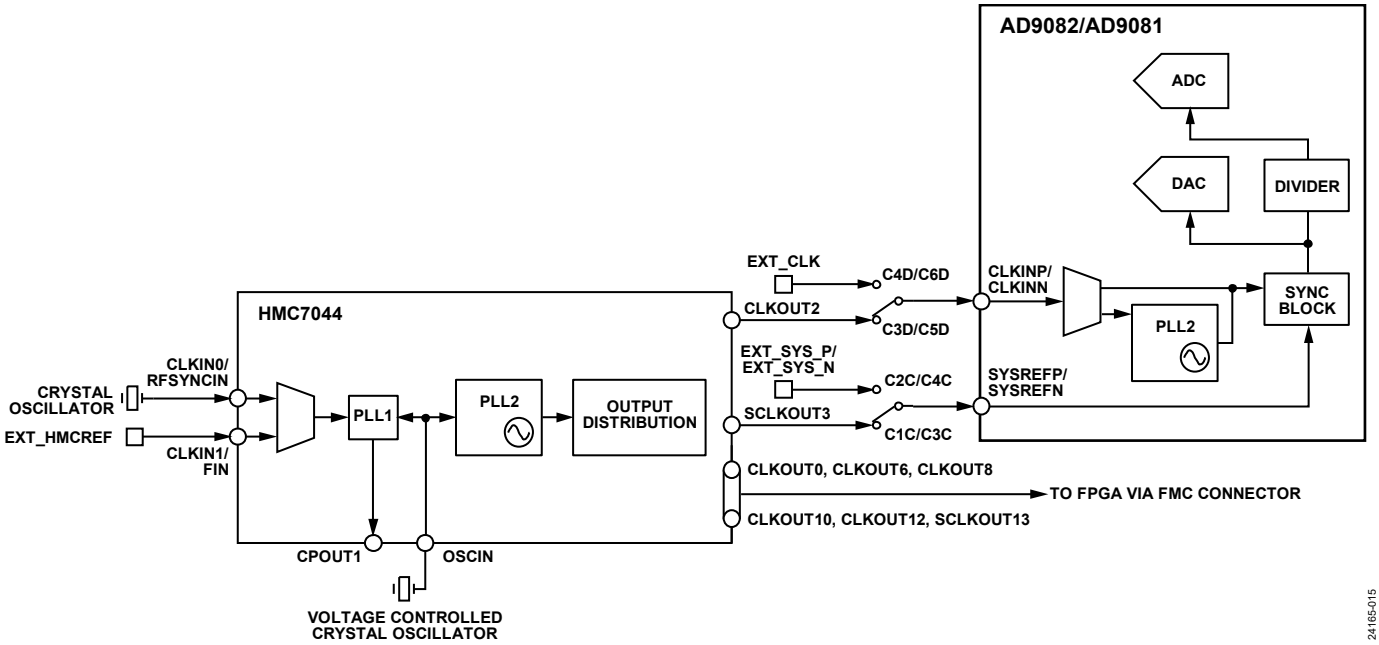


Figure 14. Default Clocking Scheme Used for AD9081-FMCA-EBZ or AD9082-FMCA-EBZ Evaluation Board

SET UP THE INSTRUMENTATION

To use on-board clocking, the user only needs to provide an analog input signal using a signal generator. To analyze digital-to-analog (DAC) outputs, a spectrum analyzer is needed.

The following are recommended instruments and connectors:

- Signal generator: a low phase noise signal generator such as the Rohde & Schwarz SMA (100A or 100B), Keysight UXG/EXG series
- Spectrum analyzer: Keysight PXA/UXA, or Rohde & Schwarz FSW/FSWP
- Cables: use a shielded, RG-58, 50 Ω coaxial cable

Ensure that the 10 MHz references are shared between the instruments.

Analog Devices recommends the coaxial, 48.0 in. (1.2 m or 4.0 ft), RG-316 DS, SMA to SMA, male to male cable assembly from Cinch Connectivity Solutions Johnson, Part Number 415-0033-048 for the setup.

Set Up the Spectrum Analyzer

Analog Devices recommends the following configuration for the spectrum analyzer:

- Start frequency = 50 MHz (or 0 MHz)
- Stop frequency = 5 GHz
- Resolution bandwidth = 30 kHz
- Use an average or rms detector setting, and set the input attenuation to 6 dB or as desired

These settings can be changed to satisfy the particular use case.

It is recommended to have all the instruments share a common reference. Usually, this common reference is achieved by connecting the 10 MHz reference output from one instrument to the reference input of the next, and so on.

USING THE AD9081 OR AD9082 BOARD VIEW

The board view allows the user to quickly set up the AD9081 or AD9082 to a predetermined use case for evaluation. The board view uses the on-board clocking solution to manage the clocks to the AD9081 or AD9082, as well as the FPGA. For more details on the clock setup, refer to Figure 14. Figure 16 shows the hardware connection needed when using the board view, with the AD9082-FMCA-EBZ board as an example.

USE CASES

The use cases in Table 2 are supported for JESD204B and JESD204C modes for the AD9081-FMCA-EBZ/AD9082-FMCA-EBZ board. Tx means transmit, and Rx means receive.

SETTING UP THE AD9081 OR AD9082 IN FULL BANDWIDTH MODE

Set up the evaluation board as explained in the Evaluation Board Hardware Setup section. Open the board view. This section uses the board in its default configuration with the HMC7044 clock enabled (C3D and C5D are placed, and C4D and C6D are DNI). See Figure 13 for more information.

In the **QUICK CONFIGURATION** pane, select the **DAC@6.0GHz, ADC@3.0GHz, JESD204B (Full Bandwidth)** from the **Select Use Case** pulldown box, and click **Apply**.

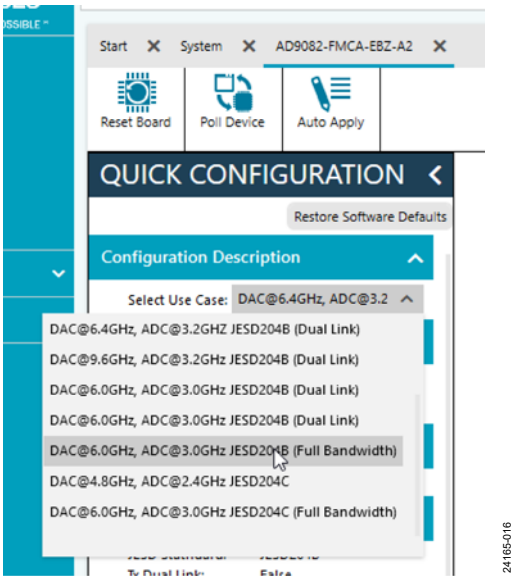


Figure 15. Selecting Full Bandwidth (JESD204B) Mode in the Board View

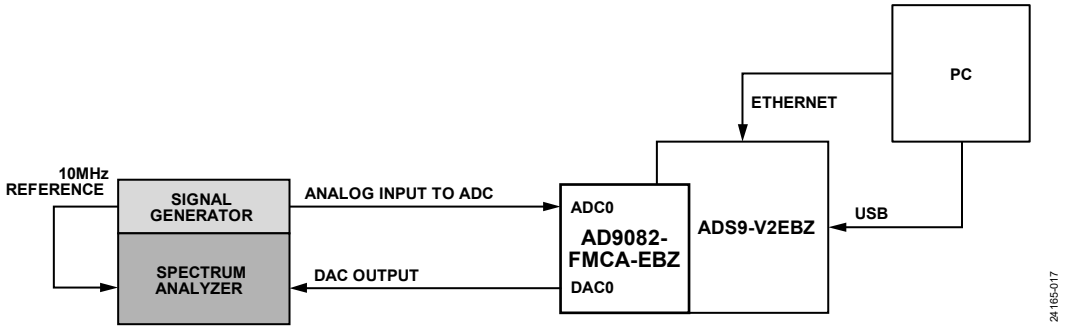


Figure 16. Hardware Setup for Using the Board Wizard (10 MHz Reference Connection)

Table 2. Use Cases: Evaluation Boards with 100 MHz On-Board Crystal Oscillator (AD9081-FMCA-EBZ/AD9082-FMCA-EBZ)

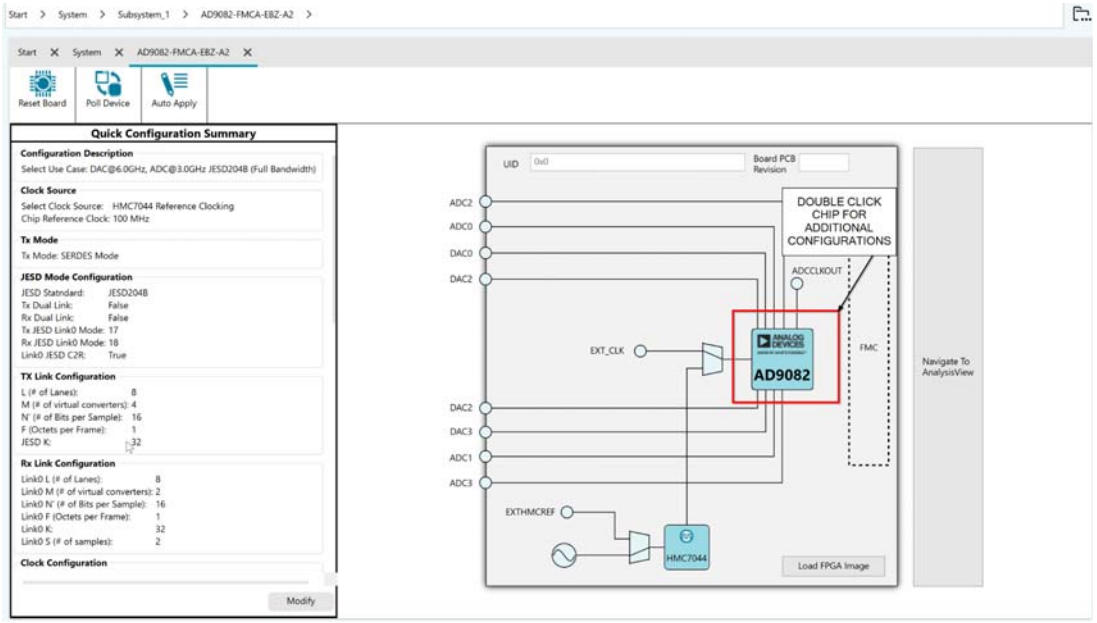
Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Tx Link	Rx Link	JESD204x Protocol
Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine							
4.8	2.4	9B	10B	4	4	2	4	300	4	300	4	Single	Single	JESD204B
7.2	2.4	16B	10B	6	4	2	4	300	4	300	8	Single	Single	JESD204B
6.4	3.2	10B	7B	4	4	2	4	400	2	400	4	Single	Dual	JESD204B
9.6	3.2	10B	7B	6	4	2	4	400	2	400	2	Single	Dual	JESD204B
6	3	17B	11B	4	1	4	1	1500	2	750	2	Single	Dual	JESD204B
6	3	62B	11B	4	1	4	1	1500	3	750	2	Dual	Dual	JESD204B
6	3	17B	18B	4	1	1	1	1500	1	3000	1	Single	Single	JESD204B
4.8	2.4	15C	16C	8	1	4	1	600	4	600	4	Single	Single	JESD204C
6	3	17C	18C	4	1	1	1	1500	2	3000	2	Single	Single	JESD204C

[1] B means JESD204B, and C means JESD204C. For more information about the JESD204x modes, refer to the UG-1578, *System Development User Guide for the AD9081 and AD9082 Direct RF Sampling Transceivers*.

After clicking **Apply**, the **Quick Configuration Summary** pane displays. Double click the **AD9081** or **AD9082** chip for further analysis. Figure 17 shows the **AD9082** chip as an example.

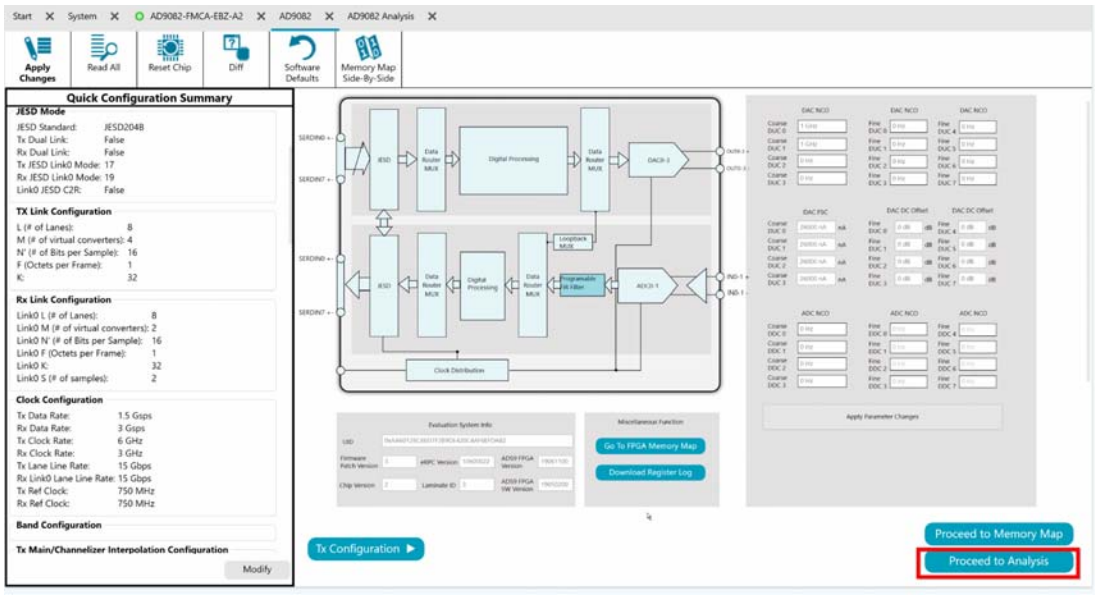
A block diagram that allows transmitter, receiver, and programmable filter configurations loads, as shown in Figure 18.

Click **Proceed to Analysis**. See the Using ACE and DPGDownloaderLite for Analysis and DAC Output Setup section for additional information.



24165-018

Figure 17. Navigating to Chip View for Additional Controls



24165-019

Figure 18. Additional Controls Including Analysis Features

USING ACE AND DPGDOWNLOADERLITE FOR ANALYSIS AND DAC OUTPUT SETUP

This section explains how to use ACE for analysis of ADC data, and DPGDownloaderLite for sending waveforms out the DAC channels. Regardless of whether the board view or the chip view is used, the same procedure applies to using ACE and the DPGDownloaderLite software.

CAPTURE AND ANALYSIS OF ADC DATA

After setting up the AD9081 or AD9082 using the **QUICK CONFIGURATION** pane in the board view, open the ADC data analysis window by clicking the **Proceed to Analysis** button in the **AD9081** or **AD9082** chip view. Set up a signal generator with a single-tone sinusoid at 1.81 GHz and ~6.5 dBm output power. Supply this signal to the ADC0 input. Select the **Waveform** and **FFT** boxes on the left pane, and then click **Run Once** to run the FFT analysis. A graph displays, together with details of the analysis.

DAC WAVEFORM GENERATION USING DPGDOWNLOADERLITE SOFTWARE

To generate a waveform using the DPGDownloaderLite software, open DPGDownloaderLite (**Start** > **All Programs** > **Analog Devices** > **DPGDownloaderLite**), and ensure the evaluation board is displaying the product number matching the hardware used. Ensure **AD9081** or **AD9082** is selected under **Eval Board** (**AD9082** is shown in Figure 20).

Next, select **Single Tone** from **Add Generated Waveform** (see Figure 20).

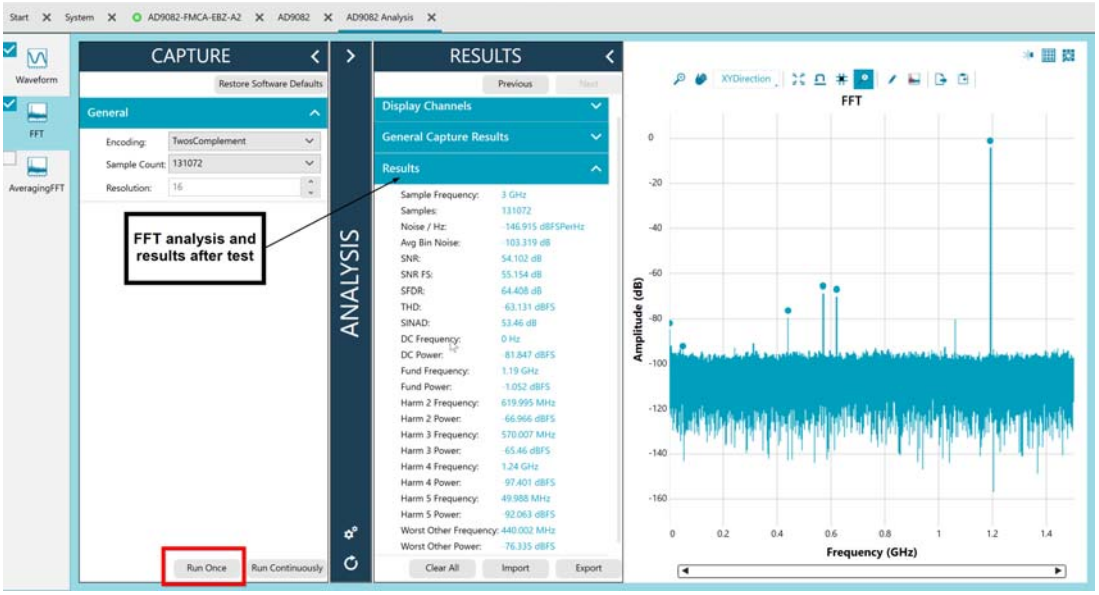


Figure 19. FFT Analysis Window Showing a 1.81 GHz Tone Sampled at 3 GSPS

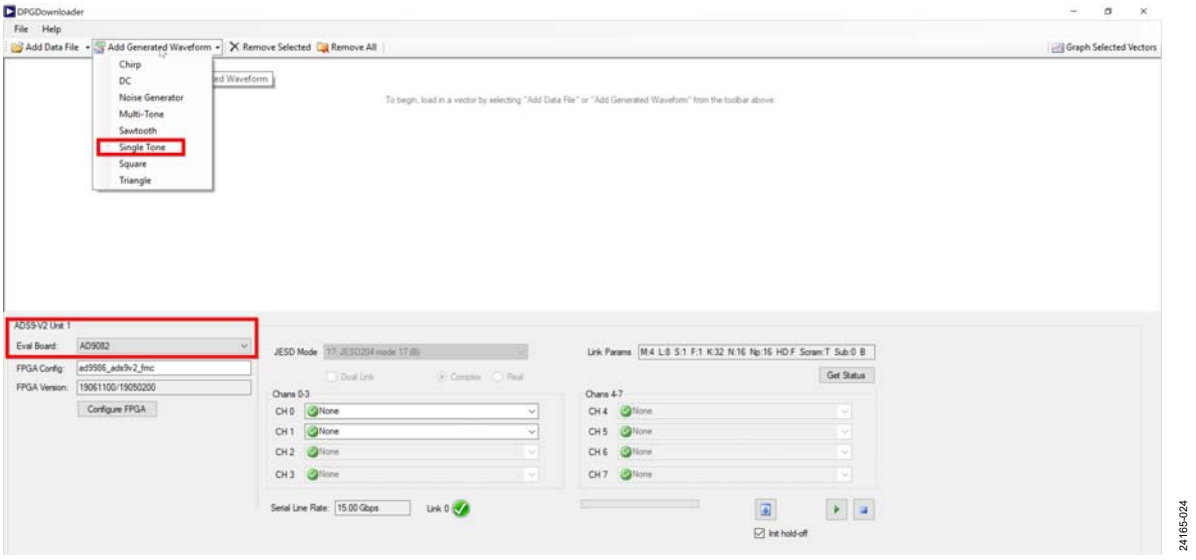


Figure 20. Single-Tone Generation

Then, in the DPGDownloaderLite software, follow these steps:

1. At the top of the window, enter or verify the following data values, as shown in Figure 22:
   a. **Data Rate**: this must match the selected **Tx Data Rate** field under the **Clock Configuration** section in ACE, as shown in Figure 18.
   b. **DAC Resolution**: 16 bits.
   c. **Record Length**: 16384.
   d. **Offset**: 0.
   e. **Desired Frequency**: 10 MHz.
   f. **Amplitude**: 0.0 dB.
   g. **Relative Phase**: 0 degrees.
   h. **Unsigned Data**: cleared.
   i. **Allow even cycle count**: cleared.
   j. **Generate Complex Data (I & Q)**: selected.
2. Select the channels. In Figure 22, two channels are selected.
   a. **CH 0** dropdown box: **Single Tone - 10.025 MHz; 0.0 dB; 0.0°(C)**
   b. **CH 1** dropdown box: **Single Tone - 10.025 MHz; 0.0 dB; 0.0°(C)**.
3. Click the **Download** button.
4. Click **Play** to display the waveform on the spectrum analyzer.

Connect the DAC0 or DAC1 output to a spectrum analyzer. A 1.85 GHz single tone appears on the spectrum analyzer as shown in Figure 21.

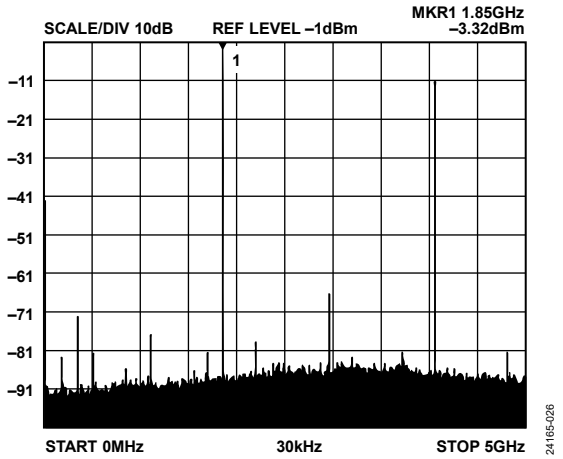


Figure 21. Spectrum Analyzer Plot Showing Single Tone at 1.85 GHz

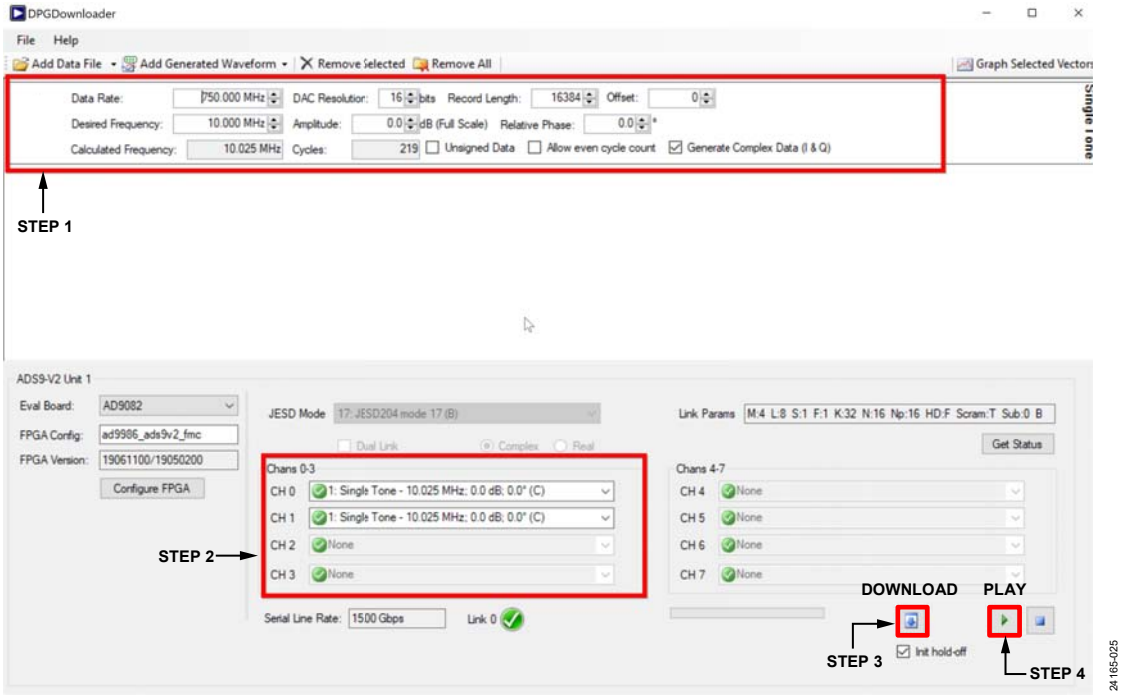


Figure 22. Downloading the Single-Tone Signal to the DAC

USING THE AD9081 OR AD9082 CHIP VIEW

The chip view enables the user to customize the AD9081 or AD9082 beyond the functions available in the board view. Use the chip view if using a direct external clock. The chip view provides a more customizable user interface (UI) that directs the user through the various aspects of the device setup. For optimal use of the chip view, provide a direct external clock to the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ. Refer to Figure 13 for information on how to modify the board for a direct external clock. When using direct external clock mode, the user must provide the device clock as well as the FPGA reference clock.

SETTING UP THE AD9081 OR AD9082 IN FULL BANDWIDTH MODE WITH EXTERNAL CLOCKING

To set up the AD9081 or AD9082 in full bandwidth mode with external clocking, follow these steps:

1. Set up the evaluation board hardware and instrumentation as shown in Figure 24.
2. Set the clock signal generator to 6 GHz, with an amplitude set to 5 dBm. Provide this signal to J6 of the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ evaluation board.
3. Set the reference clock signal generator to 750 MHz with an amplitude set to 5 dBm. Provide this signal to the J1 EXT CLK connector of the ADS9-V2EBZ.
4. Set the analog input signal generator to 1.81 GHz with an amplitude set to ~6.5 dBm. Turn the signal generator output off for this setup.
5. Open the chip view. In the **QUICK CONFIGURATION** pane, select the clock source to be **External Direct Clocking (J6)**, as shown in Figure 23.

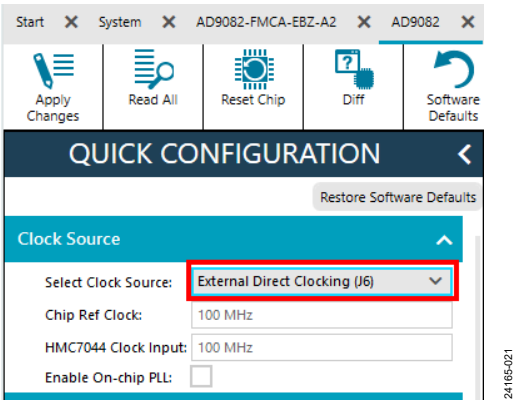


Figure 23. Selecting the Clock Source in Chip View

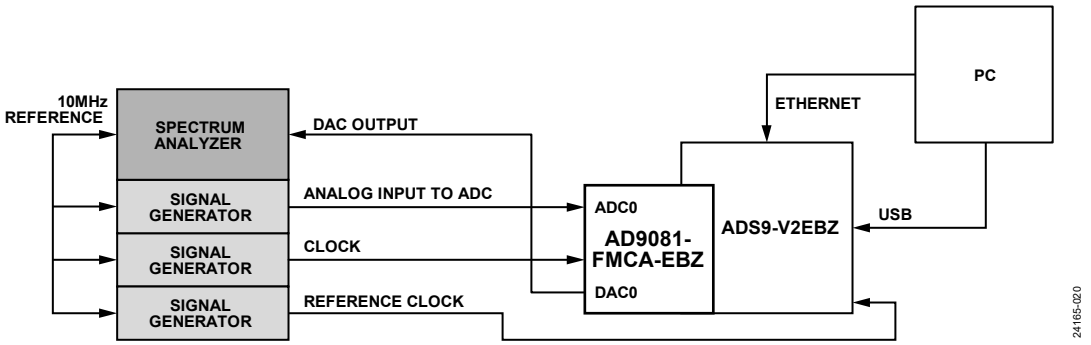


Figure 24. Hardware Setup for Using the Chip View (10 MHz Reference Connection)

6. Select the options for the other sections (**TX Link Configuration**, **Rx Link Configuration**, and **Clock Configuration**) in the **QUICK CONFIGURATION** pane as shown in Figure 25.
7. Click **Apply** to open the **Quick Configuration Summary** pane.
8. Click the **Proceed to Analysis** button for further analysis.

See the Using ACE and DPGDownloaderLite for Analysis and DAC Output Setup section for more information.

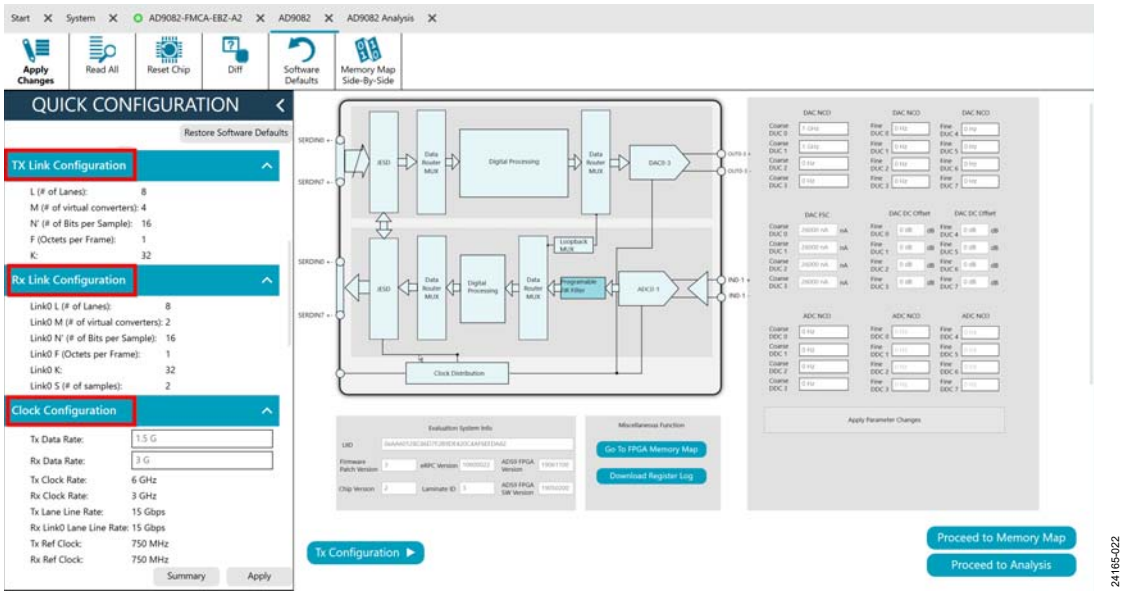


Figure 25. Configuring the AD9081 or AD9082 for Full Bandwidth Mode Using Chip View and Direct External Clock

ADDITIONAL FEATURES

USING THE AD-FMC-SDCARD

This section explains how to use the supplied microSD card, AD-FMC-SDCARD, to evaluate the AD9081 or AD9082 using FPGA development boards from Intel or Xilinx.

The AD-FMC-SDCARD is a microSD Card and SD card adapter (to use the microSD card in an SD card slot), preformatted with an Analog Devices supported Linux image on it, which can be used for development and prototyping with the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ evaluation board on Xilinx Zynq®, Zynq UltraScale+™, and Intel system on a chip (SoC) platforms. The AD-FMC-SDCARD uses a publicly facing hardware description language (HDL) and software reference design to enable the use of this hardware setup for algorithmic prototyping and development. For more information, visit wiki.analog.com/ad-fmc-sdcard. For questions about the contents on this disk, ask on the Analog Devices EngineerZone at ez.analog.com/fpga for HDL questions or ez.analog.com/linux-software-drivers for software questions.

ADDITIONAL USE CASES AND CUSTOMIZATION

The ACE plugin for the AD9081 or AD9082 supports additional use cases and some level of customization. Because the AD9081 or AD9082 are highly configurable devices, not all these modes are described in this user guide. Additional use cases and features are described in wiki.analog.com/resources/eval/ad9082.