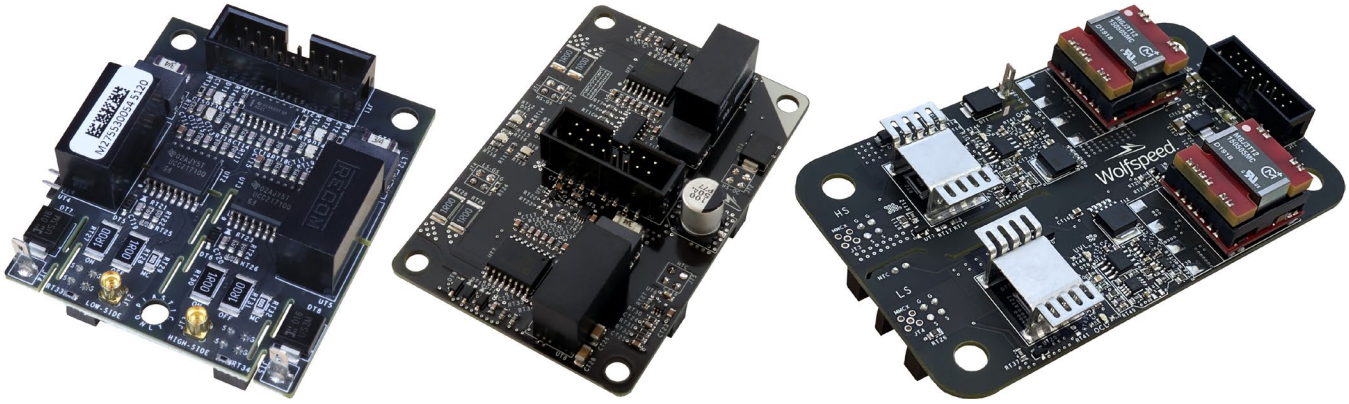
Application Note **PRD-09301**

Gate Driver Design for SiC Power Modules



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Transitioning from silicon (Si) to silicon carbide (SiC) semiconductors can yield substantial system-level efficiency and power density improvements. While the straightforward replacement of legacy power modules with SiC-based modules can provide immediate benefits, a SiC-optimized gate driver design can facilitate additional performance enhancements. Many principles for developing gate drivers in SiC-based systems align closely with those used in Si-based systems. However, any deficiencies in the gate driver design are exacerbated in demanding SiC-based applications, which may necessitate a reduction in system ratings. This document outlines best practices for gate driver design and provides design examples to achieve high performance when utilizing SiC power modules.

Contents

1. Introduction

Silicon carbide (SiC) power modules can modulate high voltages and currents with fast edge rates, enabling significant system-level power efficiency and density improvements compared to silicon (Si) devices. In contrast to logic-level semiconductors used in many embedded applications, power semiconductors require a high-performance circuit, referred to as a gate driver, to reliably and safely operate the power semiconductor at elevated currents and voltages. This section details some of the requirements of a gate driver for power modules.

1.1 Kelvin-Source Connection

Figure 1(a) shows a notional three-terminal MOSFET with the terminals labeled by their functionality: drain (D), gate (G), and source (S). To turn-on the MOSFET, the gate voltage must exceed the intrinsic threshold voltage of the MOSFET, with respect to the source terminal of the device. Specifically, the gate-to-source voltage (V_{GS}) must be greater than the MOSFET threshold voltage, V_{TH}. Therefore, to bias the gate properly, the gate driver must be referenced to the source terminal of the device, as shown in Figure 1(b). In this configuration, the output of the gate driver is referenced to the same potential as the MOSFET, enabling the gate driver to control the on and off states of the MOSFET.

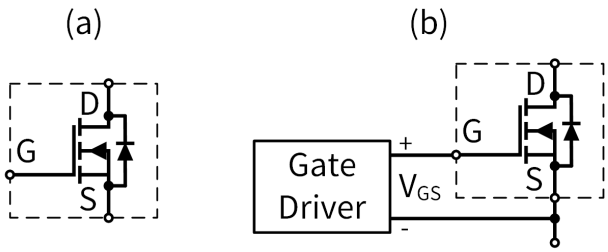


Figure 1: (a) Notional three-terminal MOSFET and (b) associated gate driver connections

In a physical system, internal packaging connections result in parasitic inductances between the semiconductor die and the power module terminals. These inductances are minimized through diligent design and manufacturing but are still present in all power semiconductor packaging for both Si and SiC devices. Since gate drivers are referenced to the MOSFET source terminal, the source terminal inductance appears in both the gate and power loops of the device, as shown in Figure 2(a). This inductance, referred to as common-source inductance, can introduce significant coupling between the gate and power loops which can influence switching dynamics and make the MOSFET more susceptible to false turn-on events. Though this inductance is typically small, it can still have a large impact on the switching dynamics. A common approach to eliminate its influence is to add a dedicated Kelvin connection directly to the MOSFET die, which is used for the gate driver reference. This connection bypasses the source inductance and decouples the gate and power loops from each other as shown in Figure 2(b). The Kelvin-source in Wolfspeed power modules is connected directly to the die, minimizing the inductance that is present in both the power and gate loops, as shown in Figure 2(c). Notably, this connection is referred to as the Kelvin-source pin since it provides a low-current (in comparison to the power loop) connection directly to the MOSFET source terminal. In this document, this pin will be referred to as the Kelvin-source pin or KS pin. However, often in literature, this pin is abbreviated to the Kelvin pin (K) or the source pin (S). In these cases, it is important to ensure the pin has the expected Kelvin-source functionality.

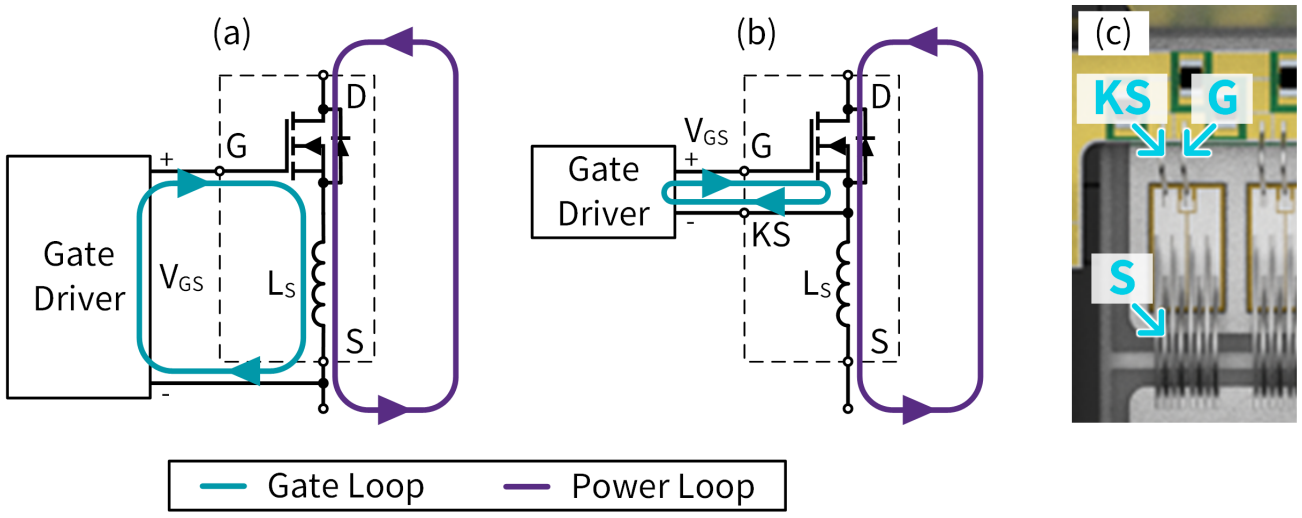


Figure 2: (a) Three-terminal MOSFET with shared inductance, (b) four-terminal MOSFET with Kelvin-source, and (c) example power module wirebonds with dedicated Kelvin-source connection

Most Wolfspeed power modules include a dedicated true Kelvin-source connection for each switch position to ensure the module achieves high-performance switching dynamics. For example, Figure 3 shows the pinout of the Wolfspeed CCB021M12FM3T baseplate-less six-pack power module, taken from the module datasheet. Even though the module has six MOSFETs, each switch position has a dedicated Kelvin-source connection for attaching a gate driver. Notably, this pinout diagram abbreviates the Kelvin-source connection as simply *Sx* where *x* is the switch position number. From the context of the circuit diagram, the locations of the *Sx* identifiers indicate that these terminals function as Kelvin-source, despite the abbreviated nomenclature.

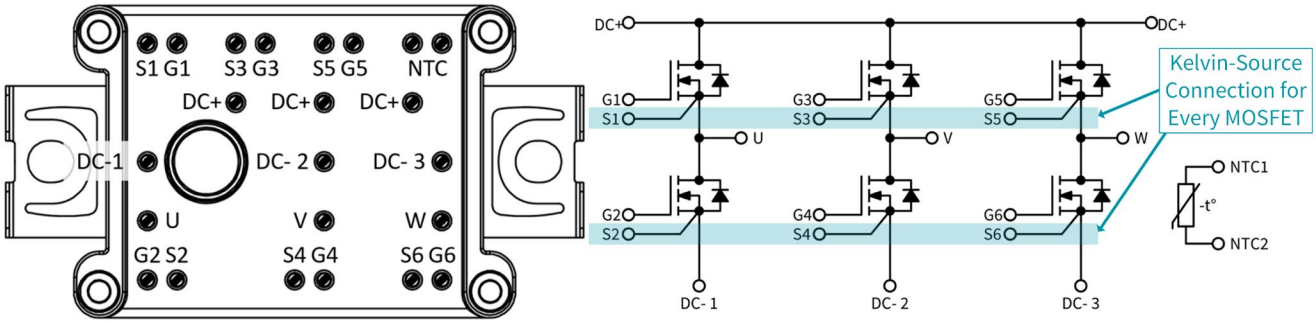


Figure 3: Wolfspeed CCB021M12FM3T baseplate-less six-pack power module pinout

The circuit diagram does not directly show the source inductance since it is a small parasitic element of the circuit. Despite the *Sx* terminals appearing to be directly connected in the schematic to the *U*, *V*, *W*, and *DC-* pins, respectively, it is important to recognize that the circuit still includes some minimal source inductance. For this reason, the *Sx* pins of the module should remain disconnected from the associated power loop pin when the power module is attached to the circuit. For example, in the first half-bridge, *S1* should not be connected in circuit to *U*, and *S2* should not be connected in circuit to *DC-1*. Directly connecting these terminals in the layout can reintroduce some of the issues of common-source inductance and can cause a reduction in device lifetime due to the internal Kelvin-source wire bonds not being sized to handle elevated power loop currents.

1.2 Isolation Requirement

A fundamental building block of power electronics is the half-bridge circuit, notionally shown in Figure 4(a). In the half-bridge circuit, the source terminal of the high-side MOSFET is connected to the drain terminal of the low-side MOSFET, forming the mid-point of the half-bridge. This mid-point voltage, V_{MID}, can vary drastically as the high-side and low-side devices alternate turning on and off, as shown in Figure 4(b). This fluctuation – often changing tens of thousands of times per second – generally alternates between several hundreds of volts. To properly bias the high-side switch position, the associated gate driver must be referenced to the source of the device, meaning the gate driver reference is also fluctuating between large voltages. Without proper isolation, the high-voltage present on the gate driver circuit can cause noise issues on the low-voltage controller, cause catastrophic failure, and/or create a significant safety risk. To prevent these issues, it is essential that a gate driver circuit offers suitable isolation to operate at the intended voltages.

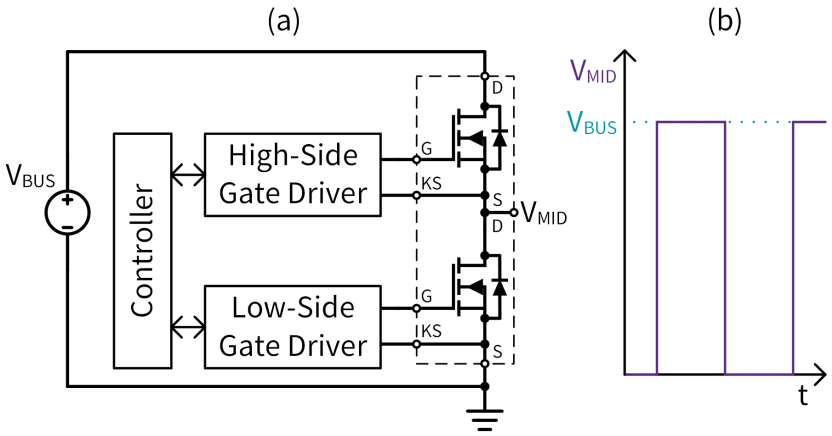


Figure 4: (a) Half-bridge gate driver locations, and (b) notional mid-point voltage

Though the low-side gate driver does not fluctuate at a high potential as in the Figure 4 example, the low-side gate driver also requires suitable isolation. Wolfspeed recommends using an isolated gate driver for all power module switch positions. The reasons for this isolation requirement include:

Improve System Safety. In case of a failure in the power stage, the isolation protects the low-voltage circuitry and operators from the dangerous voltages. Depending on the application, this isolation may be required to pass various regulatory requirements.

Remove Noise Paths. Without the isolation barrier, fast edge rate (*dV/dt* and *di/dt*) noise can directly couple from the power stage to the controller, causing sporadic or catastrophic failures. This noise can be reduced drastically through the addition of an isolation barrier.

Remove Ground Loops. Isolation eliminates direct ground loops in the system by decoupling the reference of the low-voltage control circuitry from the reference of the high-voltage power circuitry. This prevents uncontrolled transient currents from flowing from the power stage.

Modular Design. Isolation enables the same gate driver circuit to be used in all switch positions. Other topologies besides half-bridge circuits (such as neutral-point clamped inverters) have the low-side switch position referenced to fluctuating voltages.

1.3 Ampacity Requirement

During the manufacturing process of all power semiconductors, stray capacitance is introduced, which can influence circuit operation. Figure 5 shows the typical influential parasitic capacitances in a standard MOSFET. These capacitances can vary significantly in size and are generally voltage dependent. For the semiconductor to function as intended, a gate driver must have a sufficient peak ampacity rating to quickly charge and discharge these capacitances. Power modules, which feature multiple MOSFETs in parallel and therefore sum the capacitances, require even higher peak ampacity to quickly charge and discharge these capacitances.

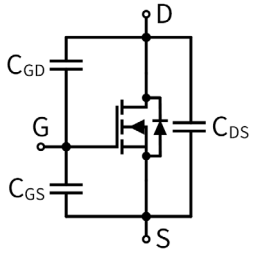


Figure 5: Simple MOSFET model including influential parasitic capacitances

The gate peak ampacity requirements of power modules can be easily observed in a clamped inductive load (CIL) simulation. To recreate this simulation, template simulations and power module models for all Wolfspeed power modules are available for download here. Many of the Wolfspeed power module models are also included directly in the Analog Devices® LTspice® simulation software. Figure 6(a) shows an example CIL simulation circuit in LTspice (template file *DPT_Test_Stand_HB.asc*) using the Wolfspeed CAB006M12GM3 baseplate-less half-bridge power module. For more information about the clamped inductive load test, see PRD-08333. The simulation was configured with a gate resistance of 1 Ω, bus voltage of 800 V, and a source current of 200 A. The power source and gate currents were monitored during the simulation, and the results are shown in Figure 6(b). In this simple example, the gate current reaches a peak current of approximately 6 A during transient events. It is essential that the gate driver can support these current transients to achieve high-performance operation of the power module. Notably, the peak currents are observed in both turn-on and turn-off events, so the gate driver must be able to both sink and source the required current.

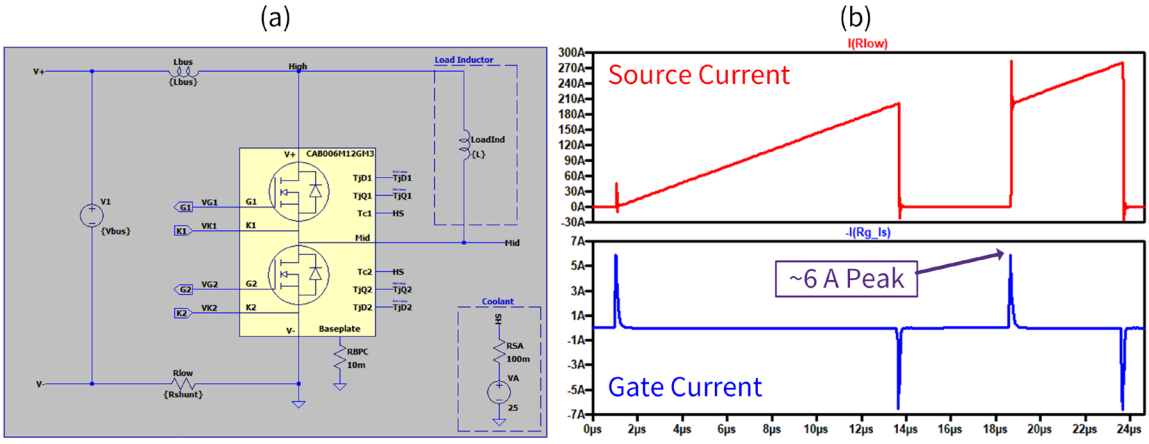


Figure 6: (a) Example CIL simulation schematic of CAB006M12GM3 module and (b) simulated currents

1.4 Low-Inductance Requirement

The physical connection between the gate driver and the SiC MOSFET will introduce some parasitic inductance into the system. This inductance, L_G, can introduce delay into the system and can cause the gate signals to violate safe operating bounds due to excessive overshoots or ringing. Though parasitic inductance is not as impactful in the gate loop as it is in the power loop (where it is critical to high performance operation), it is still important to limit its inductance by adopting best-practice component placement and routing.

To demonstrate the influence of parasitic gate inductance, Figure 7 shows the results of the Figure 6(a) simulation with varying gate inductance. The results demonstrate the sensitivity of gate inductance on the gate-to-source voltage (V_{GS}), drain-to-source voltage (V_{DS}), and drain current (I_D). Several trends are observed in the results. First, the drain-to-source voltage and drain current are delayed as the gate inductance is increased, with respect to the start of the gate voltage transition. This can cause issues when implementing fast control loops or parallelling modules, and it could require increasing system deadtime to avoid shoot-through conditions. Furthermore, this influence can delay any short-circuit protection since this same delay would be present when shutting the system down after detecting a fault. Second, gate inductance limits the peak gate current supplied by the gate driver IC and decoupling capacitors (see Section 2.6) which slows the device transients and increases switching energy. This influence is observed in the gate current waveforms of Figure 7. Third, the gate-to-source oscillations are exacerbated with higher gate inductances. The ringing peaks are greater and oscillate longer, potentially leading to reduced device lifetime. Notably, the gate inductance does not have a significant impact until higher inductance values are observed, so power loop inductance should always be prioritized over gate loop inductance. Additionally, gate drivers are often connected to the power stage through a connector. The connector itself often dominates the overall inductance of the gate driver, so it is important to keep the inductance of the board low since the connector will add significant additional inductance.

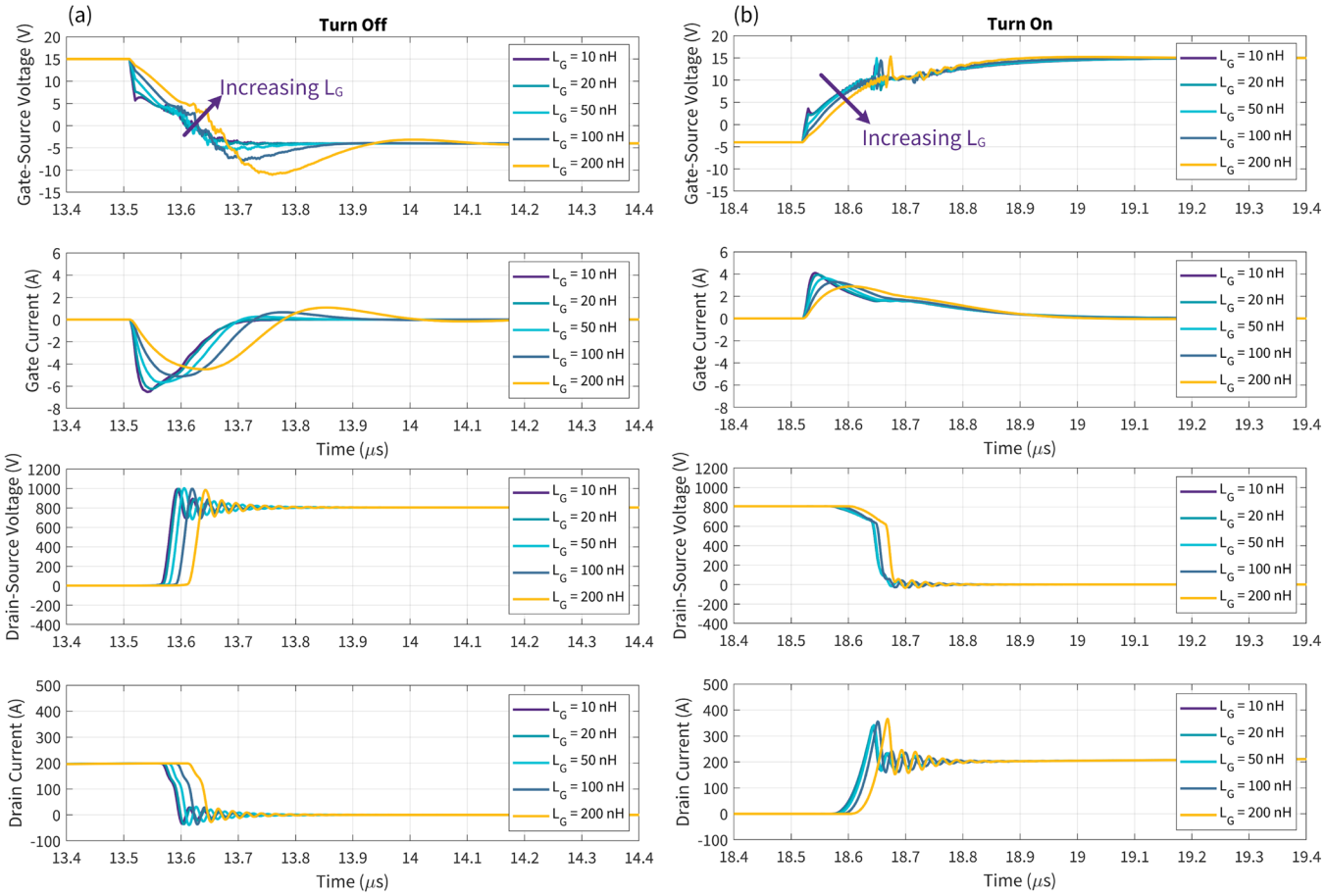


Figure 7: Simulated gate inductance sensitivity during (a) turn off and (b) turn on

2. Gate Driver Layout Guidance

SiC MOSFET circuit board layout requirements are fundamentally the same as layout needs for Si-based semiconductors. However, the fast edge rates of SiC-based devices exacerbate any mistakes in circuit layout. To achieve the full performance of SiC power modules, the gate driver layout should follow the guidelines and recommendations detailed in this section.

2.1 Isolation Barrier

Gate drivers serve as the connection between low-voltage control circuitry and high voltages/currents of the power stage. The gate driver must first and foremost decouple the power circuitry from the logic-level control circuitry to prevent dangerous potential from coupling to the control circuitry or operator. To achieve this, the gate driver must include an isolation barrier, which introduces a galvanic barrier between the control and power sides of the gate driver. Often, gate driver integrated circuits (ICs) include an integrated isolation barrier, rather than requiring an additional chip to provide the protection. This barrier separates the low-voltage signals of gate driver inputs from the high-potential signals on the power side of the gate driver. Figure 8 shows a notional gate driver IC, which separates the two types of circuits on the left and right side of the chip.

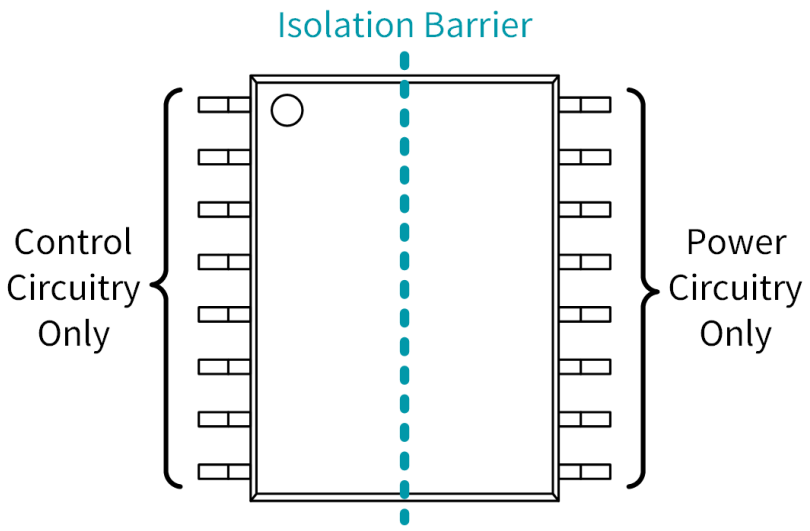


Figure 8: Isolation barrier of a notional gate driver IC

It is important that the IC used for the gate driver has an isolation voltage greater than the voltage of the circuit. The isolation ratings are typically provided by the device manufacturers, along with any applicable isolation safety certifications or testing procedures. Any component that crosses the isolation barrier of a gate driver circuit must also have a suitable isolation rating for the target operating voltages. This requirement applies to the gate driver IC, the isolated power supply (Section 2.4), and any other devices that bridge the isolation barrier. Notably, this isolation barrier cannot be crossed by copper since this would result in a system with no isolation. For example, having a ground pour traverse from the low-voltage side to the high-voltage side would defeat the isolation, introduce noise, and potentially damage the controller. Incorrect and correct layout implementations when considering isolation are notionally demonstrated in Figure 9.

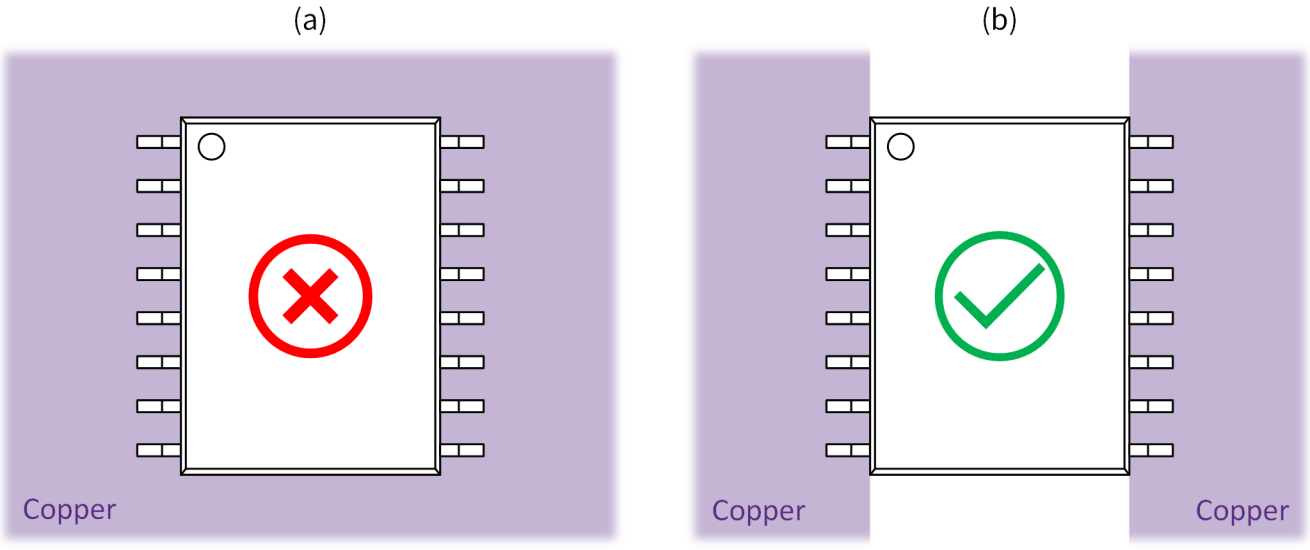


Figure 9: (a) Incorrect layout where copper violates isolation barrier, and (b) correct layout with no violation

Since the high-side and low-side switch positions are referenced to different voltage potentials, it is also critical that suitable isolation exists between the two switch positions of a half-bridge. In most cases, no components need to bridge the barrier between the high-side and low-side switch positions; however, it is still critical that no copper coupling paths exist between them. Otherwise, the high *dV/dt* of switching events can couple into the other position and cause unintended turn-on events. This isolation barrier can often be smaller than the gate driver IC barrier (functional vs basic/reinforced creepage distance) since a failure of the high-side/low-side isolation barrier does not affect a system element that may be controlled by a user.

Figure 10 shows an example of isolation barriers implemented on the CGD1700HB2M-UNA gate driver designed by Wolfspeed. The CGD1700HB2M-UNA is intended to drive a half-bridge power module, so it includes a separate gate driver circuit for the high-side and low-side switch positions. The figure shows all the copper of the various circuit board layers, including all the internal layers. Despite the board using multiple layers, the design follows isolation requirements by ensuring no copper bridges across the isolation barriers of the design. This clearly divides the entire circuit into the control and power circuitry sides. The design also features board cutouts in the isolation regions for improved creepage distance (see Section 2.7). The CGD1700HB2M-UNA gate driver is intended for system commissioning and early design-in work. For designs requiring large volumes, Wolfspeed partners with several gate driver manufacturers to develop solutions which adhere to suitable compliance standards and can support high-volume production. The full list of SiC-optimized gate drivers for Wolfspeed parts is found here and more information about the various isolation implementations is provided in Section 4.5.

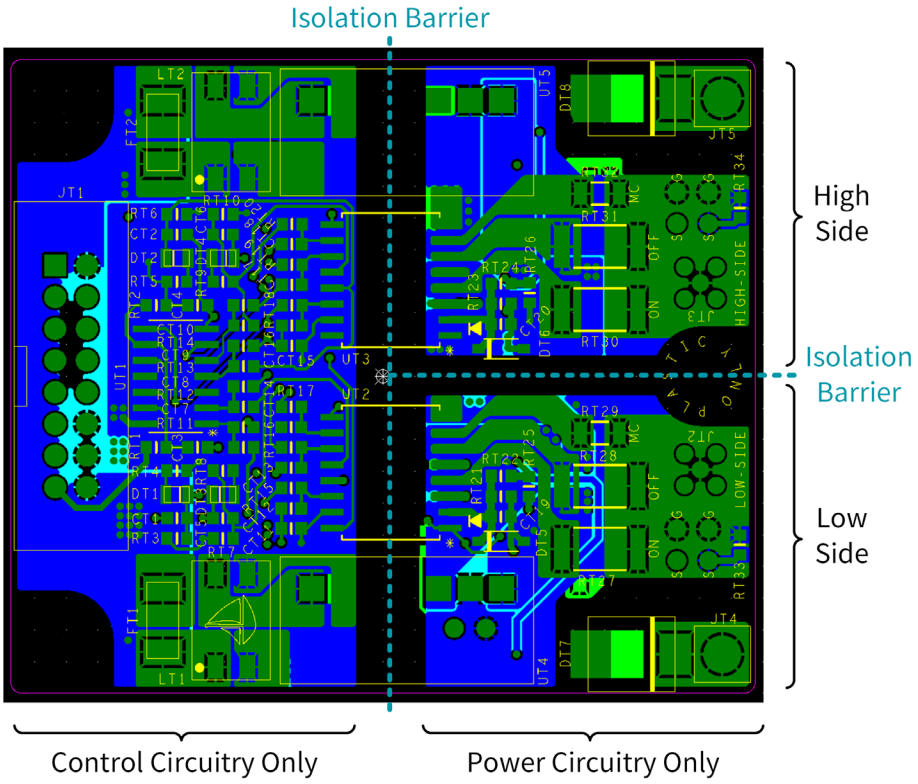


Figure 10: Wolfspeed CGD1700HB2M-UNA isolation barriers

2.2 Adjacent Gate and Kelvin-Source Layers

High gate inductance can introduce overshoot and ringing into the gate, which can lead to exceeding maximum and minimum ratings or cause inadvertent turn-on events (see Figure 7). Many designers already recognize the significance of low-inductance requirements in the power loop to limit overshoots; special care must also be taken to reduce the inductance of a gate driver. Though the power loop should always take priority over the gate loop since its impact is more influential, it is still important to reduce the inductance of the gate loop. The most important method for reducing gate loop inductance is for the gate and Kelvin-source connections to be on adjacent layers of the printed circuit board (PCB). Rather than routing the signals on the same PCB layer, one copper polygon (also commonly referred to as a "pour") should be directly below the other polygon. These connections should be implemented with wide polygons/pours instead of simple PCB traces to reduce gate loop inductance, gate loop resistance, and signal delay. Additionally, as will be discussed in Section 2.3, the Kelvin-source connection should always be used to "shield" the gate signal from any other circuitry on the board. Adjacent layers create magnetic flux cancellation between the gate and Kelvin-source which significantly reduces the gate loop inductance. This flux cancellation is demonstrated in Figure 11, and it is the most influential aspect of gate inductance and should be prioritized over other inductance reduction techniques.

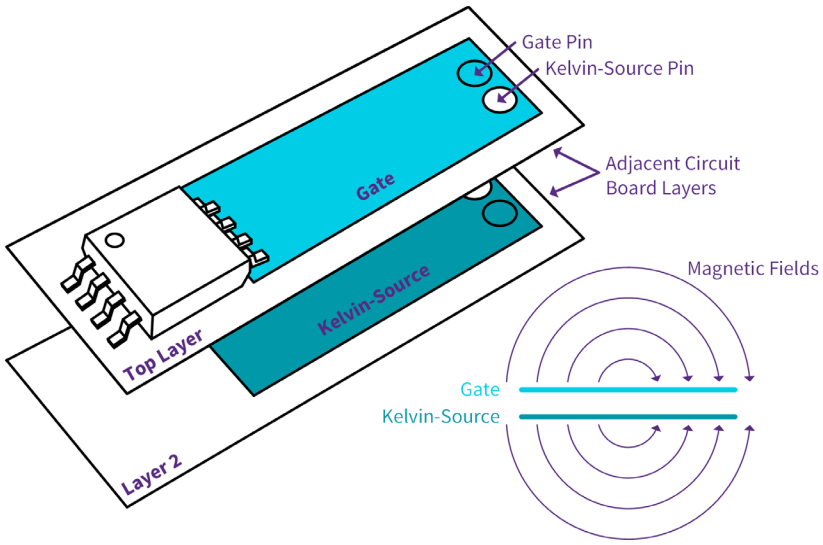


Figure 11: Adjacent gate and Kelvin-source PCB layers reduce gate inductance through flux cancellation

2.3 Kelvin-Source Shield

When implementing the adjacent gate and Kelvin-source layers as described in Section 2.2, Wolfspeed recommends that the Kelvin-source layer is between the gate layer and any circuitry on other layers. For example, Figure 12 shows an example multi-layer PCB stack-up in a section of the board where the gate signal must be routed over the DC+ and DC- nets on the circuit board. In this example, the Kelvin-source of the gate driver (Layer 2) is between the gate signal (Top Layer) and the other circuitry (Layers 3 through Bottom Layer). The adjacent layers improve the gate loop inductance whereas the shielding reduces the noise introduced into the gate signal. For further reference, the CRD25DA12N-FMC three-phase inverter design demonstrates adopting the Kelvin-source as a shield layer.

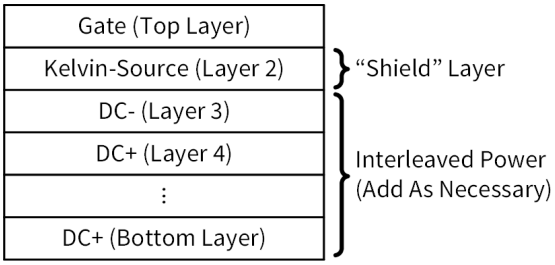


Figure 12: Example stack-up using Kelvin-Source as a "shield" layer

2.4 Isolated Power Supply

There are two isolation types on a typical gate driver: signal isolation and power isolation. Most of this document focuses on the gate driver IC and its surrounding circuitry, since power isolation can typically be achieved with a single standalone unit. This section provides some details about the power isolation requirements. Signal isolation is typically integrated into the gate driver IC itself or through a dedicated digital isolator (see Section 4.5) for routing pulse control and feedback signals. However, signal isolators are not generally capable of sourcing enough power to modulate a power module. To source the required power, gate drivers also require an isolated power supply unit (PSU). In contrast to signal isolation which can be achieved capacitively, magnetically, or optically, power isolation is typically implemented using an isolation transformer, since the other isolation methods generally cannot achieve the target power output requirements for driving SiC semiconductors.

For power module reference designs and gate drivers, Wolfspeed typically adopts PSUs with integrated split power rail outputs to generate separate positive and negative output voltages (see Section 3.5). These PSUs already feature an isolation barrier and are available from multiple manufacturers with the required output voltages to drive Wolfspeed power modules. These units typically only require adding input and output capacitance and/or output voltage adjustment resistors. The PSUs adopted on the CGD1700HB2M-UNA gate driver are shown in Figure 13. Notably, these PSUs do not always have tight regulation of the output voltage. If the output regulation is unsuitable for an application, a low dropout (LDO) linear voltage regulator can be added to the PSU output for tighter regulation. Though Wolfspeed power module designs typically adopt an all-in-one isolated PSU, depending on cost and size constraints, there are other methods for creating the output voltage rails such as a flyback or push-pull converter. See PRD-04814 for more information about these alternative strategies.

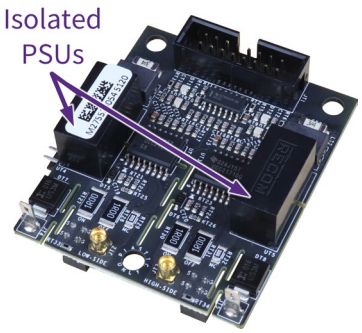


Figure 13: Isolated PSUs on CGD1700HB2M-UNA

When an isolated PSU is adopted which does not include split power rails by default, a Zenor diode can be added to create the split output. For example, Figure 14(a) shows an isolated PSU with integrated split rail outputs, and Figure 14(b) shows an isolated PSU without integrated split rail outputs which utilizes a Zener diode to create the split rails. In this approach, the negative voltage is regulated by the Zener diode voltage rating, and the positive voltage is set based on the difference between the full output voltage and the negative voltage. To control the negative voltage rail, simply select a Zener diode with the appropriate voltage rating. To control the positive voltage rail, regulate the total output voltage (V_{OUT+} - V_{OUT-}) using an LDO. More information about creating split output rails using a Zener diode can be found in PRD-04814.

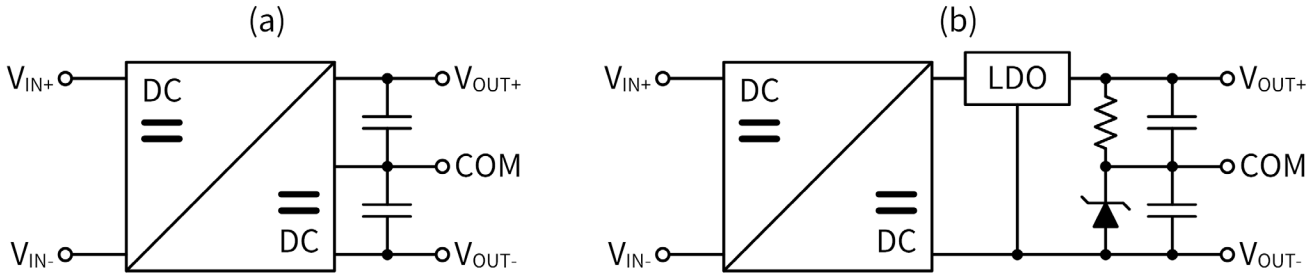


Figure 14: Isolated PSUs: (a) with and (b) without integrated split rail outputs

2.5 Compact Gate Loop

As discussed previously, the inductance of a gate driver is a critical parameter to ensuring the system is reliable and robust. Best practices such as adjacent planes for gate and Kelvin-source layers immediately provide significant benefits to the gate loop inductance. The inductance can be further improved by ensuring that the gate driver and gate terminal of the MOSFET are physically close. Shorter connections between the gate driver and the MOSFET will immediately reduce the gate loop inductance. Furthermore, a compact gate loop has additional benefits such as the following.

Impactful Decoupling Capacitors. As will be discussed in Section 2.6, decoupling capacitors are necessary to support the high transient currents required to turn the MOSFET on and off quickly. These capacitors are most effective when placed near the gate driver IC. Having a compact gate loop aids in this goal and enables the decoupling capacitors to better support large transient currents.

Less Noise Susceptibility. Gate signals operate at significantly lower voltages (tens of volts) compared to the power stage (hundreds of volts), so the gate signals are more susceptible to noise than other parts of the circuit. Reducing the physical size of the gate loop reduces the circuitry that can serve as an antenna for noise and electromagnetic interference (EMI).

Reduced Area Requiring Isolation Barrier. As shown in Section 2.1, the gate driver requires an isolation barrier for safety and improved operation. This barrier requires areas of the PCB to be bare (no components or copper). Maintaining a compact gate loop reduces the amount of area requiring an isolation barrier, thus enabling smaller overall PCBs and reducing cost.

Less Signal Delay. In fast control loops and in fault conditions such as overcurrent events, delay can lead to preventable failures. Limiting the gate loop size reduces system delay, ensuring fast response times.

Referring again to the CGD1700HB2M-UNA gate driver, the isolated section of the high-side (HS) and low-side (LS) gate driver positions have dimensions of only 25.4 mm by 30.5 mm, as shown in Figure 15(b). Furthermore, the entire gate driver – including the control circuitry – is only 50.8 mm by 61.0 mm, as shown in Figure 15(a). This compact component placement and circuit routing enables this gate driver to be used for high-performance, high-frequency applications.

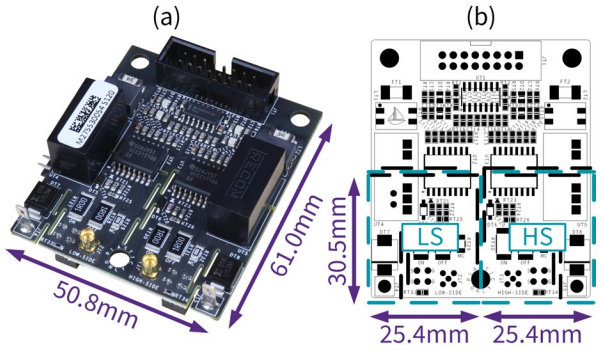


Figure 15: Dimensions of compact gate driver: (a) full CGD1700HB2M-UNA and (b) high/low-side driver circuits

2.6 Decoupling Capacitors

Though a gate driver IC may have the necessary peak ampacity rating to support operation at a particular operating condition, the power supply on the circuit can likely not support the transient energy requirements. Decoupling capacitors are used to stabilize the gate driver voltage rails during peak transient conditions, and to provide the energy required to charge and discharge the MOSFET gates. The gate loop inductance is therefore governed by the size of the combined loop area between the gate driver IC, the MOSFET, and the decoupling capacitors, since the high-frequency content will primarily route through this path. A notional example of the high-frequency gate loop through the decoupling capacitance, C_D, is shown for a turn-on event in Figure 16. The decoupling capacitors need to be suitably sized to handle the transient pulses of power modules, which might have high gate capacitance due to several paralleled power MOSFETs.

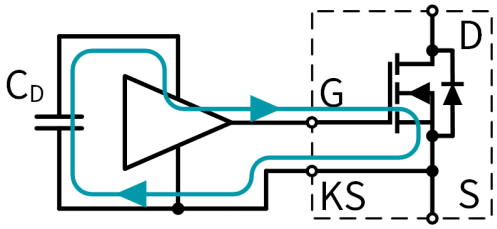


Figure 16: High-frequency gate loop through decoupling capacitor (C_D) during turn-on event

For example, the CGD1700HB2M-UNA gate driver includes 20 µF of capacitance between both V_{DD}-to-Source and V_{SS}-to-Source on the high- and low-side positions. The capacitor connections for the high-side switch position are shown in Figure 17(a). In addition to having high capacity, these capacitors are placed close to the gate driver IC and the MOSFET gate pins to limit the gate loop inductance. The corresponding capacitors shown in the Figure 17(a) schematic are indicated on the circuit board with respect to the gate driver IC and the output pins of the circuit board in Figure 17(b).

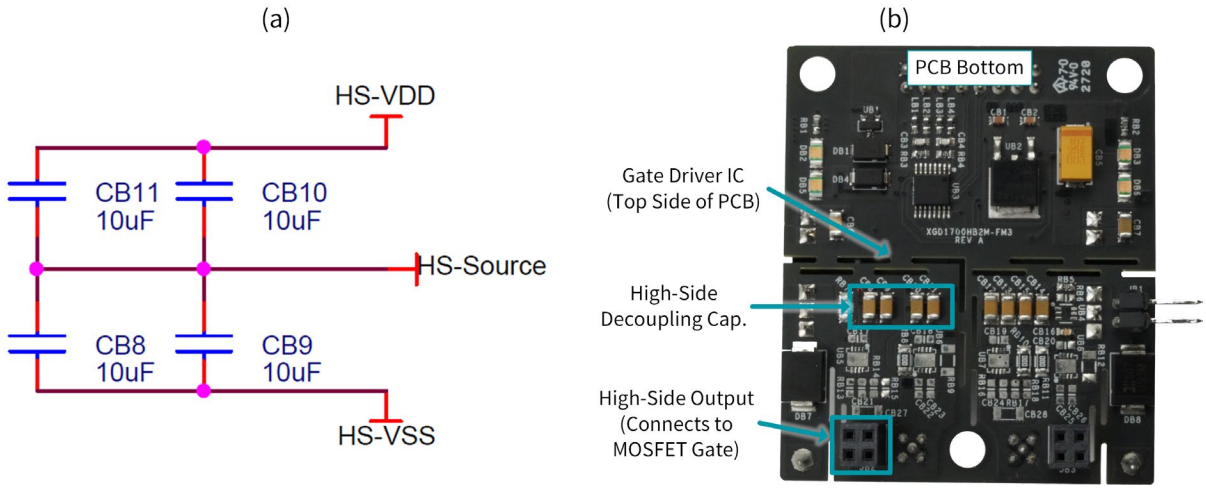


Figure 17: CGD1700HB2M-UNA high-side decoupling capacitance on (a) schematic and (b) layout

2.7 Creepage and Clearance

The elevated voltages employed in SiC designs introduce a greater risk to electrical arcing through the air or due to pollution such as dust. The shortest distance between two voltage potentials represents its clearance distance, and the shortest distance along the surface of a material between two voltage potentials represents its creepage distance. This distinction is shown visually in Figure 18 which notionally compares the creepage and clearance distances between two pins on close ICs with a board cutout in between. The clearance distance is unaffected by the board cutout, since the air gap distance between the two pins remains the same, even with the board cutout. To increase the clearance distance between these two pins would require physically separating the two ICs further[1]. In contrast, the board cutout increases the creepage distance since it introduces a physical barrier on the surface of the circuit board.

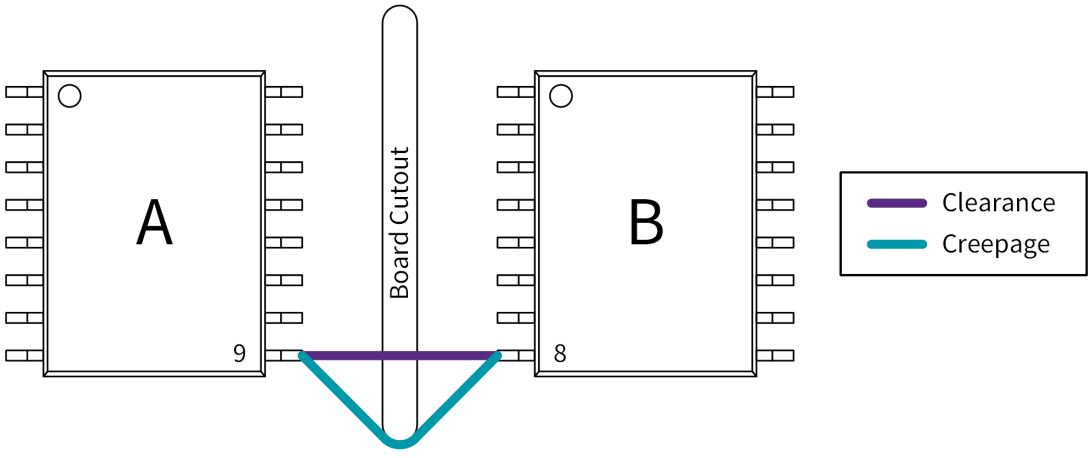


Figure 18: Comparison of creepage and clearance paths

[1] Clearance distance can also be increased by introducing an insulator such as conformal coating.

Required creepage and clearance distances are generally governed by regulatory bodies based on the operating voltage of the design. Example regulatory standards that specify creepage and/or clearance requirements include UL 61800-5-1, IEC 60664-1, and IPC-2221A. The exact standard to follow is based on the application and country where the system will be used. Creepage distance requirements are often much larger than clearance distances to account for the risk of pollution such as dust buildup on the circuit board which can influence arcing. Creepage distances can be increased by employing techniques such as adding board cutouts or barriers between violating parts[2]. Notably, many signals on a gate driver have very little voltage potential difference. For example, in a typical half-bridge application, even though the bus voltage might be hundreds or thousands of volts, the pins of the same gate driver only have ~20 V of potential difference and thus require minimal creepage and clearance requirements. Figure 19 shows how the gate driver elements can be grouped based on similar voltage potentials. The various groups must still achieve creepage and clearance requirements for the elevated voltages with respect to other groups, but the signals within the same group can be routed close together. In many PCB design software programs, these groupings are called *Net Classes*.

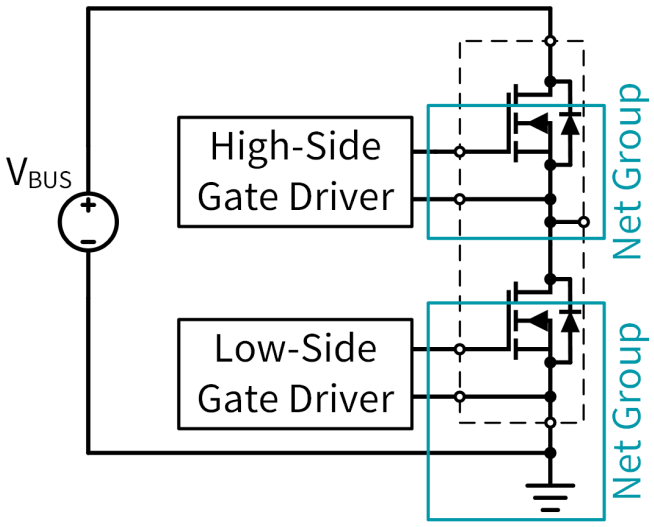


Figure 19: Example grouped nets based on similar voltage potentials

It is important to note that the group-to-group voltage difference is still high and the proper creepage and clearance distances must be considered in these cases. Furthermore, when implementing overcurrent protection such as desaturation circuits (see Section 5.1), the gate driver circuit requires feedback from MOSFET drain terminal. It is also important to note that the drain terminal will be blocking full bus potential, so in this case, the full creepage and clearance distances must be followed. Figure 20 shows the example net class groupings on the CGD1700HB2M-UNA and the corresponding creepage distances between the groups. Slots are included on the board to increase the creepage distance between groupings. Notably, the high voltage DESAT diodes have a large creepage distance to the other net class groups since these diodes could be blocking the full bus voltage.

[2] Creepage distance is also dependent on the surface material, though this discussion focuses on printed circuit boards.

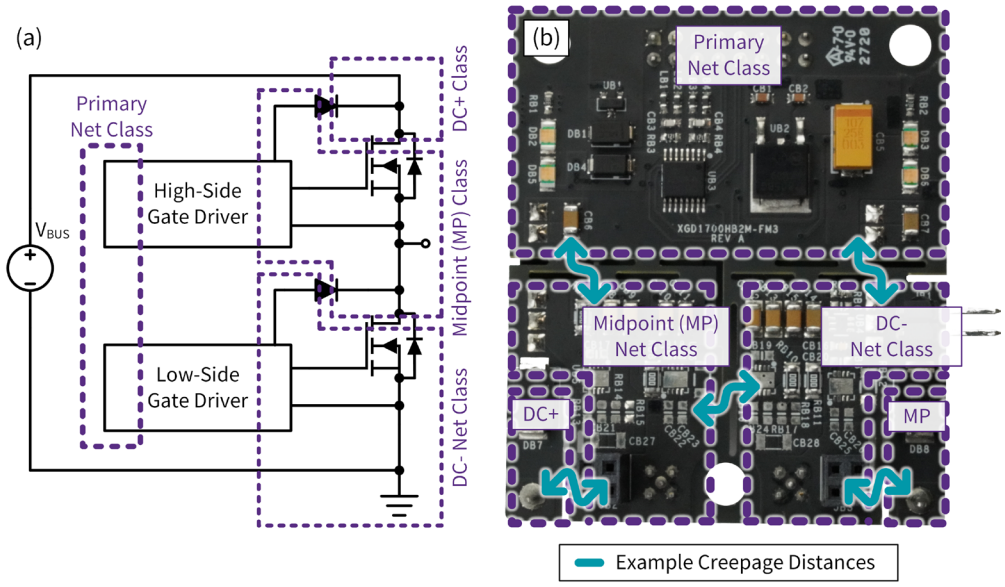


Figure 20: Example net classes on (a) schematic and (b) CGD1700HB2M-UNA

3. Improve Gate Driver Performance

The previous section detailed the requirements and best practices for gate driver design to ensure reliable and consistent operation. This section details guidelines to further improve the gate driver's performance and discusses the tradeoffs of various approaches for reducing system cost.

3.1 Selecting A Gate Resistor

One of the simplest methods for a designer to control the dynamics of a SiC power module is to vary the external gate resistance (R_G). The gate resistor is placed between the output of the gate driver and the gate pin of the MOSFET, as shown in Figure 21. Designers can tune switching power losses, slew rates, and overshoot by varying the gate resistance. This influence is shown in Figure 22 where the simulation from Figure 6 was modified to demonstrate the switching dynamics with various external gate resistance values. As the gate resistance increases, the *dV/dt* and *di/dt* decrease. This behavior reduces overshoot and ringing but increases switching losses. The tradeoffs when selecting an external gate resistor are listed below and should be evaluated on a case-by-case basis by the designer. Generally, designers select the most aggressive R_G value (lowest value) that complies with the maximum V_{DS} rating of the device and/or any regulatory or external component ratings.

Safe Operating Area. Fast edge rates can lead to high V_{DS} spikes due to parasitic inductances and body-diode reverse recovery. When selecting external gate resistor values, a high enough value should be selected to prevent the device from exceeding the breakdown voltage rating of the device. Notably, tuning the gate resistor is not the only parameter available to designers for reducing the V_{DS} overshoot. Designers can also reduce V_{DS} overshoots by improving the circuit board layout (lower inductance) or selecting devices with less reverse recovery spikes.

Power Loss Budget. Higher gate resistors decrease the edge rates of the device, leading to more voltage-current overlap during switching events and resulting in higher switching losses. Depending on the

system switching frequency, efficiency requirements, and cooling solution, the higher switching losses due to a higher gate resistor could be irreconcilable. Reducing the gate resistor will improve system efficiency and thermals.

EMI Requirements. High slew rates and the subsequent high-frequency oscillations can contribute to EMI. Slowing the system dynamics with a higher gate resistor can be used to mitigate the EMI emissions and aid with passing regulatory EMI standards. Notably, these EMI emissions can also be mitigated through strategic PCB layout, component selection, and filtering elements, so alternative options exist besides increasing the gate resistor. Additionally, some applications such as motor drives have a maximum *dV/dt* rating based on insulation or motor manufacturer ratings. Often, a higher gate resistor needs to be adopted to comply with these system requirements.

Passive Component Ratings. Capacitors often have a maximum transient current rating, *di/dt*, that they can support, and magnetics can sometimes include maximum *dV/dt* ratings. In cases where these passive elements cannot be changed for a higher rated part(s), the power module slew rates may need to be limited using the gate resistor to comply with these ratings.

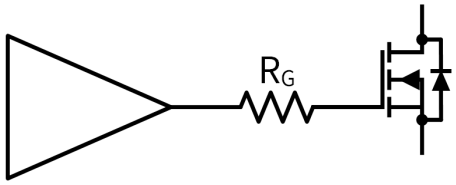


Figure 21: External gate resistor location

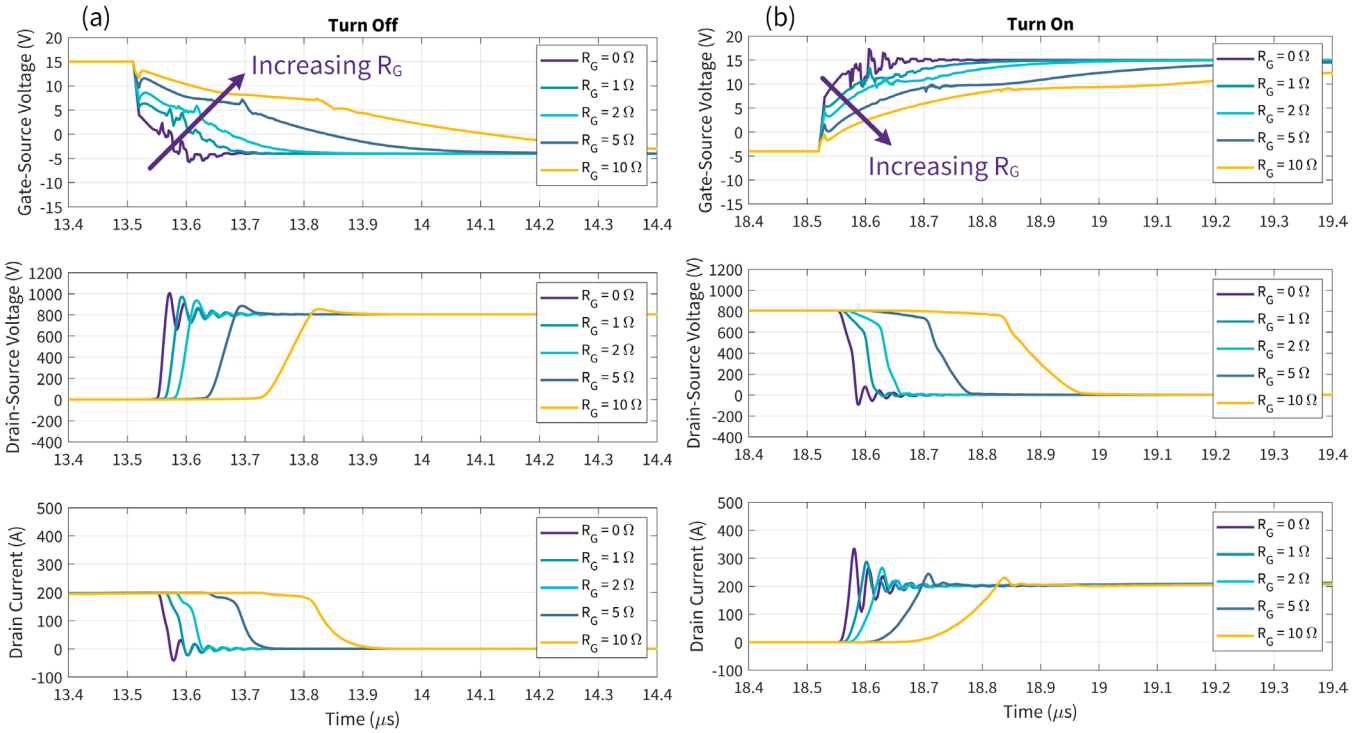


Figure 22: Simulated gate resistance sensitivity during (a) turn off and (b) turn on

3.2 Independent Turn-On and Turn-Off Gate Resistors

For the best performance, designs should support separate gate resistors for turn-on and turn-off. This enables independent tuning of these dynamics, enabling designers to choose dynamics based on criteria such as matching slew rates or maximizing efficiency within the safe operating area. In many cases, approximate gate resistor values can be predicted simply by using the datasheet values for switching losses and slew rates.

For example, suppose a designer identifies a maximum *dV/dt* limit of 25 V/ns for their design using a CAB425M12XM3 power module. The relevant switching loss and slew rate plots from the CAB425M12XM3 datasheet are shown in Figure 23. Using Figure 23(a), the designer can identify the lowest gate resistance to keep the voltage slew rates below the required limit. In this case, a 3 Ω turn-on and 1.3 Ω turn-off resistor are selected. If only a single gate resistor is used for both turn-on and turn-off dynamics, then the higher of the two resistors – 3 Ω in this case – would have to be selected. Higher gate resistors increase the switching losses, so reducing the turn-off resistance from 3 Ω to 1.3 Ω reduces the turn-off loss (E_{OFF}) from 13.1 mJ to 8.3 mJ, a 37% reduction. Ultimately, this independent gate resistor tuning – while requiring few additional components – can significantly improve system performance.

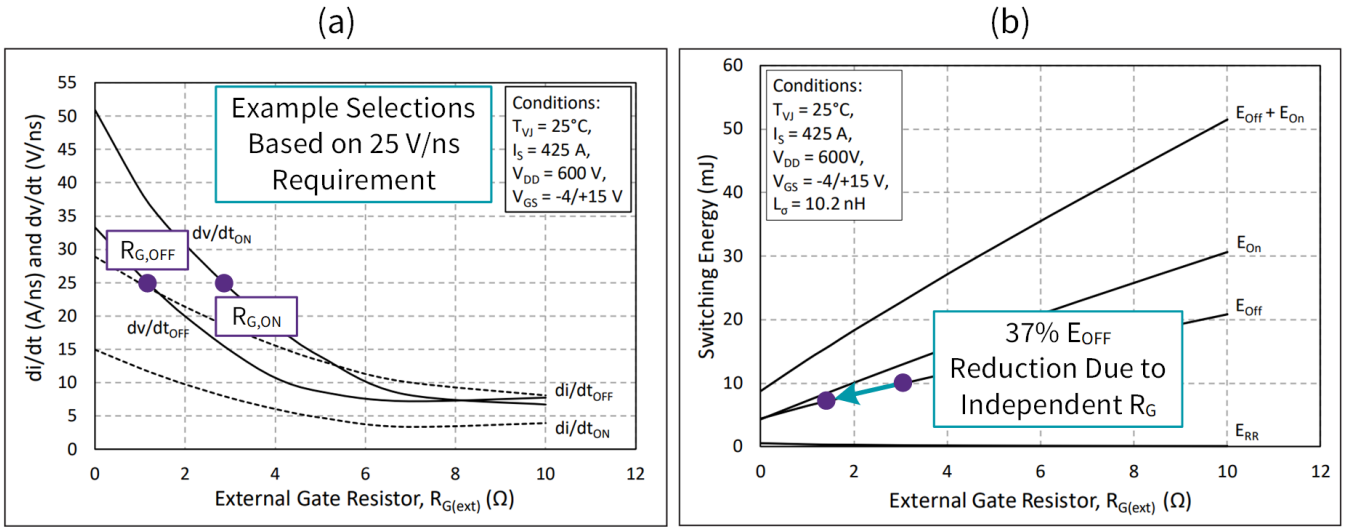


Figure 23: CAB425M12XM3 (a) dV/dt and di/dt, and (b) switching energy vs external gate resistance

The predictions from the datasheet can be further tuned using SPICE simulations, clamped inductive load tests, or end-application testing. Notably, it is important in these tuning steps to have an accurate estimation of the parasitic inductance of the system, since high-inductance systems could perform worse than the datasheet measurements. Precise tuning of the gate drivers in high performance applications is best performed on a test bench with the exact hardware to ensure that all parasitic inductances are included in the measurement.

Many gate driver ICs include separate turn-on and turn-off outputs by default to support independent gate resistor tuning (shown in Figure 24(a)). In these cases, the independent gate resistors simply need to be attached to the separate outputs. This implementation is adopted on the CGD1700HB2M-UNA gate driver. Its independent turn-on and turn-off resistor implementation is shown in Figure 25. When using ICs without this functionality, it can easily be added using “steering” diodes, as shown in Figure 24(b) and Figure 24(c). Figure

24(b) completely decouples the two gate resistances while Figure 23(c) leverages that the turn-off resistor is generally smaller than the turn-on resistor, since turn-on dynamics are typically more at risk for violating overshoot restrictions. In this configuration, current flows through $R_{G,ON}$ during turn-on dynamics, and current flows through both $R_{G,ON}$ and $R_{G,OFF'}$ during turn-off dynamics, resulting in a lower equivalent turn-off resistance. When implementing a solution with steering diodes, the diodes should be selected to have minimal impact on the circuit dynamics. Any diode inductance or slow dynamic behavior will impact the MOSFET dynamics.

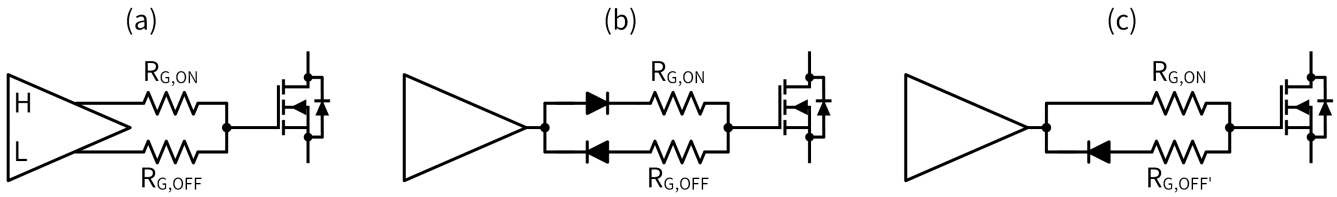


Figure 24: Separate turn-on vs turn-off resistor examples: (a) gate driver IC with separate outputs, (b) independent steering diodes, and (c) turn-off steering diode

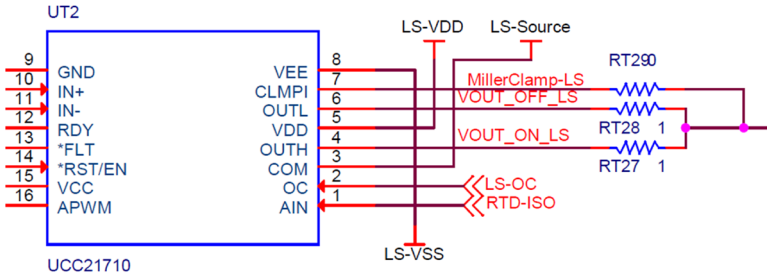


Figure 25: Separate turn-on and turn-off resistors implementation on CGD1700HB2M-UNA

3.3 Integrated vs Separate Gate Drivers

Gate drivers can be integrated into a design in one of two ways: (1) the power stage and gate driver can be on separate circuit boards, or (2) the power stage and gate driver can be integrated into a single circuit board solution. In high power circuits (~200+ kW), designs typically use laminated bussing or PCBs with high copper thicknesses, so it is often not practical to try to place a gate driver circuit on the same board as the power stage. In lower power applications – where PCBs with lower copper thicknesses are employed – the tradeoffs between the potential gate driver locations become more application dependent. This is especially true when the power terminals and the gate terminals of a power module share the same mounting application type (such as the press-fit pins in the WolfPACK series of power modules). Both integration options have advantages which are discussed below in more detail and summarized in Table 1.

Serviceability. When the gate drivers and power stage are integrated into a single circuit, the entire assembly must be serviced or replaced when there is an issue with a gate driver. In contrast, in a separated design, a single gate driver circuit board can be independently replaced when an issue is observed.

Cross-Product Sharing. In a separate approach, a single gate driver design can be used to support multiple projects. For example, a single gate driver for the XM product portfolio (such as the CGD12HBXMP gate driver) can be used for a motor driver or a DC/DC converter, which reduces overall

cost by increasing the design volume and achieving higher economies of scale. In the integrated design, the gate drivers cannot be used independently for different designs.

Cost. The integrated gate driver solution is generally the more cost-effective solution since the design can be reduced to a single printed circuit board, which reduces the system assembly bill of materials (BOM). No additional steps are required to attach gate driver boards to the assembly, since all the components are attached in the board fabrication process. However, the separate gate driver design can still be completed in a cost-effective manner by sharing the gate driver design across multiple products and achieving higher economies of scale.

Performance. The gate driver signals and components of an integrated design often block or hinder optimized routing of the power stage. When planned well, the power stage can be routed with little impact to the system inductance, but this added inductance might be unacceptable in high-performance applications. With separate gate drivers, the components and routing for the drivers do not impact the routing of the power stage, so the power stage can be optimized to minimize the system inductance.

Table 1: Comparison of integrated vs separate gate driver circuits

Description	Integrated Drivers	Separate Drivers
Serviceability	Poor. Requires replacing/servicing entire assembly.	Good. Replace/service gate drivers individually.
Cross-Product Sharing	Poor. Only the entire assembly hardware can be shared.	Good. Single gate driver can be used in multiple designs.
Cost	Good. Single circuit board cost. No assembly steps to attach gate drivers.	Poor. Requires more circuit boards (can be offset sharing drivers across designs).
Performance	Medium. Power routing not optimized to avoid gates. Gates not through connector.	Good. Optimized power rails are not hindered by gate signals.

In general, integrated gate drivers are adopted with lower power modules such as the WolfPACK product portfolio and separate gate drivers are employed in high-performance designs such as those using the XM product portfolio. WolfPACK designs already require a PCB and these designs are generally extremely sensitive to cost, so the integrated gate driver is preferred. An example design using gate drivers on the same PCB as the power circuitry is the CRD25DA12N-FMC reference design, shown in Figure 26(a). Designs using the XM product family often use laminated bussing for the power stage, and thus it is not practical to combine the gate drivers with the power stage. Additionally, the higher cost of these modules (compared to WolfPACK modules) makes it more attractive to be able to replace a faulty gate driver circuit board, rather than having to service an entire power and gate driver assembly. An example design using separate power circuitry and gate driver boards is the CRD300DA12E-XM3 three-phase inverter, shown in Figure 26(b).

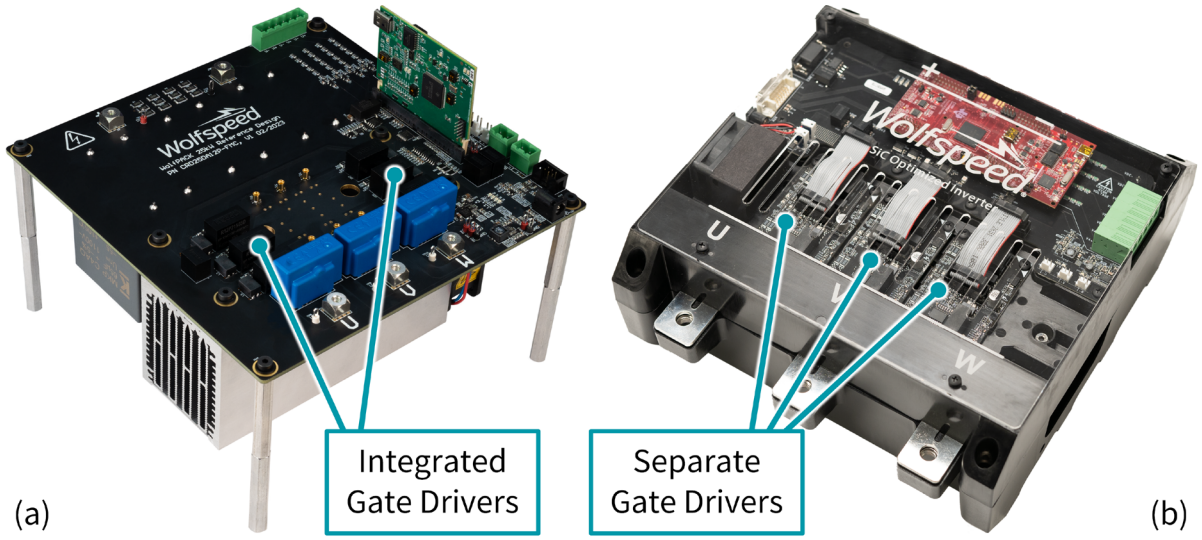


Figure 26: (a) Integrated gate drivers on CRD25DA12N-FMC and (b) separate gate drivers on CRD300DA12E-XM3

3.4 NTC Feedback

Wolfspeed case power modules include an integrated negative temperature coefficient (NTC) sensor inside the modules for measuring the substrate temperature of the module during operation. The sensor can be useful for checking that the cooling system is operating as expected and can be used to modulate the cooling system. More information about the thermals of power modules can be found in PRD-08376. The integrated NTC is isolated from all voltage potentials of the power module. However, in the unlikely case of a catastrophic failure in the module, a wire bond or other debris may bypass this isolation barrier to the NTC sensor. For this reason, Wolfspeed recommends adding an isolation barrier to the feedback signals from the NTC sensor usually in the form of a digital isolator on the gate driver board. This will ensure that the primary-side circuitry and the operator are protected if a system failure were to occur.

This section discusses several approaches for providing isolated feedback from the NTC sensor. All the feedback strategies discussed follow the same approximate feedback flow shown in Figure 27. The NTC resistance is biased to produce a voltage which is proportional to the temperature and that can be interpreted by the isolator. The isolator output is filtered with simple RC conditioning or with more advanced conditioning to a form which can be interpreted by the controller. Each of the NTC sensor feedback strategies is discussed in detail below.

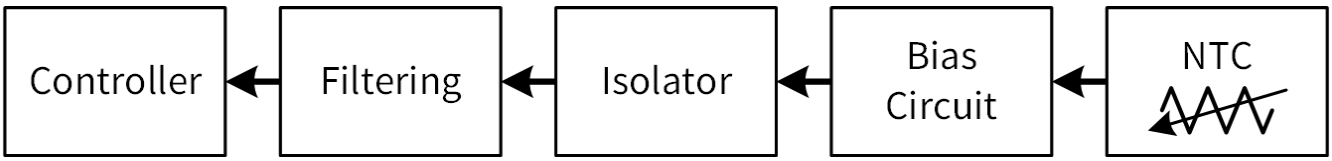


Figure 27: Notional NTC feedback block diagram

Integrated Gate Driver IC Feedback. The simplest method for transmitting the NTC sensor status to the controller is to use a gate driver IC with an integrated isolated feedback pin. When gate driver ICs include this functionality, often an analog measurement is converted to an isolated pulse-width

modulation (PWM) signal with varying duty cycle or frequency depending on the measured analog voltage. This strategy requires few additional BOM components as only the bias and filter circuit components must be added. This is the NTC sensor feedback strategy employed in the CGD1700HB2M-UNA gate driver, as shown in Figure 28. The corresponding PWM signal can be measured directly with a digital input pin of the controller or converted back to an analog signal and measured with an analog-to-digital conversion (ADC) pin. If using the digital input pin strategy, it is important that the controller has a suitable sampling rate to capture the PWM signal from the gate driver IC. When the feedback signal is a variable duty cycle, the controller digital input pin must be able to capture at a much higher sampling rate than the transmission frequency. Given the slow time constants of temperature measurements, it is generally recommended to use an ADC measurement instead. In this configuration, the output of the gate driver IC is converted to an analog signal, often simply through an RC circuit with a large time constant. The ADC measurement can be performed by the controller at fixed time intervals, rather than consuming resources to sample the PWM signal regularly.

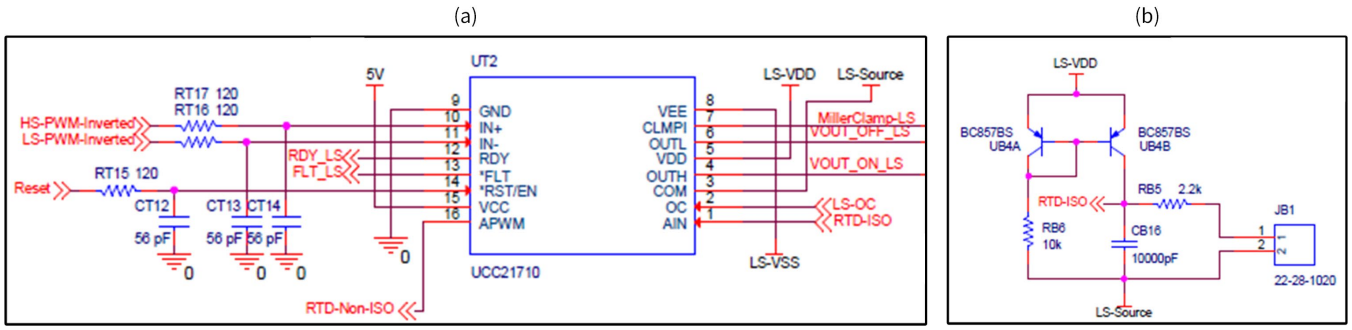


Figure 28: Integrated gate driver IC NTC sensor feedback example from CGD1700HB2M-UNA: (a) IC and (b) bias

When possible, it is recommended that the NTC sensor feedback is attached to a gate driver referenced to a consistent voltage rail. For example, in a standard two-level half-bridge configuration (see Figure 4), the NTC sensor should be connected to the low-side gate driver (referenced to DC-), rather than the high-side gate driver (reference to the varying mid-point) for a better measurement. If a topology is adopted where all module switch position references are varying, it might make sense to use one of the other feedback strategies with a separate isolated power supply. This will vary depending on the end application.

Custom Analog-to-Duty Cycle Conversion. When a gate driver IC does not include feedback by default, analog-to-duty cycle circuits can be added and routed through a digital isolator back to the controller. This is the NTC sensor feedback strategy employed in the CGD1700HB2P-XM3 gate driver, as shown in Figure 29. Like the isolated gate driver feedback approach, the resulting PWM signal can be directly measured with a digital input pin of a controller or converted to an analog signal and measured with an ADC input. This circuit can be operated off power provided by an isolated gate driver PSU already on the circuit board or off a dedicated isolated PSU.

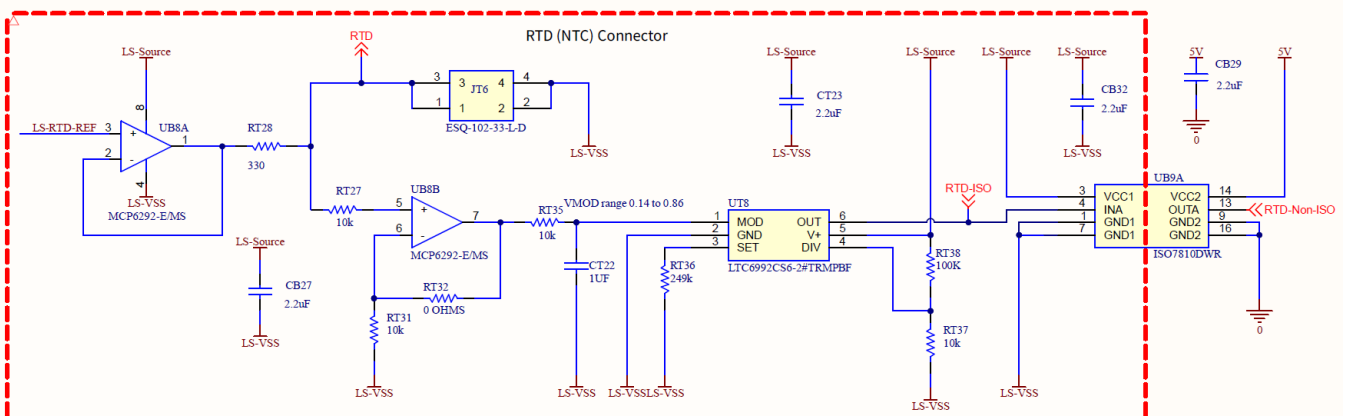


Figure 29: Custom analog-to-duty cycle conversion NTC sensor feedback example from CGD1700HB2P-XM3

Isolated Operational Amplifier. Several manufacturers offer operational amplifiers with an integrated isolation barrier. These circuits can perform the same functionality of a normal operational amplifier with the addition of an isolation barrier. This feedback strategy is employed in the CRD25DA12N-FMC three-phase inverter in version 2.0+, as shown in Figure 30. Some isolated operational amplifier options also include an integrated low-power isolated DC/DC converter, allowing this circuit to be operated independently of a gate driver PSU. This is an attractive option since it enables an NTC sensor measurement on a power module where all the switch positions are referenced to fluctuating voltages. This configuration can also employ fewer components than the custom analog-to-duty cycle conversion, though this configuration can be more susceptible to transmission noise, especially if the output of the operational amplifier is not differential.

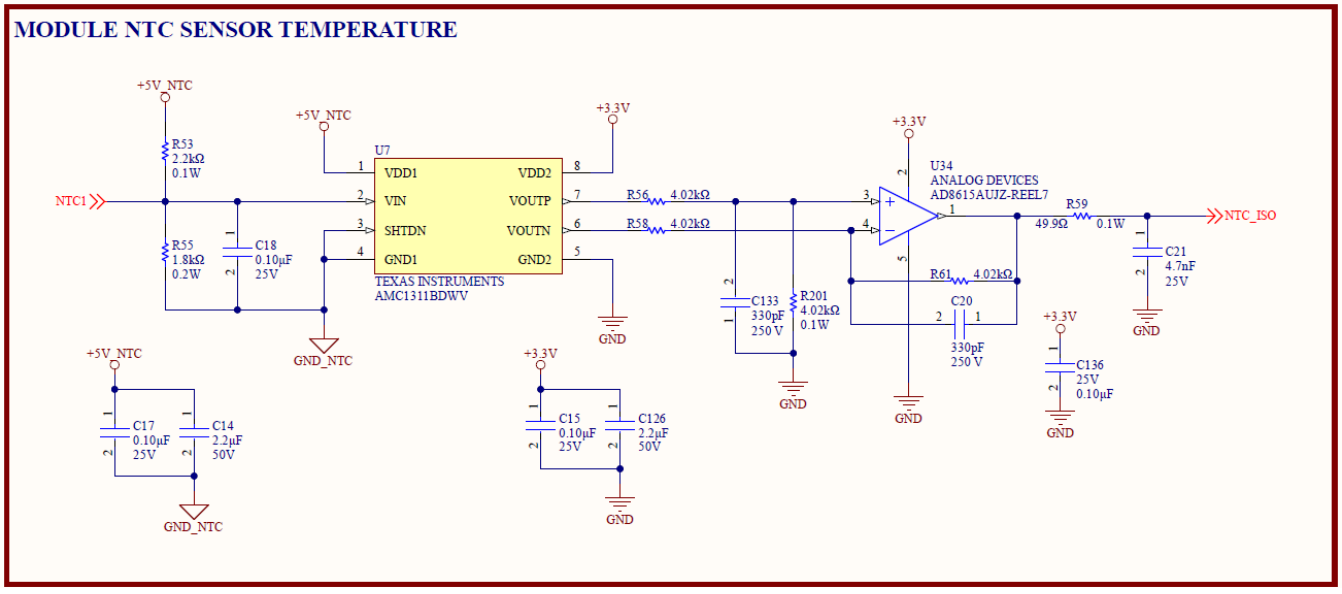


Figure 30: Isolated operational amplifier NTC feedback example from CRD25DA12N-FMC V2.0+

A summary of the common NTC sensor feedback types is shown in Table 2. A corresponding Wolfspeed design employing each of these strategies is also presented in the table.

Table 2: Summary of various NTC sensor feedback types with example Wolfspeed designs

NTC Sensor Feedback Type	Reference
Integrated Gate Driver IC Feedback	CGD1700HB2M-UNA
Custom Analog-to-Duty Conversion	CGD1700HB2P-XM3
Isolated Operational Amplifier	CRD25DA12N-FMC V2.0+

With any of the abovementioned approaches, the data received by the microcontroller at the end of the signal chain will need to be calibrated to determine the corresponding temperature. Wolfspeed power modules featuring built-in NTC thermistors include the resistance vs. temperature information of the sensor in the datasheet. For example, Figure 31 shows the CAB004M12GM4T NTC sensor characterization. An easy method to perform calibration of the NTC signal chain is to use a potentiometer in place of the NTC sensor to set the equivalent NTC sensor resistance, which bypasses the need to heat and cool the power module during calibration.

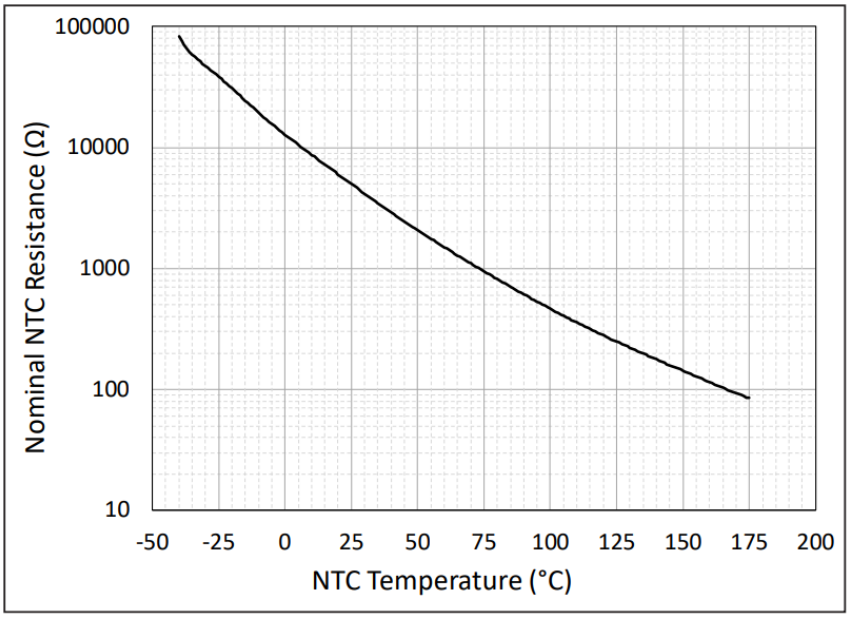


Figure 31: CAB004M12GM4T nominal NTC sensor resistance vs NTC sensor temperature

3.5 Negative Bias Voltage Selection

When a MOSFET is off, it is essential that the gate voltage does not increase sufficiently to induce significant channel conduction. This is especially critical when other switch positions are actively switching, which often injects noise into the inactive switch positions. One common technique to reduce this susceptibility is to bias the MOSFET gate to a negative voltage during the turn-off state. The negative voltage introduces margin to reduce the risk of the MOSFET gate voltage significantly exceeding the threshold voltage, as shown in Figure 32. Biasing the gate voltage negative also aids in turning off the device faster as the negative bias improves the capability of the gate driver to more quickly deplete the MOSFET's input capacitance during transient events.

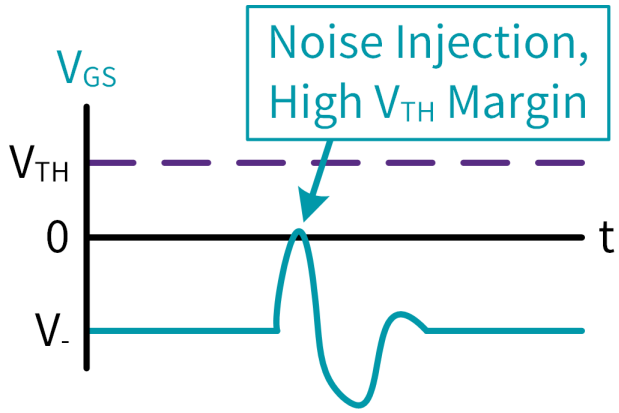


Figure 32: Increased V_{TH} margin using negative-bias gate driver during turn off

A negative bias voltage is not required for operating Wolfspeed devices since V_{TH} is not a strict boundary. Short V_{GS} spikes above V_{TH} do not cause large magnitude drain currents to flow through the channel due to the low transconductance of the MOSFET when V_{GS} is between V_{TH} and the Miller plateau. Exceeding V_{TH} by even 3 V during transients may cause slightly higher switching losses and peak current values, but it will not cause shoot-through conditions. Figure 33 shows example switching results comparing -3 V and 0 V gate biases on a discrete C3M0045065L device. Referring to Figure 33(a), with the 0 V off bias, the gate voltage does not significantly exceed threshold (2.6 V) and only exceeds V_{TH} for a short duration (26 ns). In comparison, as expected, the added margin of the -3 V bias prevents the gate voltage from ever exceeding V_{TH}. The exceeded threshold voltage of the 0 V bias setup is reflected in slightly higher measured device currents as shown in Figure 33(b), though the device can operate consistently under these conditions. Wolfspeed recommends closely evaluating switching results on a case-by-case basis when determining whether to adopt a 0 V turn-off bias.

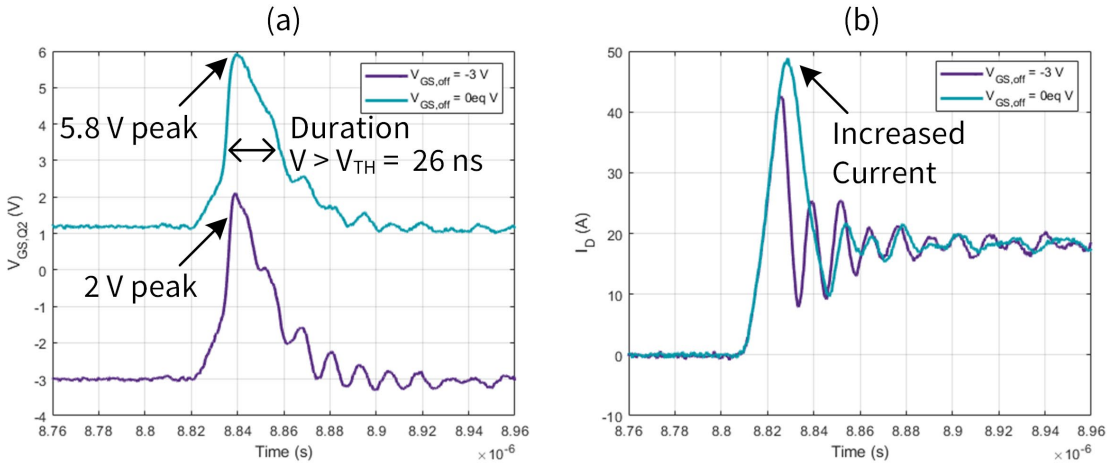


Figure 33: C3M0045065L CIL results comparing 0 V and -3 V gate bias: (a) gate voltage and (b) device current

Wolfspeed power module datasheets list the recommended gate bias voltages under the line item "Operational Gate-Source Voltage." However, as mentioned previously, there is some flexibility to operate at other voltages besides the recommended voltages such as adopting a 0 V turn-off bias. If adopting voltages that differ significantly from the recommended voltages, it is suggested to work with a Wolfspeed representative to ensure

the device will operate as intended. Regardless of the gate voltage adopted, good layout practices on the gate driver and the power stage will reduce gate driver noise and ensure the system is more reliable. With 0 V bias, the sensitivity to gate driver noise is heightened, so adhering to best layout practices is critical.

3.6 Shared Isolated Power Supply

As discussed in Section 1.2, isolation is critical in gate driver circuits to decouple the logic-level control signals from the power stage. Because of this isolation requirement, all gate drivers which are referenced to different voltage potentials must be isolated from each other and therefore require their own isolated power supplies. However, in some circuit topologies, gate drivers can share the same isolated power supply. When all MOSFETs are referenced to the same circuit location, each switch position needs an independent gate driver IC but can share an isolated power supply unit.

The most common topology that can leverage the shared isolated PSU is the three-phase two-level inverter shown in Figure 34. The gate drivers of Switch Positions *1, 3*, and *5* are all referenced to different voltage potentials (*U*, *V*, and *W*, respectively) and therefore require independent gate driver ICs and PSUs. However, Switch Positions *2*, *4*, and *6* are all referenced to the same potential (DC-) and can share the same PSU. The PSU and individual gate driver ICs still provide isolation from the power circuitry to the control circuitry, but the circuit no longer requires isolation between the references of the individual switch positions. The CRD07500AA12N-FMC three-phase motor drive adopts a shared PSU configuration for its inverter stage. For reference, Figure 35 shows the implementations of the shared low-side PSU on the CRD07500AA12N-FMC reference design. Please note that this does not apply if source-referenced current viewing resistors are utilized to measure the source current for each phase of the inverter.

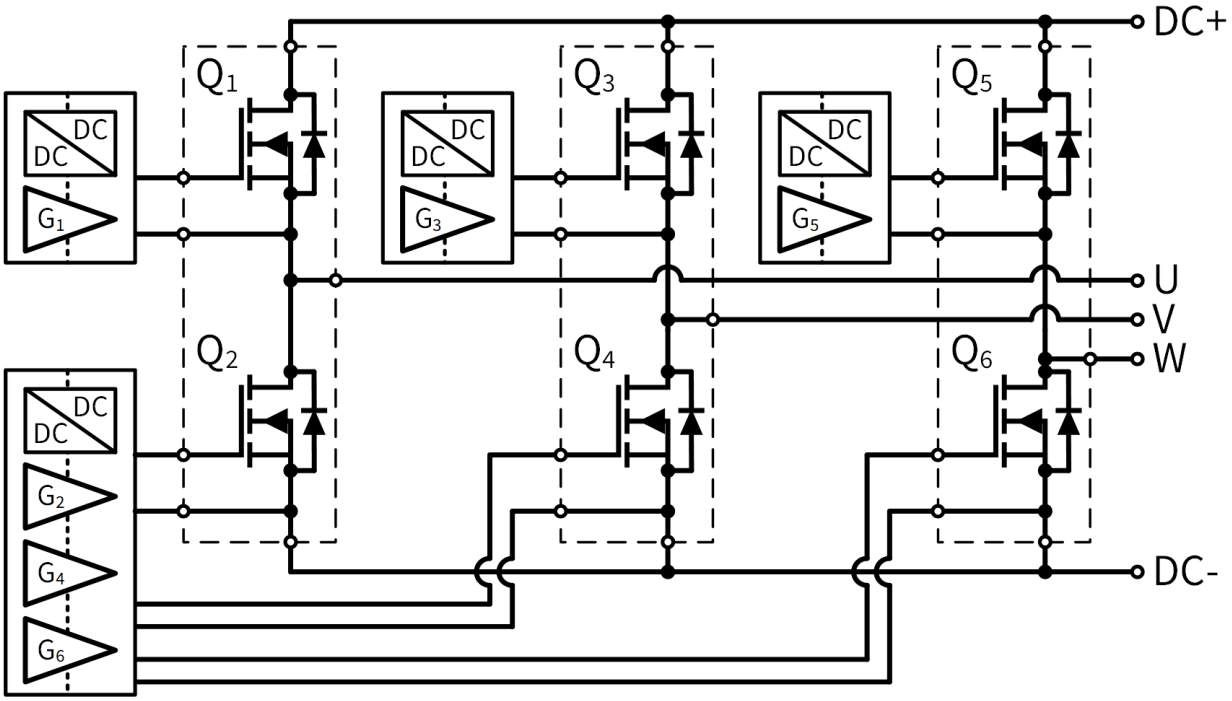


Figure 34: Shared isolated power supply for low-side switch positions in a three-phase inverter application

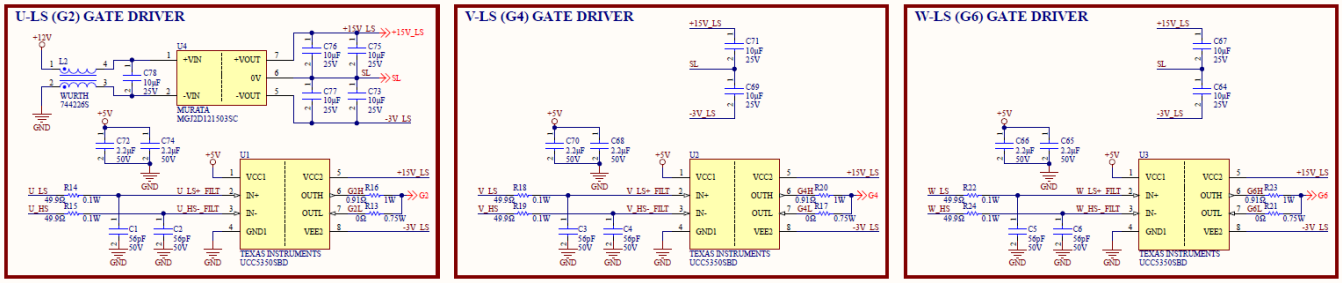


Figure 35: [CRD07500AA12N-FMC] implementation of shared isolated power supply

Leveraging a single power supply for multiple switch positions introduces system benefits such as reduced cost and complexity. Isolated power supplies are often a costly BOM item, so removing one or more can result in large cost savings. Additionally, requiring less components on the board can result in simplified circuit board routing and may result in a smaller circuit board size, further improving cost.

A single PSU configuration also has disadvantages which must be considered when determining whether the configuration is applicable for an application. First, using a single PSU introduces a path for circulating or balancing currents between the Kelvin-source connections of the gate drivers. Though no power stage currents should flow between the Kelvin-source connections of the gate driver, it is possible that poor power stage layout such as extreme imbalance between switch positions could result in non-negligible currents flowing through the Kelvin-source connections of the gate drivers. When adopting shared PSU gate drivers, mistakes and imbalances in the power stage layout are amplified. Notably, in addition to having unintended electrical behavior, this problem could easily cause thermal issues due to elevated currents flowing through the smaller Kelvin-source wire bonds/connections inside the power module. Second, noise is more likely to be coupled between phases due to the direct connection between them. This impact is negligible in most cases since the different switch positions are already directly connected through the power-source connection, but this could become an issue in some cases. Third, as will be discussed in Section 3.7, the maximum gate driver switching frequency is governed by the maximum power output of the isolated PSU. In the shared PSU configuration, more MOSFETs are driven by a single power supply. If the power supply size is not increased accordingly, the maximum switching frequency is reduced with a shared PSU. Fourth, it is difficult to place the shared PSU in a location that is equivalent distance to all the driven switch positions. This impact can be minimized by having symmetrical gate drive IC and decoupling capacitor placement close to the MOSFETs, but it is possible that asymmetrical placement of the shared PSU could become problematic. Table 3 summarizes the trade-offs of adopting a shared isolated power supply for multiple switch positions.

Table 3: Trade-offs of using a shared isolated power supply for multiple switch positions

Advantages	Disadvantages
BOM Cost Reduction	Circulating Currents and Higher Coupling
Less Components to Route	Reduced Maximum Switching Frequency
Potentially Smaller PCB	Hard to Maintain Symmetry Between Gate Drivers

It is noted that, even if individual PSUs are adopted for all switch positions, designers can still leverage the fact that the potentials are all similar. Since all the gate drivers are referenced to the same potential, these gate driver circuits require very small creepage and clearance distances between them and thus can be routed extremely close together (see Section 2.7 for more information about net grouping). Recognizing this, the circuit board layout size can still be reduced compared to a design which includes an isolation barrier between all the switch positions.

3.7 Maximum Gate Driver Switching Frequency

The faster slew rates of SiC MOSFETs compared to Si IGBT devices immediately lowers the losses – and therefore heat generated – in applications where Si is replaced with drop-in SiC and all other operating parameters are maintained. This leads to significant reduction opportunities with the cooling solution. Furthermore, when a design is optimized for SiC MOSFETs, the faster speeds can be leveraged further by increasing the switching frequency while still maintaining lower system losses compared to Si-based converters. The higher switching frequency available in SiC-based applications leads to a significant reduction in passive element size since capacitors and magnetics no longer require as much energy storage. Figure 36 shows a case study example of Si- and SiC-based converters with equivalent output power ratings. The Si system is limited to a switching frequency of only 8 kHz whereas the SiC system can easily operate at 25 kHz. The lower losses of the SiC-based solution along with the higher switching frequency results in a 42% reduction in passive component volume.

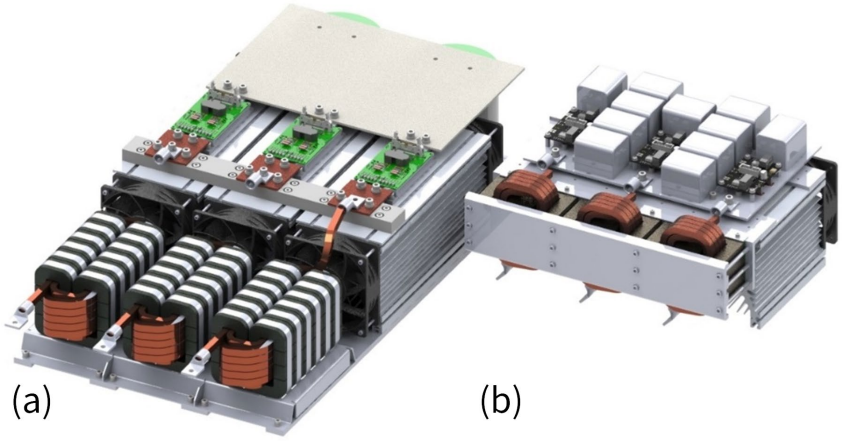


Figure 36: Case study comparison of equivalently rated converters: (a) Si-based and (c) SiC-based

The maximum switching frequency of the gate driver is governed by the isolated power supply used and the semiconductor being modulated. Though the MOSFET slew rates are limited by the gate driver IC output ampacity and the selected gate resistance, the maximum switching frequency is limited by the amount of power available to the gate driver circuit. It is crucial to ensure the gate driver PSU has sufficient continuous output power capability to support the desired switching frequency of the system. These calculations become more critical if a design is employing a single isolated PSU for multiple switch positions, as described in Section 3.6. The required calculations to determine the maximum gate driver switching frequency are determined based on the power consumed by the MOSFET, the MOSFET's gate charge, the desired switching frequency, and the PSU voltage rails. The power consumed by the MOSFET (P_{SW}) during switching is calculated by

$$P_{SW} = Q_G \cdot F_{SW} \cdot \Delta V_{PS} \quad (1)$$

where Q_G is the total gate charge, F_{SW} is the switching frequency, and ΔV_{PS} is the difference in the isolated power supply voltage rails. Solving for F_{SW} in equation (1) results in

$$F_{sw} \leq \frac{P_{SW,max}}{Q_G \cdot \Delta V_{PS}}. \quad (2)$$

Equation (2) is used to determine the maximum switching frequency of the gate driver in a system, limited by the maximum per-channel output power of the gate driver, $P_{SW,max}$. For example, consider a system using the CAB450M12XM3 power module with the CGD1700HB2M-UNA gate driver. From the module datasheet, the gate charge is 1330 nC when driven at the recommended operating voltages of +15 V / -4 V. From the gate driver datasheet, the maximum per-channel output power is 2 W. Per equation (3), the maximum F_{SW} is calculated to be 79 kHz. With margin, the recommended maximum switching frequency would be approximately 70 kHz.

$$F_{sw} \leq \frac{2\ W}{1330\ nC \cdot (15\ V - (-4\ V))} \rightarrow F_{SW} \leq 79\ kHz \quad (3)$$

3.8 Common Mode Choke

A primary influential parameter for noise being introduced into a system is common-mode (CM) currents flowing from the power stage to the logic-level circuitry on the protected side of the gate driver isolation barrier. A prevalent path for CM currents to flow is through the capacitive coupling across the isolation of the gate driver PSU. To limit this potential CM path or as a troubleshooting method, it can be beneficial to add a CM choke to the inputs of the gate driver PSU, as shown notionally in Figure 37(a). The choke increases the CM impedance of this path, reducing the CM current flow to the protected side of the isolation barrier. The CGD1700HB2M-UNA includes CM chokes on both the high- and low-side PSUs. The implementation of the CM choke on the high-side PSU is shown in Figure 37(b). For best performance, the CM choke should be placed physically close to the isolated PSU. Notably, the input PSU decoupling capacitor (reference designator CB6 in Figure 37(b)) is placed between the CM choke and the isolated PSU to limit the impedance between the capacitor and the PSU.

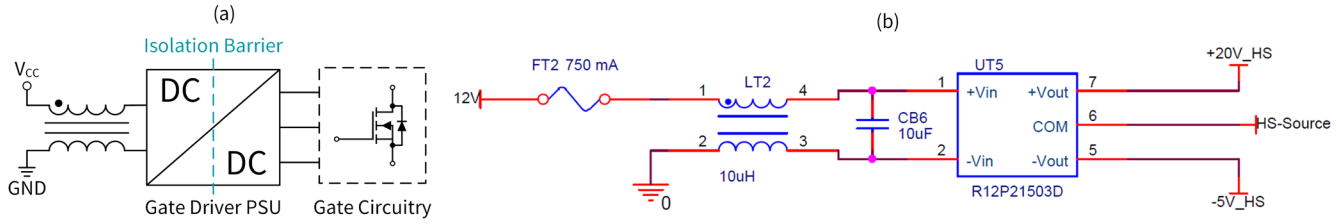


Figure 37: Gate driver PSU CM choke implemented (a) notionally and (b) on the CGD1700HB2M-UNA driver

3.9 Gate Drivers for Paralleling Modules

In many cases, power modules are adopted over discrete solutions to increase circuit ampacity, without introducing additional complexity. Power modules feature an optimized internal layout, symmetrical routing between internal die, and have been tested extensively as a system. These design criteria would have to be considered when trying to develop a custom parallel discrete semiconductor solution. In some cases, however, the higher ampacity provided by power modules is still not enough to satisfy system design requirements. In these cases, designers can choose to interleave multiple phases or to parallel modules.

In interleaving applications, each power module still utilizes its own gate driver, with the added complexity being on the controller that modulates the gate drivers. In interleaved applications, all the gate driver design practices discussed in this document remain the same.

In parallel module applications, power modules can be driven in one of three ways: (1) a single gate driver can control all the parallel power modules, referred to as *Common Gate Driver*; (2) a single gate driver can control independent buffer stages which independently control the power modules, referred to as *Additional Buffer Stages*; (3) multiple gate drivers can be employed to control each power module independently, referred to as *Multiple Gate Drivers*. These approaches are summarized in Figure 38 (from PRD-08911). Note that the figure also includes parasitic gate inductance for each power module. All the configurations have advantages and disadvantages. For more information about these trade-offs, see PRD-08911 which details the requirements for paralleling power modules with experimental results to support the conclusions. This section will simply address the specific gate driver design requirements to support these approaches to paralleling.

Common Gate Driver. All the best practices and guidance described in this document thus far are still applicable. When using a common gate driver, it is important to have symmetrical power module connections to improve the module-to-module current sharing. In addition to the abovementioned guidance, Wolfspeed recommends using a dedicated gate resistor for each module and adding a Kelvin-source resistor to each module, as shown in the *Common Gate Driver* section of Figure 38. Both the gate resistor and the Kelvin-source resistor should be placed physically close to the power module input terminals. The addition of the Kelvin-source resistor reduces the current flow into each gate caused by crosstalk between devices or coupling from the power loop. Wolfspeed recommends allocating approximately 2/3 of the total resistance to the gate and 1/3 of the total resistance to the Kelvin-source, as depicted in Figure 38. In practice, fixing the Kelvin-source resistor at 1 Ω and adjusting the gate resistor as necessary has resulted in optimal switching performance. In designs with independent $R_{G,ON}$ and $R_{G,OFF}$ (see Section 3.1), the Kelvin-source resistor is included in both the turn-on and turn-off loops and should be considered when determining the equivalent turn-on and turn-off resistances. In this case, Wolfspeed recommends either adopting a 1 Ω constant Kelvin-source resistance or optimizing the Kelvin-source resistance to achieve approximately the 2/3 to 1/3 ratio for both gate resistances. For designs using a 0 Ω gate resistor, evaluate the system thoroughly to ensure that its operation is stable across all load conditions.

With this approach, it is important to ensure that the gate driver ampacity and the isolated PSU continuous power ratings are sufficient to drive the higher capacitances of paralleled power modules. The higher capacitance due to the additional parallel MOSFETs will reduce the maximum switching frequency (see Section 3.7) and slew rates (see Section 1.3). These reductions can be offset by upgrading the gate driver IC and/or PSU to higher ampacity/power rated devices, but this will result in a cost increase that should be considered.

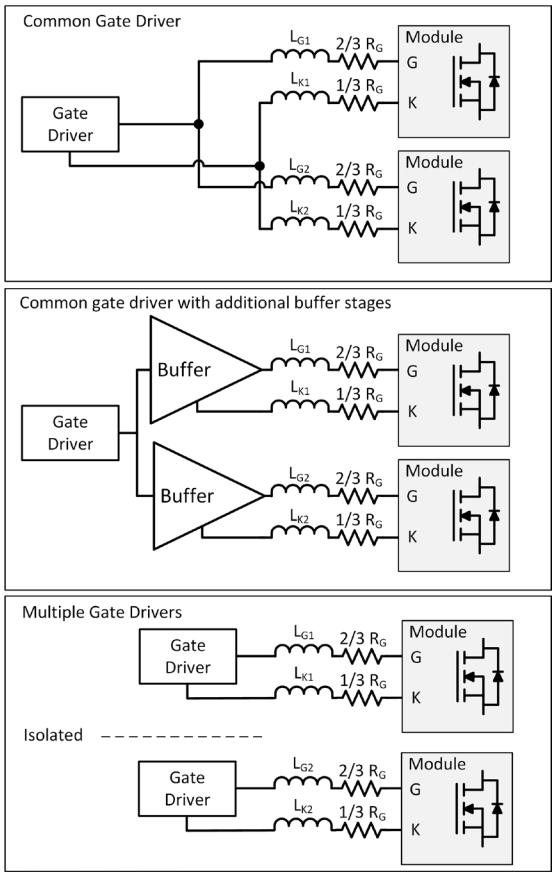


Figure 38: Gate driver solutions for controlling parallel power modules (PRD-08911)

Additional Buffer Stages. The buffers increase the drive output strength of the circuit and reduce the gate inductance. The gate loop inductance is reduced since the loop is defined between the buffer stage and the module, rather than between the common gate driver and the module. The gate driver guidance for the *Additional Buffer Stages* approach is identical to the *Common Gate Driver* approach. However, asymmetry is amplified more when using *Additional Buffer Stages*, so matched routing between the different buffer stages is critical to paralleling success using this approach.

Since the buffer stages now source the transient gate current spikes, the *Additional Buffer Stages* approach is not limited by reduced slew rates like the *Common Gate Driver* (assuming the buffer stage is sufficiently designed and/or rated). However, like the *Common Gate Driver* approach, the switching frequency is still limited by the isolated PSU employed (see Section 3.7).

Multiple Gate Drivers. Each power module is driven by an independent dedicated gate driver (shown in Figure 39). In this approach, adding more power modules in parallel does not change the maximum switching frequency or slew rates since each gate driver is independent. This approach requires simply following the guidelines and recommendations outlined in this document. The split resistance in Figure 38 between the gate and Kelvin-source for this configuration is not strictly necessary, since the Kelvin-source connections do not share a common return path. However, it may be beneficial in some cases to implement the split resistance.

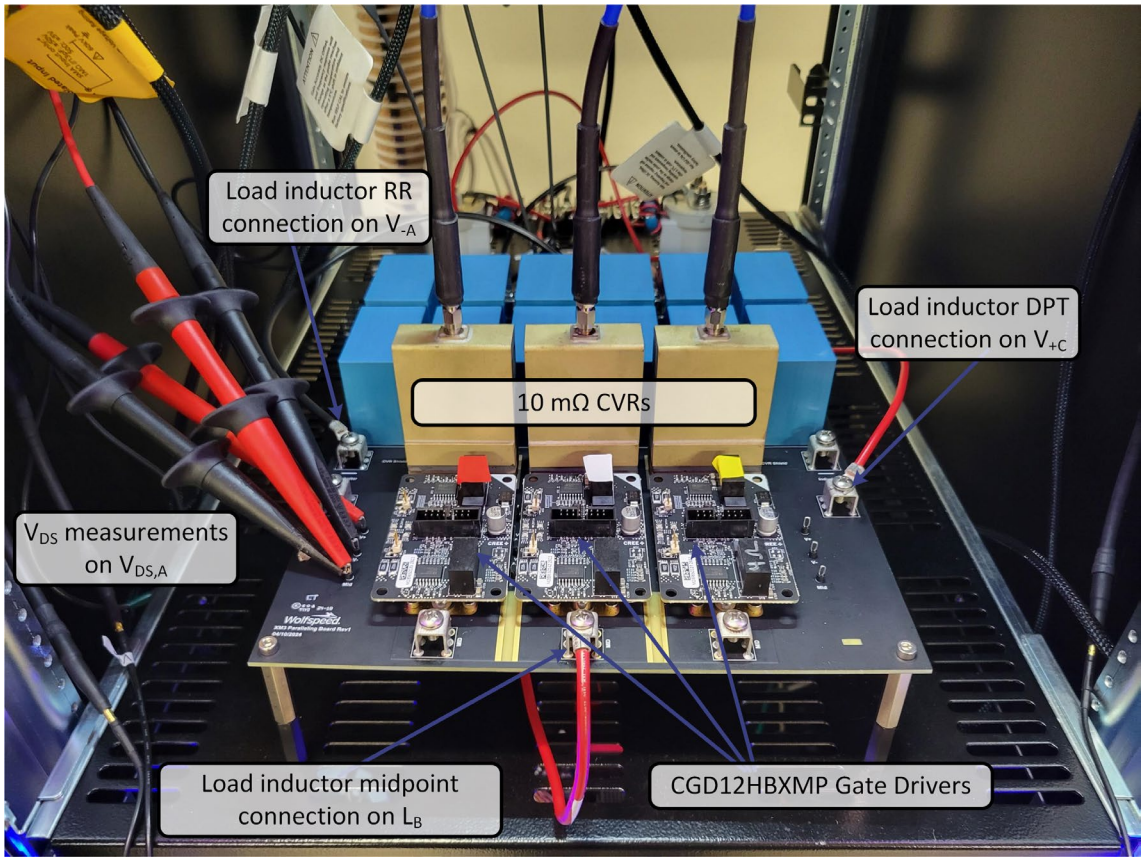


Figure 39: Multiple gate drivers approach for paralleling power modules (PRD-08911)

3.10 Gate Drivers for Elevated Voltages

As SiC semiconductors continue to mature, higher voltage MOSFETs are becoming commercially available, which have already reached mainstream adoption over the last decade. Wolfspeed offers commercially released 2.3 kV and 3.3 kV rated parts, as shown in Figure 40. At these higher voltages, the same best practices should be employed as discussed in this document. However, some of the design requirements are amplified due to the higher voltages. These heightened criteria are listed below.

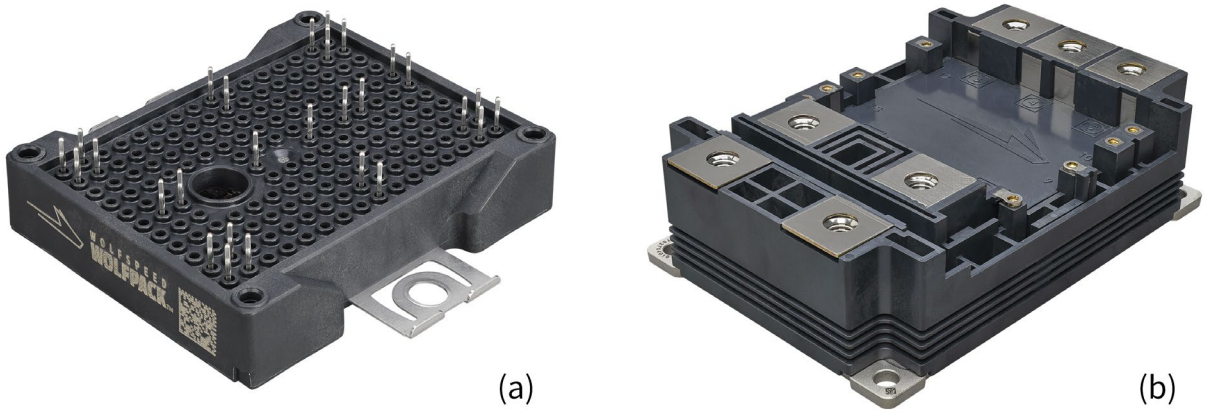


Figure 40: (a) 2.3 kV GM power module and (b) 3.3 kV LM power module

- *Creepage and Clearance.* Higher voltages require greater distances between components and routing to ensure creepage and clearance requirements are followed (see Section 2.7). Additional effort should be made to ensure all suitable regulatory requirements are considered.
- *Noise Immunity*. Higher voltages can create an EMI-rich environment which makes low-voltage signals more susceptible to noise. As voltage increases, single-ended signaling (see Section 4.1) becomes more risk prone due to the elevated noise. At higher voltages, differential signaling (see Section 4.2) becomes necessary to ensure reliable communication and fiber optic signaling (see Section 4.3) becomes more attractive.
- *Component Sourcing.* Fewer gate driver ICs and isolated PSUs are commercially available which support higher voltage operation. This can create challenges when trying to determine multi-sourcing strategies and/or when trying to identify a gate driver IC with a suitable feature-set for a target application.

3.11 Using All Module Gate Pins

Some power modules include multiple gate pin connections for each switch position. One example of this configuration is the CAB006A12GM3T module, shown in Figure 41, which includes two gate pins (and associated Kelvin-source pins) for each switch position. Using multiple gate pins can improve transient current sharing between parallel MOSFETs and reduce gate inductance. Wolfspeed recommends connecting both sets of gate pins to the gate driver circuit. The pins are electrically connected internally, so using both sets of pins is not strictly required. The power module will function using only one set of gate pins, but all Wolfspeed testing and characterization are performed using all sets of pins, so it is recommended to use all sets to match the intended module performance. For optimal performance, the gate driver should attach to the middle of the gate pins. See the KIT-CRD-CIL12N-GMA evaluation board for an example of how to route a gate driver to a module with multiple gate pins.

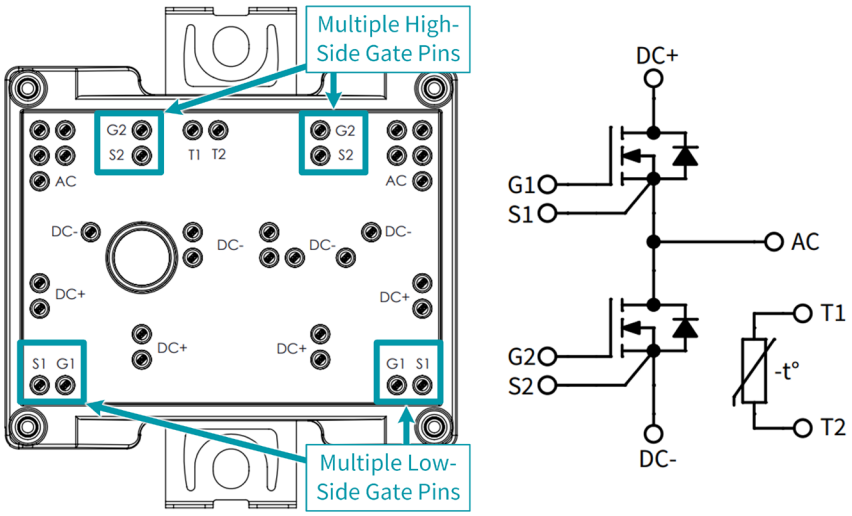


Figure 41: CAB006A12GM3T half-bridge module with multiple gate pins per switch position

4. Noise Immunity

Incorporating the best practices listed in previous sections will limit noise from bridging the isolation barrier and coupling back to the controller. However, all the signaling between the logic-level controller and the gate drivers is still in an EMI-rich environment due to all the *dV/dt* and *di/dt* events occurring in close proximity. This section presents some methods to limit the impact of this noise. A comparison of these methods is summarized in Table 4.

Table 4: Comparison of signal methods between a controller and gate drivers

	Single-Ended	Differential	Fiber-Optic
Noise Rejection	Worst	Neutral	Best
Cost	Best	Neutral	Worst
Complexity	Best	Neutral	Worst

4.1 Single-Ended Signaling

The easiest method for controlling a gate driver is where the controller directly modulates the gate driver IC with a common reference, as shown in Figure 42. This approach, referred to as *Single-Ended Signaling*, requires few components since the controller can be directly tied to the gate driver IC with only minimal filtering. However, this approach can be susceptible to noise over long distances, since this approach requires a stable and consistent reference potential. Performing this single-ended connection over long PCB distances or over a connector/ribbon-cable degrades this reference potential and introduces long leads which can serve as antennas. When requiring gate drive connections in noisy environments or over long distances, it is recommended to use one of the other signaling techniques described in the following sections.

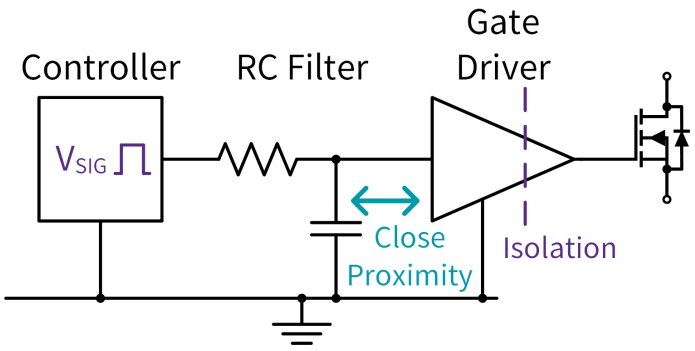
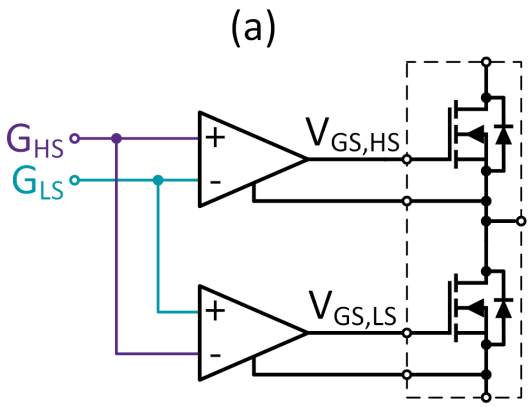


Figure 42: Single-ended signaling with RC filter

In short distances, such as in close proximity on a single PCB, the single-ended approach can be employed successfully. Notably, even in close proximity, there are still best practices to achieve high performance using the single-ended approach. First, it is recommended to drive the signals with a high-drive-capable buffer stage, rather than a low-drive-capable general-purpose input/output pin (GPIO) of a controller. This ensures the gate drive IC can be driven properly. Second, the buffer stage can be used as a step-up logic converter. This enables

operating the gate driver IC at its highest input threshold which improves signal immunity. Third, the signals should all include filtering. This is often accomplished through a simple resistor-capacitor (RC) filter but can be employed with more advanced filters. It is noted that this filter should have a time-constant selected to avoid interfering with the target switching frequencies. These filter requirements are discussed in more detail in Section 4.4.

When using the single-ended approach, if a gate driver includes the functionality, Wolfspeed recommends always incorporating input interlock protection into the gate driver design. This functionality comes in multiple formats, but in general, it means that the gate driver IC has a non-inverting and inverting input (designated + and - in this work). These signals, while not differential, prevent turn on when both gate signals are commanded on simultaneously. This feature is best utilized by attaching both the high- and low-side signals of a MOSFET into both gate drive ICs, as shown in Figure 43(a). This feature works with XOR logic (shown in Figure 43(b)) to prevent both switch positions from being commanded on simultaneously, regardless of whether this commanded signal comes from the controller or from noise propagating through the system.



(b)

G_{HS}	G_{LS}	$V_{GS,HS}$	$V_{GS,LS}$
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

Figure 43: (a) Input interlock protection, and (b) corresponding logic table

In cases where a gate drive IC does not include this functionality by default, designers can add it using a combination of XOR and AND logic gates in the configuration shown notionally in Figure 44. The CGD1700HB3P-HM3 design using this approach for signal interlock protection (see the “Non-Overlap” section of the schematic). This circuit implementation is also shown in Figure 45.

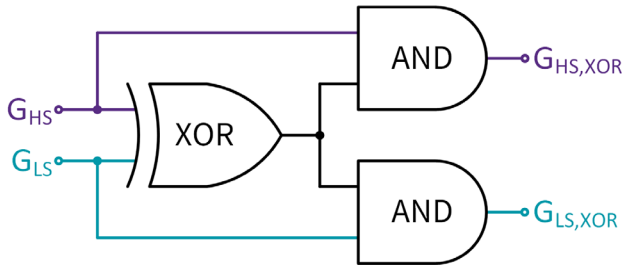


Figure 44: Notional logic gate implementation of input interlock protection

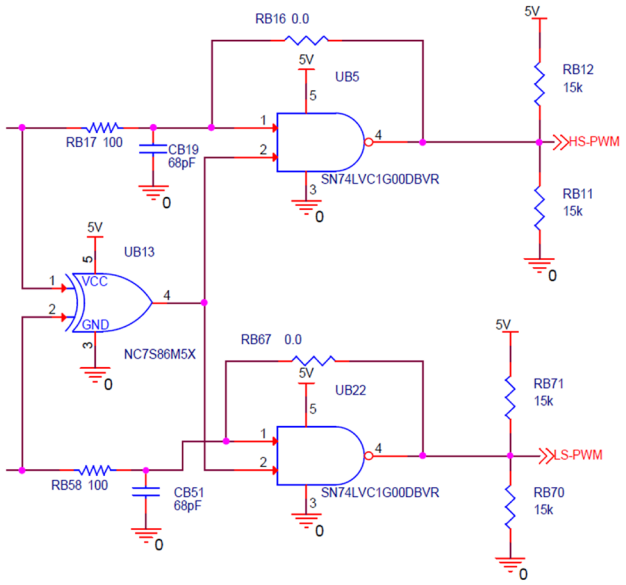


Figure 45: Input interlock protection example on [CGD1700HB3P-HM3]

4.2 Differential Signaling

An improvement over single-ended signaling is to use differential signals, where two connections are dedicated for every signal transmission, as shown in Figure 46. The two signals are transmitted as complementary signals, referred to as V_+ and V_-. When the signals are received, the difference between the two signals (V_+ - V_-) is calculated to determine the intended logic. This behavior is demonstrated notionally in Figure 47. Since the input signals are complementary, when the signal difference is determined, the calculated voltage can be greater than the individual voltages[3].

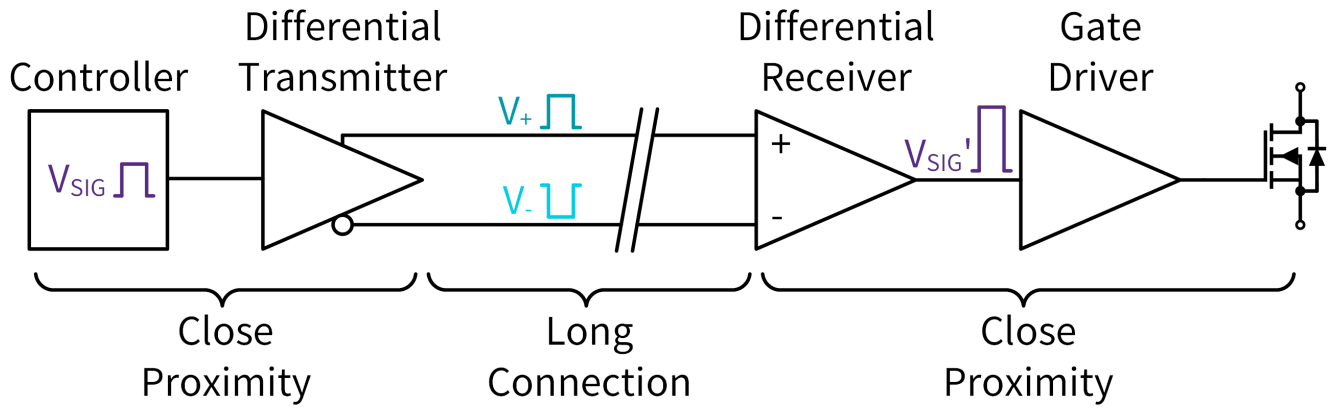


Figure 46: Differential signaling

[3] Many differential receivers cannot use negative voltages. In most of these cases, the differential signals are referenced to $V_{CC}/2$ instead of 0 V or V_{CC}. This configuration results in V_{SIG} of 0 V to V_{CC}, but with increased noise immunity. The concepts discussed in this section still apply to these ICs, though the implementation is different. Refer to the relevant differential transceiver datasheet for exact details about its implementation.

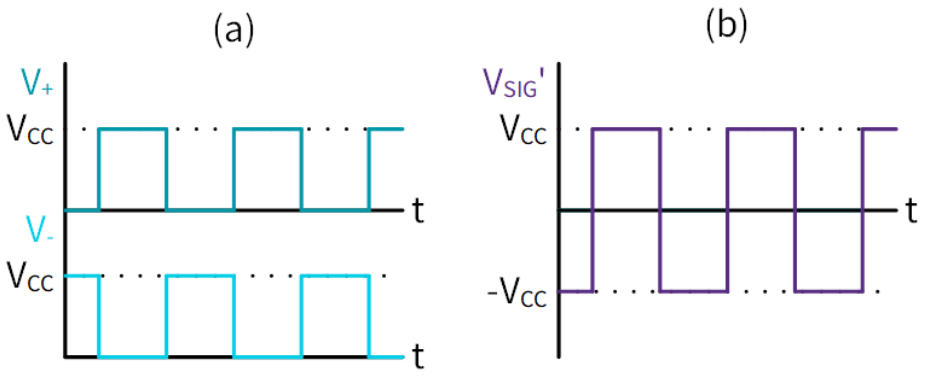


Figure 47: Differential signaling (a) transmission signals and (b) corresponding received signal

While the potential for increased dynamic range can make differential signaling attractive, a more prominent benefit involves the ability to reject noise. On a PCB, differential signals should always be routed directly adjacent to each other, and in cables, Wolfspeed always recommends using twisted pair cables. By having the signals always in proximity to each other, most noise sources will influence both signals equally. This behavior is shown notionally in Figure 48(a), which has the same transmission signals as Figure 47(a) with injected noise. Since the received signal, V_{SIG}', is the difference between the two transmissions, the noise does not influence the final signal, as shown in Figure 48(b). Notably, once the differential signal is received, it is converted to a single-ended signal to be used by the gate driver. This single-ended signal is susceptible to all the vulnerabilities discussed in Section 4.1. Therefore, when adopting differential signaling, it is essential that all long connections are performed with differential signaling, and the single-ended conversion is performed close to the gate driver circuit to minimize susceptibility (as shown in Figure 46).

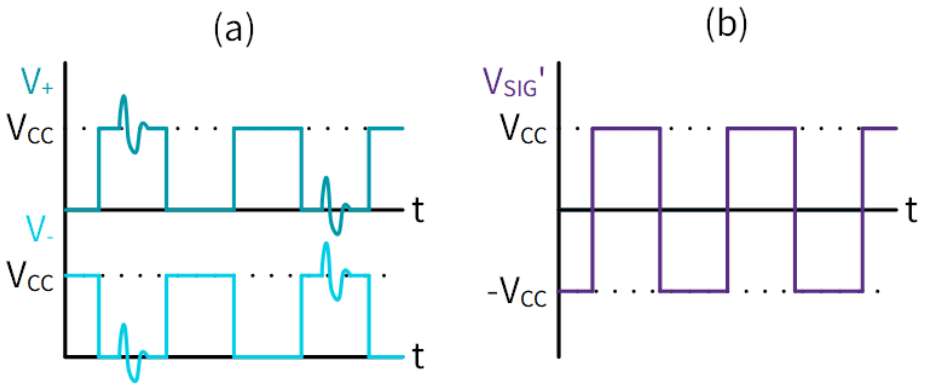


Figure 48: Differential signaling (a) transmission signals with noise and (b) corresponding received signal

4.3 Fiber Optic Signaling

To achieve the highest level of noise immunity, systems should utilize fiber optics for transmitting signals from the controller to the gate driver(s). This strategy, shown in Figure 49, lets the controller be placed physically far from the gate driver and potentially noisy environment, since the fiber optics create a near-perfect isolation barrier to prevent CM emissions from coupling to the logic-level controller. Though the notional diagram only demonstrates fiber signals from the controller to the gate driver, feedback signals from the gate driver to the

controller can also utilize fiber transmission. Similar to differential signaling, even with the near perfect noise immunity of fiber cables, the signal must eventually be converted back to a single-ended signal for the gate driver IC. It is important that this single-ended signal is as short as possible to avoid its susceptibility to noise. Any long-distance connections should be included in the fiber cable section of Figure 49.

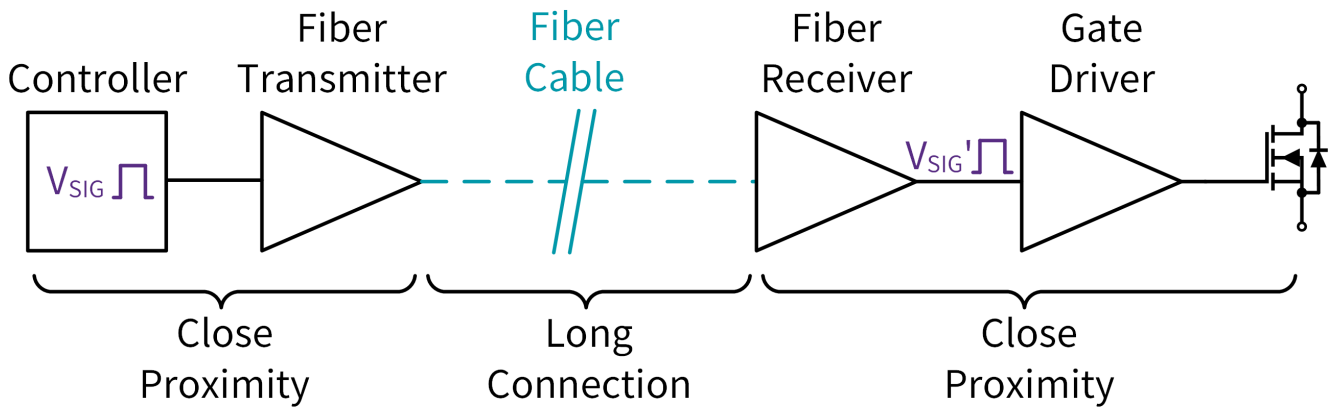


Figure 49: Fiber optic signaling

Though fiber optic signaling is the best strategy for systems requiring high noise immunity and isolation, there are several trade-offs which prevent fiber optic solutions from being adopted outside of extreme high-performance systems. Some of the disadvantages to fiber optic solutions for gate driver communications are listed below.

High Cost. Fiber cables are significantly more expensive than copper wires, even compared to twisted pair cables. Additionally, the fiber signals must be converted to and from electrical signals, requiring fiber transceivers in these conversion locations. In many cases, a fiber transceiver can be the most expensive BOM element on a circuit board, and a gate driver board will often need multiple of them. In addition to PWM signals to control the gate driver, control/feedback signals (RESET, ENABLE, NTC, FAULT, etc.) will require additional fiber cables and transceivers. While upgrading from single-ended to differential signaling introduces a marginal cost increase, upgrading from differential to fiber optic introduces a significant cost increase.

Physically Large. Fiber transceivers must mate/attach to fiber cables (which are made from flexible glass). These cables generally have a larger diameter than logic-level carrying electrical wire. The larger diameter means that fiber transceivers are often physically large, requiring larger PCB dimensions to support the transceivers. Figure 50 shows an example gate driver implementation using optical transceivers on the LM power module [1].

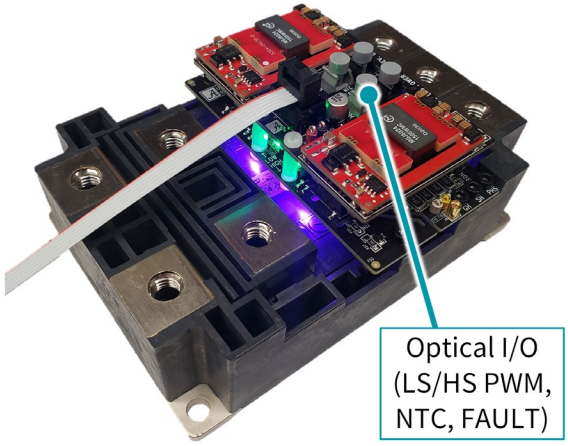


Figure 50: Example of physically large fiber transceiver requirements [1]

Difficult Wire Routing. Fiber cables have strict bend restrictions on cables and are less flexible than electrical wires. This can make cable routes difficult when avoiding violation of these bend restrictions. Additionally, the often-larger diameter of fiber cables compared to electrical wires, further restricts the flexibility and the ability to route fiber cables.

Power Circuit Vulnerability. Though fiber optics provide an optimal isolation barrier for the logic-level signals to the gate driver, electrical noise can still couple across the isolation barrier through the isolated power supply[4]. Simply converting logic-level signals to fiber optics is not a universal fix for issues, since leakage paths still exist in the circuit. It should be noted that this should not deter adoption of fiber optics, since converting logic-level signals to fiber can introduce significant noise immunity improvements; designers should simply be aware that other potentially problematic paths still exist.

Generally, for systems with bus voltages less than 2 kV, Wolfspeed recommends adopting differential signaling over fiber optic solutions for a balance between high noise immunity and cost. Most Wolfspeed gate drivers, such as the CGD1700HB2M-UNA, adopt differential signaling.

4.4 Signal Filtering

Even in systems adopting differential or fiber optic protection, it is important to recognize that gate drivers are often operating in EMI-rich environments due to the high *dV/dt* and *di/dt* events. For this reason, Wolfspeed always recommends using RC filters on all the signals to limit spurious noise. These RC filters should have short time constants to avoid interfering with the rise/fall times of the control signals and should be placed as close as possible to receiving circuit elements, as shown in Figure 42. In addition to the gate control signals, Wolfspeed recommends adding RC filters to all the control signals to and from the gate driver such as reset and fault signals. An example implementation of some of this filtering is shown in Figure 51 from the CGD1700HB2M-UNA gate driver.

[4] There is ongoing research to develop power-over-fiber (PoF) for gate drivers, specifically in >10 kV applications. When paired with fiber logic-level signaling, PoF would create a near-perfect isolation barrier to the gate driver circuit. However, current designs need to achieve higher efficiency, higher output power, and lower cost to be practical.

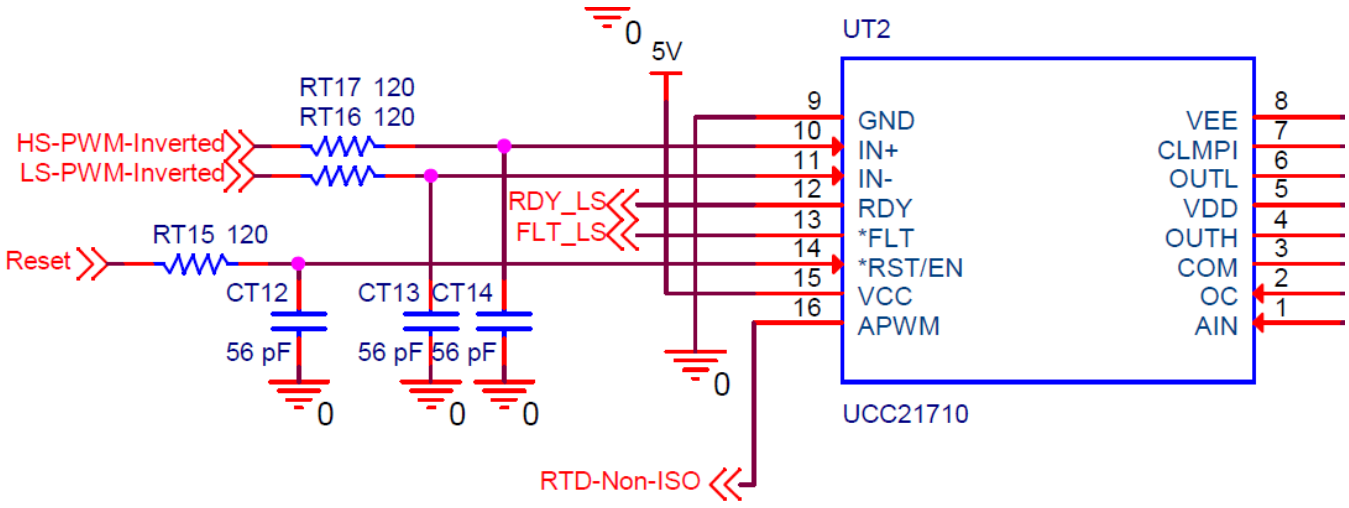


Figure 51: RC filtering example implementation on CGD1700HB2M-UNA

4.5 Signal Isolation

As discussed in Sections 1.2 and 2.1, it is critical for gate driver ICs to include an isolation barrier in most applications. Internally, gate driver ICs can create this isolation barrier using a variety of different methods. This section details the common isolation approaches and the associated high-level trade-offs of each technology type, which are summarized in Table 5. These trade-offs are general in nature and thus may not apply to all gate driver ICs that adopt these technology types. Wolfspeed recommends referring to the gate driver IC datasheet for the specifics of the isolation type and its performance ratings.

Table 5: Trade-offs of different isolation types

Isolation	Advantages	Disadvantages
Capacitive	Very fast; Small propagation delay	Concern in high electric field applications; Not suitable for analog signals
Magnetic	Mature technology; Can also transfer power	Concern in high magnetic field applications; Relatively bulky
Optical	Highest isolation	Slower; Limited bandwidth; Potential photo gain deterioration & temp. sensitivity

4.5.1 Capacitive Isolation

In this approach, shown in Figure 52, signals are transmitted through capacitive coupling across a dielectric. The input signal is modulated and transferred across the isolation barrier and then demodulated on the receiving side. This approach can achieve very low propagation delay and transmit at a very high rate. Capacitive isolation is generally the least expensive isolation type and can be made very small. However, it does not work with analog signals and power cannot be transferred across the isolation barrier, so this isolation requires a separate bias voltage on both sides of the barrier.

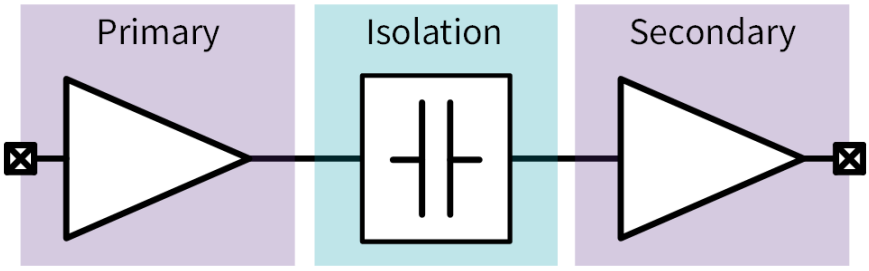


Figure 52: Capacitive isolation

4.5.2 Magnetic Isolation

In this approach, shown in Figure 53, signals are transmitted through magnetic coupling across a high-frequency transformer to provide isolation. Along with transmitting the data, the transformer can also be used to transfer small amounts of power, eliminating the need for a secondary-side bias voltage like the other topologies. This type of isolation is very mature, but can be bulky in comparison to capacitive isolation.

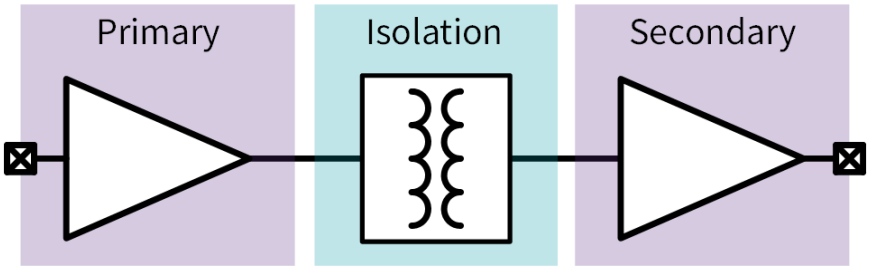


Figure 53: Magnetic isolation

4.5.3 Optical Isolation

In this approach, shown in Figure 54, LEDs transmit light through an insulating material to receiving photodiodes or phototransistors. This approach is the same as the fiber optical signaling discussed in Section 4.3, except the transmitter, signal medium, and receiver are all contained within the same IC. Optical isolation can typically achieve the highest isolation rating since no electrical signals cross the barrier, and the LED-receiver combination can be placed physically far apart. However, the switching speeds and forward bias requirements of LEDs along with their requirement for driving circuitry limit their maximum speed. Furthermore, these isolators are known to degrade over time, and these isolators require separate bias supply voltages on the primary and secondary sides.

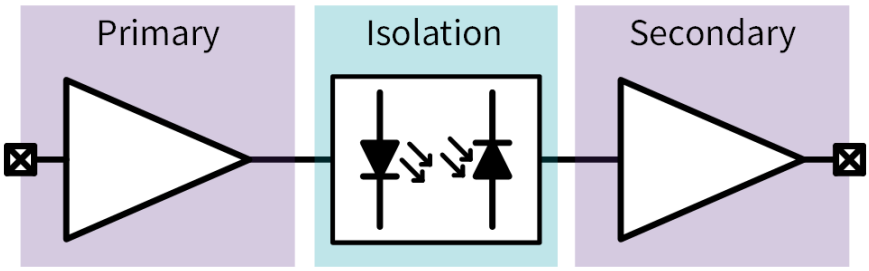


Figure 54: Optical isolation (could use other receiving elements such as phototransistor)

5. Protection

Many potential gate driver issues can be mitigated by implementing the guidance outlined in this document. However, even when considering all these best practices, fault conditions can still occur when the gate driver is integrated into a system. Often these issues arise due to other parts of the system such as a short-circuit event occurring on the output of a converter, insufficient power to operate the gate driver, or poor controller operation. This section details some of the features that can be added to a gate driver to protect from some of these external failure conditions.

5.1 Overcurrent

The most catastrophic fault condition is an overcurrent event which typically occurs in one of two ways: (1) both switch positions in a half-bridge are commanded on simultaneously which creates a short circuit across the full bus voltage, referred to as a "shoot-through" event (shown in Figure 55(a)); (2) the circuit load is shorted to one of the power rails, bypassing one of the switch positions and causing a short-circuit event when the other switch is activated (shown in Figure 55(b)). The risk of the first fault condition can be significantly reduced by adopting *Input Interlock* protection (see Section 5.6) and deadtime (see Section 5.7). In either of these fault events, one or both switch positions will conduct current well beyond their rated value until the MOSFET(s) fails due to thermal overload. For more information about short circuit events in power MOSFETs, refer to PRD-08296. To prevent this issue, a gate driver should include overcurrent detection to safely turn off the device(s) if an overcurrent event is detected.

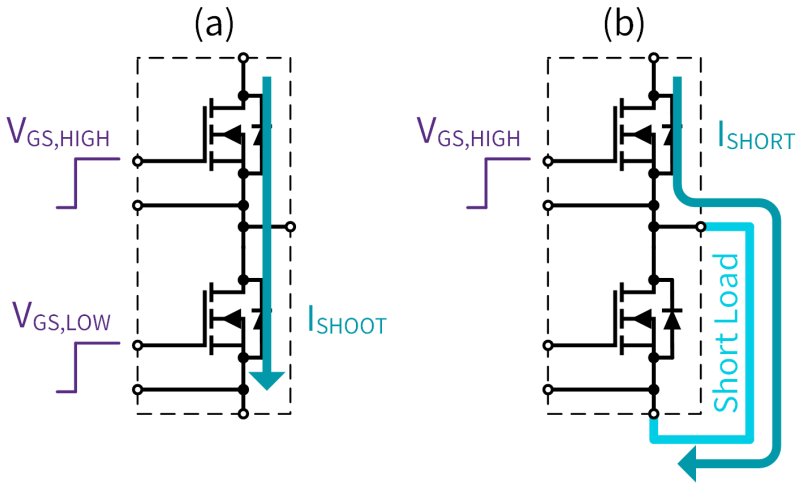


Figure 55: Overcurrent events due to (a) shoot through and (b) shorted load

Considering the low on-state resistance ($R_{DS,ON}$) of SiC MOSFETs, shorting the device can result in significant current conducting through the device and causing device failure in only a few microseconds. Thus, the overcurrent protection circuit must be able to perform detection and shut down the device faster than the potential device failure time. Relying on a controller to read a current sensor using an ADC register requires too many controller clock cycles to be relied upon for this protection. For low-power systems, current viewing resistors (CVRs) can be employed for overcurrent detection by configuring a comparator to trigger if the CVR voltage exceeds a predetermined threshold. However, this measurement requires placing a resistor directly in

the power loop. This approach therefore only works in extremely low power systems, since the resistive losses are too great in power module applications which require high currents to conduct through the CVR, leading to high losses.

For power modules, Wolfspeed recommends using a desaturation circuit, or DESAT circuit, for overcurrent protection of power modules. The generic DESAT circuit, shown in Figure 56, works in three states, described below.

MOSFET Gated Off. When the MOSFET is gated off, the DESAT circuit is disabled by shorting the overcurrent circuit to the Kelvin-source of the MOSFET. During this time, the high-voltage diode(s) block the full operating voltage, so the diode(s) must have a voltage rating equal to or greater than the MOSFET. In many cases, to achieve a higher voltage rating or to ease routing with large creepage and clearance constraints, multiple series-connected high-voltage diodes are employed in DESAT circuits. The high-voltage diodes should be selected to have a fast response time in order to minimize the influence on the detection circuit. This DESAT state is shown in Figure 57(a).

MOSFET Gated On Without Overcurrent. When the MOSFET is gated on, the high voltage blocking diodes are forward biased and current flows from V_{DD} of the gate driver through the bias circuit, blocking diodes, and MOSFET as shown in Figure 57(b). A fully turned-on MOSFET can be approximated as an equivalent resistor. The bias circuit is designed such that in normal operation the MOSFET equivalent resistor will never develop a large enough voltage drop to engage any of the overcurrent detection circuitry.

MOSFET Gated On With Overcurrent. If an overcurrent event does occur while the MOSFET is gated on, the MOSFET equivalent resistance develops a voltage greater than the predefined threshold. The threshold is configured by adjusting the filter circuit, and overcurrent threshold voltage. Once the threshold is exceeded, the DESAT circuit immediately begins to turn off the MOSFET. Typically, the MOSFET is gated off until a controller resets the circuit or the source of the overcurrent causing problem is identified. This DESAT state is shown in Figure 58(a). A notional timing diagram of the DESAT overcurrent fault is shown in Figure 58(b). In the diagram, the MOSFET starts as gated on and enters the *MOSFET Gated On Without Overcurrent* state. While the MOSFET is on, a short circuit event occurs. This could be due to the complementary switch position also turning on or due to the circuit load creating a short circuit. Due to the elevated current, the measured drain-to-source voltage (V_{DS}) begins to increase, causing the overcurrent voltage (V_{OC}) to increase. Both V_{DS} and V_{OC} continue to increase until V_{OC} exceeds the detection voltage, V_{DET}, at which point the DESAT control engages the turn-off resistor to gate the MOSFET off until the fault is identified, and the gate driver is reset. For diagram simplicity, this notional diagram uses a hard shutdown approach when the fault is detected; however, Wolfspeed recommends adopting soft shutdown (see Section 5.2) in an end application.

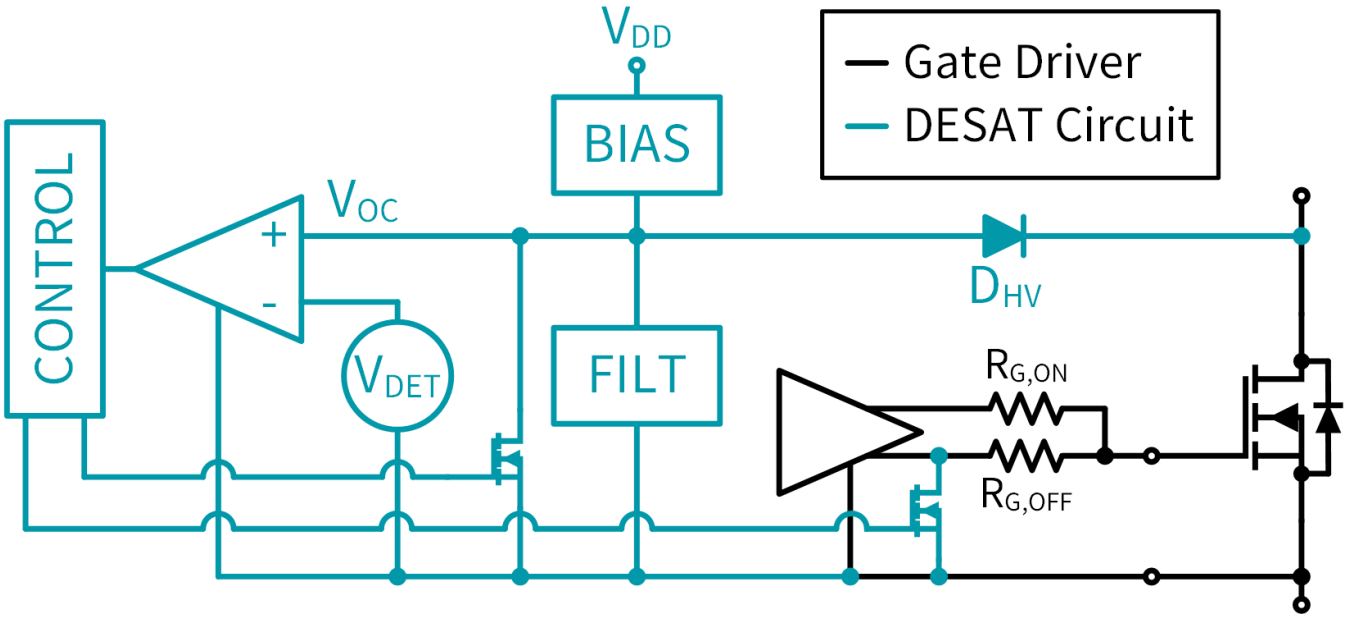


Figure 56: Notional DESAT circuit

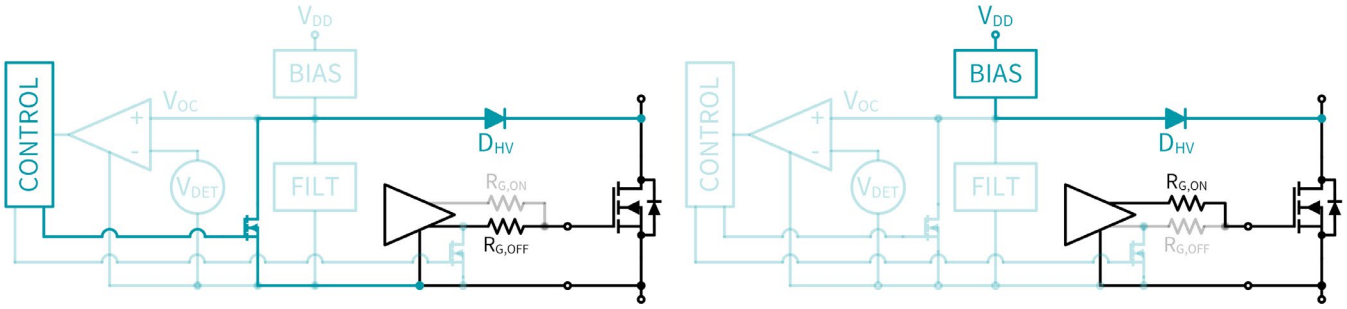


Figure 57: DESAT circuit in (a) off state and (b) on state without overcurrent

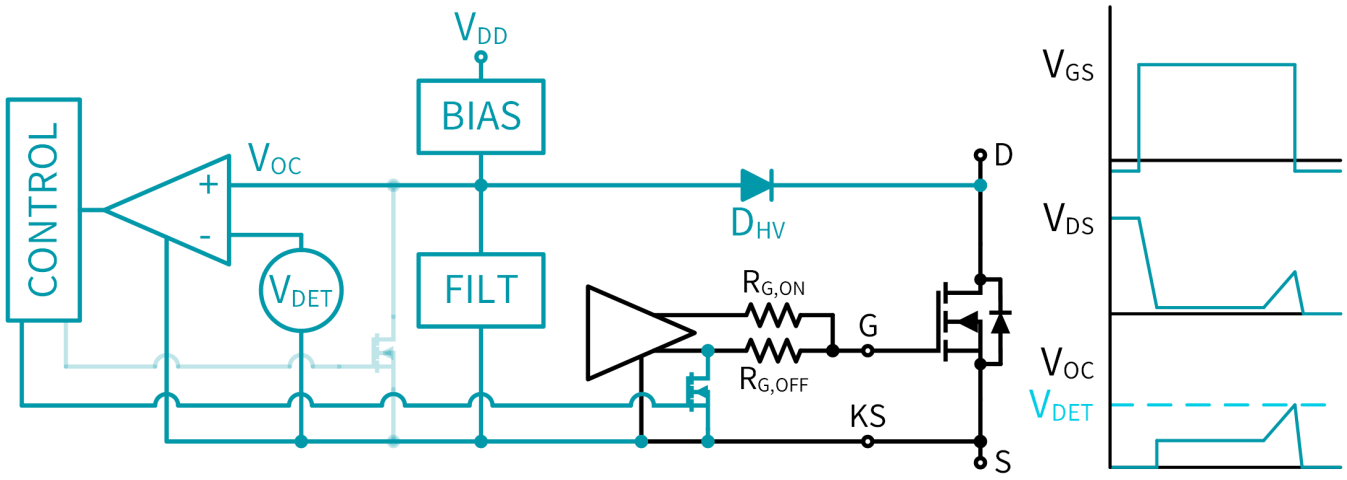


Figure 58: (a) DESAT circuit in turn-on state with overcurrent, and (b) associated notional timing diagram

Different gate driver ICs will implement the DESAT circuit in various ways, so it is important to consult the datasheet of the specific gate driver IC adopted for the exact DESAT configuration. Notable variations include integrated vs external bias circuits and differing threshold voltages. The primary impactful parameters that are available to circuit designers on all gate driver circuits are the blanking time and overcurrent trip value. Both of these parameters can be modified by the designer and are discussed in more detail below.

Blanking Time. When a power MOSFET switches between on and off, each transition introduces some ringing into the system. Through a good power stage layout, this ringing can be minimized, though some ringing is unavoidable when operating the MOSFET(s) in a high-performance application requiring fast slew rates. Since the DESAT circuit is directly attached to the MOSFET drain terminal through the high voltage diodes, this ringing can easily couple into the DESAT circuit, leading to false overcurrent triggers. To prevent these false trips, the *Filter Circuit* includes an RC filter with a tunable blanking capacitor. This capacitor serves as a filter element which can be sized to prevent ringing from influencing the DESAT measurement for a configurable duration. Fundamentally, sizing the blanking capacitor requires a tradeoff between the risk of a false trip and the delay introduced into the overcurrent detection circuit. A larger blanking capacitor ensures that all ringing dynamics are cleared before beginning the overcurrent detection, but the larger capacitor means that a short circuit event could be occurring for the entire extended blanking time before the shutdown procedure begins. This could result in the MOSFET(s) being required to dissipate significant energy during an overcurrent event and may result in a device failure due to a slow response time by the overcurrent detection circuit. In contrast, a small blanking time ensures that the DESAT circuit reacts quickly to any detected fault, ensuring the MOSFET(s) remain usable after the overcurrent event. However, the short blanking time may cause the DESAT circuit to falsely trip due to any extended ringing dynamics. The best approach to sizing blanking capacitors is to do the following. First, identify the risk tolerance of faults versus false trips. A risk-adverse system which can be easily maintained/serviced will likely be more amendable to a short blanking time. A system which requires extended uptime will likely require a longer blanking time. Second, with an understanding of the risk tolerance, measure the system dynamics in circuit and add additional blanking time margin based on the risk level. For reference, the low-side DESAT circuit implementation on the CGD1700HB2M-UNA gate driver is shown in Figure 59.

Overcurrent Trip Value. The overcurrent trip value is set by the combination of the bias circuit, high-voltage diodes, power module on-state resistance, and the comparator trip voltage of the gate driver circuit. The exact way to configure the circuit is generally provided in the datasheet for the gate driver IC. The foremost value in these calculations is the target current which triggers an overcurrent event. Similar to the blanking time, setting a value too low can cause false overcurrent faults while setting the value too high delays the response time of the circuit to actual fault conditions. Additionally, the MOSFET on-state resistance – which is used as a current viewing resistor to identify an overcurrent event – has dependence on operating temperature. It is therefore often difficult to fine-tune the trip value to a precise current and a higher overcurrent trip value must be selected. Once the MOSFET overcurrent target trip value is identified, the remaining circuit elements are employed to bias the circuit such that the corresponding V_{OC} voltage is equal to V_{DET} at the right operating conditions. For this to work, the forward voltage drop of the high-voltage diodes must be considered. Additionally, some

designs include tunable components in series to easily modify the trip value. For example, the CGD12HBXMP gate driver employes a tunable Zener diode to allow the trip value to be easily changed.

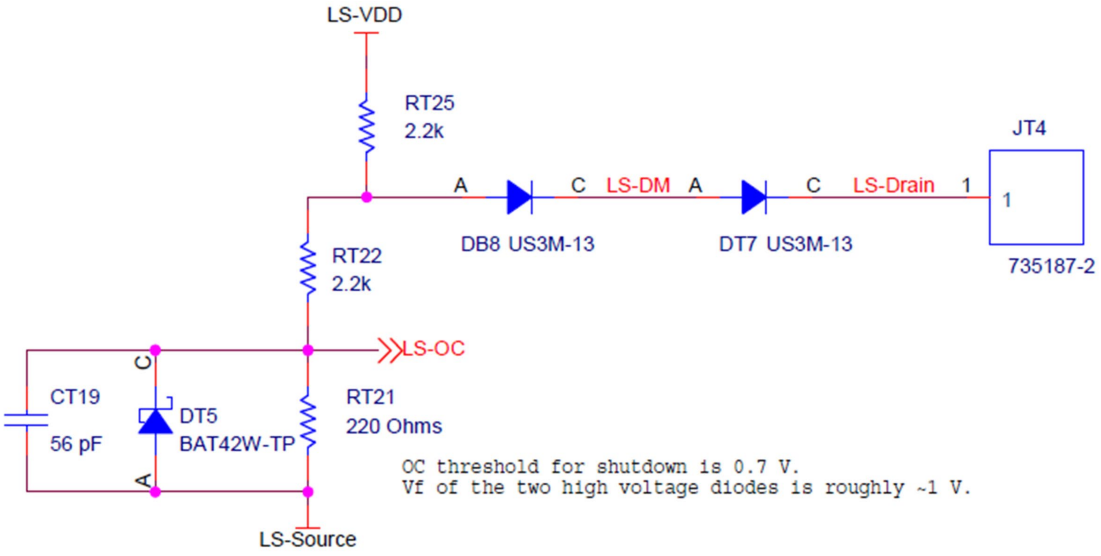


Figure 59: Low-side DESAT implementation on the CGD1700HB2M-UNA gate driver

5.2 Soft Shutdown

In some short circuit fault conditions, the MOSFET(s) conducts extremely high current levels (several kiloamperes), which can introduce a significant voltage overshoot when the MOSFET(s) is quickly turned off using normal turn-off resistors. This hard shutdown effect is demonstrated on a 1200 V-rated part in Figure 60. To reduce the drain-to-source voltage overshoot, some gate drivers introduce a soft shutdown (also referred to as soft turn off) feature which introduces circuitry to limit the turn-off *di/dt* through the device. Typical approaches for limiting the turn-off *di/dt* include the following.

Current Source. The gate driver connects a fixed current source between the MOSFET gate and the turn-off voltage rail of the gate driver, as shown in Figure 61(a). The current source limits how quickly the device turns off, thus limiting the *di/dt* and subsequent voltage overshoot. Gate drivers such as the Texas Instruments® UCC21710 employ this strategy, which uses a nominal 400 mA current source.

High Resistance MOSFET. The gate driver connects the MOSFET gate to the turn-off voltage rail of the gate driver through a high-resistance MOSFET, as shown in Figure 61(b). Similar to the current source approach, the higher resistance slows the turn-off dynamics of the power device, thus limiting voltage overshoot. Gate drivers such as the Analog Devices® ADuM4135 employ this strategy, which uses a soft shutdown MOSFET with approximately 35 times higher resistance than the typical turn-off MOSFET.

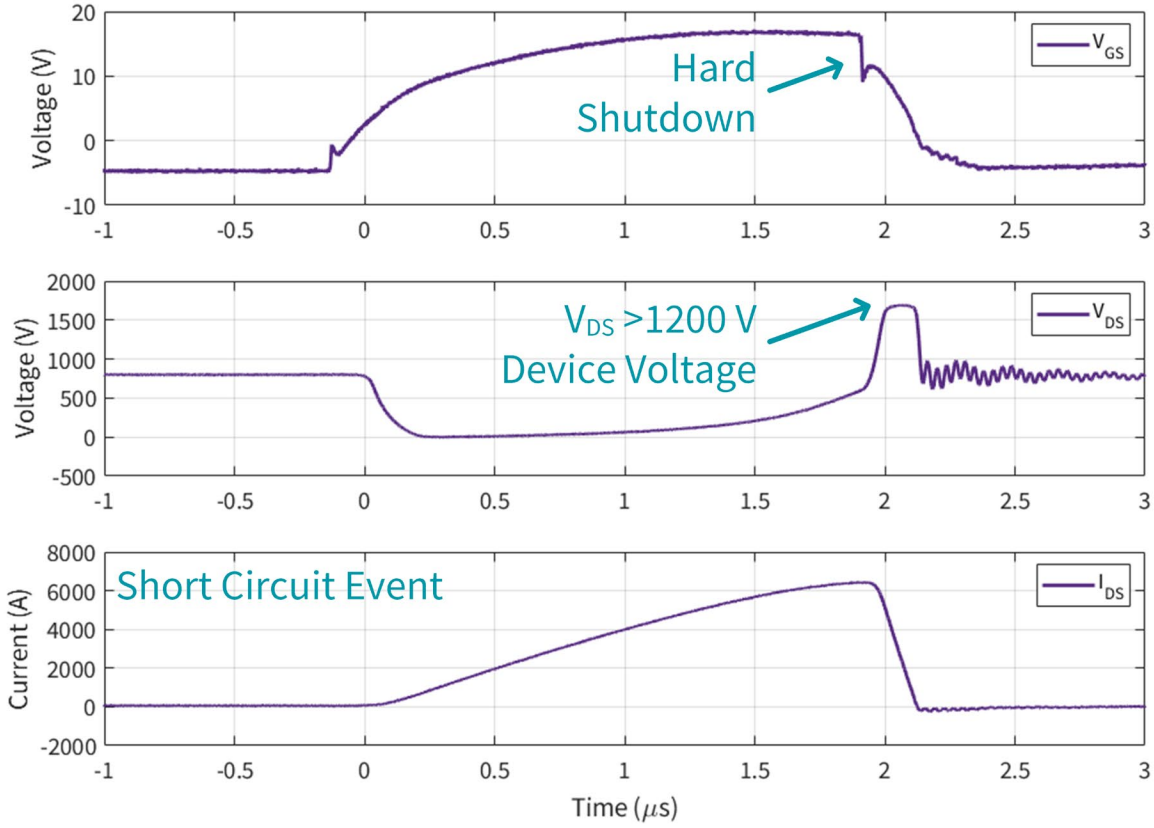


Figure 60: High drain-to-source voltage after short circuit hard shutdown

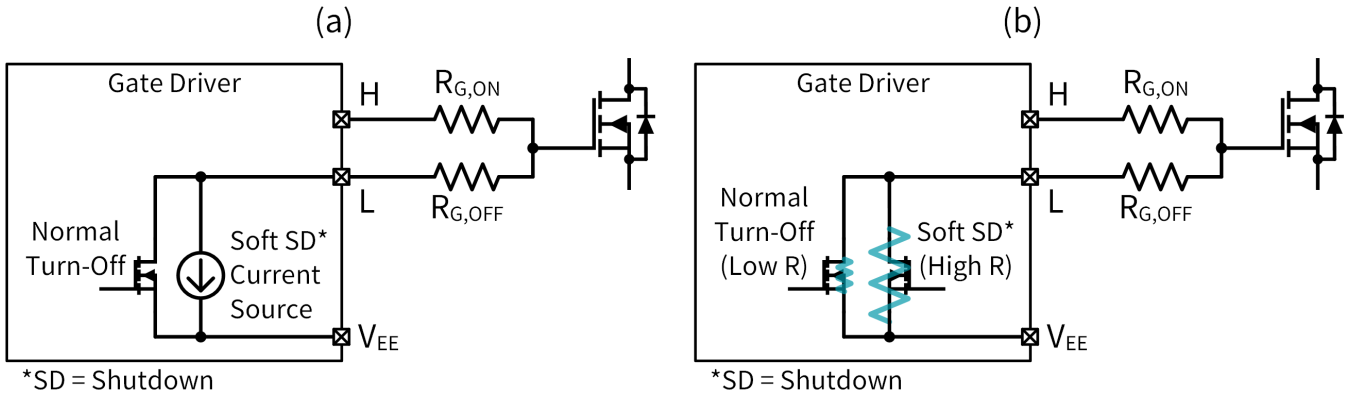


Figure 61: Soft shutdown implemented with (a) current source and (b) high resistance MOSFET

The soft shutdown features are only engaged during an overcurrent event (see Section 5.1), not during typical operation. Additionally, these soft shutdown features can also be employed outside of the gate driver IC. However, it is easier to select a gate driver IC which already includes these features, since separate soft shutdown circuitry would also have to be linked with the DESAT overcurrent detection circuitry.

5.3 Two-Level Turn Off (Not Recommended)

An alternative (not recommended) approach to turning off a MOSFET during a short circuit event is to perform two-level turn off. This feature performs a staggered turn-off procedure when an overcurrent fault is detected. In the two-level turn off approach, an intermediate voltage rail is introduced between V_{DD} and V_{EE}, enabling the gate driver to first reduce the gate voltage to the intermediate voltage before fully gating the device off. The reduced gate voltage is expected to reduce the current flow through the channel of the power MOSFET(s) and reduce the V_{DS} overshoot when the device is fully turned off. Figure 62 shows the measured gate voltage of an XM3 power module when two-level turn off is employed during a short circuit event. Though the benefits of two-level turn off appear attractive, Wolfspeed does not recommend employing two-level turn off with power modules. Two-level turn off puts extreme stress on individual cells of the MOSFET(s) during the short circuit event (Spirito Effect) and can force significant short circuit energy to be dissipated by the power module, far in excess of the recommended amounts.

Figure 62: Example two-level turn off (not recommended)

5.4 Gate to Kelvin-Source Overvoltage Clamp

To protect the gate of the MOSFET from overvoltage transients – which can degrade the expected lifetime of the MOSFET – some designers include a Zener diode attached from the gate to the Kelvin-source of the MOSFET, as shown in Figure 63. The intent is for the Zener diode to clamp overvoltage transients observed on the gate of the MOSET. However, Zener diodes often respond too slowly to adequately protect the MOSFET gate during fast transient conditions. In addition, there is non-negligible inductance between the internal power module die and the protective Zener diode – even when the Zener diode is placed close to the terminals of the power module – so the Zener diode is often too decoupled from the dynamics at the die level to provide suitable

protection. Zener diode clamps are therefore generally only considered useful for clamping steady-state issues. Wolfspeed recommends focusing on developing robust gate driver power rails to ensure consistent steady-state gate voltages rather than relying on a Zener diode for this protection. Therefore, Wolfspeed does not include the Zener diode clamp in any power module gate drivers.

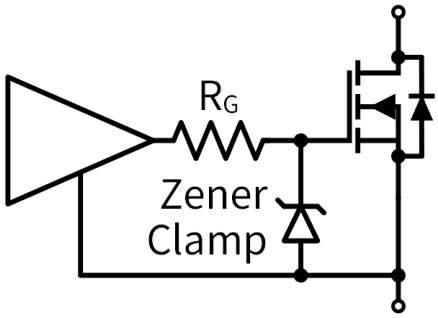


Figure 63: Gate to Kelvin-source overvoltage clamp

5.5 Undervoltage Lockout

When a gate driver PSU is not operating correctly, the gate driver output voltage can be limited from reaching its full dynamic range. This could happen due to a variety of reasons such as failure of the PSU, overload of the PSU, or insufficient input voltage. When the PSU is not operating as intended, it can cause multiple issues in the power stage including but not limited to the following.

- Reduced magnitude in the turn-off voltage can cause the turn-off voltage rail to be closer to the MOSFET threshold voltage, which makes the device more susceptible to unintended turn-on events
- Reduced magnitude in the turn-on or turn-off voltage can slow the device slew rates, leading to increased switching losses and therefore increased operating temperature
- Reduced turn-on voltage can cause the device to operate in the linear operating region, which could increase power losses considerably and is not recommended
- Reduced turn-on voltage could prevent a device from turning on when intended which could be detrimental to system operation in several topologies such as ones that require reverse conduction through the MOSFET to limit body diode conduction

To prevent system failures due to gate driver output voltage issues, it is recommended that all gate driver circuits include circuitry to identify if there are issues with the input and output power rails. This circuit, typically referred to as undervoltage lockout (UVLO), is included in many commercially-available gate driver ICs. Though the exact implementation may vary, most gate driver UVLO circuits operate as follows. When a UVLO fault is detected, the gate driver IC stops modulating the switch position and transmits a fault signal back to the controller. The gate driver IC either begins modulating again once the fault is cleared or waits for the controller to reset the circuit before resuming operation. Gate driver ICs either have fixed UVLO thresholds or have configurable thresholds. In cases where the gate driver IC does not include UVLO or if its configuration is not suitable, the functionality can be achieved using a comparator circuit. The CGD1700HB3P-HM3 gate driver demonstrates UVLO implemented using a comparator circuit (shown for the high-side in Figure 64).

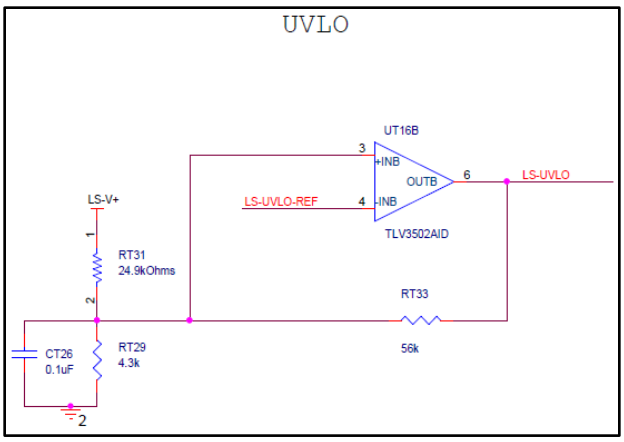


Figure 64: High-side undervoltage lockout implementation in CGD1700HB3P-HM3 gate driver

In many systems, it is advantageous to combine the overcurrent fault with the UVLO fault and any other fault signals present on a gate driver. A single unified fault signal can be transmitted back to a controller, only requiring a single connection (could be single ended, differential, or fiber optic). This approach is employed on the CGD1700HB2M-UNA gate driver. The relevant circuitry is shown in Figure 65 where the *RDY_xS* signals represent the UVLO signals and the *FLT_xS* signals represent the overcurrent faults. Both the high- and low-side signals are combined into a single global fault signal.

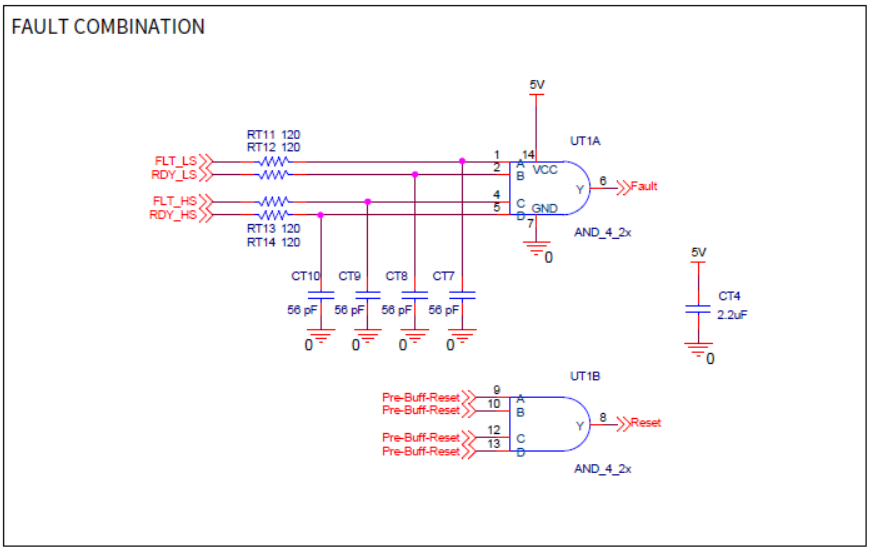


Figure 65: Example combining fault signals on CGD1700HB2M-UNA gate driver

5.6 Input Interlock

When adopting single-ended, differential, or fiber optic signaling, the signals will eventually be converted to single-ended to be routed into the gate driver IC. As discussed in the differential and fiber optic sections (Section 4.2 and Section 4.3, respectively), this conversation to single-ended should occur as close as possible to the gate driver IC in order to reduce noise susceptibility introduced by single-ended signaling. When the signals are converted to single ended, both the high- and low-side signals should be configured in an interlocked approach. The interlock protection applies an XOR logic gate to the two input signals, preventing the output from going

high if both signals are commanded on simultaneously, as shown in Figure 43. This can be used as a preventative measure to eliminate the risk of a controller commanding both switch positions of a half-bridge to be on at the same time. Interlock protection also helps further with noise immunity, since it prevents potential catastrophic failure if noise flips one of the commanded signals. It is important to note that this protection will save the power electronics from immediate catastrophic failure, but it will cause the system to not be conducting current when expected. This could still be problematic in circuits which rely on timely conduction, such as circuits using reverse channel conduction to limit body diode conduction. Therefore, input interlock protection should not be relied upon in normal operation outside of rare erroneous conditions; all efforts and best practices should still be employed to ensure the controller never commands both switches on simultaneously and to reduce noise susceptibility in the signal chain. For gate drivers that support interlock protection by default, the high and low input signals can be connected directly to the inputs of the gate driver IC, as shown in Figure 43. If a gate driver IC does not include interlock protection, designers can add the functionality using AND and XOR gates, as shown in Figure 44. This alternative approach was adopted for interlock protection on the CGD1700HB3P-HM3 gate driver design (see the "Non-Overlap" section of the schematic).

5.7 Deadtime Generation/Enforcement

Though SiC MOSFETs switch significantly faster than similar Si-based semiconductors, the devices still have non-instantaneous switch dynamics. As a switch position (e.g. high-side position) transitions from a turn-on state to turn off, the device will be in the transition time for a short duration. While this transition occurs, it is essential that the other switch position (e.g. low-side position) remains off. If the low-side position begins to turn on during the transition state of the high-side position, the devices will begin to conduct significant current through MOSFETs. This overlap of transitions can degrade the lifetime of the device, increase system losses, require a larger cooling solution, or lead to a catastrophic shoot-through event (see Section 5.1). To avoid this overlap, a short duration is introduced – referred to as "deadtime" – between when the complementary switch positions are commanded to switch states. The introduced deadtime delay is shown notionally in Figure 66 for the low-side and high-side gates.

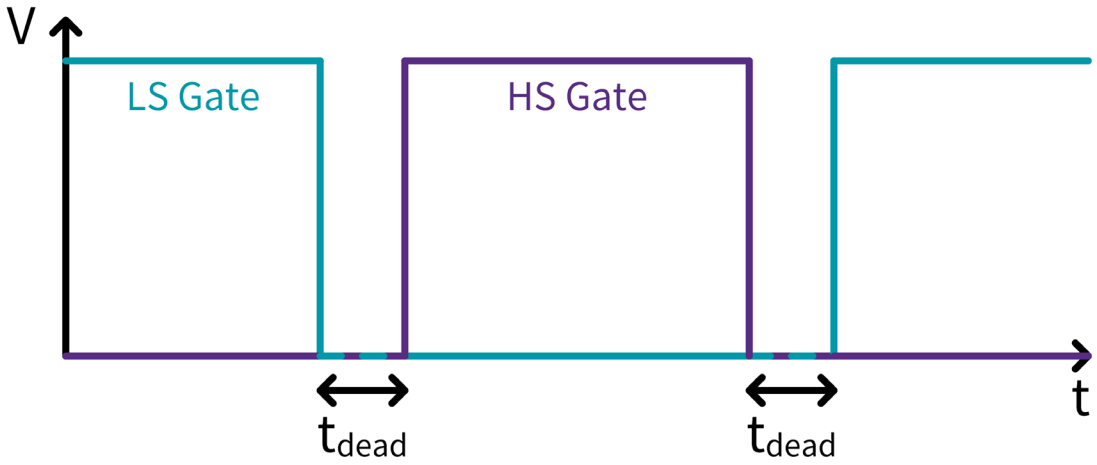


Figure 66: Notional deadtime implementation

During deadtime, no power transfer occurs and often the MOSFET body diode (or anti-parallel diode) must conduct. Designers are incentivized to identify the shortest deadtime which ensures no transition overlap during any operating conditions. Generally, power module deadtimes are on the order of a few hundred nanoseconds. To identify a deadtime, designers can refer to the datasheet measured rise/fall times and turn on/off delays to select approximate deadtimes. For example, Figure 67 shows the switch timings for the CAB004M12GM4 half-bridge power module. Assuming a designer is operating a switch at the same operating conditions and a 150 A source current, the designer would need to select a dead time of at least 80 ns to ensure a switch position is completely turned off before commanding the other switch to turn on. For an aggressive setup with well-defined operating conditions, a designer might select 100 ns of deadtime, or a more conservative selection of 150 ns. Notably, if selecting an aggressive deadtime, Wolfspeed always recommends simulating and testing the hardware extensively to ensure no overlap occurs on the hardware implementation.

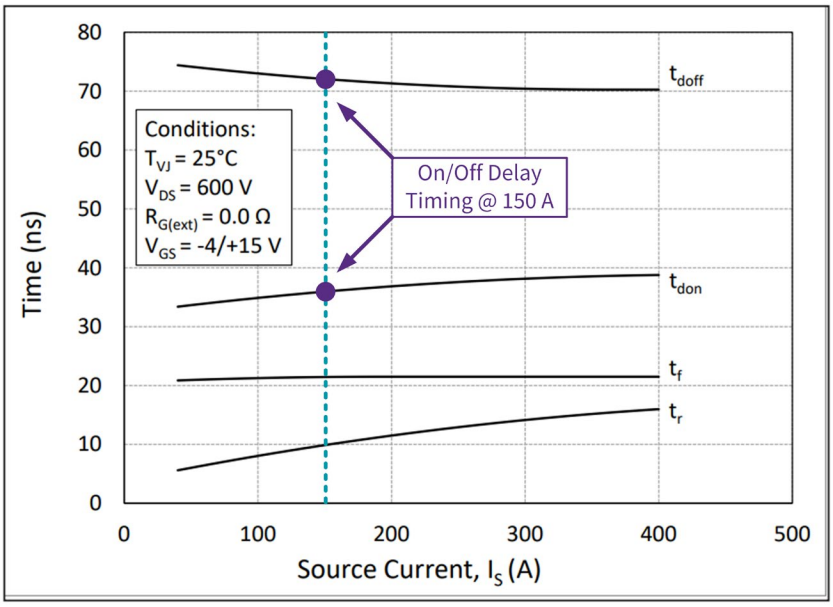


Figure 67: Measured timing parameters of CAB004M12GM4

Often, a controller (independent of the gate driver) is responsible for generating the turn-on and turn-off command signals and therefore also handles deadtime generation. In these cases, Wolfspeed recommends to still include interlock protection (see Section 5.6) as a final barrier for overlap protection. Some gate drivers – such as the Texas Instruments® UCC21520-Q1 – include provisions for generating the deadtime at the gate driver level. Performing the deadtime at the gate driver level has some advantages such as the following.

Less Compute Required. Deadtime generation typically demands a higher resolution time step for the controller compared to PWM generation requirements. Eliminating controller generated deadtime can enable use of a controller with a slower clock speed or can open compute resources for other system functions.

Deadtime Enforcement. The gate driver level deadtime can be used for redundancy to ensure deadtime is always enforced. The controller can still generate deadtime, and the gate driver can be used as a backup. This can also be adopted as a more practical input interlock protection which enforces a minimum deadtime requirement.

However, generating the deadtime at the gate driver level is not flexible since it can only be adjusted in hardware. Some converter topologies leverage changing the deadtime depending on the operating conditions to optimize system efficiency, which would not be possible with gate driver level deadtime implementation. Furthermore, adopting a single gate driver solution across multiple designs (see Section 3.3) would be more difficult since the deadtime would have to work across multiple designs. Because of these reasons – and due to the limited gate driver IC options with deadtime enforcement integrated – Wolfspeed does not include gate driver level deadtime enforcement on any of the power module specific gate drivers designed by Wolfspeed.

5.8 Active Miller Clamp

When the complementary switch position of a power module is modulated, the Miller effect of the device can couple voltage from the power loop of a MOSFET to its gate, potentially increasing the gate voltage significantly beyond the threshold of the device, causing a shoot-through condition. This impact is emphasized in circuits with high gate resistances since a large voltage potential can build across the gate resistor. To reduce this risk, gate drivers often include an *Active Miller Clamp* which provides a low-impedance path between the gate terminal and the turn-off voltage rail. The clamp connection is independent of the gate resistor selection, since it bypasses the gate resistors. A notional *Active Miller Clamp* circuit is shown in Figure 68.

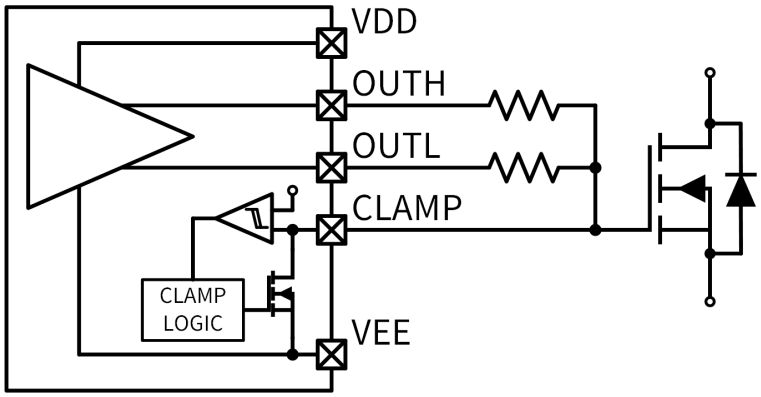


Figure 68: Notional Active Miller Clamp circuit

Though the exact implementation of the *Active Miller Clamp* differs between gate driver ICs, generally the MOSFET will turn off normally using the turn-off resistance. This enables the gate driver IC to control switch dynamics through the turn-off resistance, the same way it would without the *Active Miller Clamp*. After the gate voltage reaches a predefined threshold voltage or time after the turn-off event, the *Active Miller Clamp* is enabled, providing a low impedance to the turn-off voltage that is independent of the turn-off resistor. The clamp connection on the CGD1700HB2M-UNA gate driver is shown in Figure 25. The clamp circuit will be disabled again when the gate driver begins to turn on. The *Active Miller Clamp* circuit can also be added separately when the feature is not included in the gate driver IC by default or if higher ampacity clamping is required. It is noted that in cases with low gate resistance values and low-inductance routing, the *Active Miller Clamp* circuit is not strictly needed, since the power module already has a low-impedance connection to the turn-off voltage rail.

5.9 Gate Capacitance Discharge Resistor

As shown in Figure 5, MOSFETs include parasitic capacitances that are intrinsic to the manufacturing process. These capacitances, like any capacitor, can store charge. To prevent charge build-up on the gate capacitors, Wolfspeed always recommends including a high resistance attached from gate-to-source. This will ensure that the gate is discharged if the gate driver circuit has a sudden loss of power. More importantly, it will ensure the gate has no charge before a gate driver circuit has turned on, which is especially critical in circuits where the gate driver circuit is powered from a step-down converter off the main power rail. In these circumstances, it is possible that the MOSFETs are already blocking significant voltage before the gate driver circuits are enabled. Typically, a discharge resistor value of 10 kΩ is suitable to keep the gate capacitance depleted. The location of the resistance is shown in Figure 69. Notably, the resistance should not have any components between it and the MOSFET gate (i.e. it should be on the MOSFET-side of the gate resistor). The implemented location of the discharge resistors on the CGD1700HB2M-UNA gate driver are shown in Figure 70.

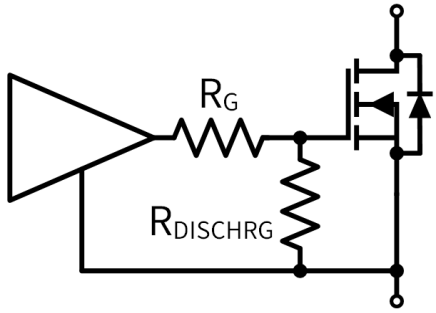


Figure 69: Discharge resistor placement

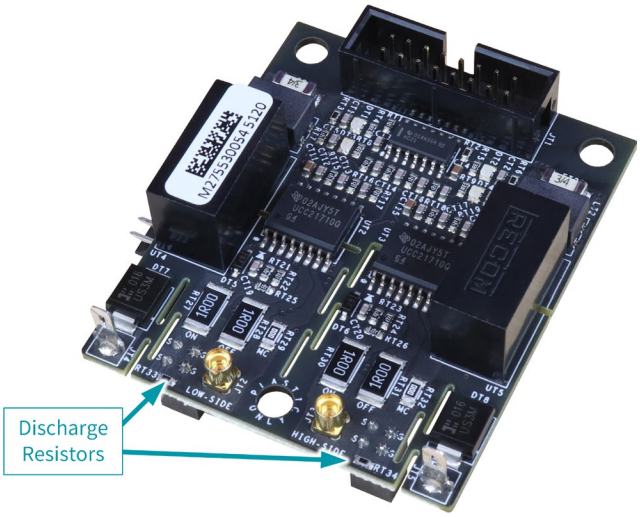


Figure 70: Discharge resistor placement on CGD1700HB2M-UNA gate driver

5.10 Reverse Voltage Input Protection

In situations where the gate driver may be handled or configured by an operator, it can be beneficial to include voltage protection on the input power to the gate driver. Typically, the most beneficial form of protection is reverse polarity protection to prevent inverted power leads from damaging the gate driver. This can be accomplished with a dedicated protection IC, though it can alternatively be easily and reliably performed using

inexpensive methods such as a diode or a P-channel MOSFET. Wolfspeed gate drivers use the P-channel MOSFET approach since the losses using this approach are minimal compared to the diode configuration. The P-channel MOSFET reverse voltage protection circuit is shown in Figure 71. If V+ and V- are configured correctly, the P-channel MOSFET conducts, and the gate driver functions as expected. If V+ and V- are inverted, the P-channel MOSFET is gated off and blocks the input voltage to the gate driver, protecting the gate driver. For reference, the input protection implementation on the CGD1700HB2M-UNA is shown in Figure 72.

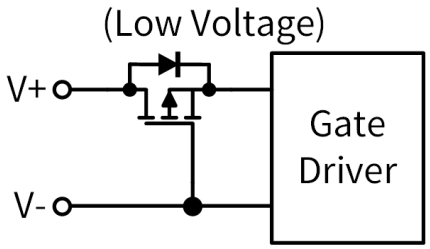


Figure 71: Reverse voltage input protection circuit using low-voltage P-channel MOSFET

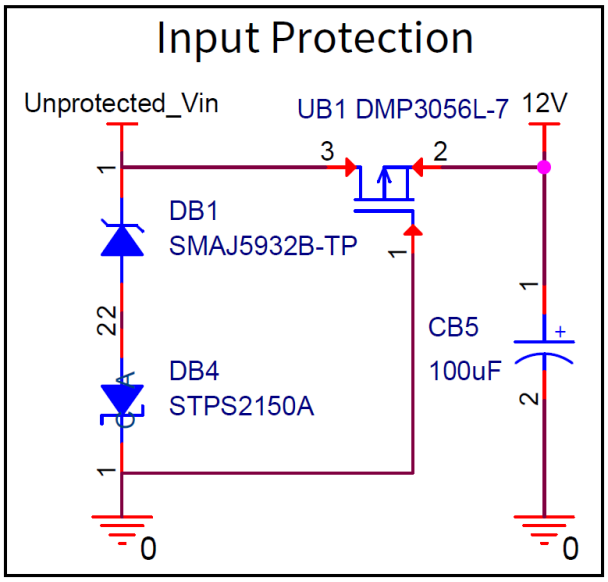


Figure 72: Input protection implementation on CGD1700HB2M-UNA gate driver

6. Metrology

Following the best practices and guidance provided in this document will aid with developing power module gate drivers for high-performance systems. Even with a well-designed gate driver, the system will need to be experimentally measured for troubleshooting and/or system validation. This section details methods to probe the gate driver for high-fidelity, high-accuracy measurements.

6.1 Gate-to-Source Voltage Measurement

The MOSFET gate-to-source voltage (V_{GS}) is an important tool for evaluating switching performance of a power module. It can offer insight into whether a controller is commanding the device on at the appropriate times, if noise is coupling into the gate loop causing partial turn-on, how long the device is in the Miller plateau, and the quickness of a switching event. However, improper instrumenting can introduce measurement artifacts that

are not representative of the actual system dynamics. For example, the long ground lead that is included with most oscilloscope probes, notionally shown in Figure 73, introduces significant inductance into a measurement. This inductance can introduce artificial ringing into the measurement, regardless of the actual system dynamics. It is important that all measurements are performed with instrumentation having suitable bandwidth and dynamic range, and furthermore it is important that the metrology is integrated into the circuit in a compact manner to reduce the influence of the probes. Wolfspeed recommends using probe adapters to attach to high-frequency connectors on the gate driver such as MMCX connectors to maintain a tight and shielded measurement loop. Example V_{GS} measurement MMCX connectors are shown on the CGD1700HB2M-UNA gate driver in Figure 74.

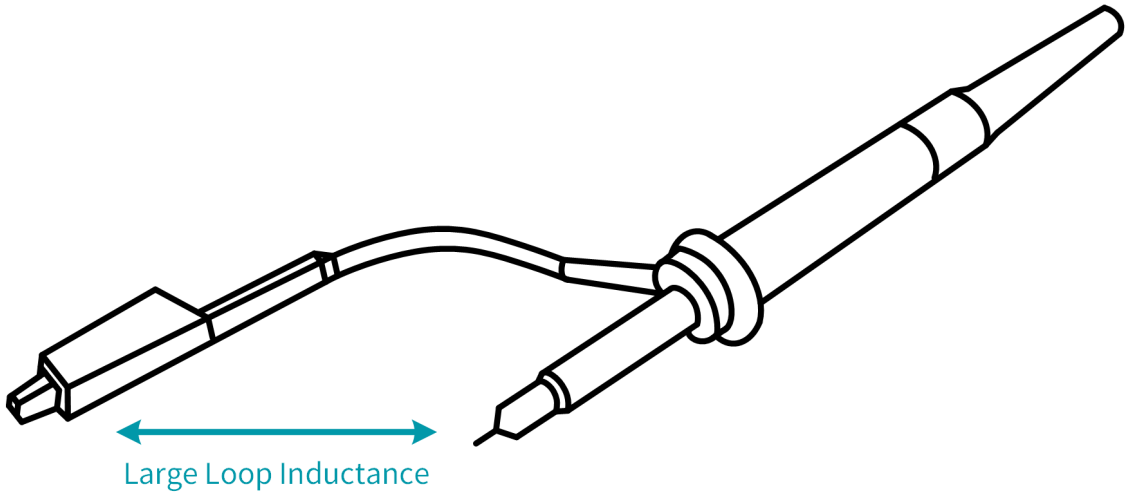


Figure 73: Large loop inductance introduced by long oscilloscope probe ground lead

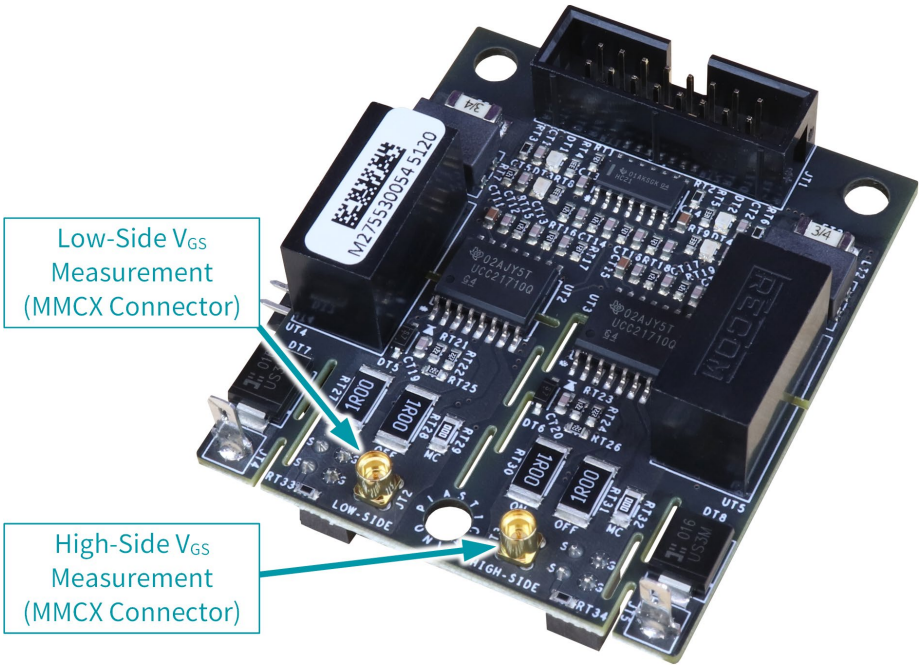


Figure 74: Example V_{GS} measurement locations on the CGD1700HB2M-UNA gate driver

When adding a V_{GS} measurement to a gate driver circuit, it is important that the measurement is performed on the MOSFET-side of the gate resistor. This measurement location is shown in Figure 75. If the measurement is instead performed on the other side of the gate resistor, the measurements will appear to change near instantaneously, but the actual V_{GS} on the MOSFET is slower to respond. To demonstrate this behavior, a CIL simulation (see Section 1.3 for more information about the simulation setup) was performed at 350 A with a CAB450M12XM3 power module. The gate driver section of the simulation was modified to enable the gate voltage to be monitored in both the "incorrect" and "correct" measurement locations, as shown in Figure 76.

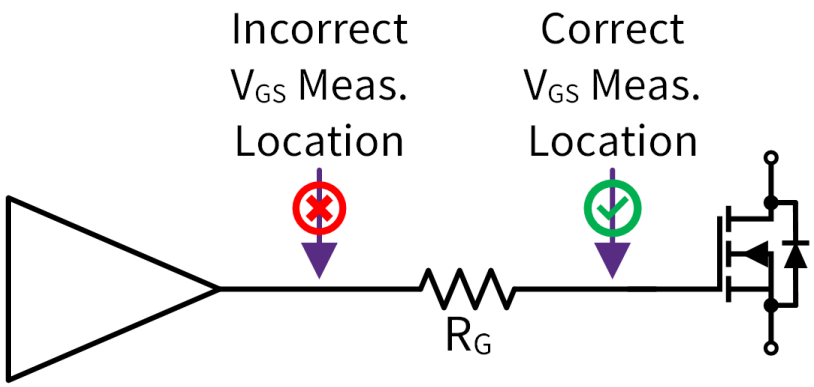


Figure 75: V_{GS} measurement location with respect to the gate resistor

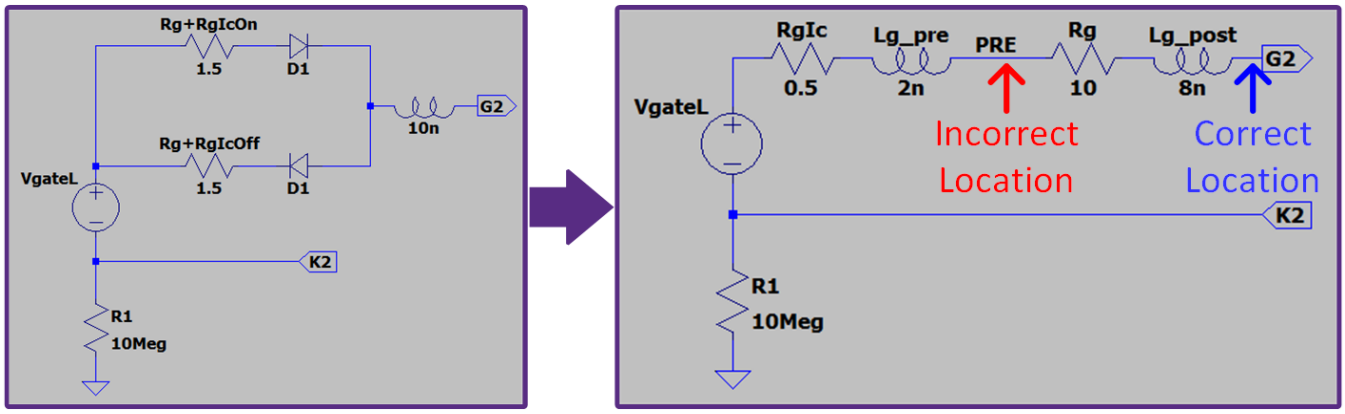


Figure 76: CIL gate driver simulation modifications to show V_{GS} measurement location influence

The results of the simulation are shown in Figure 77. The incorrect measurement location indicates a near-instantaneous step change when the gate is actually slowly charging to the gate driver voltage rail. The incorrect location obfuscates dynamics and reduces the accuracy of time-alignment between measurements. The correct probe placement allows the V_{GS} measurement to be as close as possible to the power module MOSFETs, improving the fidelity of the measurement. Notably, this behavior is most influential with high gate resistances, since the higher resistance provides more decoupling between the MOSFET gate and the gate driver output (before the gate resistor). To emphasize this phenomenon, a high gate resistor (10 Ω) was selected for the example simulation. However, this behavior will still influence V_{GS} measurements even when utilizing more aggressive gate resistors.

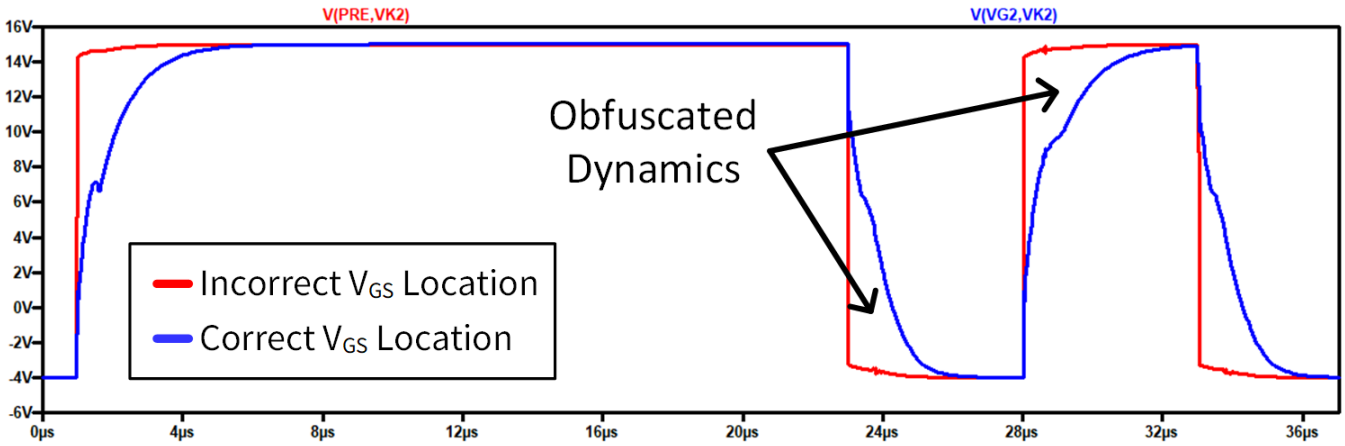


Figure 77: Influence on gate-voltage measurement when probed in the incorrect location

6.2 High-Side Gate-to-Source Voltage Measurement

When measuring the high-side gate voltage, it is important to remember that the probe will be referenced to the midpoint voltage, just like the high-side gate driver shown in Figure 4. Therefore, the probe will also require isolation to perform the measurement safely and accurately. Wolfspeed recommends performing high-side V_{GS} measurements with optically isolated probes such as the Tektronix IsoVu series of probes. Figure 78 shows an Tektronix IsoVu probe connected to the KIT-CRD-CIL12N-FMC evaluation board [2]. The optical isolation provides extremely high levels of CM rejection, and the probes can perform low-voltage measurements in EMI-rich environments. Figure 79 shows an example V_{GS} measurement using a standard differential voltage probe compared with an optically isolated probe. Both at turn off and turn on, high-frequency ringing is observed on the gate measurement with the differential probe. While some ringing is expected due to coupling between the gate loop and power loop (as indicated in the optical measurement), the differential probe indicates extreme and unrealistic ringing. When troubleshooting or commissioning a system, this ringing could be worrisome to a system designer; however, this ringing is due to the changing reference voltage of the differential probe inducing CM currents within the probe and is an artifact of the standard differential probe. Adopting the optically isolated probe for these measurements enables a designer to avoid troubleshooting or root causing non-existent issues due simply to the metrology selection. For more information about high-fidelity probe selection for power electronics, see PRD-08333 which provides more information about gate voltage measurements and other power module measurements such as drain-to-source voltage and current.

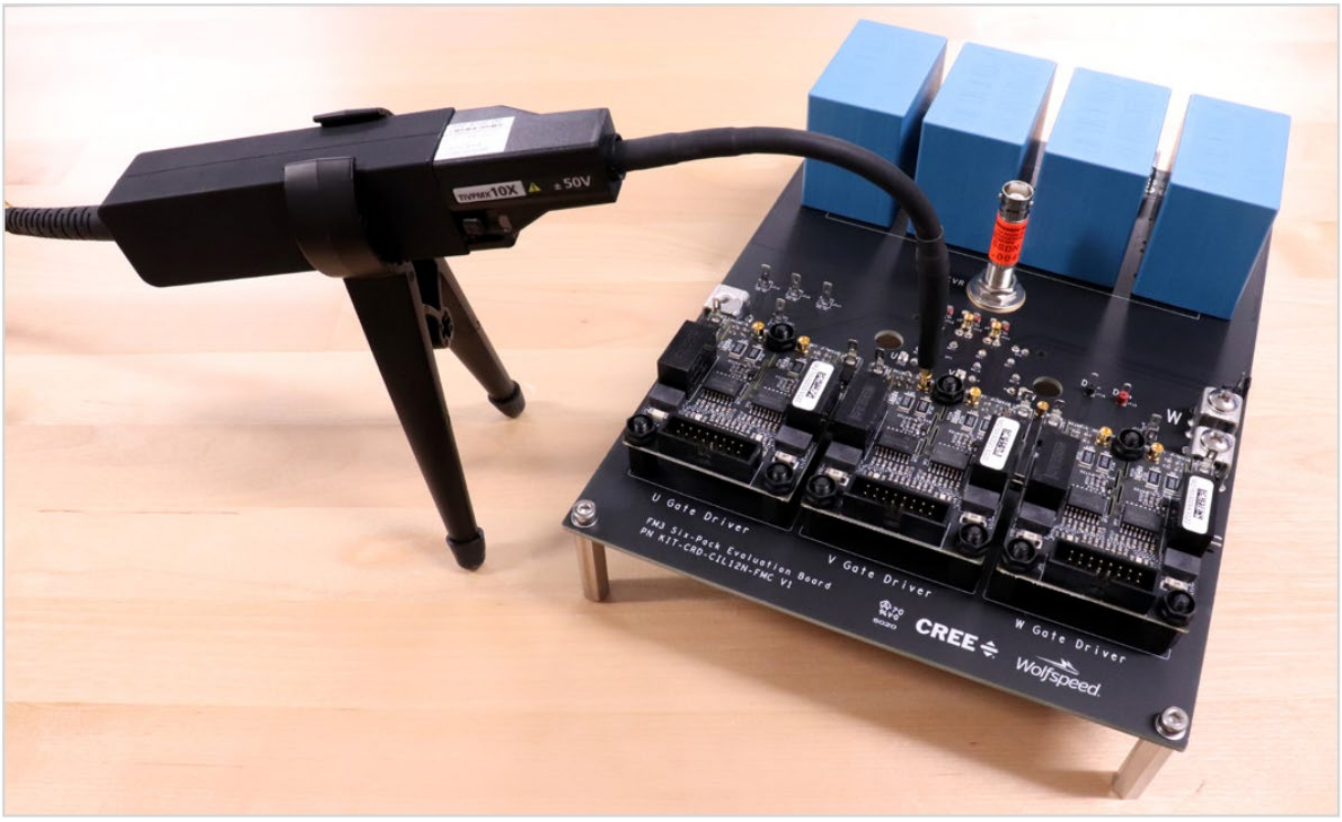


Figure 78: Tektronix IsoVu optically isolated probe connected to KIT-CRD-CIL12N-FMC evaluation board [2]

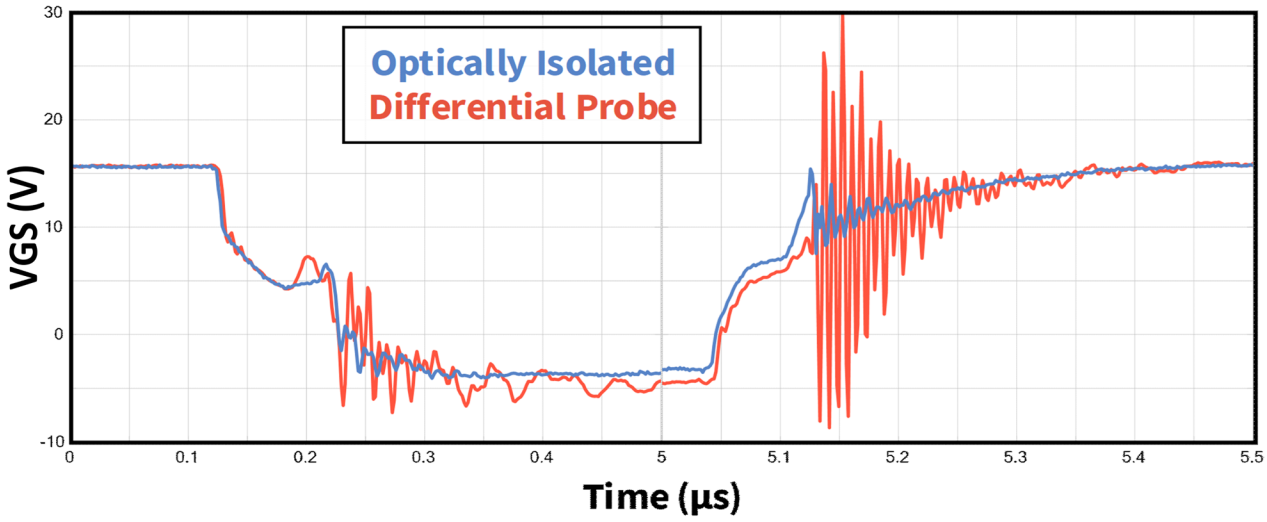


Figure 79: Differential vs optically isolated probe measurements of high-side gate voltage (PRD-08333)

6.3 Gate Current Measurement

During troubleshooting, evaluation, and system commissioning, it can often be beneficial to measure the gate currents of the device to understand system operation. This measurement can be difficult to perform accurately due to the floating nature of the measurement and the sensitivity required. For these reasons, Wolfspeed

recommends leveraging simulations as much as possible for identifying gate current trends. In cases where hardware measurements are still required, the measurement instrumentation must first be identified. Hall-effect sensors, current transformers (CTs), and Rogowski coils can be attractive options due to their intrinsic galvanic isolation. However, these sensors often require significant changes to the gate loop to insert the metrology. Changing the gate loop often introduces system artifacts due to higher inductance and more susceptibility to noise. Furthermore, these sensors often have limited bandwidth at high frequencies (e.g. Hall-effect sensors) or at low frequencies (e.g. CTs and Rogowski coils). These factors must be considered when using one of these sensor types for the gate current measurement.

The preferred method for measuring the gate current is to utilize the external gate resistor already employed on the gate driver circuit board. Notably, this technique does not include intrinsic galvanic isolation, so this measurement should always be performed with an isolated probe. Wolfspeed recommends performing this measurement with an optically isolated probe such as the Tektronix IsoVu series of probes. This measurement approach is easiest when only a single gate resistor is employed (rather than independent $R_{G,ON}$ and $R_{G,OFF}$ resistors discussed in Section 3.1) as shown in Figure 80(a). The single resistor allows both the turn-on and turn-off gate current dynamics to be captured in a single measurement. In cases where independent resistors are employed, both resistors can be monitored to capture both turn-on and turn-off dynamics, as shown in Figure 80(b). Alternatively, a Kelvin-source resistor can be added, shown in Figure 80(d), between the Kelvin-source of the MOSFET and the return connection of the gate driver. This approach allows for a single measurement to be used to capture all gate dynamics. Notably, the Kelvin-source resistor functions the same as a gate resistor and acts in series with the gate resistors. Equations (4) and (5) should be employed to determine the equivalent turn-on and turn-off resistors without the presence of the Kelvin-source resistor.

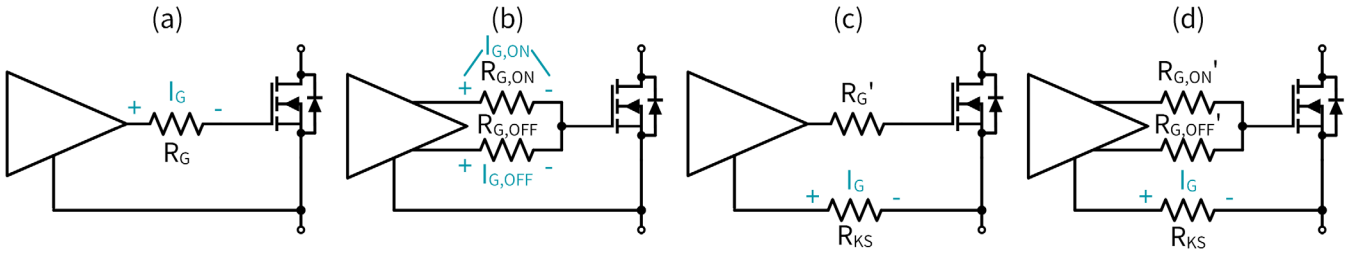


Figure 80: Gate current measurement options: (a) single gate resistor, (b) turn-on and turn-off resistors, (c) single gate resistor with Kelvin-source resistor, and (d) turn-on and turn-off resistors with Kelvin-source resistors

$$R_{G,ON} = R'_{G,ON} + R_{KS} \quad (4)$$

$$R_{G,OFF} = R'_{G,OFF} + R_{KS} \quad (5)$$

In some cases, a Kelvin-source resistor can provide a more reliable gate current measurement due to the source being a better reference than the gate for the measurement. In these cases, it can be attractive to add a Kelvin-source resistor even to the single gate resistor configuration, as shown in Figure 80(c). Again, the influence of the Kelvin-source resistor needs to be summed to any resistance attached to the gate in order the determine the total equivalent gate resistance, as shown in equation (6). Adding a Kelvin-source resistor may introduce some additional gate loop inductance – though typically less than introducing a CT, Hall-effect sensor, or

Rogowski coil – so this trade-off should be considered when evaluating this option. Furthermore, it can be difficult to add the R_{KS} resistor in late stages of testing, where it cannot easily be added to a board. When employing a Kelvin-source resistor, the probe should be configured such that the probe reference (indicated "-" in Figure 80) is attached to the Kelvin-source of the module. This will ensure that the probe has the same reference as the other measurements on the MOSFET (e.g. V_{GS} and V_{DS}).

$$R_G = R'_G + R_{KS} \quad (6)$$

6.4 Drain Measurement

The gate driver circuit requires feedback from the MOSFET drain to perform most overcurrent (OC) measurements such as DESAT protection discussed in Section 5.1. The optimal connection for this measurement is a short sense connection as close as possible to the drain of the MOSFET. This type of connection will limit delays and issues due to the voltage drop of parasitic resistances and inductances. For example, the CGD1700HB2M-UNA gate driver includes spade connectors, shown in Figure 81, to attach a dedicated sense wire to the drain of the device. Connecting these spade connectors – or whatever interface connection is adopted – to the MOSFET drain terminals as close as possible to the power modules will ensure reliable overcurrent protection.

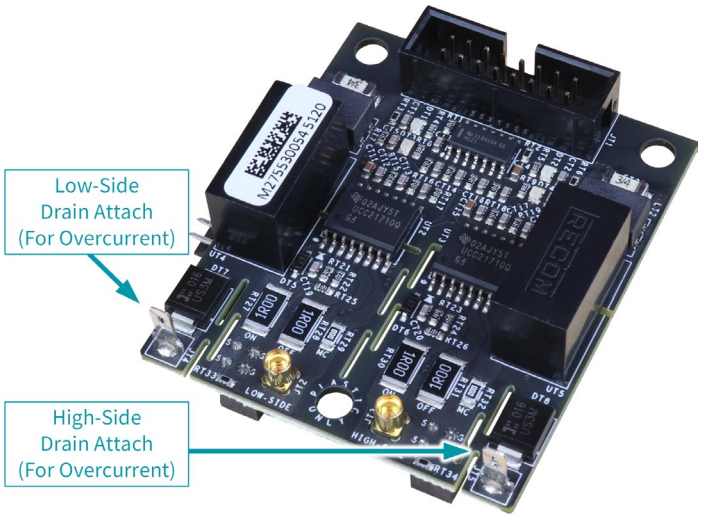


Figure 81: Example drain feedback locations on the CGD1700HB2M-UNA gate driver

For overcurrent detection, the drain feedback requires a precise low-voltage measurement of a terminal which varies significantly in voltage (hundreds of volts, see Section 5.1). When routing the overcurrent circuit, the direct connection to the MOSFET drain terminal has a higher immunity to noise – in comparison to the low-voltage detection circuit – since it is a power terminal fluctuating at high voltages[5]. For this reason, when routing the overcurrent circuit, the low-voltage detection circuitry should be prioritized. This circuitry should be routed compactly with shielding. The divide between the high and poor noise immunity of the overcurrent circuit is separated at the high voltage blocking diodes, as shown in Figure 82. If long routes/connections are

[5] Though the drain connection is more immune to noise than the low-voltage overcurrent detection circuitry, the signal should still be routed using best practices such as short connections and avoiding high-noise signals.

required for routing the overcurrent circuitry, perform these long connections using the “Strong OC Noise Immunity” part of the circuit. Figure 83 shows example DESAT attachment points to the gate driver on the CRD200DA23N-GMA 2300 V three-phase inverter reference design.

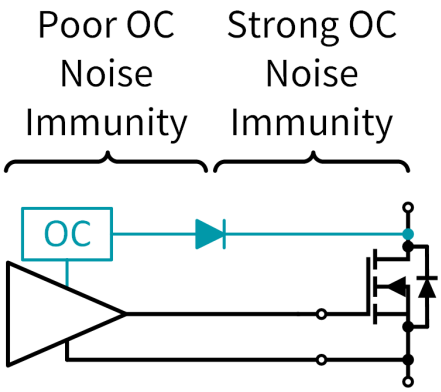


Figure 82: Noise immunity of various parts of the overcurrent detection circuitry and routing

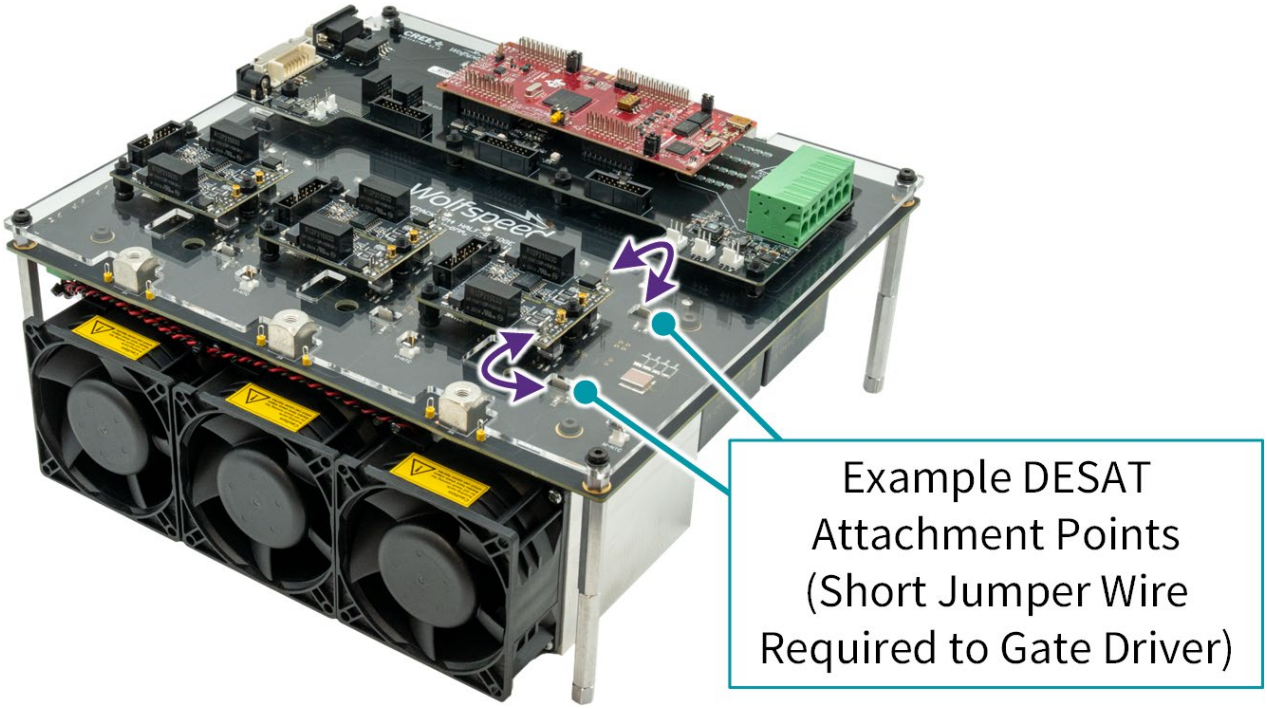


Figure 83: Example DESAT attachment points on CRD200DA23N-GMA

For low-side switch positions, it is possible to use the Kelvin-source of the high-side switch position as the drain measurement of the low-side switch, as shown in Figure 84. This approach can make gate driver design/layout simpler since the high-side Kelvin-source connection is already routed to the gate driver circuit. However, some power modules include Kelvin-source resistance inside the power module. In these cases, the Kelvin-source terminals should not be used for the low-side DESAT connection. Wolfspeed recommends evaluating this technique on a case-by-case basis since it depends on the operating conditions and power module employed.

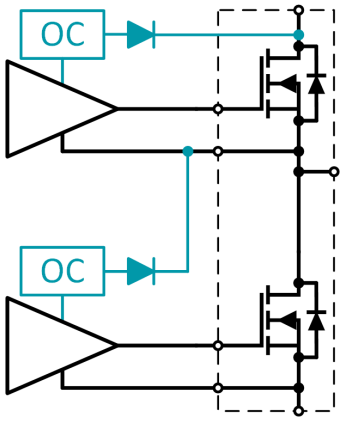


Figure 84: Low-side position using Kelvin-source of high-side position for overcurrent protection

7. Application

Wolfspeed partners with many industry-leading gate driver IC manufacturers to ensure designers have several options for implementing a solution which adheres to different cost and performance spectra. Several of these vendors have already developed off-the-shelf full gate drive circuit designs that are optimized for integrating with Wolfspeed power modules. Additionally, Wolfspeed designed gate driver solutions which provide an easy way to begin testing and evaluating Wolfspeed SiC power modules. A full list of available gate drivers can be found on the Wolfspeed website here. This section provides some specific application details about using these boards and for developing custom gate driver solutions.

7.1 Single-Ended to Differential Transceiver

As mentioned in Section 4.2, differential signaling provides a cost-effective solution for improving noise immunity between a controller and a gate driver IC. To gain the benefits of differential signaling, circuits must include a differential transceiver on both the transmitting and receiving sides of the signal chain. All 0.6-2.3 kV Wolfspeed power module gate drivers expect differential signaling for transmitting and receiving signals. For designers looking to quickly add these gate drivers to a circuit without designing a custom circuit board with differential signals, use the CDB12HB00D differential transceiver companion board developed by Wolfspeed (shown in Figure 85). This board converts single-ended signals that are typical of a microcontroller to the differential signals required by the gate drivers. When using this board, it is essential to keep the signals of the single-ended side of the transceiver as short as possible. In no cases should the single-ended connections be longer than the differential side connections since the differential side connections are more immune to noise. The CDB12HB00D board is shown attached to an evaluation board in Figure 86.

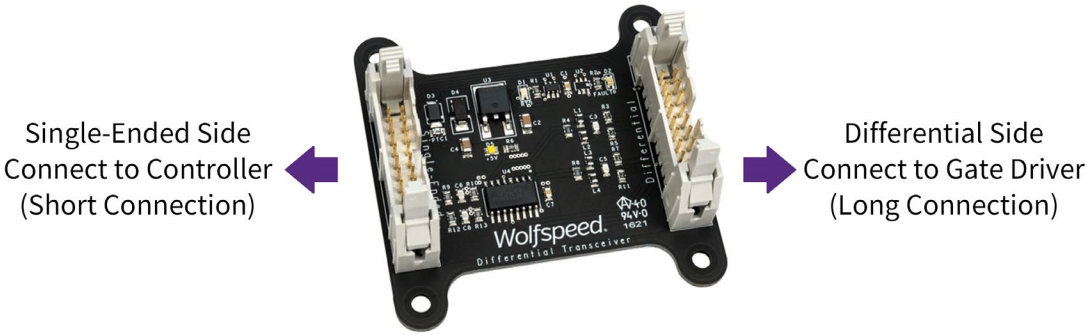


Figure 85: Wolfspeed CDB12HB00D differential transceiver companion board

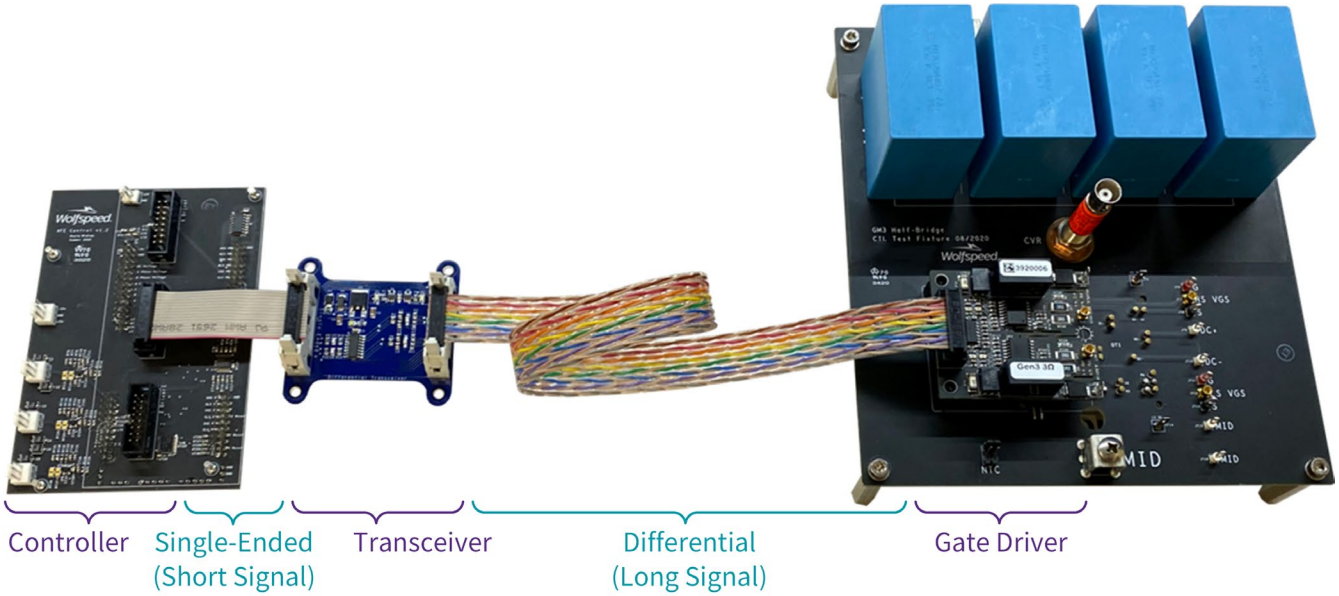


Figure 86: Wolfspeed CDB12HB00D differential transceiver companion board attached to evaluation kit

7.2 Temporarily Disabling Overcurrent Protection

As discussed in Section 5.1, many gate drivers – including the CGD1700HB2M-UNA designed by Wolfspeed – include overcurrent protection in the form of a DESAT circuit. In some cases, such as troubleshooting or controller development, it is advantageous to validate gate driver functionality without connecting the gate driver to a power module. However, when a floating gate driver (gate driver not connected to a power module) is commanded on, its overcurrent protection will immediately trip and signal a fault condition. The DESAT overcurrent protection will identify the open circuit (due to no power module being attached) as an extremely high current causing a large voltage drop across a non-existent power module (see Section 5.1 for more information about how the DESAT circuit works). To prevent this issue, the DESAT overcurrent voltage simply needs to be bypassed to the module source terminal, as indicated in Figure 87. This configuration prevents V_{OC} from ever exceeding the detection threshold (V_{DET}). This bypass circuit will even work when the gate driver is attached to the module and a high voltage bus since the high-voltage diode(s) still protects the DESAT circuitry. Still, it is not recommended to use this bypass method in circuit or while performing system-level testing since the power module would be unprotected from any overcurrent events.

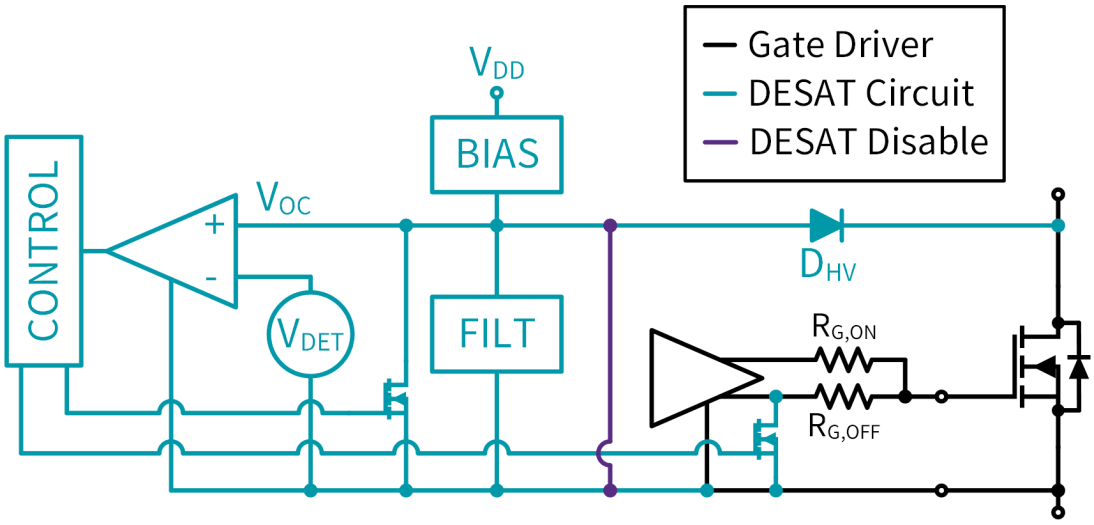


Figure 87: Disable DESAT circuit (not recommended for system-level testing)

For circuits that require an external connection to the DESAT circuit – such as the spade connectors of the CGD1700HB2M-UNA shown in Figure 81 – the DESAT can also be quickly bypassed by connecting the external connector to the source of the MOSFET, as shown in Figure 88. This configuration can be useful for evaluating controller fault signal response by modulating whether the DESAT circuit is configured or not be engaging/disengaging this connection. However, though this connection is simple, do not bypass DESAT in this manner if the DESAT connection is already attached to the MOSFET drain terminal. This DESAT disable method bypasses the protection of the high-voltage diodes and will cause an immediate short circuit. Furthermore, it is not recommended to bypass DESAT while using the gate driver in circuit or during system-level testing since the power module would be unprotected from any overcurrent events.

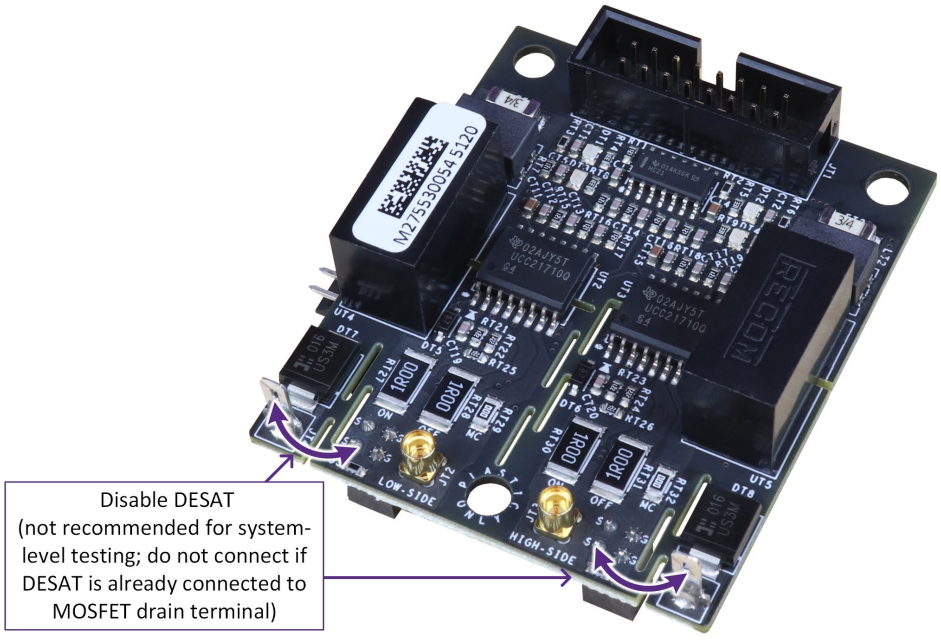


Figure 88: Disable DESAT circuit on CGD1700HB2M-UNA (not recommended for system-level testing; do not connect if DESAT is already connected to the MOSFET drain terminal)

7.3 XM Power Module Gate Pins

There are two signal pinout variants in the XM module family: the inline pinout (shown in Figure 89) and the cross pinout (shown in Figure 90). The cross pinout improves the dynamic control of new and future generation SiC MOSFETs at peak switching speeds. Incorrectly pairing a power module and a gate driver can result in a short circuit condition on the output of the gate driver board, which can damage the gate driver. More information about the cross-pin differences and the proper gate drivers to employ for each XM module pinout variant is provided in PRD-07128.

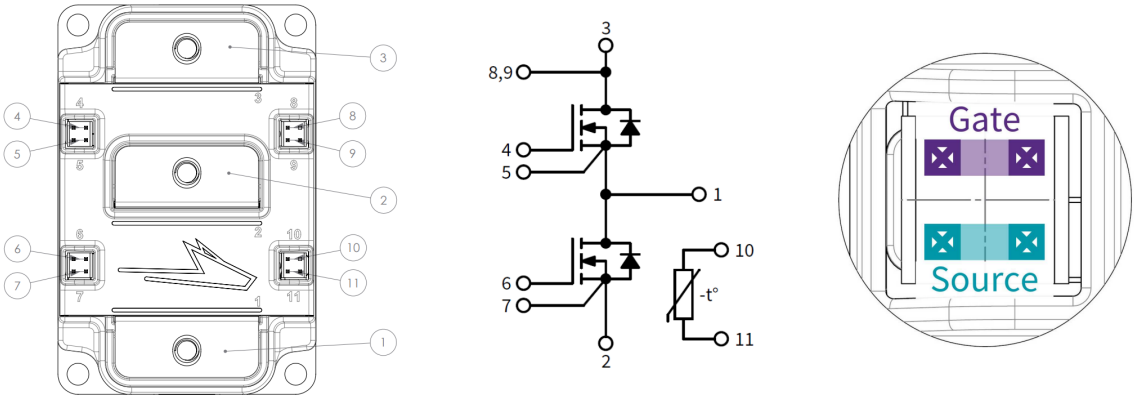


Figure 89: XM module family inline pinout

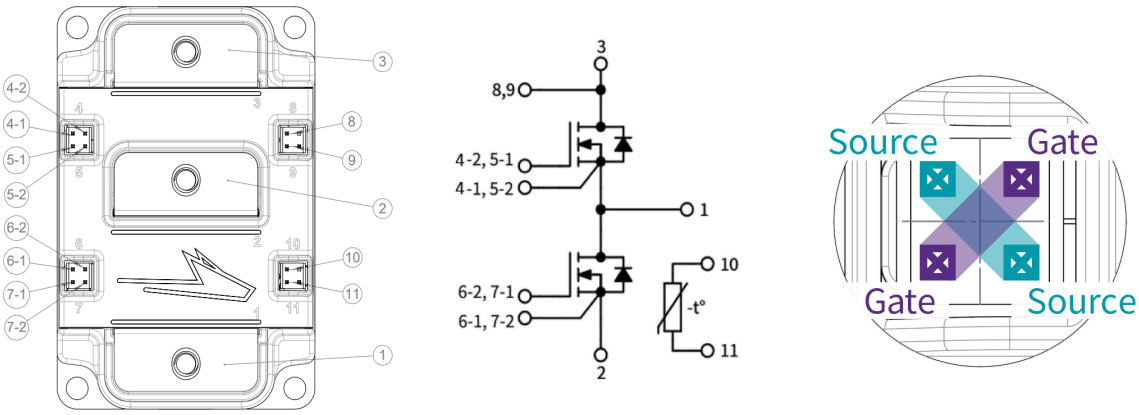


Figure 90: XM module family cross pinout

8. Universal Gate Driver Daughter Card Specifications

As discussed in Section 2.1, Wolfspeed partners with many industry-leading gate driver IC and isolated power supply manufacturers to provide customers with a range of options to evaluate in end applications. The full list of partner gate drivers can be found here. Please contact Wolfspeed for the relevant requirements for any potential partners to be added to the list of Wolfspeed partner gate drivers.

Revision History

Date	Revision	Changes
May 2025	1	Initial Release

References

[1] C. D. New, "Metrology Considerations for Medium-Voltage Wide Bandgap Power Electronics," The University of Alabama, Tuscaloosa, 2022.

[2] Tektronix, "Effective Measurement of Signals in Silicon Carbide (SiC) Power Electronics Systems," [Online]. Available: https://www.tek.com/fr/documents/technical-brief/effective-measurement-of-signals-in-silicon-carbide-%28sic%29-power-electronics-systems. [Accessed 10 Mar. 2025].