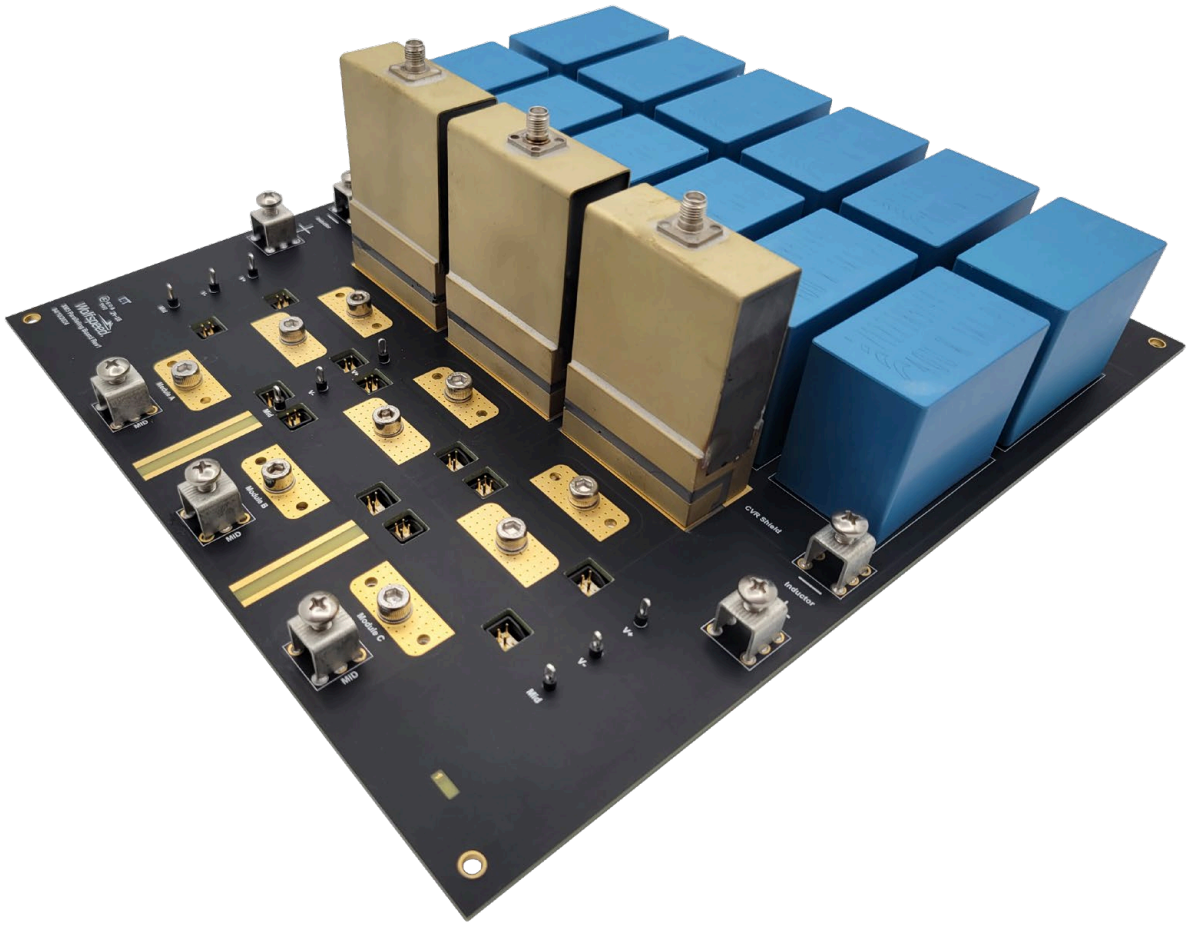
Application Note **PRD-08911**

Considerations for Current Balancing in Paralleled SiC Power Modules



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Considerations for Current Balancing in Paralleled SiC Power Modules

Paralleling power modules is a useful method for increasing the ampacity of power electronics systems while using cheaper, smaller modules. However, successful implementation requires careful attention to the layout and implementation to maximize performance. This document provides a detailed overview of how to parallel SiC power modules in applications. The document discusses layout considerations, gate driver implementations, module parameter matching, and mitigation methods, with an emphasis on current sharing. Light discussion on general implementation is also provided.

Contents

1. Scope

This document focuses on the current imbalance between paralleled power modules during operation. General design or operational issues in applications utilizing paralleled modules may not be covered. Best-practice power electronic design principles (minimizing stray inductance, maximizing symmetry) should be implemented in all designs.

2. Introduction

Designing a power electronics system requires balancing numerous tradeoffs to meet the target specifications. These tradeoffs include size, efficiency, peak power capability, reliability, and any other design specifications. One of the first and most important considerations to make during the design process is selecting the switching semiconductor device that the system will be developed around. However, selecting a device suitable for a given design is complex, and requires careful analysis of the characteristics of available parts. In some cases, it may be necessary to place multiple power modules in parallel to achieve the desired current rating. Doing so requires implementing proper layout techniques and considering the inherent differences between devices. This document will give an overview of the challenges, considerations, and solutions to improve designs that leverage paralleled power modules.

2.1 Paralleling Configurations

With the growing demand for high-current applications, it becomes necessary to parallel multiple MOSFETs to achieve the desired power levels. The paralleling of these devices can be performed both at the die level and the package level, as shown in Figure 1.

Package-level paralleling describes when packaged single-chip devices are paralleled. This is most often performed with discrete devices, shown in the left of Figure 1. These systems can achieve high power density and offer high flexibility, but present significant design challenges regarding layout and isolation. In addition, the large size of discrete packages relative to the die limits the number of devices that can be placed in parallel

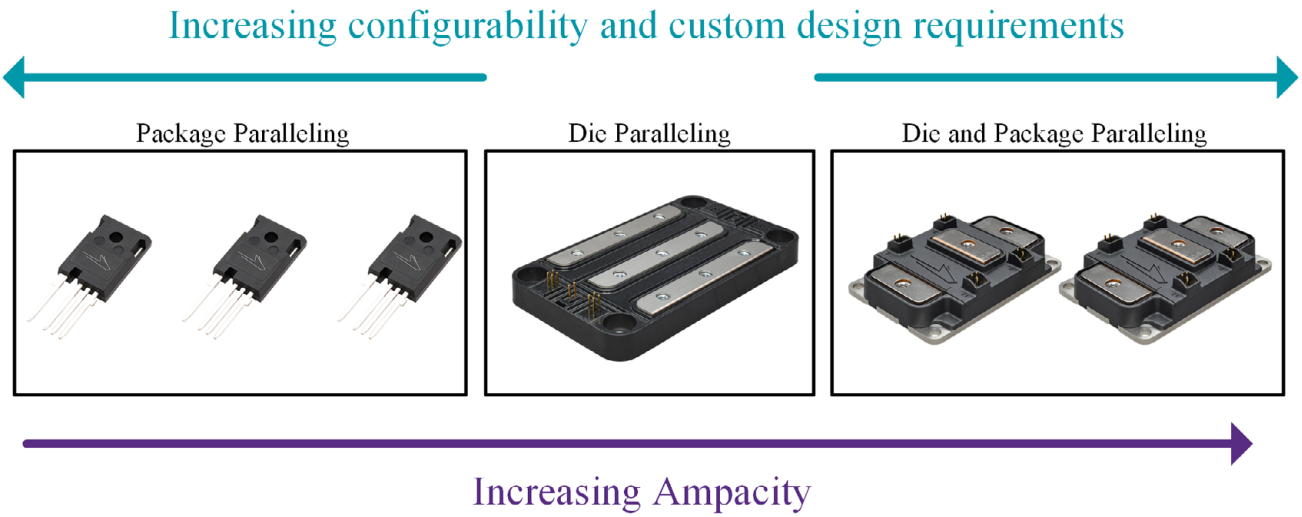


Figure 1: Trends in complexity and optimization for power device packaging

before the size of the layout becomes a limitation. Ultimately, it is the system designer's responsibility to ensure that the current distribution between each device meets their specifications.

Die-level paralleling describes when the bare MOSFETs are attached to the same substrate within a package. These packages are referred to as multi-chip power modules (MCPMs) and allow designers to seamlessly integrate high-current devices into their system without considering the balance between die. Manufacturers optimize the package layout to balance the parasitics and provide easy-to-connect terminals for integration. Power modules are also provided in various topologies, such as single-switch, half-bridge, full-bridge, or six-pack configurations, and can include integrated features such as Schottky diodes, DESAT protection, and temperature measurements. An example of a half-bridge SiC MOSFET power module capable of over 760 A DC operation is the Wolfspeed® CAB760M12HM3 shown in the center of Figure 1. Overall, the high performance and ease of integration of power modules makes them an attractive option for system designers.

For very high current applications, commercially available power modules may not be suitable or available. There are several reasons for this. Physically larger modules are more specialized and manufactured at lower volumes, thereby decreasing availability and increasing cost. Larger modules also have increased distance between the terminals and the die within the package, increasing parasitic inductance in the power and gate loop. As the required current levels exceed ~500 - 1000 A, it becomes more attractive to instead parallel power modules to further increase the ampacity of the system, as shown in the right of Figure 1. When properly implemented, paralleled power modules offer the highest available ampacity for a system. However, paralleling power modules presents the same current balancing challenges as paralleling discrete devices, and it is the designer's responsibility to ensure that each individual module will not exceed its rated specifications during operation. Module paralleling is not restricted to half-bridge devices and can be applied to full-bridge and six-pack topologies as well.

2.2 Advantages of Paralleling Power Modules

Overall, paralleling power modules can provide the following advantages:

- Higher current-carrying capability than discrete or single-module implementations
- More design options, as low-current commercial modules are more readily available in industry-standard packages
- More flexible gate driver design and implementation (and can use smaller, less expensive driving chips)
- If a single module fails, it is less expensive to replace
- Modules can be spread out on the heatsink, increasing the effectiveness of cooling
- Lower inductance and greater symmetry are possible, as bussing can be spread out across multiple terminals

2.3 Advantages of SiC MOSFETs over IGBTs

It is the general assumption that the faster switching speeds of SiC MOSFETs would make them more difficult to parallel while maintaining proper dynamic current sharing. On the contrary, SiC MOSFETs generally have several advantages over IGBTs:

1. The switching losses of SiC MOSFETs are stable across temperature, while IGBTs exhibit higher losses with temperature. This positive feedback between temperature and losses in IGBTs exacerbates temperature imbalance.
2. SiC MOSFETs often have a higher $R_{DS(ON)}$ temperature coefficient [1] than Si IGBT V_{CE} characteristics, which acts as a balancing mechanism when temperature imbalances exist.
3. IGBTs have a steeper transconductance curve such that small changes in gate voltage near threshold have a larger effect on conduction as compared to SiC MOSFETs.
4. SiC MOSFETs are more thermally conductive, allowing for better device-level heat dissipation and stable operating temperatures.
5. IGBTs are susceptible to thermal runaway [2] and generally operate at lower temperatures than SiC MOSFETs.

2.4 Ideal Paralleling

In an ideal case, the load current (I_{Load}) of a system is shared equally among paralleled modules. So, in an application using *n* modules, the load current through each module is I_{Load}/n, as shown in the example in Figure 2 with three modules sharing a 1500 A load equally. In this configuration, where each switch position has its own gate driver, each module can be considered an independent device operating at I_{Load}/n. For example, consider an 850 A application using two CAB425M12XM3 power modules in parallel. The expected performance of each module can be determined by referencing the CAB425M12XM3 datasheet operating at 425 A, then scaled appropriately for the number of devices in parallel. If the switching losses are determined to be 20 mJ for one module, then the total switching losses for the full system is 40 mJ. For the purposes of designing the

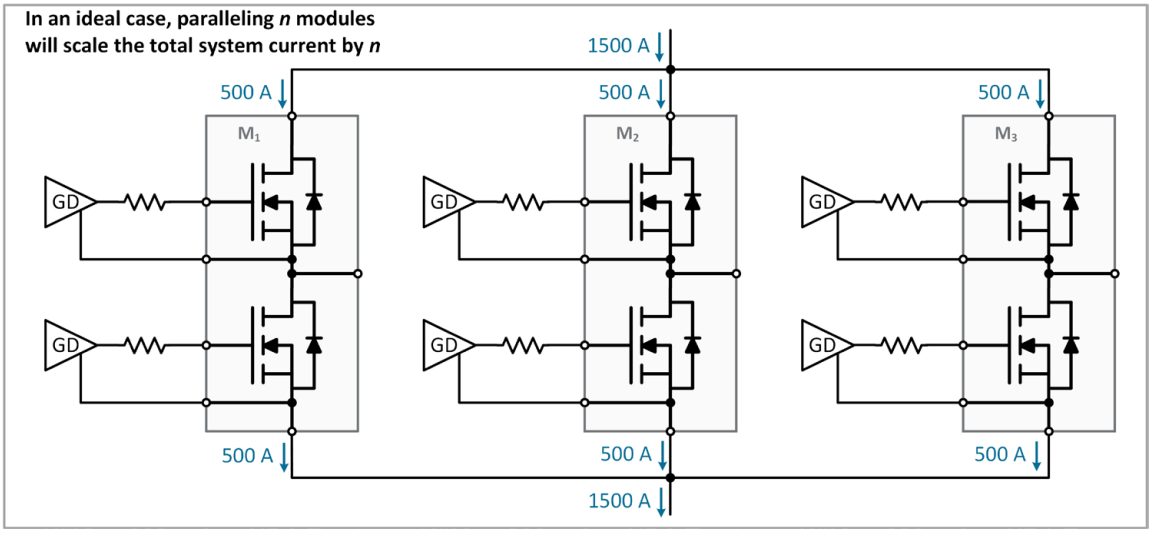


Figure 2: Ideal current sharing between half-bridge power modules

surrounding system (cooling requirements, passive elements, filtering, load size, etc.), the paralleled power electronics can be considered one single unit. Here, this system should simply be designed for 850 A.

2.5 Non-ideal Paralleling

When paralleling modules, asymmetries will inherently exist in any system that will result in an imbalance in current sharing and temperature. These imbalances can be caused by both the module characteristics and the surrounding system. The sources of imbalances that will be discussed in this document are summarized below.

System Layout: The system layout describes the electrical interface between the modules and the surrounding buswork. In general, there are two primary considerations in the layout. The first relates to the parasitic inductance of the commutation and gate loop of each module, which can affect the dynamic switching behavior of each module. The second is to the impedance to the load, which can affect the steady-state current sharing of each module.

Gate Driver Configuration: The implementation of the gate driver is highly important for balanced switching. Asymmetric driving speed or timing delays can cause current imbalance, and improper configuration can contribute to circulating currents and stability issues.

Module Parameter Mismatch: Semiconductor devices have intrinsic variations in their characteristics. When paralleling modules, these variations can cause a mismatch in current sharing. The most commonly studied parameters for current sharing are the on-state resistance ($R_{DS,(ON)}$) and the threshold voltage (V_{TH}). $R_{DS,(ON)}$ causes differences in conduction losses between modules, while V_{TH} causes differences in switching losses between modules.

Heatsink Configuration: The primary consequence of current imbalance is the resulting temperature imbalance. A heatsink that does not apply cooling evenly to each module can exacerbate this issue.

2.6 Effects of Current Imbalance

Asymmetric current flow between modules can result in a temperature imbalance that reduces lifetime and limits ampacity [3], [4]. Consider the notional diagrams of two parallel devices in Figure 3. In this system, Module A is subject to 55% of the total current and Module B is subject to 45% of the total current. In Figure 3 (a), the system is in a low-load state, and the MOSFET temperatures of each module differ by only 5°C. In Figure 3 (b), the system changes to a heavy-load state, and the temperature of each module now differs by 20°C. An important aspect here is that, between state *a* and state *b*, Module A increased in temperature by 75°C, while Module B increased in temperature by 60°C. As the temperature of the module changes, materials within it will expand and contract. Mismatch of the coefficients of thermal expansion (CTE) causes thermomechanical stress of the die attachment. Over time, this stress can cause mechanical attachments within the module to fail. The stress imparted on the module is largely dependent on the change in temperature; for example, a 1°C increase in temperature will cause very little expansion of the materials (and thus little stress), whereas a 50°C increase in temperature will be significant. Figure 4 provides a notional plot of a typical lifetime curve. ΔT_J corresponds to a change in the virtual junction temperature of the module. As ΔT_J increases, the number of cycles that a typical module will survive decreases. For the paralleled module case in Figure 3 (b), this increased ΔT_J will cause module A to fail before module B. Because a system's reliability is defined by its first failure point, this

causes an overall reduction in the system reliability. A system in which the CTE mechanical stress is imparted evenly on each module will have a longer lifetime.

The second issue is the reduction in ampacity caused by exceeding the maximum operating temperature. Consider the peak-load condition in Figure 3 (c), where the current is increased until module A reaches 175°C (the maximum rated T_J). Here, the system cannot increase in operating current further because module A will exceed its rating. However, module B is below its maximum operating T_J at 140°C. Here, the total ampacity of the system is effectively limited by the module imbalance, as module B is not carrying its full current capability.

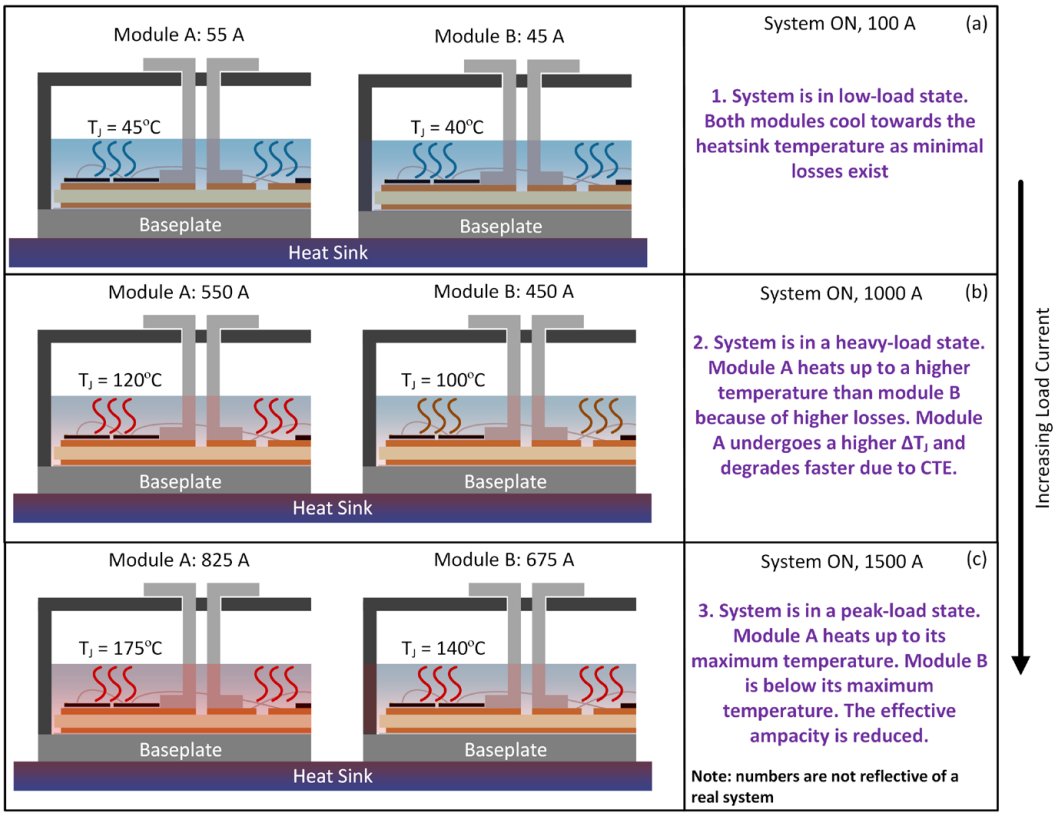


Figure 3: Effect of current imbalance on module temperature and thermal expansion degradation

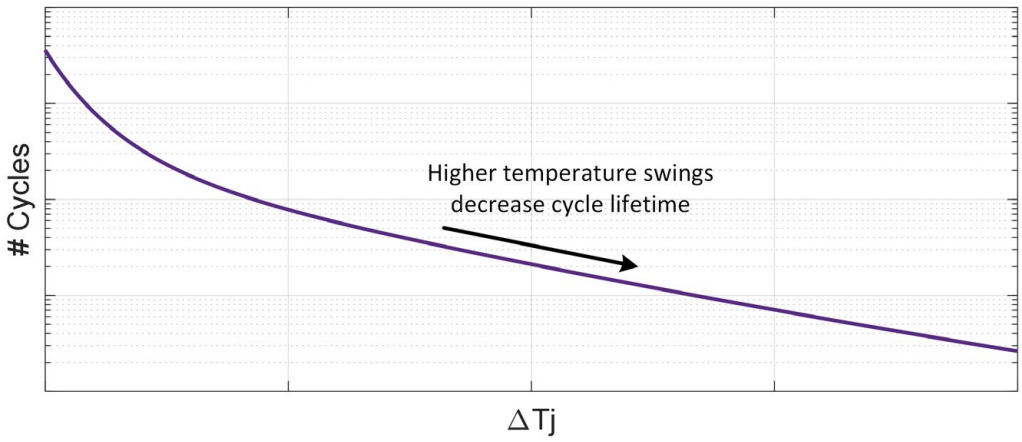


Figure 4: Notional effect of current imbalance on module temperature and thermal expansion degradation

3. Empirical Test Study Configuration

As summarized in Section 2.5, there are several device and system dependent factors that contribute to asymmetric current sharing within power modules. In this document, both an empirical setup and simulation are used to study the current imbalance between modules in paralleled applications. CAB450M12XM3 half-bridge power modules (Figure 5) are used as the paralleled switching device. This module is capable of operating at 450 A continuously with a blocking capability of 1.2 kV. This section will describe the hardware used for the empirical analysis. **This hardware implementation is for demonstrating the sensitivity of different parameters and does not represent an optimized or well-designed system.**

3.1 Double Pulse Test / Reverse Recovery

A single printed circuit board (PCB) was designed that can parallel up to three CAB450M12XM3 modules for DPT, reverse recovery, and short-circuit testing. A notional circuit diagram of this PCB is shown in Figure 6. From left to right, the modules are labeled *A, B,* and *C.* Throughout this analysis, connections or other configuration elements may be changed. This circuit represents the "default" state of the system; any results discussed herein will follow this layout unless otherwise specified.

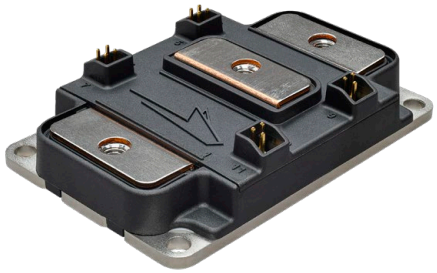


Figure 5: CAB450M12XM3 power module test subject used for analysis

For double pulse tests (DPTs), the low side of each device is actively switched while the high side is kept OFF. For reverse recovery (RR) tests, the high side of each device is actively switched while the low side is kept OFF. The load inductor connection is also changed between these two configurations. One side of the load inductor is always connected to the midpoint of the modules. The other side of the load inductor changes between V_+ for DPT and V_- for RR. A DC link capacitor (C_{DC}) is charged to the desired bus voltage for each test, and the charge pulse time is adjusted to reach the desired operating current. For more information on the fundamental operation of double-pulse and reverse recovery testing, refer to PRD-08333.

Small inductor elements indicate stray inductances. These values are not to be quantified in this document, but simply represent that the connection between those two nodes has a significant portion of stray inductance that may contribute to imbalance. Additional inductance may also be added at those locations to understand their influence on current balancing. To understand how this will be used, consider the load inductor connection. The midpoint of each module (Mid_A, Mid_B, Mid_C) are connected together on the PCB. This connection on the PCB has some inductance, creating inductance between L_A, L_B, and L_C. For example, if the load inductor is connected at L_A, then there will be additional inductance relative to module C (follow the path from L_A to Mid_C). On the other side of the inductor, it can be connected on the 'A' side (V_{+A}, V_{-A}) or the 'C' side (V_{+C}, V_{-C}); the location of this connection will change the impedance of the load to each module.

In terms of metrology, each module has a high-bandwidth 10 mΩ current viewing resistor (CVR) on its source terminal to measure the isolated current through that path. In general, there are four distinct measurements: a gate-source voltage on the high side of each module (V_{GS-HS}), a gate-source voltage on the low side of each module (V_{GS-LS}), a drain-source voltage on the high side (V_{DS-HS}), a drain-source voltage on the low side (V_{DS-LS}),

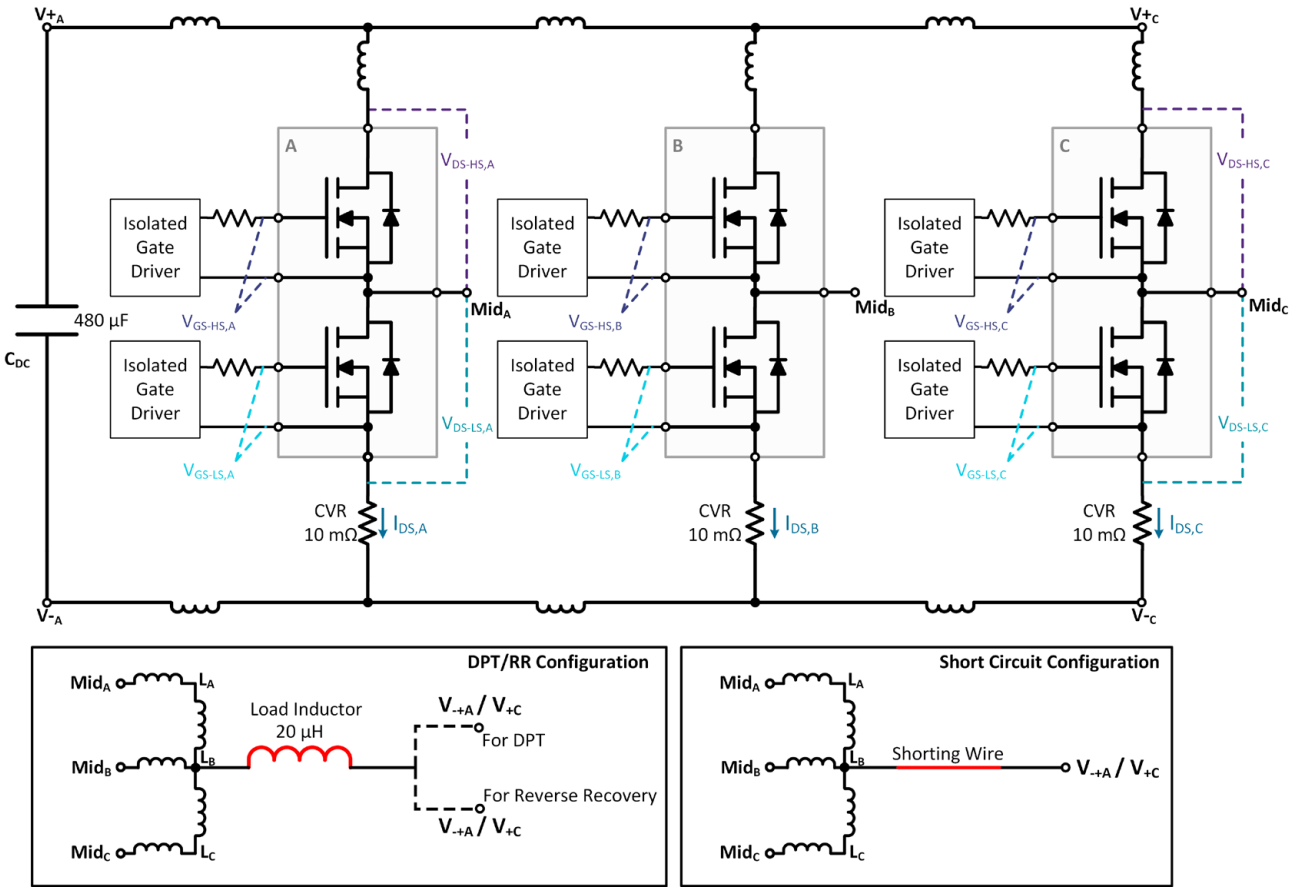


Figure 6: Paralleling study test circuit diagram

and a drain-source current through each module (I_{DS}). For the V_{GS} and I_{DS} measurements, a unique measurement exists for each module (A, B, C) and is denoted as such in the diagram. The V_{DS} measurements differ slightly as they should be identical for each module. However, on the PCB, V_{DS} can be measured on the far left of the PCB (by *A*) or on the far right of the PCB (by *C*). By default, V_{DS} is measured by module *A* unless otherwise specified. All measurements follow the procedures and recommendations described in PRD-08333.

A picture of the assembled PCB is shown in Figure 7 and Figure 8. In Figure 7, each screw terminal represents a location that the load inductor can be attached to and is labeled according to Figure 6. The board uses twelve 1.1 kV 40 µF capacitors (for a total of 480 µF) and no decoupling capacitors. The CVRs are 5 mΩ T&M Research® W-2-005-2FC, but modified to be 10 mΩ and with the insulator cut. The V_{DS} measurement test points can be found on the left and right sides of the board. Figure 8 shows the system in a measurement rack in the Figure 6 configuration. The load inductor is attached to L_B, the RR inductor connection is attached to V_{-A}, and the DPT inductor connection is attached to V_{+C} (a relay is used to automatically connect and disconnect these inductors to switch between DPT and RR tests). Each XM module is driven by its own independent CGD12HBXMP gate driver. A single CGD12HB00D differential transceiver board provides the power and logic signals to the three gate drives; the twisted-pair ribbon cable from this transceiver board connects to each gate driver from A to B to C sequentially, shown in Figure 9. This configuration will cause a non-insignificant propagation delay difference between the gate drivers of each module.

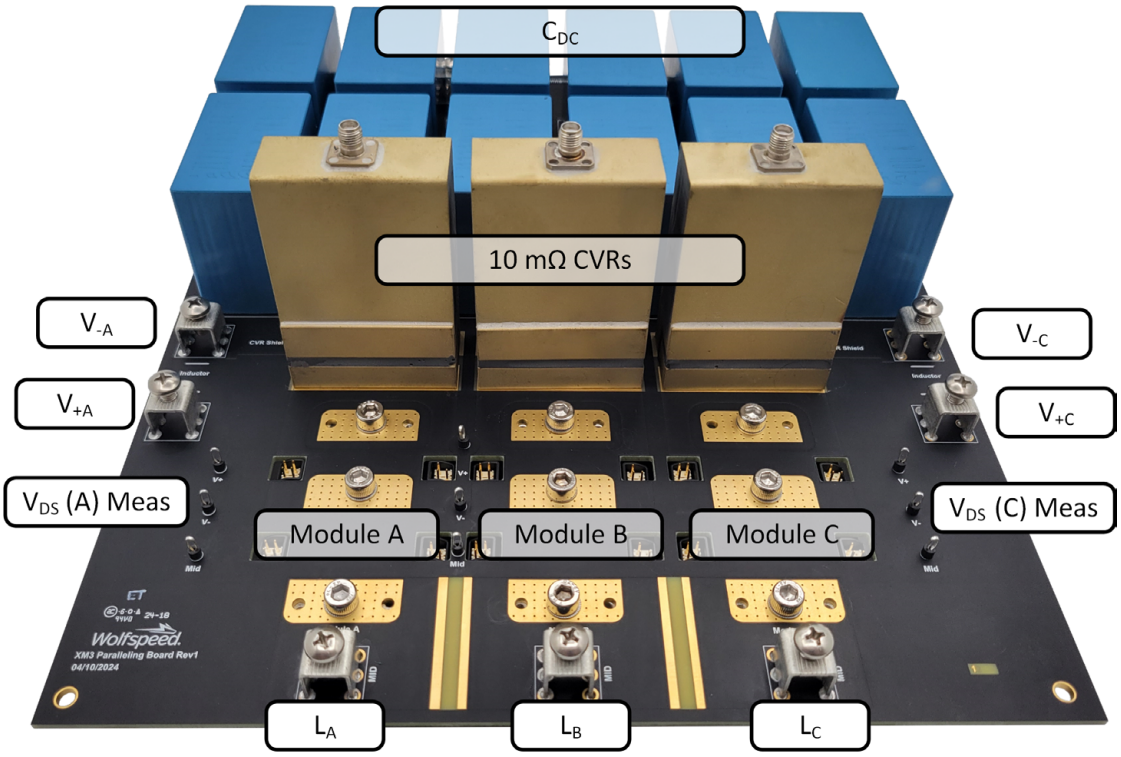


Figure 7: Paralleling study PCB (without gate drivers attached)

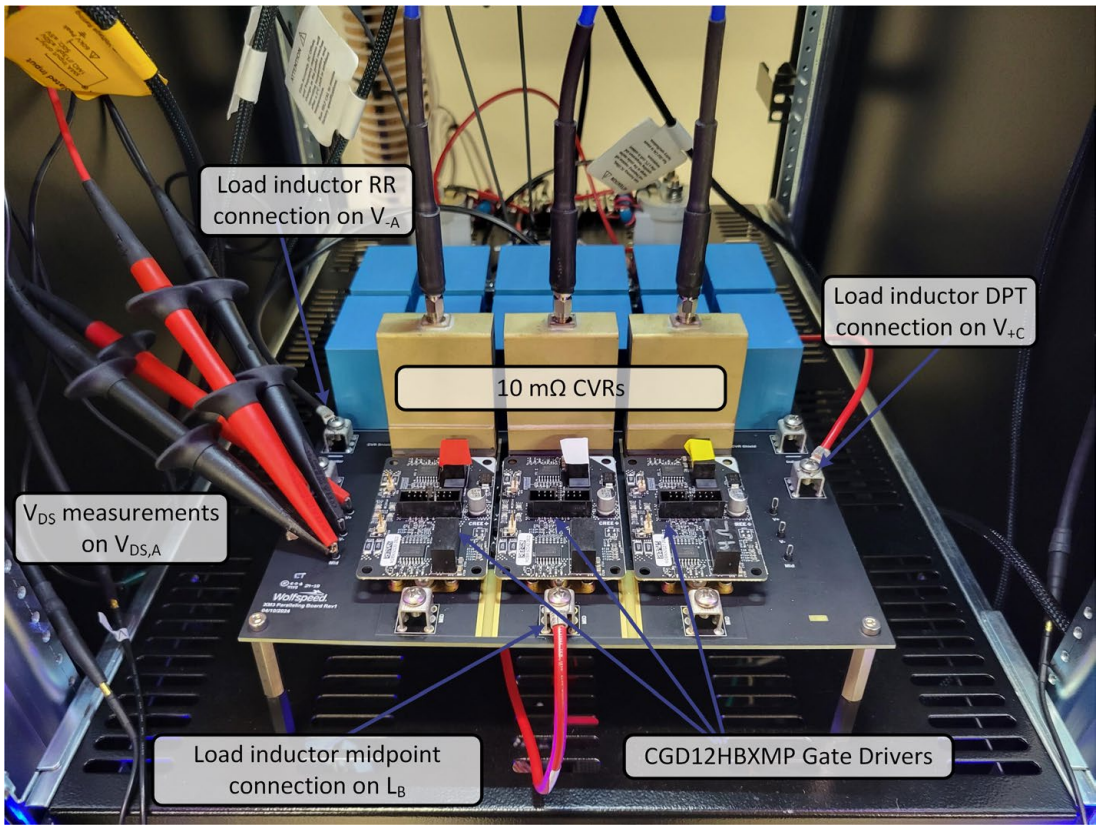


Figure 8: Paralleling study PCB (fully attached to system)

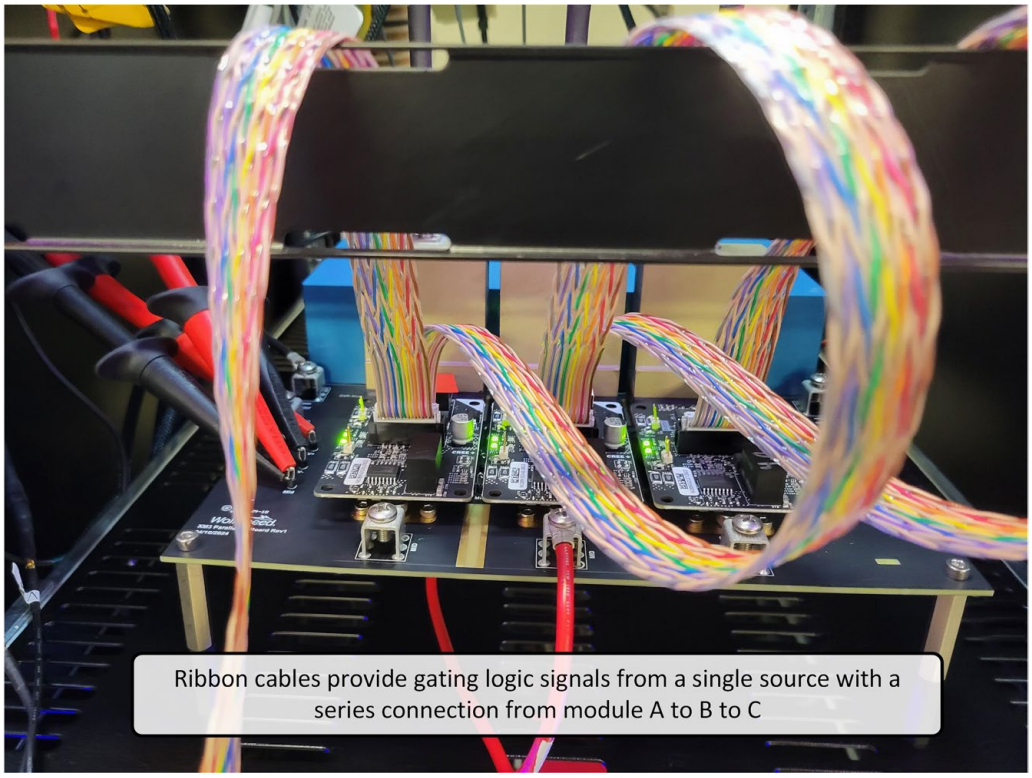


Figure 9: Ribbon cable (logic signal) connections to gate drivers

3.2 Short Circuit Configuration

During operation, failures in the system may cause the MOSFETs to be subjected to the entire bus voltage while biased ON. Such a condition is called a short-circuit event [5], [6]. The high-power loss in the MOSFET during this condition causes the device to heat up rapidly, such that material failures can occur within several microseconds. Gate drivers are often designed with short-circuit protection circuits that can turn off the device when such a fault is detected. This document will demonstrate how current mismatch can manifest in short-circuit conditions, and how short-circuit protection circuits are still effective when applied to paralleled modules.

The test circuit in Figure 6 can be adapted to perform short-circuit testing by replacing the load inductor with a shorting wire. In this testing, the shorting wire is connected across the high side of the modules between Mid and V+. During testing, the high side switches are held OFF. To initiate the testing sequence, the low side switches are turned ON. This creates a fault-under-load condition where the bus voltage falls across the low side switch while turned ON. See PRD-08296 for more information on short circuit fault types. All other equipment and metrology connections remain the same as for the DPT/RR testing.

A picture of an example short circuit test setup is shown in Figure 10. For this configuration, the shorting wire is connected from L_B to V_{+A}. The CGD12HBXMP gate driver includes a DESAT overcurrent protection circuit with a <1 µs response time.

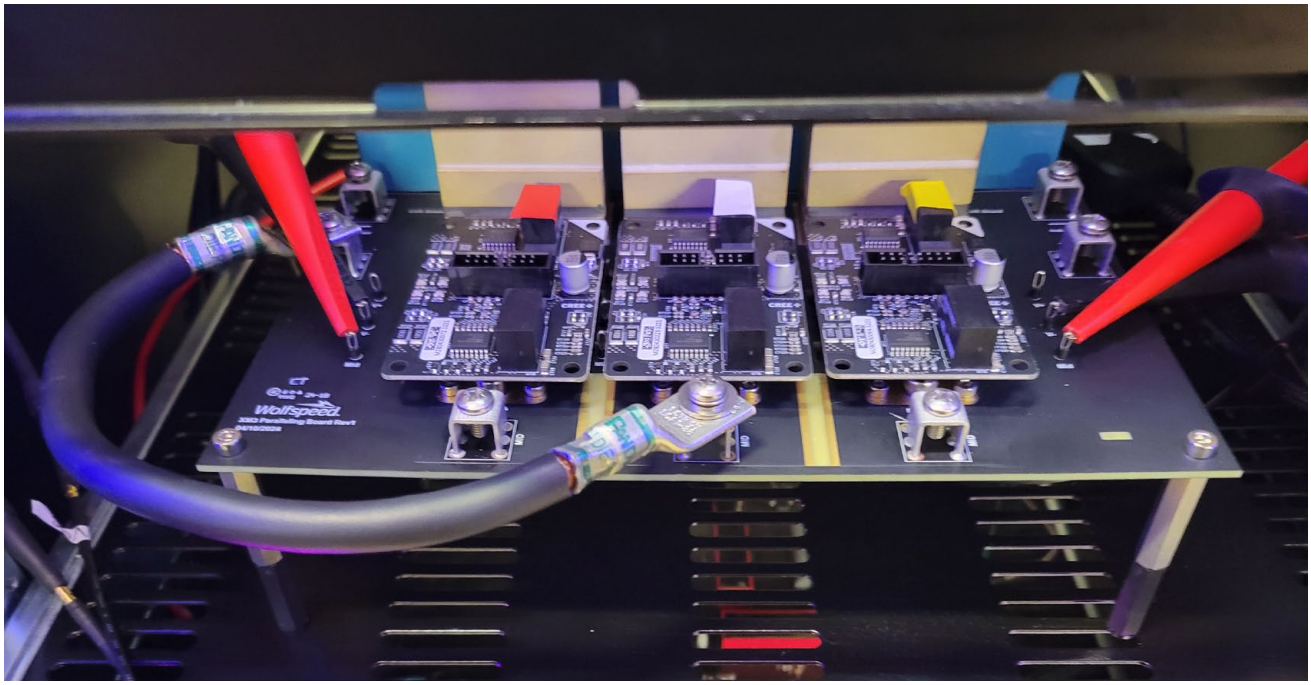


Figure 10: Example short-circuit test configuration

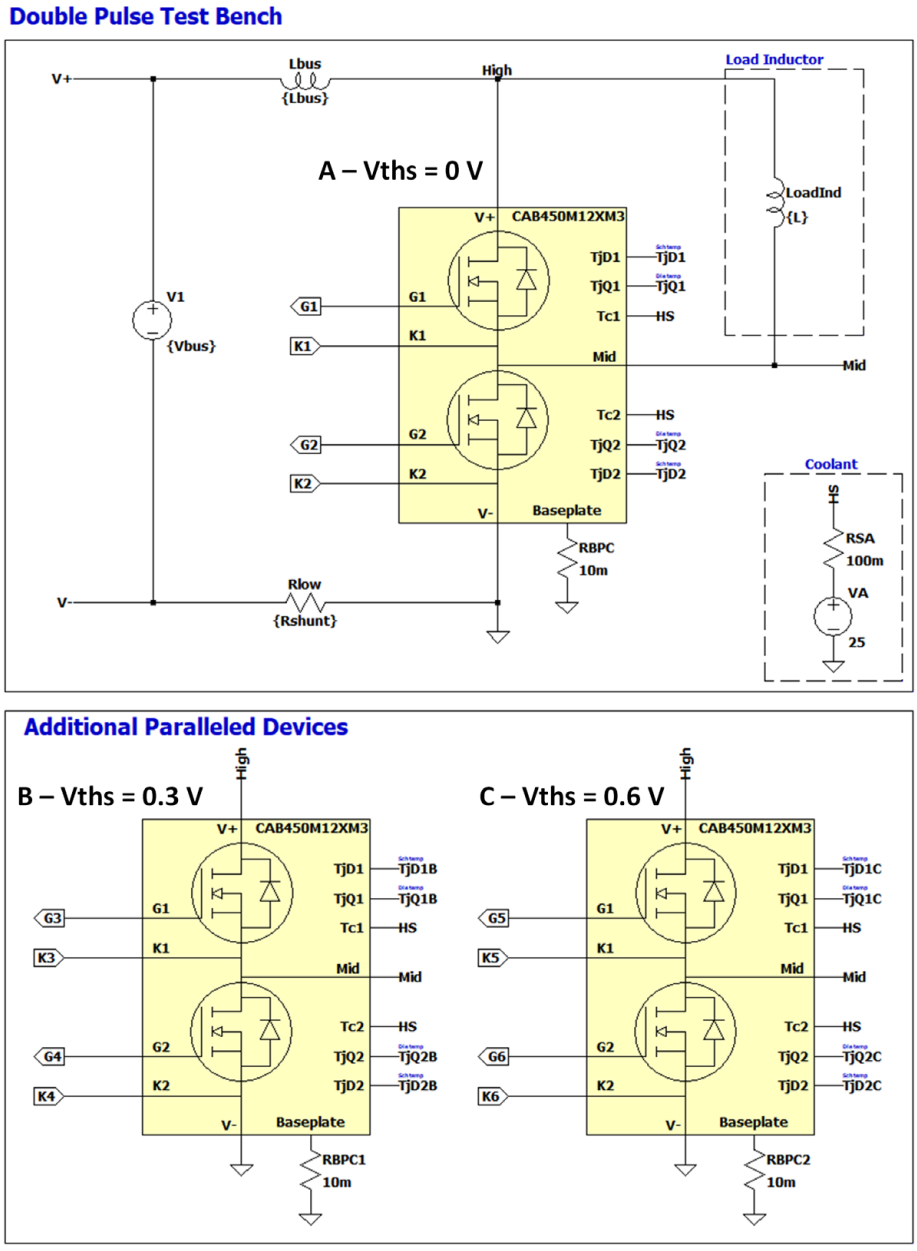
4. Leveraging SPICE Simulation Models

SPICE simulation can be leveraged in conjunction with the empirical testing to evaluate various conditions and mitigation techniques. Wolfspeed provides SPICE models of all its commercial modules. These models are highly configurable for paralleling analysis. While SPICE models will not provide exact results, they are useful for evaluating trends, estimating behavior, and evaluating mitigation techniques. These models can be used to rapidly evaluate systems without the need for physical hardware.

Refer to PRD-07913 for detailed information on downloading and using the SPICE models. Wolfspeed's video series on SPICE models may also be helpful, found here and here. The SPICE models and these documents can be downloaded from Wolfspeed's website here. When used in LTspice, Wolfspeed's module SPICE models can:

- Simulate efficiently in complex circuits [7]
- Accurately predict switching behavior due to employed dynamic tuning process [8]
- Have their internal characteristics (parasitic elements, $R_{DS,ON}$, V_{TH}, etc.) easily edited from the SpiceLine
- Predict junction temperature with embedded Z_{TH} characteristics

The Wolfspeed CAB450M12XM3 SPICE model will be used to demonstrate trends and evaluate parasitic effects. An example double pulse test circuit with two modules added in parallel is shown in Figure 11. In this example, the threshold voltage parameter, 'Vths', is changed for modules *B* and *C*. Here, setting Vths to a positive value increases the threshold voltage of the module by that value. In the simulated drain currents in Figure 11, module *A* (which has the lowest V_{TH}) turns on first and is subject to more current than *B* and *C*. These results follow the expected trends of V_{TH} imbalance in paralleled SiC MOSFETs [9].



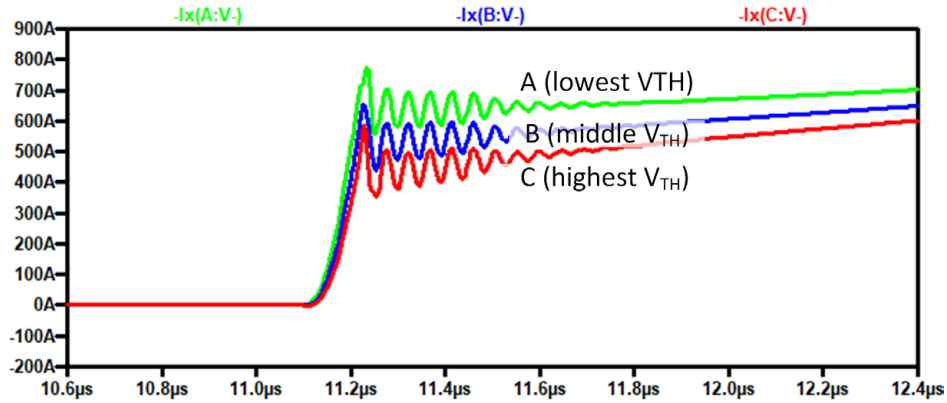


Figure 11: Example LTspice simulation setup with V_{TH} imbalance

5. General Paralleling Guidelines

This section provides a brief overview of the recommendations for paralleling power modules in designs. Some of these guidelines are discussed in more detail throughout later sections. Designing any power electronics system requires attention to detail of the system layout and gate driver configuration for various reasons – electromagnetic interference, crosstalk, stability, current sharing, manufacturability, etc. This document primarily focuses on the *thermal* influences of paralleling modules, but of course it is important to continue considering the fundamentals of power electronics design.

5.1 Gate Driver Design

The gate driver design should be carefully considered during the design process of a SiC application [10] - [13]. Wolfspeed provides design files for reference gate driver designs to assist with new designs. Some general specifications to consider when researching gate drivers are:

- A supply voltage with both positive and negative V_{GS}
- Common-mode transient immunity of 100 kV/µs and above
- Insulation voltages at or above the working voltage of the application
- Sufficient current driving capability
- Propagation delay and variability
- Active Miller clamp
- Short-circuit protection

More information on these considerations are discussed here.

There are three approaches for implementing gate drivers in paralleled applications shown in Figure 12. The first method uses a common gate driver directly connected to each paralleled switch position. The second method uses a single gate driver, but an additional buffer stage is added at the gate/kelvin-source of each module. The third uses an individual gate driver for each module switch position. Each implementation has its own advantages and drawbacks that should be considered for a design.

Common Gate Driver

The common gate driver approach is inexpensive and inherently provides an identical input to each device in parallel. When implemented properly, this approach offers the best dynamic current balancing. If it is possible to implement a common gate driver approach effectively in a design, it is recommended. However:

- It is important to ensure that the gate driver can provide the necessary current for the devices; each added device will require additional current during turn-on and turn-off events.
- Adding parallel devices may change the switching speed of the entire system
- Differences in stray inductance and slew rates (di/dt) in paralleled devices can cause a voltage differential between the kelvins of each module. This will then induce a current to flow between the module kelvins [12] which can affect the gate drive voltages of each device and present stability issues

- Routing to each module while following proper layout guidelines (minimized coupling to the power loop, minimized parasitic inductance) can be challenging.
- Implementing protection circuits becomes more complex.
- The gate loop inductance will be inherently large because of the necessary routing between the gate driver and each module.

Common Gate Driver with Additional Buffer Stages

Adding additional buffer stages at the gate-kelvin of each module alleviates some of the disadvantages of the common gate driver approach:

- The gate loop inductance is defined between the buffer stage and the module; thus, the gate loop inductance can be decreased significantly and better matched between modules with the additional buffer stage.
- Each buffer can supply the gate drive current to each switch and provide higher drive strength (faster switching) to each device.

This method does introduce minor complexities, such imbalances between the characteristics of the buffers themselves. Dynamic imbalance will be worsened by the introduction of asymmetric gate driver parts.

Multiple Gate Drivers

The multiple gate driver approach incurs additional cost and requires that the propagation delay and other characteristics of the gate drivers be matched. Imbalance will be worsened by asymmetric gate driver behavior. However, it alleviates some complexity and offers a more robust solution. Below are some advantages and disadvantages to this approach:

- The gate driver can be designed for a single module, then copied for each device (easier design)
- Adding additional devices in parallel does not change the switching speed of each individual device
- Protection circuits can be easily implemented on a per-module basis. A system may still operate at reduced capacity if one device fails (additional redundancy)
- Easier servicing of damaged components by replacing a single module/gate driver
- The kelvin of each module is isolated, and stray currents cannot flow between them (this alleviates effects caused by parasitic mismatch)

For all implementations, ensure that the gate resistance is added directly at the module pins. This will reduce the current flow into each gate caused by crosstalk between devices or coupling from the power loop. It is highly recommended to include resistance on the kelvin of each device; allocating 2/3 of the total resistance to the gate and 1/3 of the resistance to the kelvin is recommended (using a constant 1 Ω on the kelvin is also sufficient). For designs using a 0 Ω gate resistance, evaluate the system thoroughly to ensure that its operation is stable at high load conditions. In general, when evaluating the gate driver, measure the gate-source voltage directly at the G-K terminals of the module, and use an optically isolated voltage probe with high common-mode rejection ratio.

Parasitic elements in the layout can affect the system's performance. The parasitic inductances (L_{G1}, L_{K1}, L_{G2}, and L_{K2}) should be minimized and matched between paralleled devices to prevent asymmetric driving currents, minimize voltage overshoots, and improve stability at the die. Capacitance between the power loop and the gate loop should be minimized as much as possible. Voltage transients can couple from the power loop to the gate loop across this parasitic capacitance and affect switching behavior and stability. If this parasitic is mismatched across devices, the switching speed of the devices can become asymmetric and contribute to imbalance.

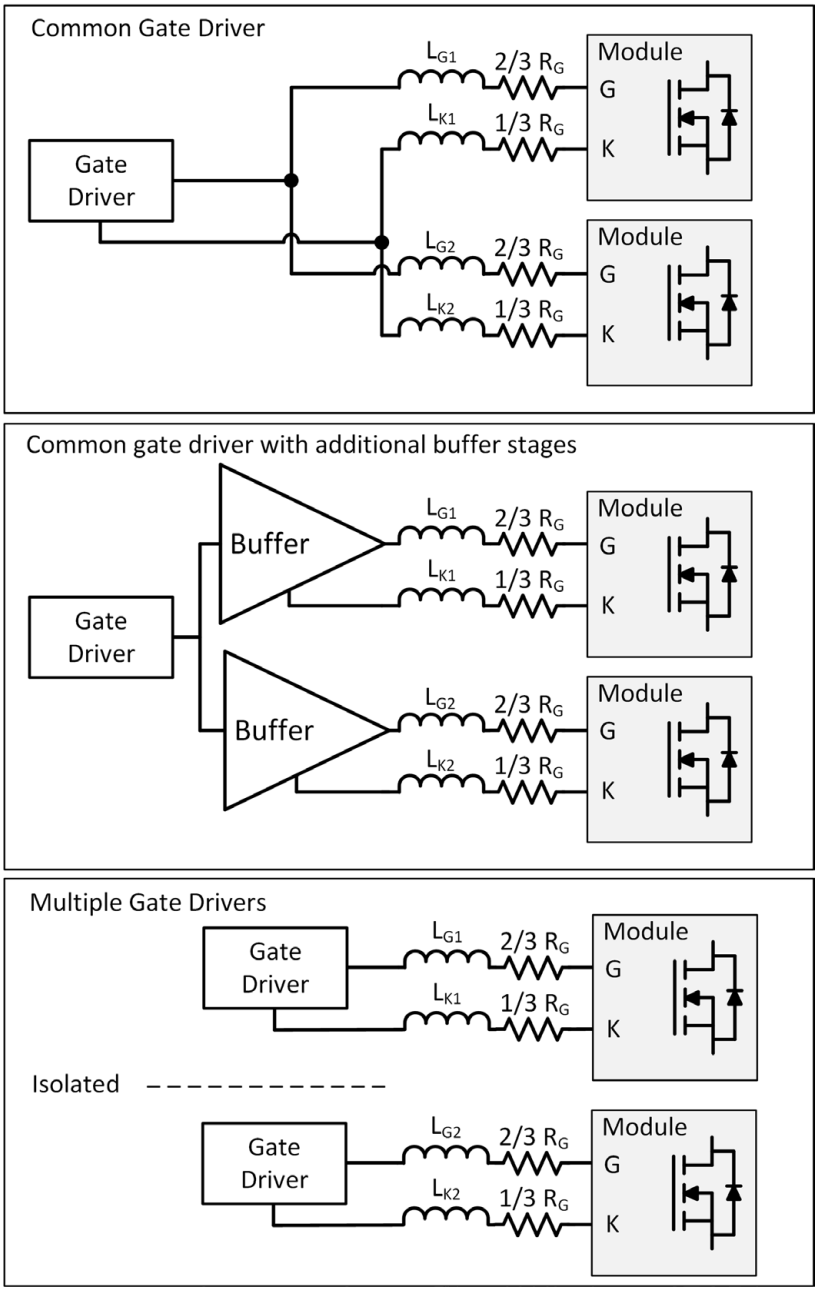


Figure 12: Common gate driver and multiple gate drivers solutions

5.2 Power Layout Design

Designing the power loop for parallel modules requires optimizing for symmetry between devices. For example:

- Ensuring that the stray inductance from each module to the decoupling and bus capacitors are identical
- Minimizing any coupling between the power and gate loops. Physical separation between the gate and power layout is recommended. If the power and gate loops are on the same PCB, do not overlap traces. Symmetric layout ensures that any coupling in the system is the same between paralleled devices.
- Ensuring load impedance matching and implementing mitigation techniques. In traditional power electronics design, connections to the midpoint of the module are often assumed to be unimportant because of the high impedance of the load. However, when paralleling devices, the switch positions of the power modules are placed directly in parallel and do not include the load, as shown in Figure 13. Thus, any mismatch between these loops will result in asymmetric current flow during dynamic events. Even small nH imbalances can result in significant imbalance. General intuition suggests directly connecting the midpoint terminals together with a bus bar; however, this may still result in a poorly matched system. Alternative approaches involve terminating the midpoints at the load (for example, connecting each midpoint to a motor using individual matched cables). Refer to section 8.2 for more detail on how this can be implemented for different topologies.
- Minimize potential module parameter mismatch by following the procedures outlined in 6.2. Ensure that all other components (gate drivers) are matched. Symmetry is the key to successful design.

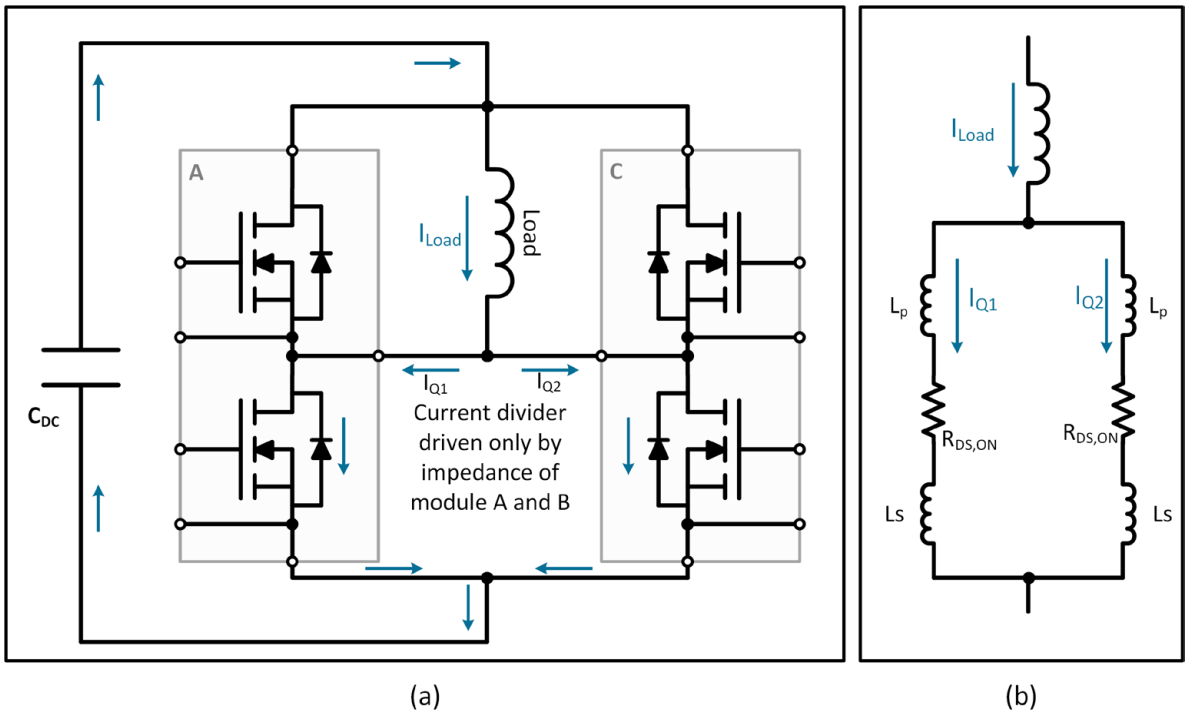


Figure 13: CIL circuit showing current divider between paralleled modules during turn-on

5.3 Cooling Design

The temperature of a device is dependent on both the power loss and the heat dissipation to the environment. Two modules with identical current flow can operate at different temperatures if one module is able to dissipate its heat more efficiently. Below are some recommendations.

- For flat baseplate modules, ensure a consistent and proper application of the thermal interface material (TIM) to each module. The TIM constitutes a non-negligible portion of thermal resistance in the system. PRD-07933 and PRD-08376 are useful resources on this topic. Modules with a pre-applied TIM application are available for some modules, which have improved consistency. When available, pin-fin modules provide the best thermal performance and matching between devices because TIM is not required. In addition, these modules are not susceptible to any pump-out or dry-out related failures caused by temperature cycling of TIMs.
- Ensure that the heat sink is at a uniform temperature for the paralleled devices. For example, consider the cooling flow in Figure 14 for three paralleled modules. As the coolant flows across each device, it will absorb energy and increase in temperature. As it exits the heatsink, it is at a slightly higher temperature than at the inlet, decreasing the potential cooling for the module on the right. This can be minimized by increasing the flow rate, increasing the thermal mass of the coolant (more volume), or adjusting the direction of flow in the heatsink.
- Add adequate spacing to the center module. The module in the center of the heatsink will have less available space to dissipate its heat, as it must share a portion of the heatsink with the surrounding modules. However, the modules on the edge of the heat sink have open edges to dissipate their heat. This is known as cross-heating, where the center device operates at a higher temperature than the edge devices. If the center device is crowded by the edge devices, it can cause the temperature imbalance to increase.

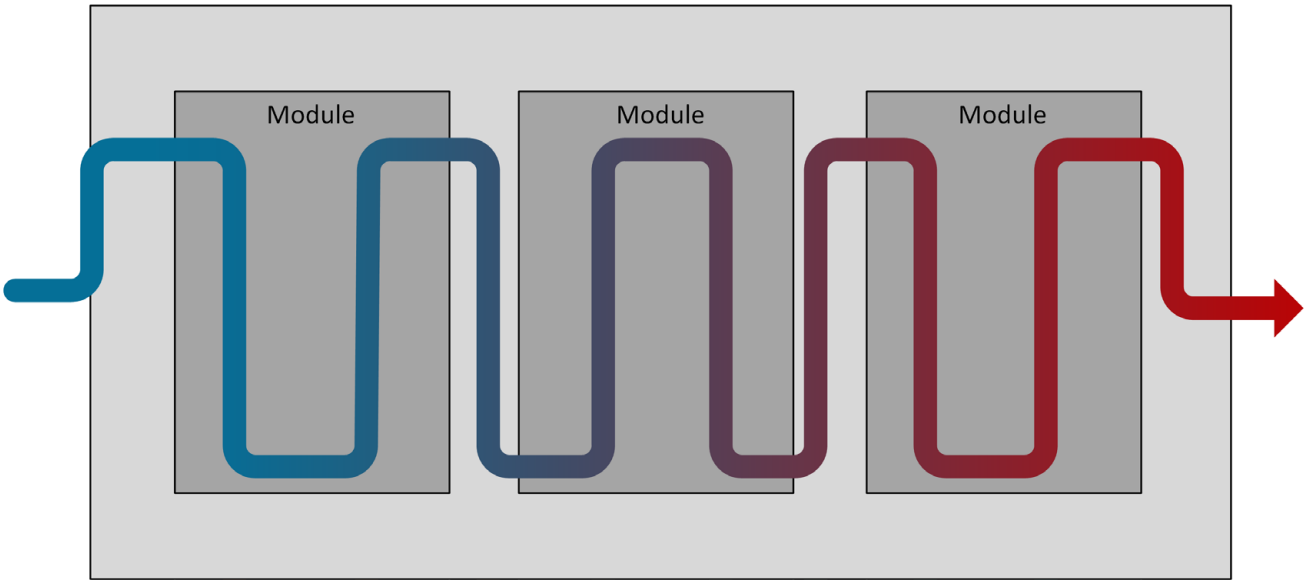


Figure 14: Non-uniform cooling sequence applied to paralleled modules

5.4 Evaluating Mismatch in Realized Systems

Quantifying the effects of imbalance during dynamic switching can be challenging because of the number of variables involved. Simulation can be useful for evaluating trends but is not practical for predicting *exact* system behavior because of the complexity of both the device behavior and the system parasitics. Evaluating an empirical setup can be useful, but this comes with the challenges of accurately measuring the signals with high bandwidth probes. In addition, for realized applications, it is notoriously difficult to measure the drain-source current of devices at high bandwidth, as measuring these signals requires inserting a shunt into the current path (example: the 10 mΩ bar shunts in Figure 7), choking the signal to a small cross-sectional area (current transformers), or have insufficient bandwidth (Rogowski coils). It is impractical for these devices to be included in final designs, and their insertion into the system can change the behavior. Another challenge is that switching can occur at various conditions – gate resistance, load current, bus voltage, etc. – which can affect dynamic current sharing, expanding the requirements for analysis.

A useful method for evaluating mismatch in a fully realized system is to probe the load current out of the midpoint of each module. There is a correlation between the mismatched dynamic current between modules and the resulting steady-state load current (section 8.2 [22]). Thus, a well-matched load current indicates well-matched current sharing between modules. In addition, because the bandwidth requirements are lower (and the load is often a cable), methods such as Rogowski coils can be used for this measurement.

6. Understanding Module Parameter Mismatch

During normal operation, the sources of loss within a MOSFET can be distinguished into two categories: conduction and switching losses (see Figure 15). Conduction losses occur when the device is fully biased ON and is conducting current. Conduction losses are sensitive to the $R_{DS,ON}$ of the MOSFET and the magnitude of the current flow through the device; higher operating current will exacerbate any imbalances associated with conduction losses. Switching losses occur when the device transitions between the OFF and ON states and are sensitive to many of the operating parameters of the system – voltage, current, gate resistance, switching frequency, etc. – along with the dynamic parameters of the device itself. These parameters include internal gate resistance, device capacitances, and threshold voltage. $R_{DS,ON}$ and V_{TH} are generally recognized as being the most critical parameter for current sharing performance in paralleled systems [9], [15]. When scrutinizing these characteristics, it's important to consider the end application. For example, a circuit breaker application, which relies almost entirely on DC current conduction of the switch, would be sensitive to $R_{DS,ON}$ and not V_{TH}. However, a DC-DC application switching at 40 kHz may be highly sensitive to V_{TH}, but not to $R_{DS,ON}$.

The influence of $R_{DS,ON}$ and V_{TH} mismatch between modules is shown in Figure 16. In Figure 16 (a), the device with lower $R_{DS,ON}$ will conduct more of the total current and have higher losses. Discrepancies in power dissipation between paralleled devices for conduction losses is easy to calculate, as it only depends on the $R_{DS,ON}$ of each part and the total current of the system. In this example, the device with lower $R_{DS,ON}$ has 28.7 % more conduction losses than the other paralleled device.

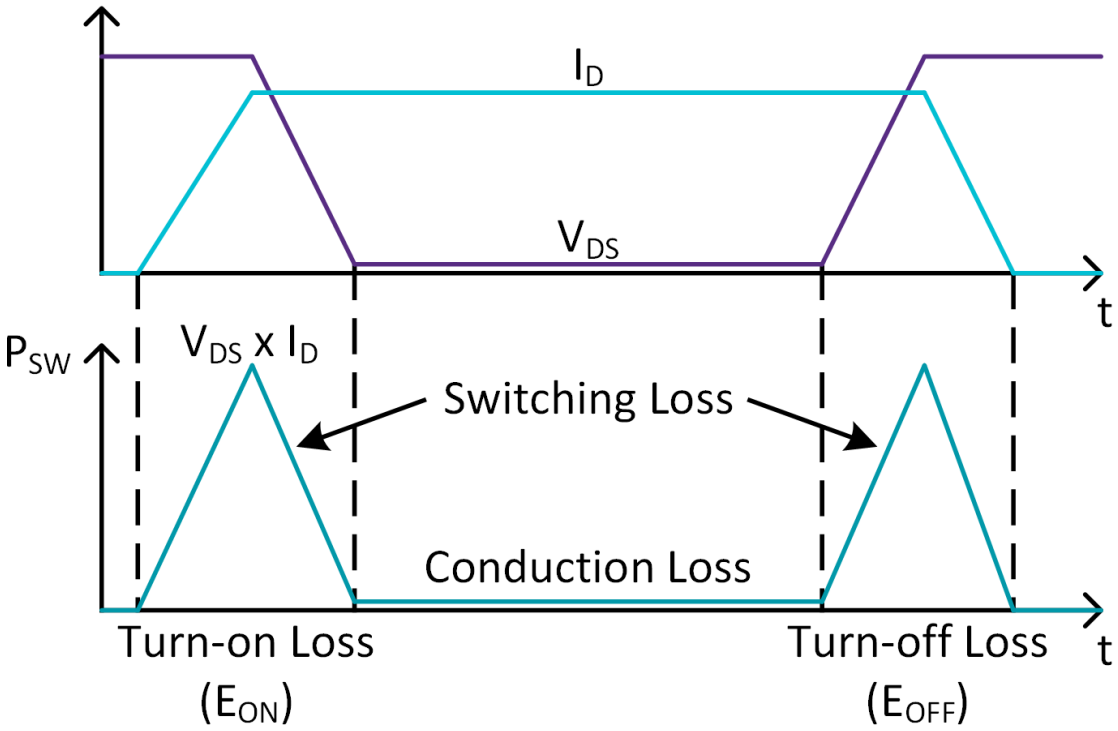


Figure 15: Distinction between conduction and switching loss

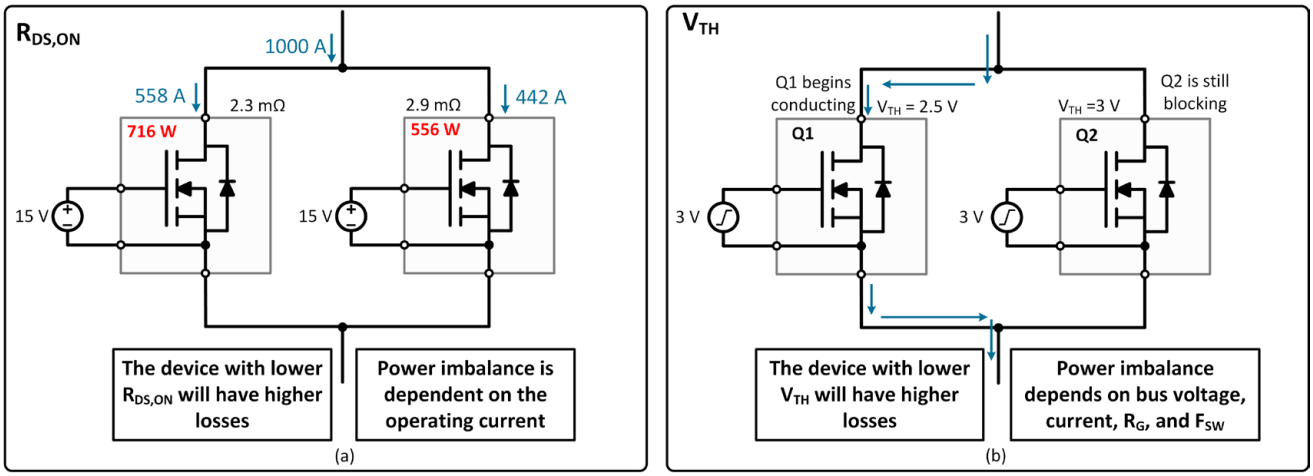


Figure 16: Influence of parameter mismatch on losses for (a) $R_{DS,ON}$ and (b) V_{TH}

In Figure 16 (b), the device with lower V_{TH} will conduct more current during the transitions between the OFF and ON states. In this example, the devices are transitioning from OFF to ON and each currently have a V_{GS} bias of 3 V. However, while Q1 has a V_{TH} of 2.5 V and will start conducting current, Q2 is still in its blocking state. Thus, during this time, Q1 will be subject to power losses while Q2 is not. In addition, even once both devices start conducting, Q1 will be further along its transconductance curve and continue to conduct more current throughout the entire switching event. The magnitude of losses due to V_{TH} are much harder to calculate than $R_{DS,ON}$ because it depends on the layout, gate driver, bus voltage, current, gate resistance, switching frequency, and the other dynamic characteristics of the device.

A major difference between $R_{DS,ON}$ and V_{TH} is how these parameters change with temperature. Figure 17 shows the relationship of $R_{DS,ON}$ and V_{TH} across temperature for a single CAB450M12XM3 power module. Between 25°C and 175°C, $R_{DS,ON}$ consistently increases, while V_{TH} consistently decreases. This trend can be observed by

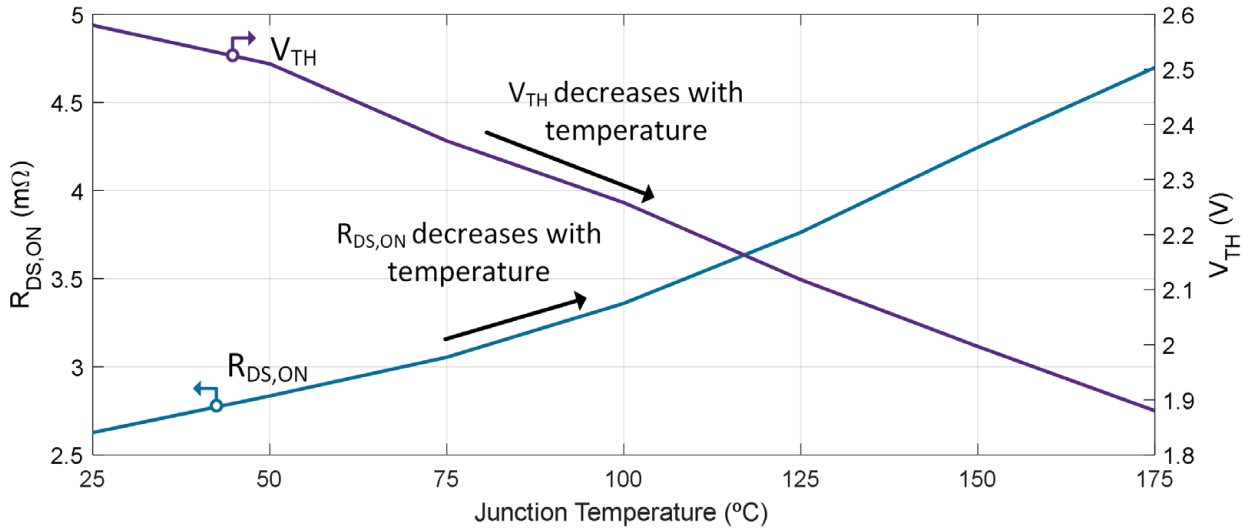


Figure 17: $R_{DS,ON}$ and V_{TH} trends for SiC MOSFETs across temperature

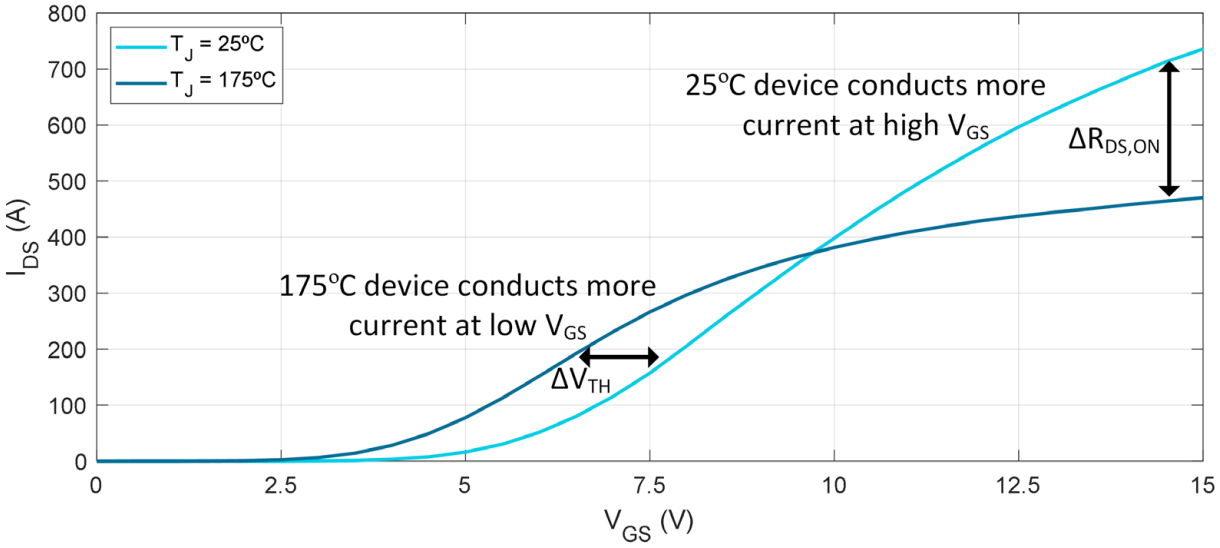


Figure 18: CAB450M12XM3 transfer characteristic comparison at 25°C and 175°C for V_{DS} = 2 V

comparing the 25°C and 175°C transfer characteristics of the device, shown in Figure 18. At low V_{GS} (between 2.5 V and 10 V), the device conducts more current at 175°C due to the lower threshold voltage. However, at V_{GS} biases above 10 V, the device conducts more current at 25°C due to the lower $R_{DS,ON}$. This concept is important for understanding how these parameters will affect the device temperature when switched continuously in an application. The characteristics of $R_{DS,ON}$ across temperature creates a negative feedback loop between power dissipation and device temperature (with regards to paralleling), as shown in Figure 19. Effectively, a device with lower $R_{DS,ON}$ will conduct more current than the other parallel devices and increase in temperature. This temperature increase causes an increase in $R_{DS,ON}$, which then reduces the imbalance relative to other devices. Eventually, the system will reach equilibrium when the $R_{DS,ON}$ of the parallel devices are matched at a certain temperature.

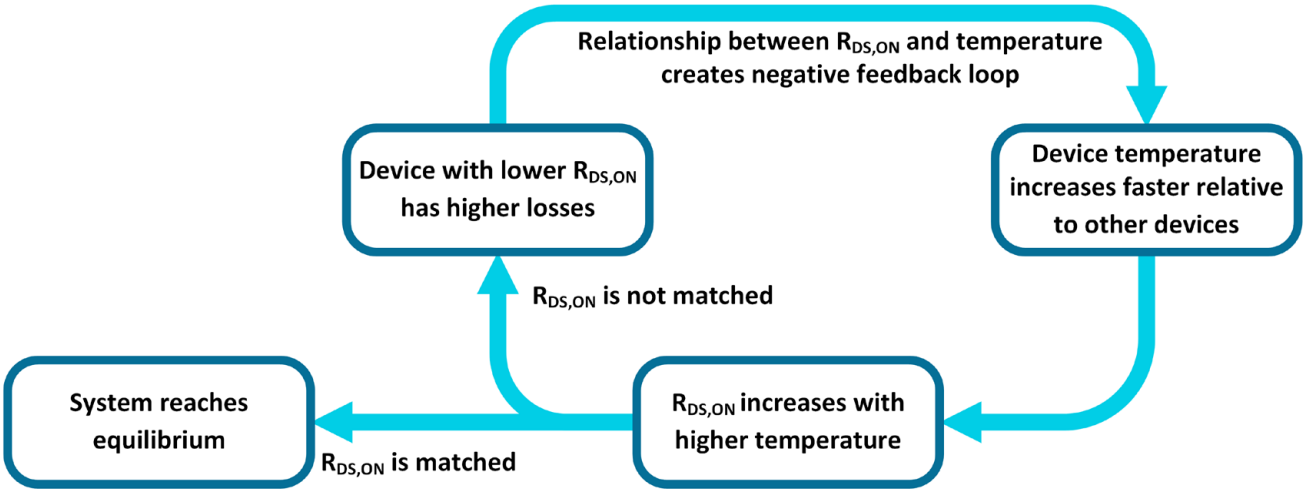


Figure 19: Negative feedback loop between $R_{DS,ON}$ imbalance and die temperature

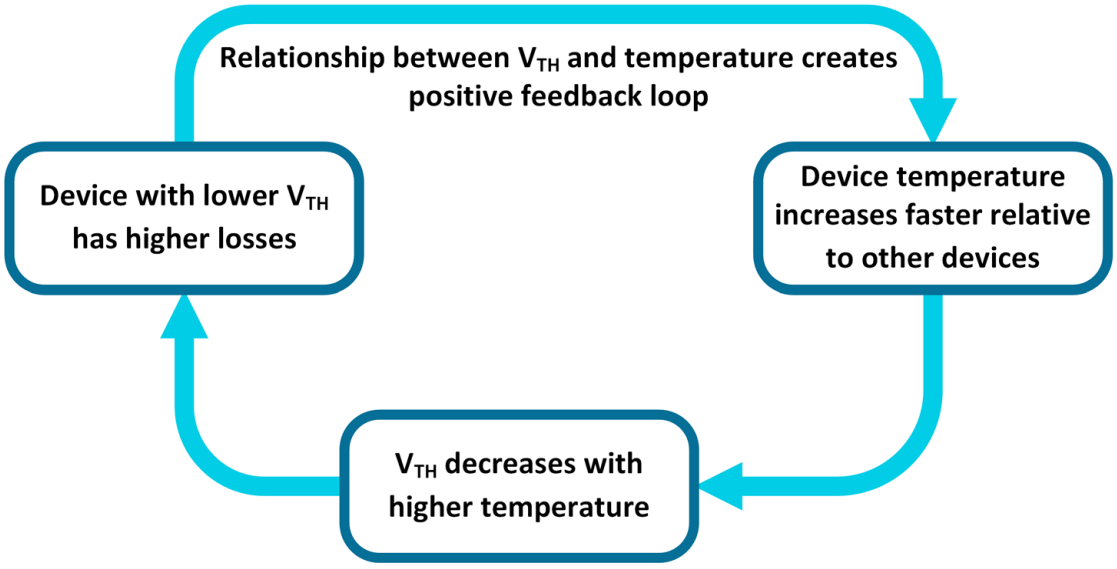


Figure 20: Positive feedback loop between V_{TH} imbalance and die temperature

On the other hand, V_{TH} creates a positive feedback loop between power dissipation and device temperature, as shown in Figure 20. Here, the device with lower V_{TH} will have higher losses and increase in temperature relative to the other die. However, this will cause the V_{TH} to further decrease, and cause the power dissipation imbalance to increase further, and so on. This feedback loop will continue until other balancing mechanisms stabilize the system. This positive feedback loop between V_{TH} and temperature exacerbates the parameter's influence on current sharing.

6.1 Other Parameters

The dynamic behavior of a SiC MOSFET is complicated and is dependent on many parameters. In this document, V_{TH} is the noted as the *most* important, as is also agreed with heavily in the literature [13] - [24]. The parameter is highly influential and easy to measure. However, other characteristics can also affect switching speed and dynamic current sharing. Figure 21 shows the most important of these parameters (device capacitances and internal gate resistance). In general, an increase in any of these parameters will cause the device to switch slower.

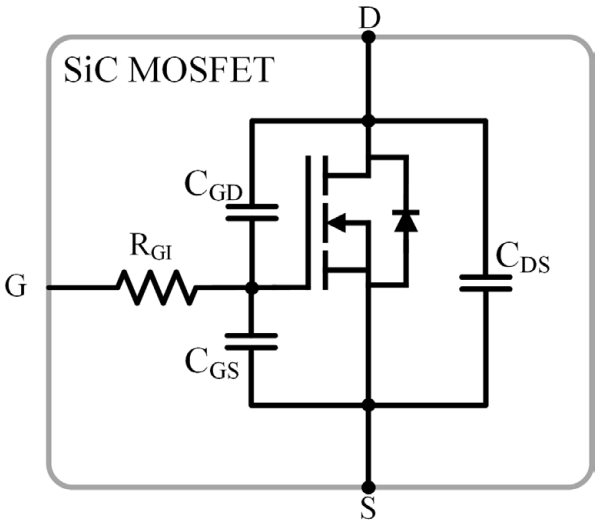


Figure 21: General structure of SiC MOSFET

6.2 Tips for Matching Modules

Matching the characteristics between paralleled modules can help mitigate current imbalance. There are several approaches to improve matching between modules described below.

Lot Matching: It is recommended that modules from the same "lot" should be placed in parallel. The lot describes a group of semiconductor chips manufactured at the same time under identical processes and will have similar characteristics. The lot can be identified by the serial number marked on an individual module. For example, two CAB450M12XM3 power modules marked H2119-N041 and H2119-N054 are from the same lot (**H2119)**, as indicated by the alpha-numeric sequence before the hyphen.

Time Matching: If modules across lots are mixed in parallel, it is important to ensure that the difference in manufacturing date is minimized. For example, two modules manufactured several years apart have a higher chance of parameter mismatch than modules manufactured within the same month due to variations in fabrication processes.

Binning: Binning describes the process of characterizing modules and placing similar devices together in parallel. This process greatly reduces the potential mismatch between devices but adds complexity to the system manufacturing process.

High-side/Low-side Matching: When paralleling modules, imbalance can exist both between paralleled high-side and low-side switch positions. The high-side and low-side switch positions of modules will have similar characteristics due to their proximity in the assembly process. Thus, it is acceptable to apply a binning process across a single switch position

7. Estimating Temperature Imbalance Caused by $R_{DS,ON}$ Mismatch

The effect of $R_{DS,ON}$ on temperature imbalance during operation is simple to estimate because losses can be calculated knowing the resistance of each module and the load current of the system. However, there are levels of complexity that can be considered. This document will discuss three methods for predicting temperature imbalance caused by $R_{DS,ON}$ differences between modules. The first is a simple analytical calculation method that only uses a single $R_{DS,ON}$ value for each device. The second is an iterative analytical method that considers the temperature dependence of $R_{DS,ON}$ for each device. The third is to leverage simulation that considers the more nuanced behavior regarding current sharing.

Option 1: Simple Analytical Calculation Method

Consider the simple circuit in Figure 22. Each resistor represents the on-state resistance of a module switch position at a particular temperature. To determine the current through each resistor, first determine the equivalent resistance, R_{eq}, of the network per equation (1). Then, use the known total load current and each individual resistor value to calculate each current per equation (2). The conduction losses can then be calculated per equation (3). These formulas can be adjusted based on the application, but it is important to be careful in converting the load current to the correct RMS value for the power calculation. For example, in a DC-DC converter system with 50% duty cycle switching at 400 A peak, the RMS current would be $400 * \sqrt{(2)} * 0.5$. Finally, use equation (4) to determine the steady-state temperature of the device. Here, $R_{TH,JC}$ is the thermal resistance from the MOSFET junction to the case, $R_{TH,SA}$ is the thermal resistance from the case to the coolant (or ambient air), and $T_{Ambient}$ is the temperature of the coolant (or ambient air). P_{nRMS} represents the average power loss during continuous operation. For example, for a buck converter with a 50 % duty cycle, P_n would be multiplied by 0.5 to get P_{navg}.

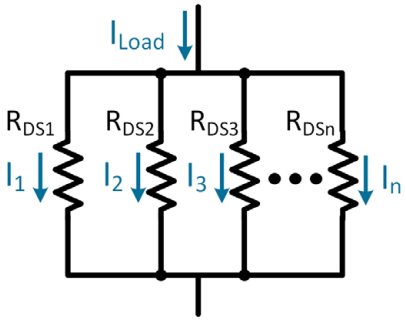


Figure 22: Equivalent circuit for n parallel modules

$$R_{eq} = \frac{1}{\sum_1^n \left(\frac{1}{R_{DSn}}\right)} \quad (1)$$

$$I_n = \frac{\left(I_{Load} * R_{eq}\right)}{R_{DSn}} \quad (2)$$

$$P_n = I_{n,RMS}^2 * R_{DSn} \quad (3)$$

$$T_{Jn} = P_n * \left(R_{TH,JC} + R_{TH,SA}\right) + T_{Ambient} \quad (4)$$

Consider the CAB450M12XM3 as an example. Figure 23 shows the relevant characteristics from the datasheet that are needed for these equations. First is the on-state resistance of the part, which for this module is provided as a typical of 2.6 mΩ and a max of 3.4 mΩ at 25°C. Second is the $R_{TH,JC}$ of the module, which is 0.094 °C/W.

Drain-Source On-State Resistance (MOSFET Only)	$R_{DS(on)}$		2.6	3.4	mΩ	V_{GS} = 15 V, I_D = 450 A	Fig. 2 Fig. 3
			4.7			V_{GS} = 15 V, I_D = 450 A, T_{VJ} = 175 °C	
FET Thermal Resistance, Junction to Case	$R_{th\,JC}$		0.094		°C/W		Fig. 17

Figure 23: CAB450M12XM3 relevant datasheet parameters

Next, assume some operating conditions: a buck converter with two modules in parallel, 50 % duty cycle, 900 A total load current, a coolant temperature of 25°C, and an $R_{TH,SA}$ of 0.1 °C/W. To determine the worst-case spread, one module is defined as 2.6 mΩ and the other at 3.4 mΩ. The below equations show the computation process to use these datasheet parameters and operating conditions to calculate the T_J of each module. For these conditions, the 2.6 mΩ module has an expected T_J of 90.6°C, and the 3.4 mΩ module has an expected T_J of 75.2°C. Recall that the results of these calculations will be more pessimistic than reality due to ignoring factors such as the change of $R_{DS,ON}$ over temperature.

$$R_{eq} = \frac{1}{\frac{1}{2.6m} + \frac{1}{3.4m}} \rightarrow 1.4733\ m\Omega \quad (5)$$

$$I_1 = \frac{(900 * 1.4733m)}{2.6m} \rightarrow 510\ A \quad (6)$$

$$I_2 = \frac{(900 * 1.4733m)}{3.4m} \rightarrow 390\ A \quad (7)$$

$$P_1 = (510 * \sqrt{2} * 0.5)^2 * 2.6m \rightarrow 338.13\ W \quad (8)$$

$$P_2 = (390 * \sqrt{2} * 0.5^2 * 3.4m \rightarrow 258.57\ W \quad (9)$$

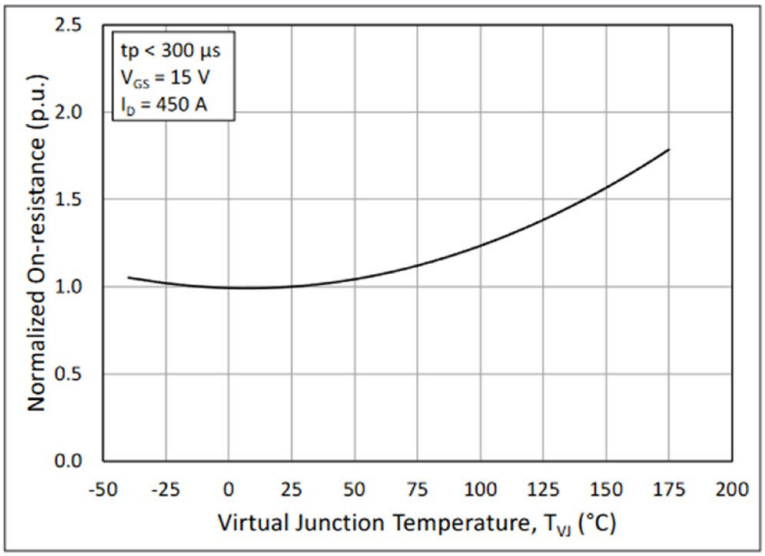
$$T_{J1} = 338.13 * (0.094 + 0.1) + 25 \rightarrow 90.6ºC \quad (10)$$

$$T_{J2} = 258.57 * (0.094 + 0.1) + 25 \rightarrow 75.16ºC \quad (11)$$

Option 2: Iterative Calculation Method

The simple calculation method will underestimate the average temperature of the modules and overestimate the difference in temperature between them. A more advanced approach is to consider the change of $R_{DS,ON}$ across temperature and use an iterative approach to solve for the final temperatures. To begin, first find the normalized On-State Resistance vs. Junction Temperature plot in the Wolfspeed datasheet. The datasheet figure for the CAB450M12XM3 is shown in Figure 24. Next, use a web-plot digitizer (example) to extract some data points from the curve. Optionally, the package resistance of the module (also shown in Figure 24) can be used to further improve the accuracy of the calculations (consider: the package resistance will change the overall current flow through each module but will not be dissipated as heat in the junction). If including the package resistance, simply modify equation (1) to equation (12) below.

$$R_{eq} = \frac{1}{\sum_1^n \left(\frac{1}{R_{DSn} + R_{package}}\right)} \quad (12)$$



Parameter	Symbol	Min.	Typ.	Max.	Unit
Package Resistance, M1 (High-Side)	R_{3-1}		0.72		mΩ
Package Resistance, M2 (Low-Side)	R_{1-2}		0.63		

Figure 24: Additional datasheet information necessary to perform the iterative calculation method

The iterative method can be performed by the following sequence:

1. Extract the normalized p.u. $R_{DS,ON}$ from the datasheet and multiply the results by the 25°C $R_{DS,ON}$
2. Use a curve fit to improve granularity of the extracted data. A 3rd order polynomial works well.
3. Define the offsets for each module in parallel (for example: two modules, +0 mΩ and +0.8 mΩ)
4. Start the iterative process by assuming that all die are at the starting coolant temperature. Use the temperature of each module and the polynomial curve fit to determine the resistance of each module.
5. Add the offsets from step 3 to each calculated resistance
6. Use equations (1) - (5) (and (12) if necessary) to solve for the temperature of each die
7. Repeat steps 4 – 6 until the temperature change of each die decreases to a desired tolerance.

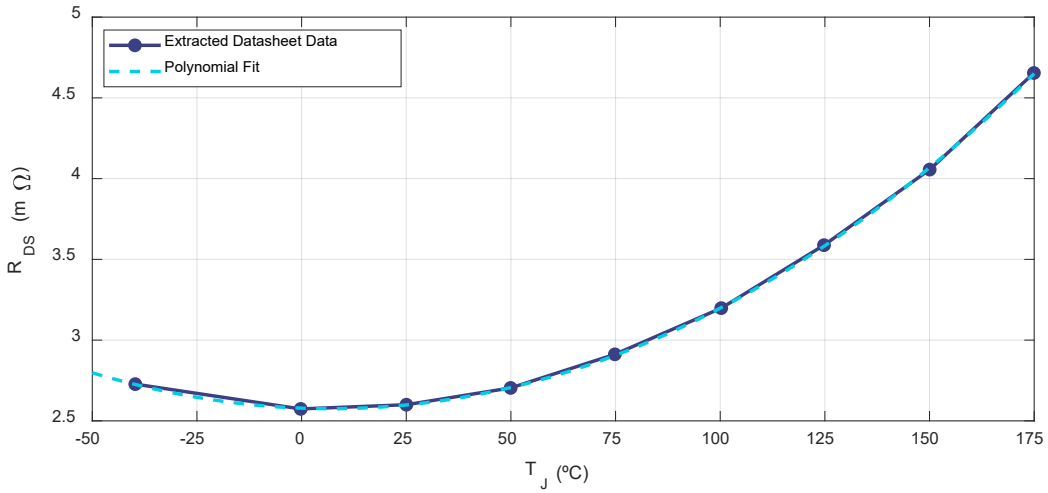


Figure 25: Polynomial fit of datasheet $R_{DS,ON}$ for a CAB450M12XM3 power module

This iterative approach was applied to the same conditions used for the simple calculation example. The polynomial fit of the digitized datasheet data for the CAB450M12XM3 power module is shown in Figure 25. The calculated temperature of both die at each iteration is shown in Figure 26. The method was calculated for two cases: one considering the package resistance, and one ignoring it. The final T_J of each die without the package resistance is 99.2°C and 86.7°C, while the final T_J of each die considering the package resistance is 97.4°C and 88.2°C – a modest difference. The average temperature of the die calculated using this result is higher than the simpler method, but the ΔT_J is much smaller – about 9°C, compared to the 15°C calculated previously.

MATLAB code for performing this iterative process described herein is provided on the following page.

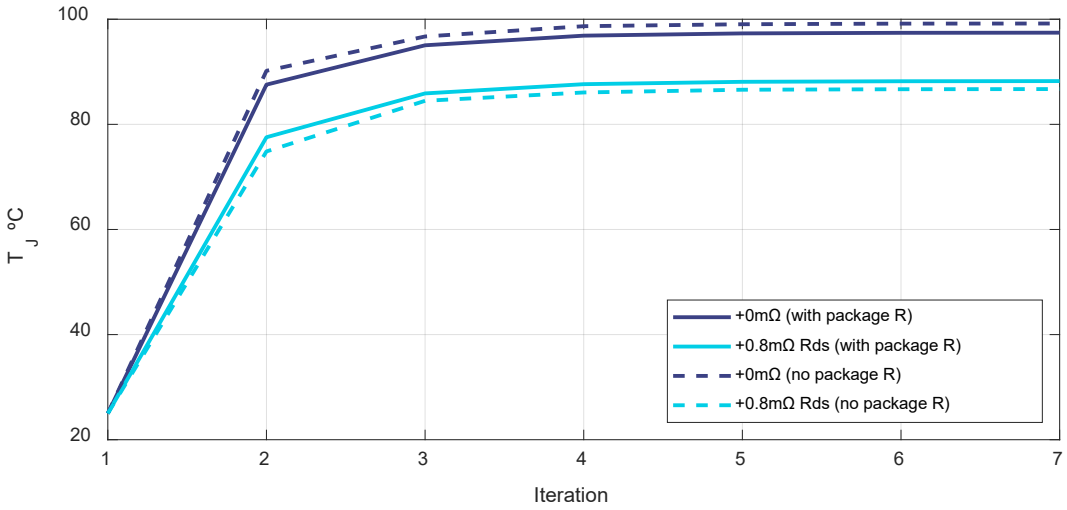


Figure 26: Junction temperature of parallel modules using iterative method

```
clear currTj saveTj

% Definitions
Rds_25C = 2.6e-3; % Rds(on) at 25C, from datasheet
R_Package = 0.63e-3; % Package resistance of analyzed switch
R_Offset = [0 0.8e-3]; % Rds(on) offset of each die. Make array larger

% Define system parameters
Rth = 0.094; % Thermal resistance from junction to case, C/W
Rsa = 0.1; % Thermal resistance from sink to coolant/ambient, C/W
Tjf = 25; % Coolant/ambient temp
duty = 0.5; % Duty cycle
Iload = 900; % Load current

% Digitized Data from Normalized On-Resistance Datasheet Plot
xdata = [-39.73, -0.209, 25.03, 49.93, 74.83, 100.24, 124.79, 150.034, 174.93];
ydata = [1.049, 0.99, 1.00, 1.04, 1.12, 1.23, 1.38, 1.56, 1.79];

% Convert p.u. Rds to actual Rds
ydata = ydata.*Rds_25C;

% Create polynomial fit
p = polyfit(xdata,ydata,3);

% Create new x data with more resolution
newx = [-50:1:175];

% Plot data and polynomial fit to validate
f = figure;
hold on
grid on
box on
xlabel('T_J (ºC)')
ylabel('R_{DS} (m\Omega)')
plot(xdata,1e3.*ydata,'linewidth',2,'color',[59 65 132]./255)
plot(newx,1e3.*polyval(p,newx),'linewidth',2,'color',[1 206 230]./255,'linestyle','- -')
set(gca,'FontName','Source Sans Pro','FontSize',13)
legend('Raw Data','Polynomial Fit','location','nw')

% Define variables to prepare for iterating
currTj(1:length(R_Offset)) = Tjf;
saveTj = currTj;
tol = 0.1;
err = inf;

% Begin iterating until specified tolerance is reached
while err > tol
    R = R_Package + polyval(p,min(currTj,175)) + R_Offset; % Calculate resistances & add offset
    Req = 1/(sum(1./R)); % Calculate equivalent resistance of network
    I = Iload.*(Req./R); % Calculate current through each Rds(on)
    Pwr = duty.*I.^2.*(R-R_Package); % Caclulate power of each Rds(on)
    currTj = Tjf + Pwr.*(Rth+Rsa); % Determine new temperature
    err = sum(currTj - saveTj(end,:)); % Determine change from last iteration
    saveTj(end+1,:) = currTj; % Store Tj in a save variable
end

% Final temperature of each die are stored in variable currTj
```

Option 3: Simulation Method

The last option discussed is to use SPICE simulation to determine the temperature imbalance. Refer to Section 3 for information on getting started with Wolfspeed SPICE models. Simulation offers the highest level of granularity and accuracy, does not require pulling information off the datasheet, and is simple to set up. Figure 27 shows an example circuit for paralleling the low side position of two CAB450M12XM3 power modules under a constant current condition. The unused temperature ports are connected to ground to disable them, the V+ node is connected to ground with a 1 GΩ resistor to prevent any current flow while removing floating nodes, and the G1/K1 pins are shorted together. The G2/K2 pins are connected to a 15 V voltage source. The TjQ2 pins are used to monitor the junction temperature of each module. The Tc2 pins are connected to their own cooling network. The 0.1 Ω resistors represent the $R_{TH,SA}$ parameter, and the 25°C voltage source represents the coolant/ambient temperature. Note that the $R_{TH,JC}$ characteristics are embedded within the thermal network of the module, so do not need to be included here. Finally, the current source injection into the model is handled with a voltage source in series with the diode. The diode has a specified current limit parameter that is used to limit the current into the modules. Vsource is set to an arbitrarily high voltage such that it will source up to the diode's current limit. Effectively, the current from Vsource will always be set to the 'Iload' parameter. This method is preferred over a simple current source, which causes issues with the DC solver.

The system was configured to match the conditions specified in the prior two methods. The load current was set to 636.4 A ($I_{RMS} = 900 * \sqrt{2} * 0.5 \rightarrow 636.4\ A$) to match the pulsed 50 % duty cycle condition with a DC signal. In the Spiceline2 of M1 (alt+right click the symbol), 'Rdss = 0.8m' was added to increase the on-state resistance of the module by 0.8 mΩ. The results of the simulation are shown in Figure 28. The top subplot shows

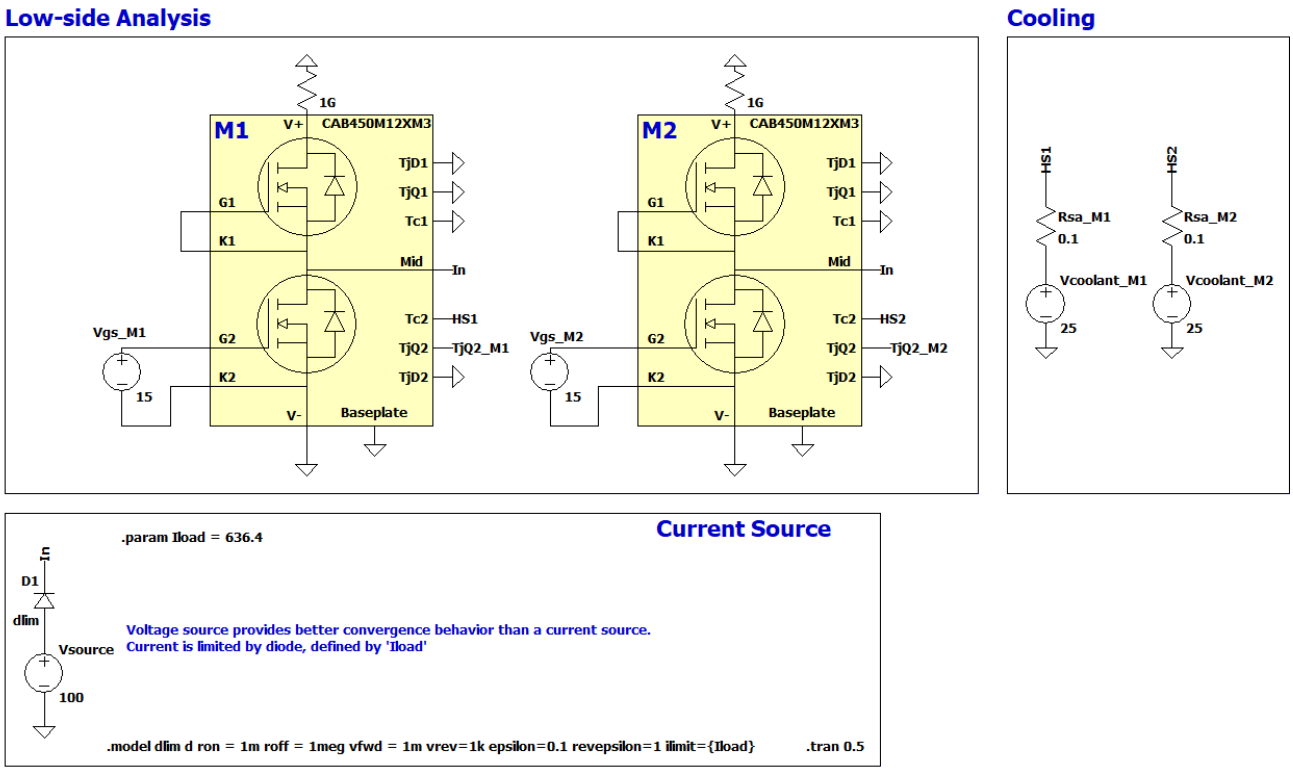


Figure 27: Simple LTspice circuit for paralleling DC current through two CAB450M12XM3 power modules

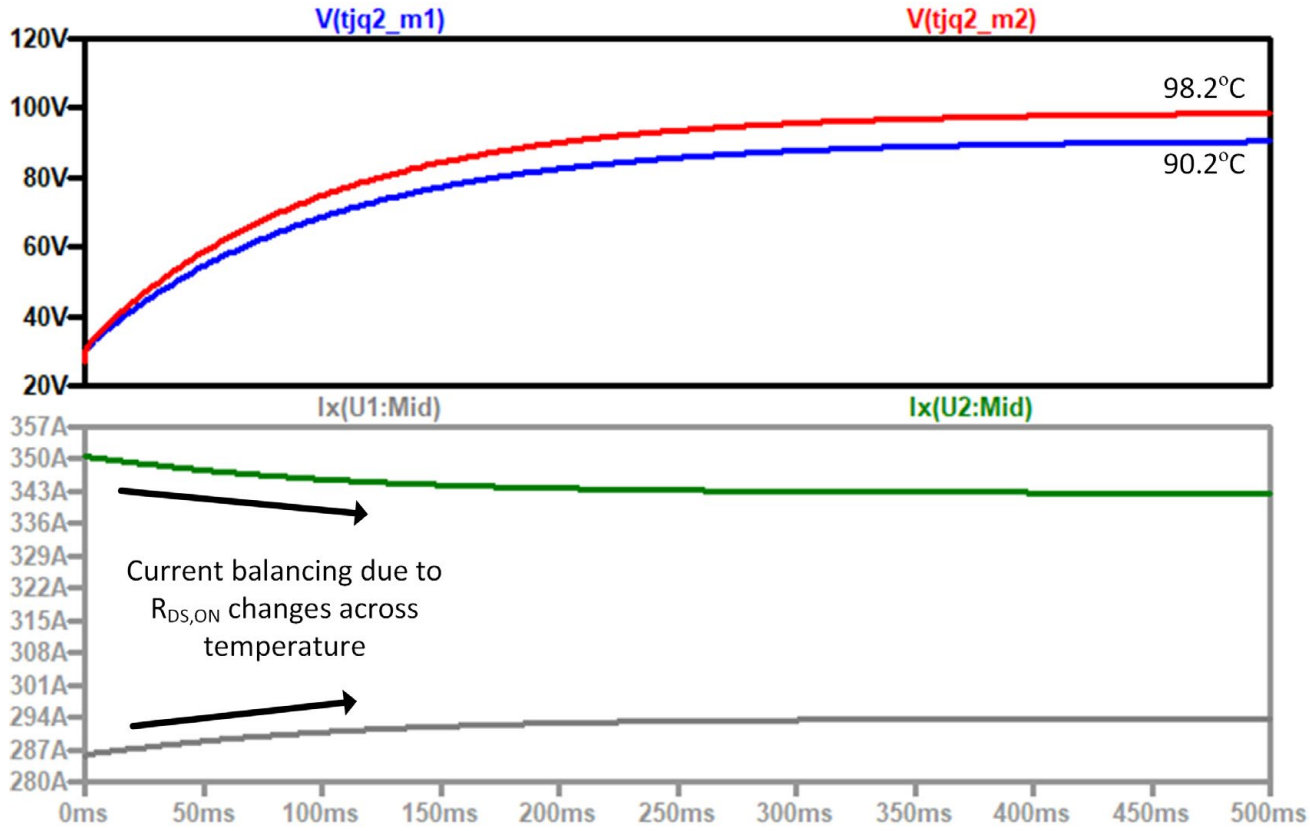


Figure 28: Junction temperature of parallel modules using LTspice simulation

the temperature of the die, while the bottom subplot shows the current through each module. The final temperature of the simulation is 98.2°C and 90.2°C – these results are very similar to the iterative method discussed previously. One interesting feature is the change in current through each module as the temperature in each junction increases; initially, module 2 carries 65 A more current than module 1. However, by the end of the simulation, the difference in current between each module is only 49 A. This is caused by the feedback loop discussed in Figure 59.

7.1.1 Conduction Analysis Caveats

It's important to note that this analysis of the conduction losses has assumed that the modules are in a perfect system in steady-state operation. However, layout asymmetries and dynamic mismatch can cause additional mismatch during the on-state condition of the devices. These effects can manifest in several ways. For example, differences in DC resistance of the bussing connections between modules can influence the current sharing, especially for modules with a very small $R_{DS,ON}$. Adding a 0.5 mΩ DC resistance to the midpoint connection of M1 in the prior simulation example changes the temperatures of M1 and M2 to 105°C and 85°C, respectively. In addition, poor layout can cause long-duration dynamic mismatch that persists well into the on-state behavior of the device; these effects and how to mitigate them are discussed in Section 8.2.

7.1.2 Conduction Distribution Analysis

Analytical Method

For designs that must be translated to high volume commercial products, it can be necessary to create a distribution of module performance that would be expected in the field. The information from this distribution can be used to design margin into the system to ensure that a minimum percentage of commercial units meet specifications. The general procedure for performing this analysis is as follows:

1. Generate a normalized distribution of module parameters from production test data
2. Select *n* modules at random (based on number in parallel) from this distribution
3. Use analytical calculations, simulations, or measurement lookups to determine the current through and subsequent temperature of each module based on the given conditions
4. The results can be displayed as a normalized distribution with the variation of junction temperature being used as an input to the design process

A notional distribution of $R_{DS,ON}$ for CAB450M12XM3 power modules is provided in Figure 29. Steps 2 – 4 were applied using this distribution and the iterative calculation method discussed in the previous section. Figure 30 shows the resulting distribution of temperature for various conditions. The left plots describe the average temperature of the modules, and the right plots describe the temperature difference between the hottest and coldest module. For two modules in parallel with a total load current of 800 A, the mean temperature is centered around 69°C with a range of +/- 5°C. For the temperature differentials, most configurations lie below a 2°C difference, with a maximum of 6°C. As the current is increased to 1000 A, the mean temperature increases to around 103°C, and the max temperate delta is around 8°C. Increasing the number of modules in parallel (while keeping the load current per module the same) yields the same mean temperature but has two additional effects: 1) the span of the mean temperature decreases, and 2) the average temperature delta between modules increases. This result is intuitive as adding additional modules will have two affects, 1) the average $R_{DS,ON}$ of the four modules is more likely to be centered around the $R_{DS,ON}$ distribution, and 2) having more modules in parallel increases the probability that modules with different $R_{DS,ON}$ will be in the system.

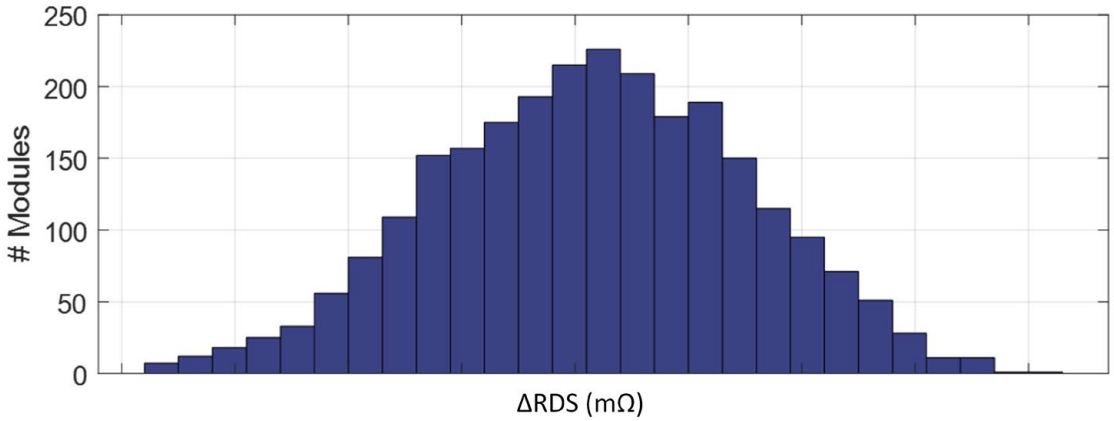


Figure 29: Notional $R_{DS,ON}$ distribution of a CAB450M12XM3 power module at 25°C

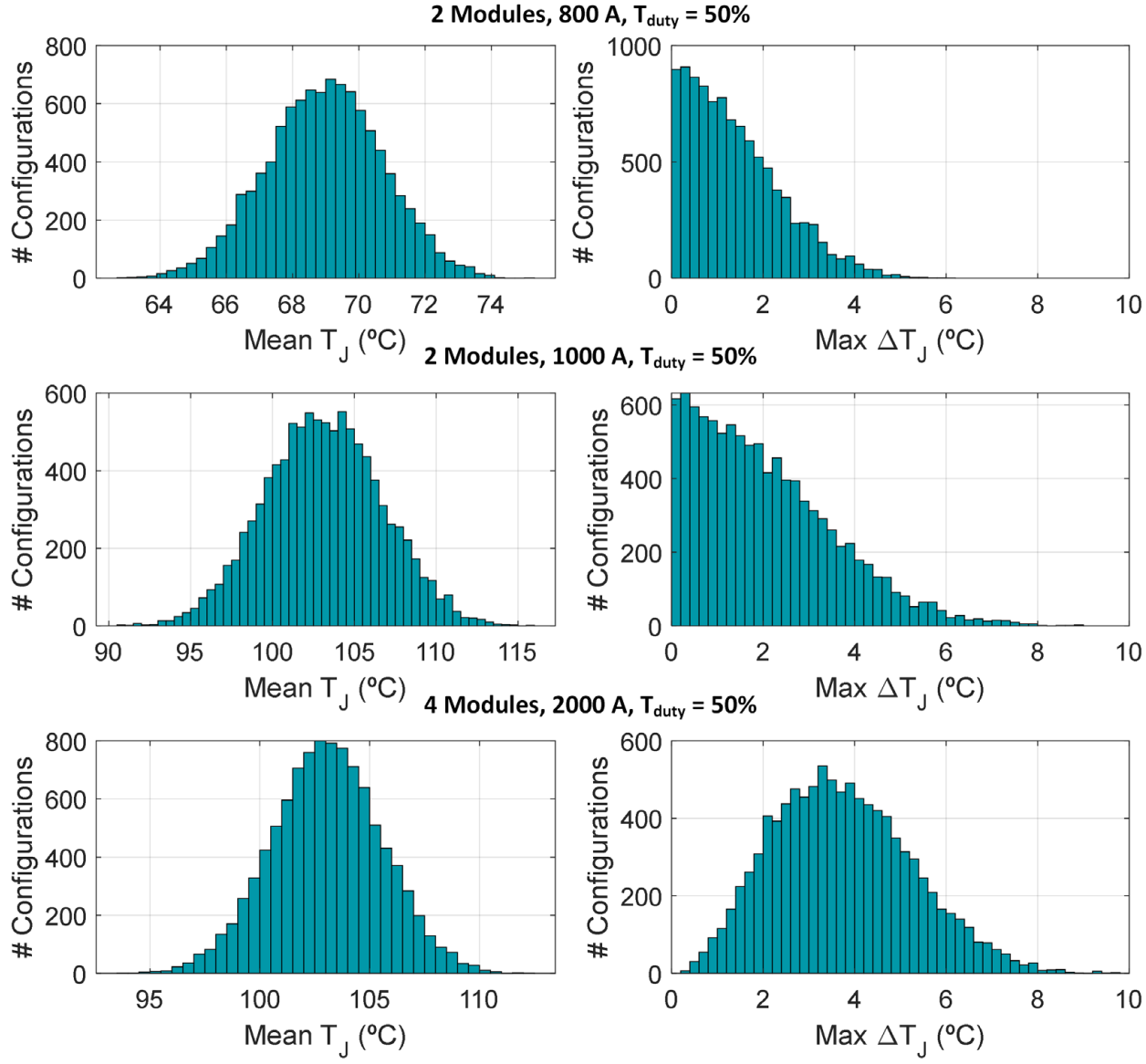


Figure 30: Example temperature distributions for CAB450M12XM3 power modules for a given $R_{DS,ON}$ distribution

Simulation Method

Distribution analysis can also be performed in LTspice with a Monte-Carlo-style simulation. Any parameter can be defined with the gauss() function in LTspice, and LTspice will randomly select a parameter value based on a normal distribution for the given tolerance. The simulation can then be rerun multiple times to understand the bounds of behavior of the system. A screenshot of the DC paralleling circuit modified for Monte-Carlo analysis is shown in Figure 31. The Spiceline2 field of M1 and M2 were modified to include the following line:

For module M1: Rdss=Rdss_M1

For module M2: Rdss=Rdss_M2

Several resistances (R1-R4) have also been added to the circuit to demonstrate how system parameters can be swept in this analysis simultaneously. All of these parameters are defined in the bottom-right of Figure 31. The syntax for each statement is given by

.param <var> = a(1+gauss(b/3)).*

Here, *a* is the mean value of the parameter, and *b* defines the tolerance. The integer *3* denotes a 3-sigma tolerance. When an LTspice simulation is called, this .param statement will be executed and use a random value for that variable given by the normal distribution specified by the provided function. (Note: alternatively, the mc(val,tol) function can be used, but this produces a uniform distribution).

So, for example, consider the below line with a mean of 0.5 mΩ and a standard deviation of 0.1mΩ.

.param R1 = 0.5e-3(1+gauss(0.5/3))*

Or the line for Rdss, which will have a mean of 0 mΩ and a standard deviation of 0.13 mΩ (matching Figure 29).

.param Rdss_M1 = gauss(0.15/3)

Finally, in the bottom left of the simulation, several .MEAS statements are used to measure the average final temperature of the modules, and the final temperature difference between the modules. The .step definition of parameter 'x' has no effect on the simulation, but is used to have LTspice called ` times.

Note: LTspice uses pre-determined random number generator; to randomize this generator across runs, go to control panel -> Hacks! -> check "Use the clock to reseed the MC generator"

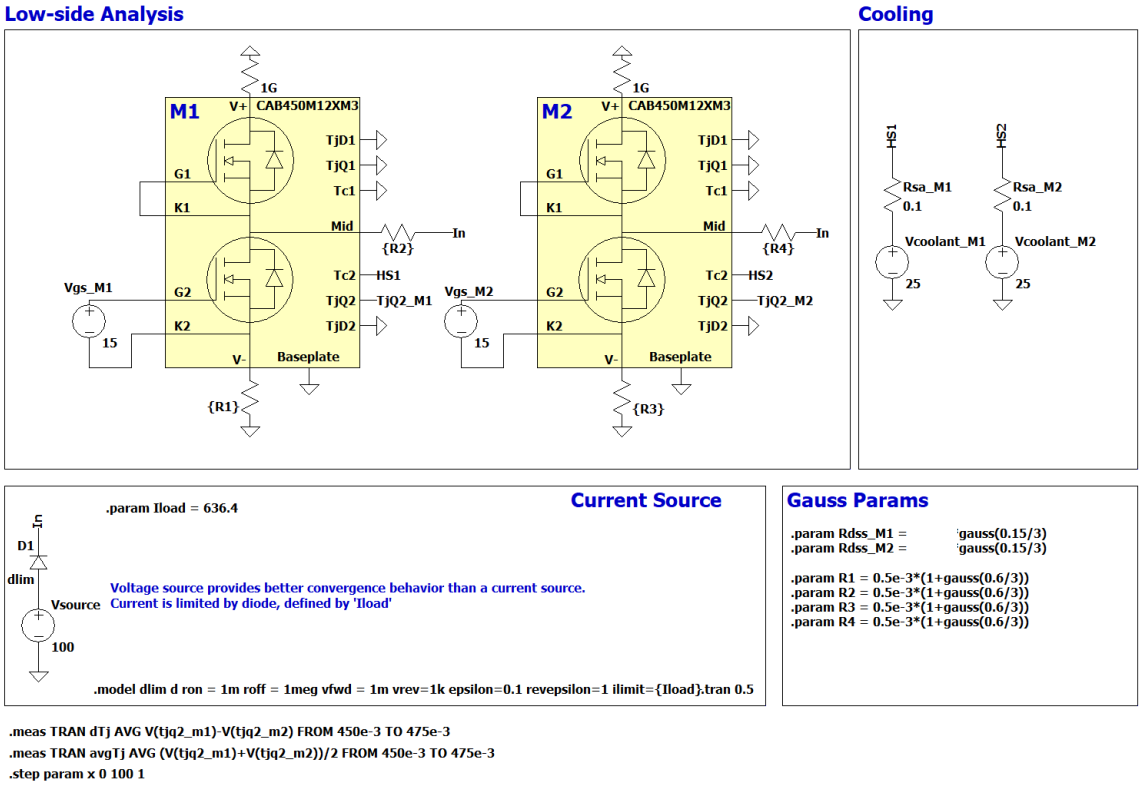


Figure 31: LTspice conduction loss paralleling circuit modified for Monte-Carlo analysis

The results of the Monte-Carlo SPICE simulation are shown in Figure 32. The top subplot shows the average temperature, and the bottom subplot shows the difference in temperature between the two modules. Each colored line represents a unique simulation with different parameter values defined for Rdss_M1, Rdss_M2, and R1 – R4. A distinct advantage of the Monte-Carlo method is that it can include system-level parameters specific to a design as part of the worst-case analysis for implementing margin. Here, for example, the worst-case ΔT_J is around 13°C, which is reasonably higher than the prior analysis that only considered the $R_{DS,ON}$ of the modules.

Note: to extract the .meas data from your simulation, press ctrl+L to open the log window, then right click and press 'Plot .step'ed .meas data.' This will open a plot window in which all .meas results can be plotted and exported for easy analysis in other software.

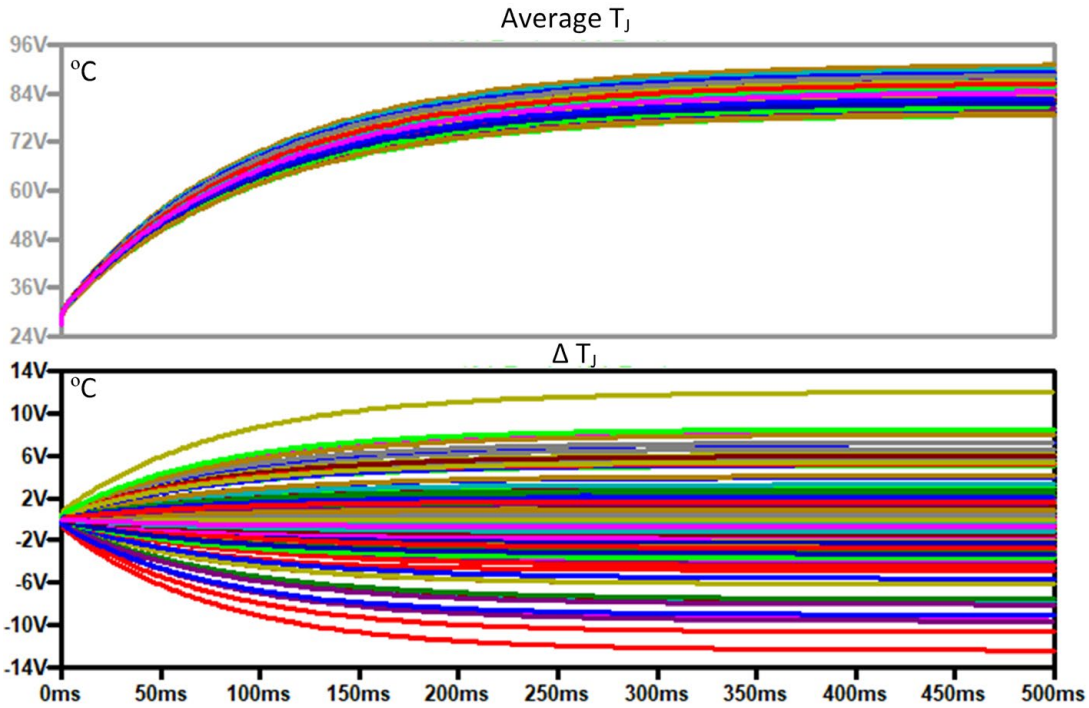


Figure 32: LTspice conduction loss paralleling Monte-Carlo simulation results

8. Understanding Current Imbalance During Switching

This section specifically discusses layout recommendations to improve dynamic current sharing. Please refer to section 5 for general tips on system design with regards to paralleling.

For further reading on this topic, refer to references [9] - [24].

One challenge with understanding dynamic current imbalance is that the module characteristics and system layout are convolved together. In general, an unoptimized system layout will cause poorly matched current sharing and can greatly exacerbate the effects of mismatched module parameters. Thus, as will be discussed herein, the first step in optimizing a paralleled system is to improve the layout; this can reduce the mismatch sufficiently such that binning is not necessary to meet design requirements.

Quantifying the effects of imbalance during dynamic switching can be challenging because of the number of variables involved. Simulation can be useful for evaluating trends but is not practical for predicting *exact* system behavior because of the complexity of both the device behavior and the system parasitics. Evaluating an empirical setup can be useful, but this comes with the challenges of accurately measuring the signals with high bandwidth probes. In addition, for realized applications, it is notoriously difficult to measure the drain-source current of devices at high bandwidth, as measuring these signals requires inserting a shunt into the current path (example: the 10 mΩ bar shunts in Figure 7), choking the signal to a small cross-sectional area (current transformers), or have insufficient bandwidth (Rogowski coils). It is impractical for these devices to be included in final designs, and their insertion into the system can change the behavior. Another challenge is that switching can occur at various conditions – gate resistance, load current, bus voltage, etc. – which can affect dynamic current sharing, expanding the requirements for analysis.

In general, the best approach for handing dynamic mismatch is to follow best practices to minimize it as much as possible and include some margin in the design to account for any remaining mismatch. Measurements of the load current of each module can be used to assess imbalance and is more practical to measure in realized designs.

8.1 Testing Overview

The testing in this section utilizes the setup described in Section 3. Several CAB450M12XM3 power modules were characterized on a Keysight® B1505A curve tracer to determine their characteristics at 25°C ($R_{DS,ON}$, V_{TH}, etc.). These modules were then attached to the PCB in various configurations to mix and match module parameters in different positions to observe how current is shared under each. For some tests, only **two** modules were populated on phases A and C, and for others, all **three** positions were populated. This provides varying degrees of complexity for analysis. Finally, for each configuration, the system was measured at different voltages, gate resistances, and load currents, to understand their impacts.

8.2 Steady-State Imbalance Current (Load Impedance Matching)

It is often assumed that during pulse-width modulation (PWM) operation the current through parallel devices will quickly reach steady state after each transient event, in which case the imbalance in current flow through each switch will be caused only by the resistance of each parallel switch. However, as described in [22] and [24], impedance mismatch between the power loops of each module creates an imbalance current with an extremely

long time constant (1 – 100 µs). In a typical system, this imbalance current causes mismatched losses much higher than would be expected.

Figure 33 (a) shows a notional CIL circuit with two parallel modules that highlights the cause of this imbalance current. In this diagram, the low-side MOSFETs of each module are ON, and the high-side is OFF. Here, current flows from the DC link capacitor, through the load inductor, then reaches a split path at the midpoint of each module. The current then acquiesces at the source terminal of each module before returning to the DC link capacitor. A simplified circuit of the split current path is shown in Figure 33 (b). The problem arises from the diverging current paths at the midpoint of each module. The current will divide between the two modules based on their impedance and does not include the load. The impedances in these paths are very small, such as the nH stray inductance of the module terminals, the $R_{DS,ON}$ of the MOSFETs, the contact resistance of the connections, the impedance of the bussing, etc., so even a very small difference in impedance from these parameters can result in a significant mismatch in how current will divide between the two modules. Furthermore, this system is sensitive to the initial current through each switch position at each transient event; this means that a difference in device characteristics (such as V_{TH}) that can cause the current flow to be asymmetric during the transient event, which then persists into the ON state even for a symmetric system. An example empirical waveform of a DPT of two modules with only slightly mismatched $R_{DS,ON}$ is shown in Figure 34. Despite the modules being fairly matched, differences in the impedance between the load and each module results in a mismatched current that persists across both ON periods of the DPT.

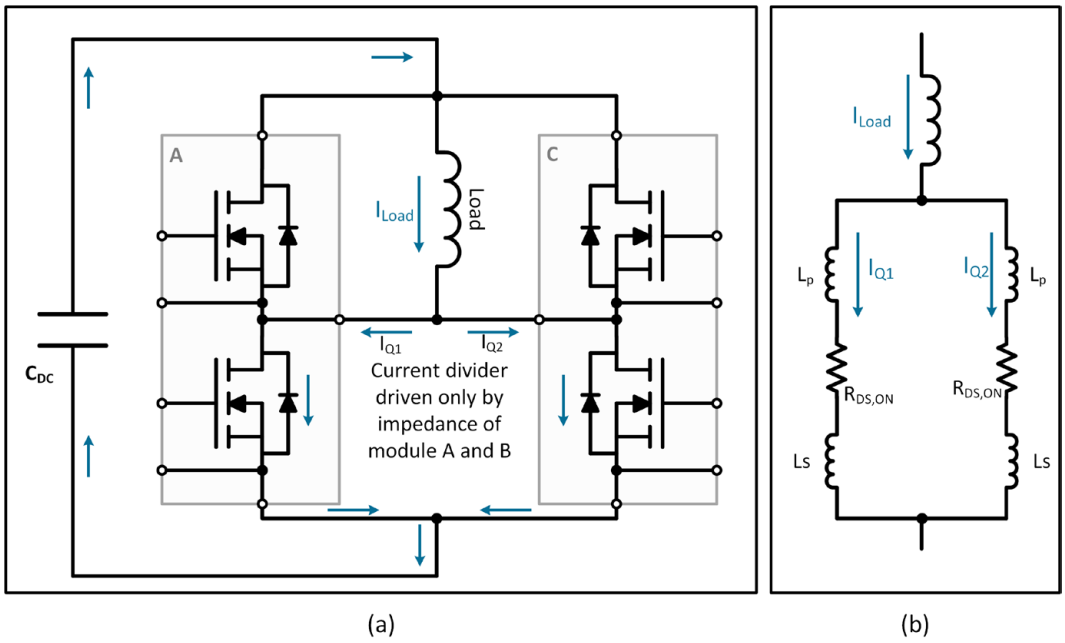


Figure 33: CIL circuit demonstrating the fundamental source of steady-state imbalance current

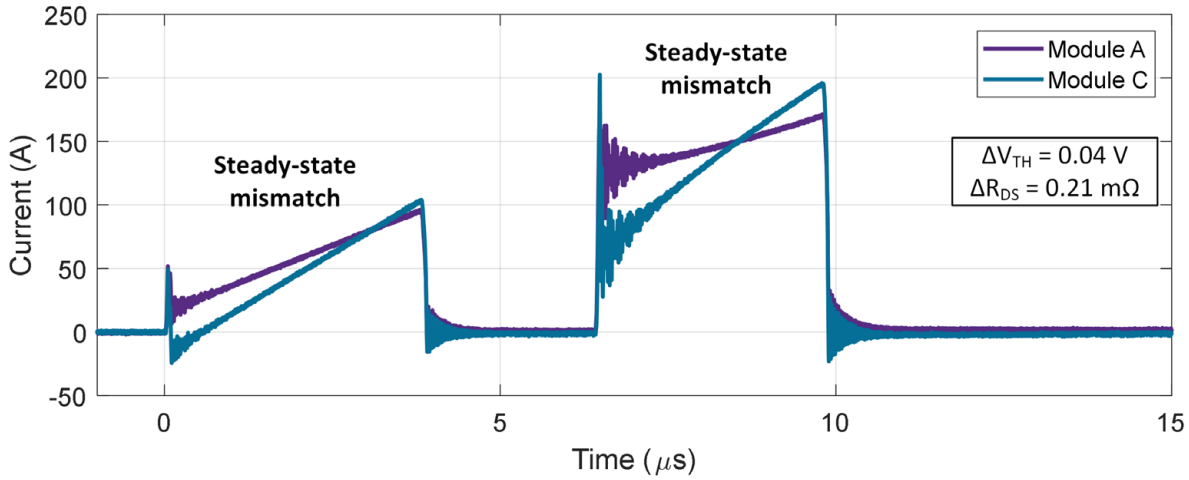


Figure 34: Example empirical DPT waveform showing mismatch during "steady state" regions

It is beneficial to break down this concept into several examples to fully understand the implications. The below DPT simulation circuit in Figure 35 is used to evaluate the following examples. The modules are attached directly together at V+ and V-, and inductances La and Lc separate each midpoint to the load. To begin, each

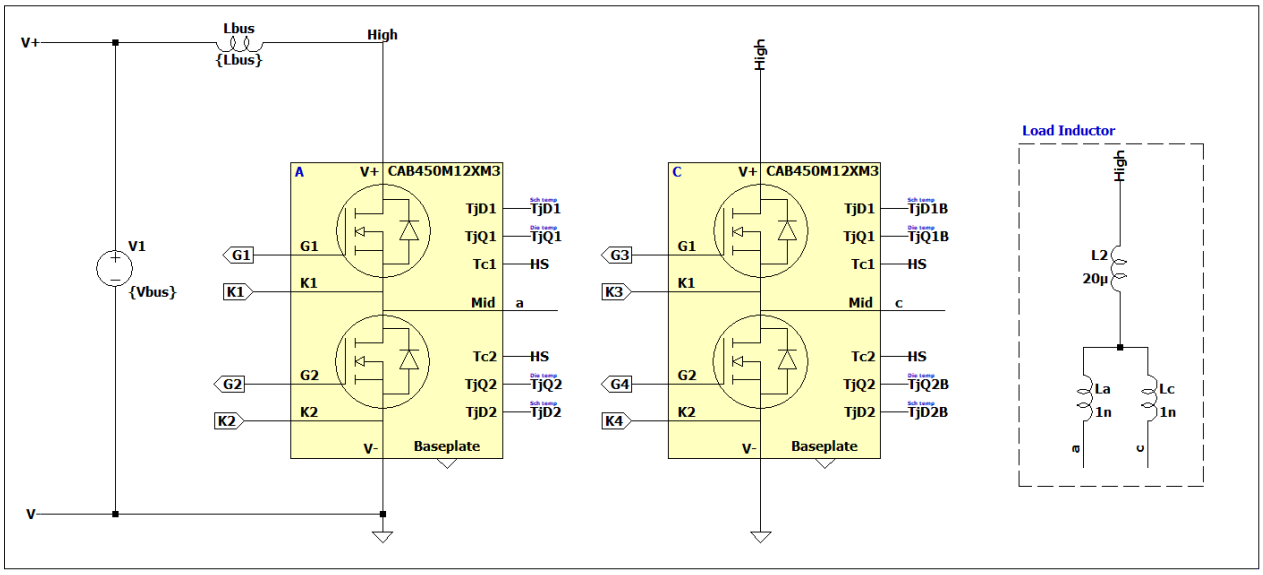


Figure 35: Parallel DPT circuit used for steady-state imbalance analysis

load inductor is set to 1 nH, which has a negligible effect on the simulation.

Scenario 1: Symmetric Impedance with Imbalanced V_{TH}

First, it is important to understand that this is a system with nH inductance and mΩ resistance – thus resulting in a time constant in the µs range (L/R). Conceptually, inductance resists changes in current, but these nH inductances are so small that any perturbation can change their state easily. Consider the simulation result in Figure 36. Here, the impedance of each module is identical (and La = Lc), but the V_{TH} of module C is decreased

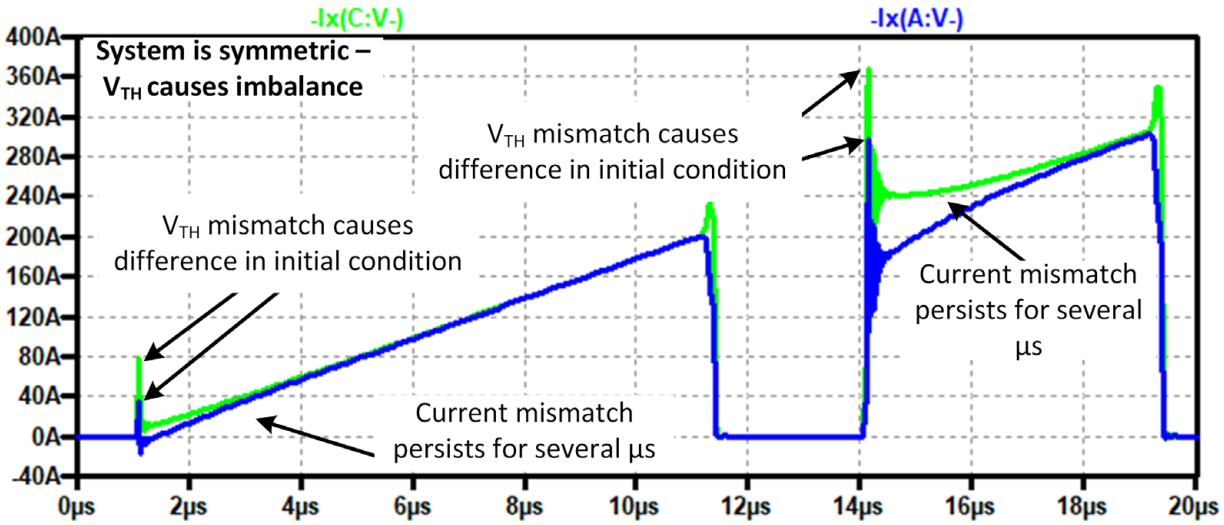


Figure 36: Parallel DPT simulation result: mismatched V_{TH} with symmetric layout

by 0.7 V in the simulation. At each turn-on event, the V_{TH} imbalance causes module C to conduct a higher share of the total current during the transient event (as expected). However, now the current through each module is unbalanced, and it takes several µs for the system to return to its true steady-state operation.

Implication: Even in a perfectly symmetric layout, differences in switching behavior between devices can cause large imbalance currents that persist for several microseconds after a turn-on event.

Scenario 2: Asymmetric Impedance with Balanced V_{TH}/R_{DS}

The second scenario to consider is one where the paralleled modules have perfectly balanced parameters, but an imbalanced load connection. In this example, an additional 10 nH is added to Lc. This level of imbalance is entirely reasonable in an actual design, especially because the midpoint connection of power modules is typically not optimized for low inductance (as it is generally in series with a large load). However, with paralleled modules, a 10 nH difference represents a large difference in impedance. Example simulation waveforms for this

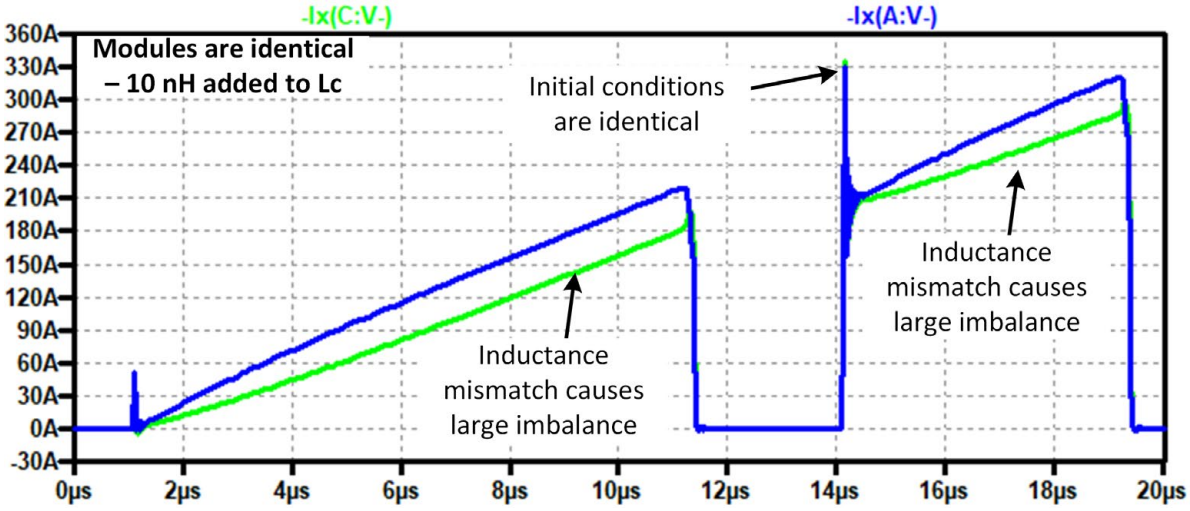


Figure 37: Parallel DPT simulation result: matched module parameters with asymmetric layout

condition are provided in Figure 37. Despite no differences in V_{TH} or $R_{DS,ON}$, module A conducts more current than module C during the ON state.

Implication: Extremely small changes in impedance from the load to each midpoint connection can result in significant changes in current sharing, resulting in a high sensitivity between layout and performance.

Scenario 3: Asymmetric Impedance with Imbalanced V_{TH}/R_{DS}

In a real system, both the module characteristics and impedance will be mismatched. This creates a complex network that can ultimately result in poor matching between devices. Module parameters will affect initial conditions, and the impedance mismatch will exacerbate the imbalance. An example simulation with V_{TH}, $R_{DS,ON}$, and La/Lc mismatched is shown in Figure 38. The resulting current waveforms show imbalance both during dynamic switching and during steady state. The layout imbalance will cause the switching and conduction loss mismatch to worsen.

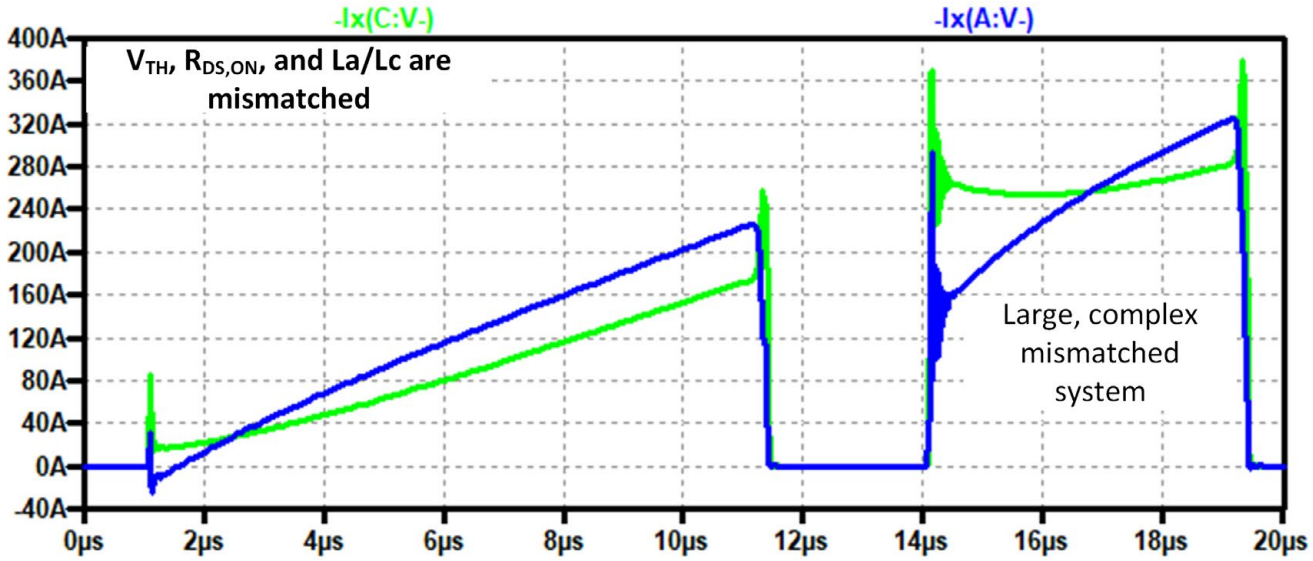


Figure 38: Parallel DPT simulation result: mismatched module parameters with asymmetric layout

Implication: An imbalanced layout compounds with module parameter mismatch and yields poor current matching and performance.

8.2.1 Example DPT Waveforms

The effect of load impedance mismatch can be observed in empirical waveforms. Consider the three sets of waveforms shown in Figure 39. Here, three modules are placed in parallel such as in Figure 7. The system is identical in the three tests, except the location at which the load inductor is changed (L_A, L_B, and L_C). This will change the inductance between the load inductor and each module. For example, connecting to L_A will result in the lowest inductance to module A, and the highest inductance to module C. In Figure 39, when the inductor is connected to L_A (top), the current through module A is significantly higher than through B or C. However, as the load inductor is moved from L_A to L_B to L_C, the current through module A decreases and the current through module C increases. When connected to L_C, the system is matched. This highlights the sensitivity of current matching to the system layout. Note that being connected to L_C is not a general method for matching, but simply offset other imbalances in this particular example.

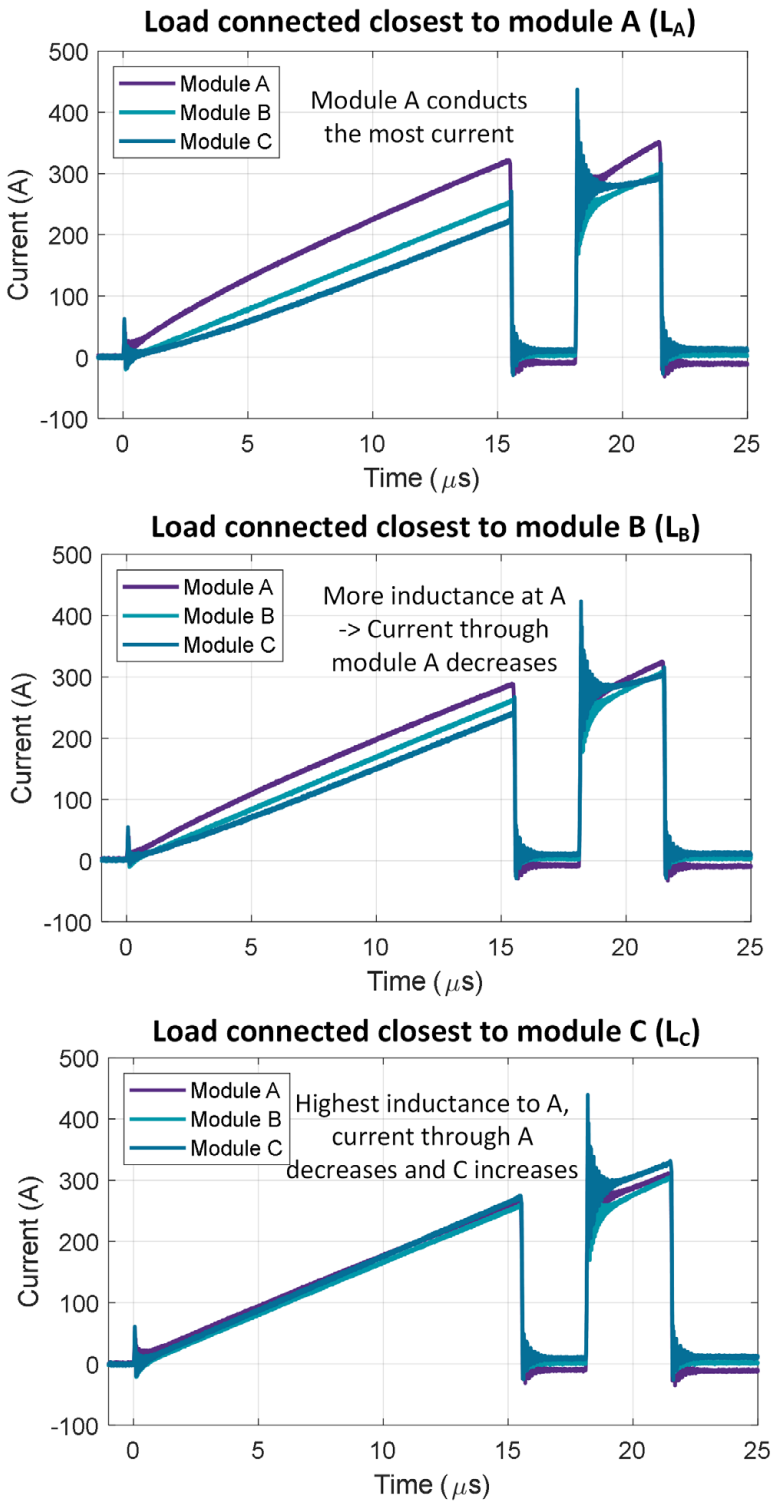


Figure 39: Empirical results comparing current balance between modules with different load impedances. Each configuration uses the same modules in the same positions under the same conditions.

8.2.2 Imbalance Evaluation Methods

An interesting consequence of this phenomenon is that **dynamic mismatch causes steady-state current mismatch.** This means that a well matched steady-steady current through the load for each module correlates to well-matched dynamics between the devices [22]. Thus, in a realized system where the drain current of individual modules cannot be measured, a useful method to evaluate the dynamic matching is to measure the load current at each module using lower bandwidth probes such as Rogowski coils (which are practical to attach to most loads). A well-matched load current indicates well matched dynamics, and vice versa.

8.2.3 Mitigation Methods

There are several methods to mitigate this source of imbalance. One is to ensure that there is no imbalance between the paralleled modules, but this is not practical nor effective due to scenario 1 described before. Instead, a more practical approach is to add inductance to each midpoint of the system before attaching it to the load or split the load to the midpoint of each module. An example of the former method if implemented into a CIL circuit is shown in Figure 40. The L_{ins} inductor here will typically be on the order of 1 – 30 µH. Adding the inductor here has the following effects. First, any small nH-level layout differences between the modules will now be negated by the large µH-level inductance in the circuit, so mismatch (scenario 2) is mitigated. Second, these inductors can store significantly more energy and are less prone to changes in state during transient events. Effectively, it increases the time constant from being on the order of µs to ms. Thus, any differences in steady-state current will be observed more at a “DC” level, rather than during short time scales on the PWM level. As shown in section 7, conduction loss differences between parts are very small, and this overall results in a much more balanced system.

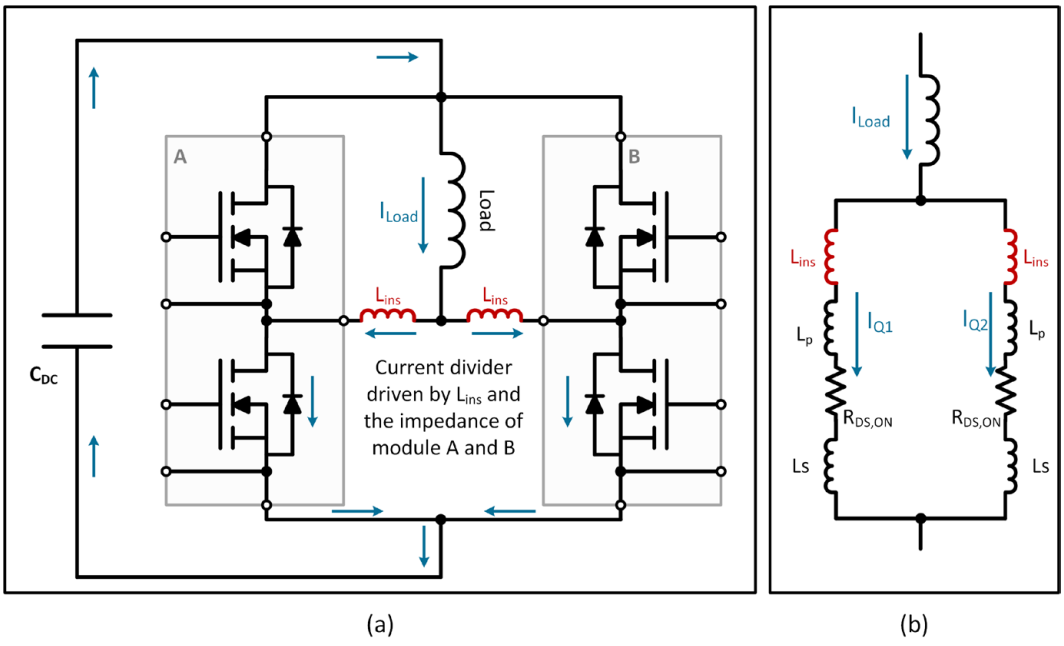


Figure 40: CIL circuit demonstrating the fundamental source of steady-state imbalance current

An example DPT simulation result using a 5 µH L_{ins} inductance (L_a, L_c = 5 µH) is shown in Figure 41. The V_{TH} imbalance is set to the same as the example in Figure 36. Both the transient mismatch and the mismatch during the ON pulse are significantly reduced by including L_{ins} in the circuit. When implementing this technique, it is important to match the impedance of the inserted inductors as best as possible. Slight differences can be tolerated and still provide benefits to the system, but large differences may introduce further imbalance. It also may be challenging to implement these inductors in an actual system.

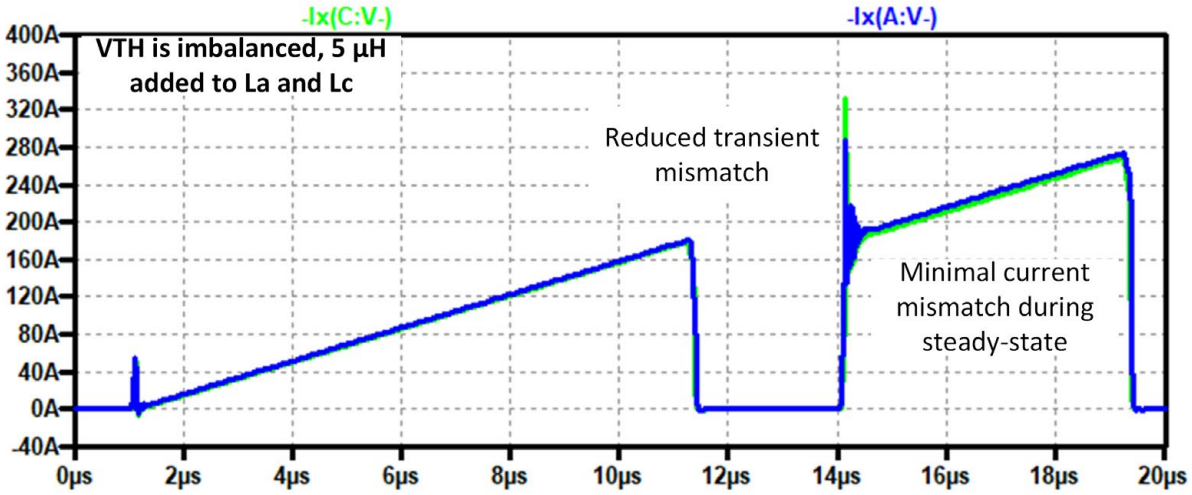


Figure 41: Parallel DPT simulation result: matched module parameters with asymmetric layout

8.2.4 Implementation in Applications

Implementing this insertion inductance into a system can be done in two ways. The first is to implement the inductance as a passive component (example: additional filter inductors in a DC-DC converter), and the second is to attach each midpoint to the load using a matched cable (example: cables attaching a three-phase inverter to an industrial motor). In general, a larger insertion inductance offers improved matching.

Consider the buck converter circuit in Figure 42. Here, the insertion inductance is added to the midpoint of the module before connecting to the primary filter inductor, L. Because both L_{ins} inductances are effectively in

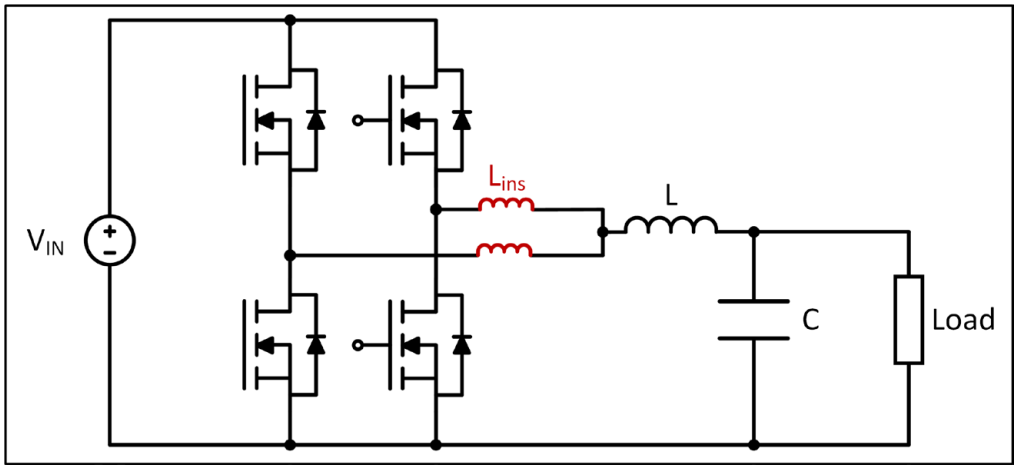


Figure 42: Parallel buck converter circuit with insertion inductors method

parallel, their total contribution to the filter inductance is $L_{ins}/2$. The system with the best balance would have L_{ins} = 2L, and L removed entirely.

Example simulation results of a synchronous buck converter using two parallel CAB450M12XM3 power modules are shown in Figure 43 (units of volts equate to °C). The simulation is configured to operate with an 800 V bus at 30 kHz with a 50 % duty cycle. The gate resistance is set to 3.3 Ω and the load current is 533 A. A V_{TH} shift is added to one of the modules to introduce an imbalance. The top plot shows the standard configuration with a direct connection between the midpoints of each module. Here, the difference in temperature between the two high-side switch positions is around 36°C. The difference in the load current includes both a large DC offset, and large transient spikes caused by the V_{TH} mismatch (similar to Figure 36). In the second subplot, 10 µH insertion inductors are added to each module before connecting to the load. This has several impacts on the results. First, the ΔT_J is decreased by around 12°C. Second, the difference in the load current becomes a steady DC

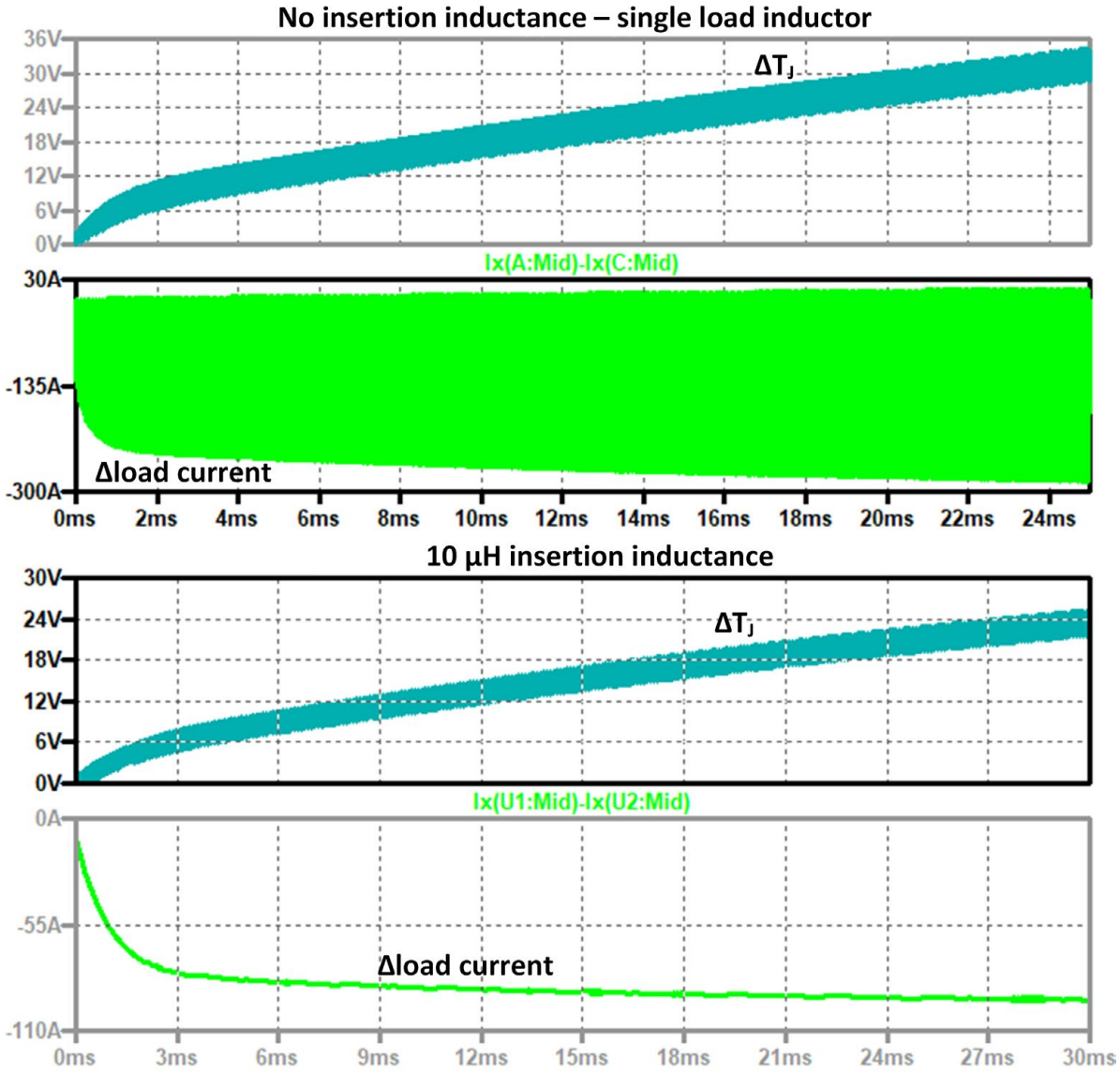


Figure 43: Synchronous Buck Converter HS mismatch between junction temperature and load current

response, and the higher-frequency mismatch is removed. Third, the system is less susceptible to layout mismatch (the standard configuration was assumed to be perfectly matched – but this is not practical). The reduction in mismatch could be improved by increasing the magnitude of L_{ins}.

For systems that drive physical machines (such as a 3-phase motor drive), the insertion inductance is more difficult to add to the system. One method is to connect the midpoint of each module to the load using an individual cable (then the midpoints of each module terminate at the load, rather than at the bussing). Each cable should have the same properties such that their impedance is matched. This method was employed in [19]. The resulting circuit for a three-phase motor drive using two parallel modules at each phase is shown in Figure 44.

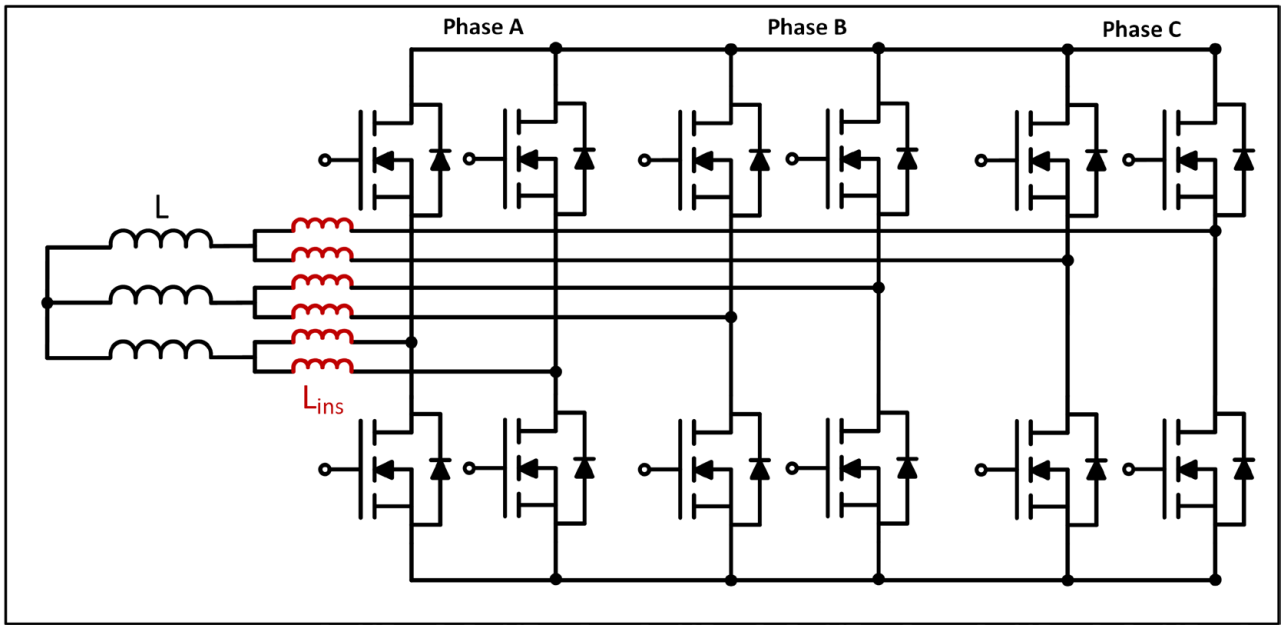


Figure 44: Insertion inductor implementation for a three-phase inverter using two parallel modules at each phase

The system Figure 44 was implemented into LTspice using CAB450M12XM3 power modules. 1 µH insertion inductors were added to the midpoints of both modules in phase A, but not to phase B or C. An identical V_{TH} shift was added to one of the modules in each phase. The results of the simulation are shown in Figure 45. The top subplot shows the ΔT_J between the die in phase A and phase B. While the two modules in phase B differ by ~30°C, the imbalance in phase A is less than 15°C. The difference in imbalance between the modules in both phases is apparent from the load current comparisons in the following subplots. Similar to what was observed with the buck converter, the high-frequency dynamic mismatch is reduced by including the insertion inductance into the system.

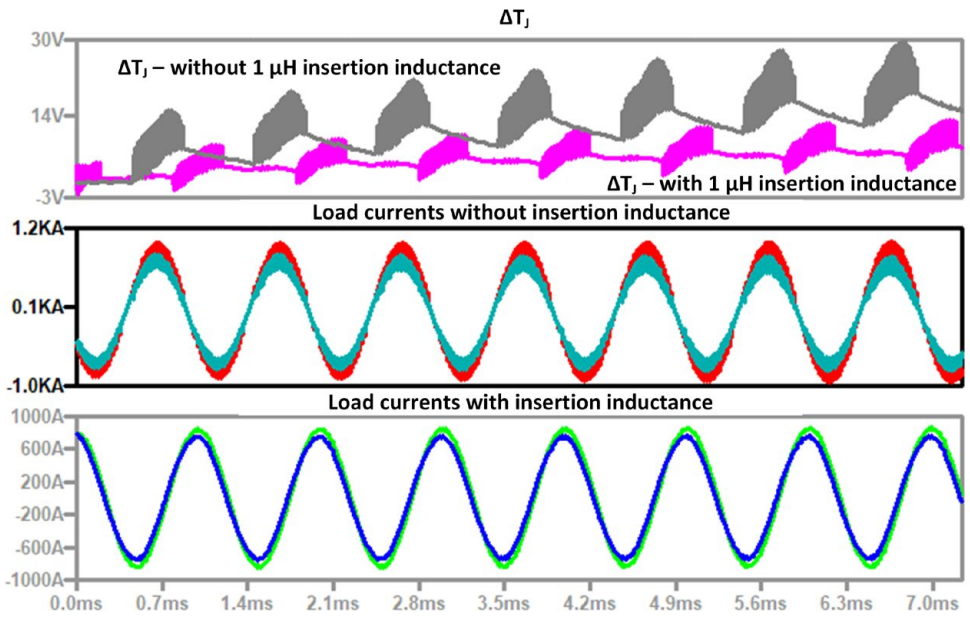


Figure 45: Mismatch comparison between two phases of a 3-phase inverter with two parallel modules. One phase uses 1 µH insertion inductors and one phase does not.

8.3 Empirical Testing: Sensitivity Analysis

This section studies the empirical setup described in Section 3 to understand the sensitivity of different circuit and module parameters on current sharing and dynamic behavior during switching.

8.3.1 Stray Inductance: Power & Gate Loop

Stray inductance is a primary contributor to voltage overshoot and ringing during switching. Here, stray inductance in the power loop refers to any inductance in the primary power path that is subject to high frequency switching transients, and the gate loop refers to any stray inductance between the output of the gate driver and the gate/source of the die. See Figure 46 for a definition of these two paths in a typical half-bridge circuit.

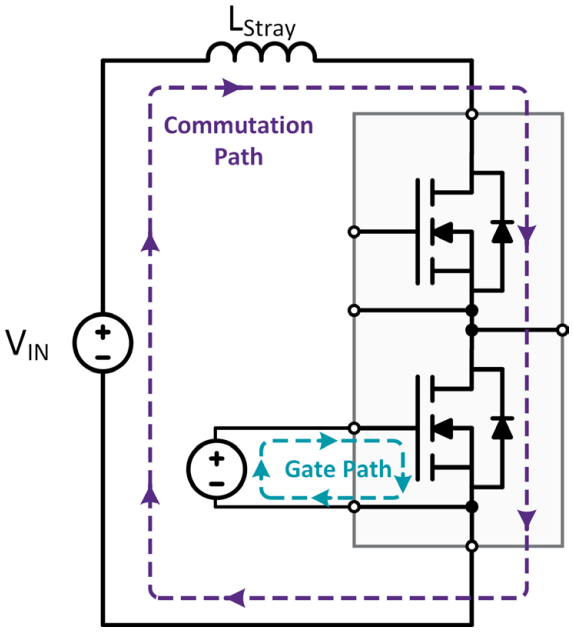


Figure 46: Power loop & gate loop stray inductance definitions

To understand the influence of power loop and gate loop inductance on current sharing, additional spacers were added to module C as shown in Figure 47. The added inductance from these spacers represents a significant increase in the power loop inductance of that module. In addition, the gate driver required an additional header extension to reach the module pins. Thus, this configuration also has an increase in the gate loop inductance.

A zoomed-out comparison of the empirical results of this testing are shown in shown in Figure 48. The results demonstrate only a minor change in the current

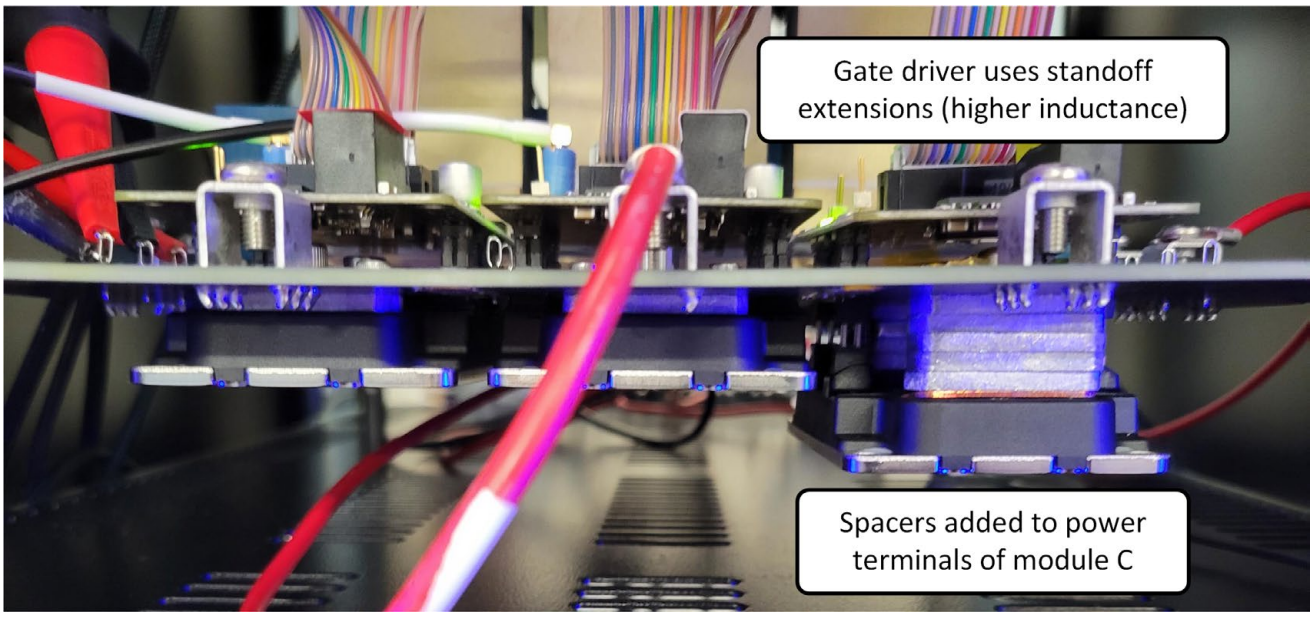


Figure 47: Configuration with additional power loop and gate loop inductance added to module C

sharing between the three modules. However, the system does demonstrate increased V_{GS} overshoot, and the additional inductance may also result in increased V_{DS} overshoot at the die in each module.

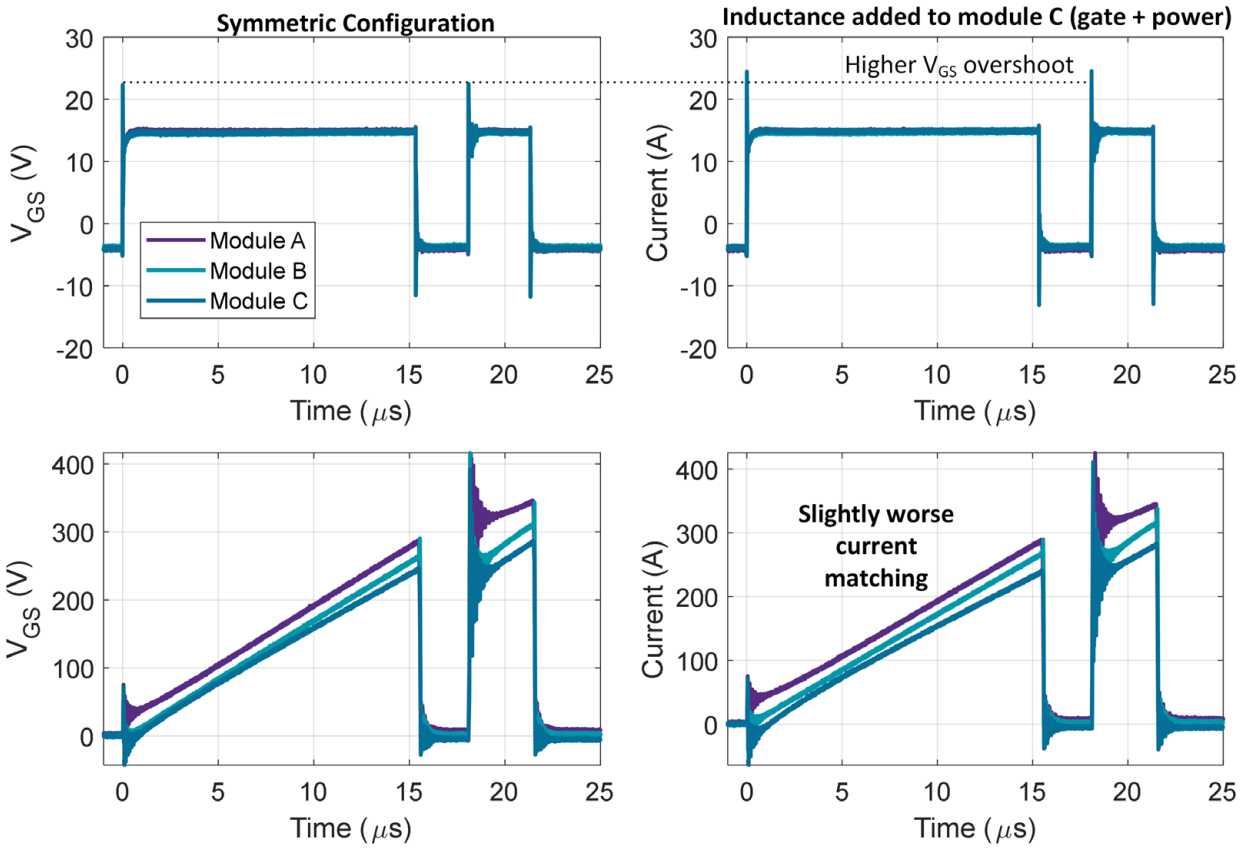


Figure 48: Zoomed-out comparison between paralleled CAB450M12XM3 power modules – symmetric configuration (left) and asymmetric configuration with additional inductance added to module C (right)

Figure 49 and Figure 50 show the zoomed-in waveforms from Figure 57 at the turn-off and turn-on events. The drain current measurements show very little difference between the two test configurations. However, it is noted there is greater mismatch during the 'steady state' operating region. This is likely caused by changes in the midpoint inductance of module C, rather than the power loop. The differences in the gate-source voltage measurements are more apparent, with increased voltage overshoot and undershoot observed in module C.

Implications

Asymmetry of the stray inductance in the power and gate loop between paralleled modules is not a sensitive parameter for dynamic current sharing. The implications of increasing these inductances are the same for a non-paralleled system: increased voltage overshoot and electromagnetic interference (EMI). It is recommended to minimize these inductances to maximize performance; asymmetry is problematic in the sense that any safe operating area excursions will be caused by the module with the highest inductance, rather than the asymmetry itself being the issue.

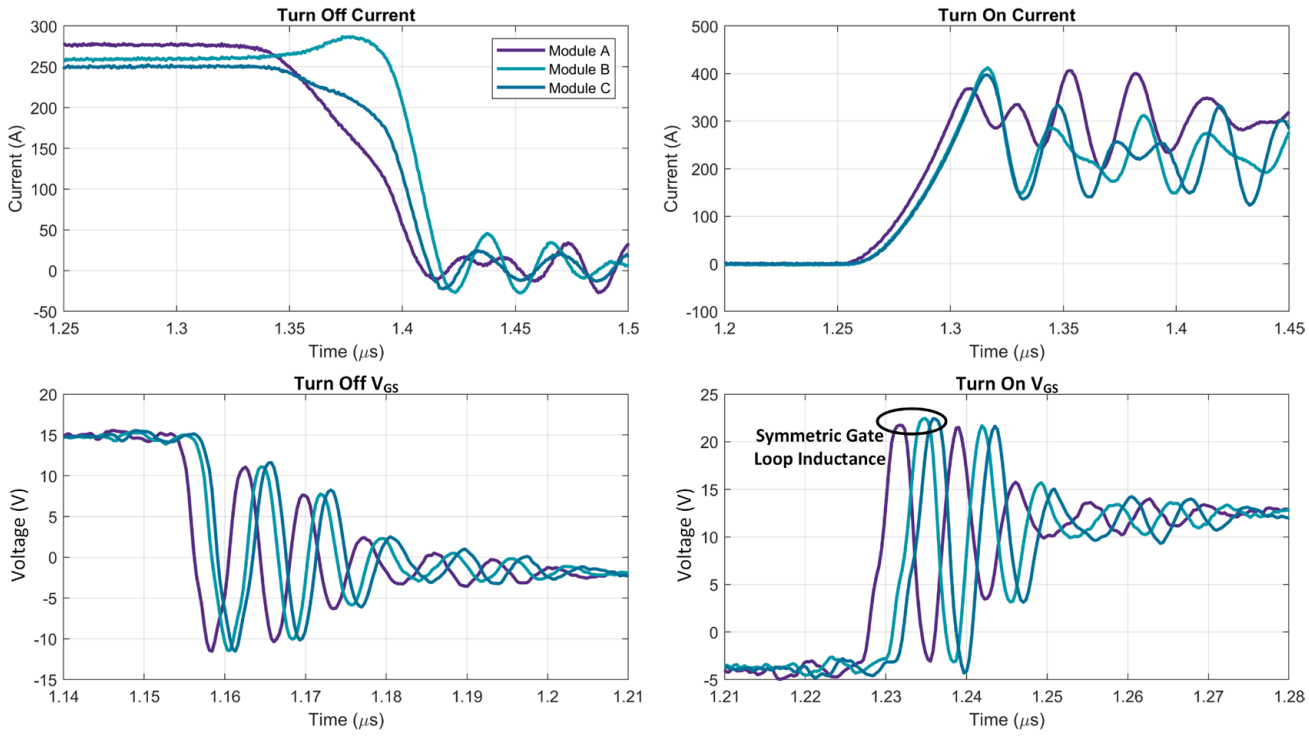


*Figure 49: Comparison of drain current and gate-source voltage of paralleled modules with **symmetric** power/gate loop*

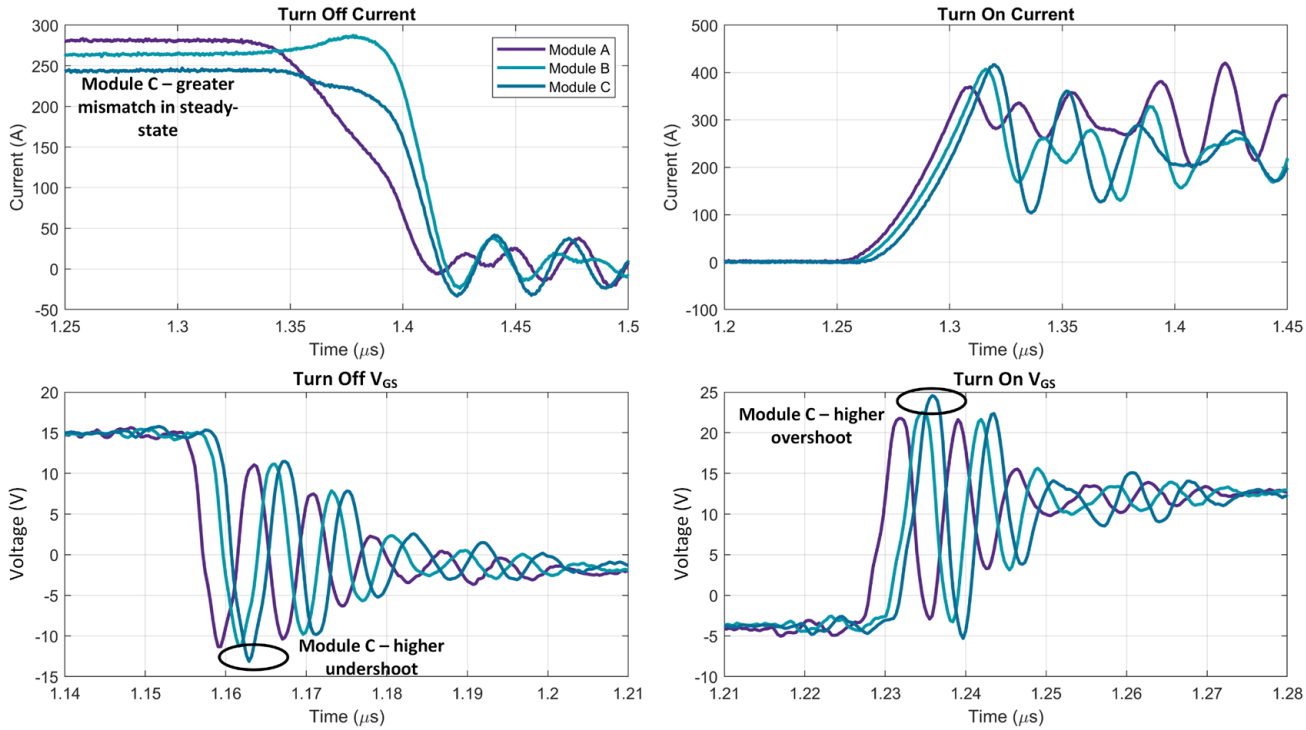


*Figure 50: Comparison of drain current and gate-source voltage of paralleled modules with **asymmetric** power/gate loop*

8.3.2 Gate Driver Variability

In Figure 9, it was noted that each gate driver is connected to the control input signal in series. That is, there is additional copper that the signal must propagate through from the controller to each gate drive, with module A having the shortest propagation time and module C having the highest. In this configuration, the gate driver for module A will be instructed to turn on before the gate drivers of modules B and C, and thus module A will be turned on sooner, resulting in imbalance.

To demonstrate this, consider the measurements of two configurations in Figure 51 and Figure 52. Figure 51 is for the baseline configuration, with the ribbon cable connected from module A to B to C. Figure 52 is of a modified configuration, with the ribbon cable connected from module C to B to A. Module C has the lowest V_{TH}, and module A has the highest V_{TH}. It is expected that lower V_{TH} will result in a module turning off last, and on first, resulting in higher losses at both turn-off and turn-on.

In Figure 51, the gate signal of module A transitions states first at both turn off and turn on, and module C transitions last. At turn off, module C (as expected) turns off last and has the highest switching losses of the three modules. At turn on, however, module A has the highest losses, despite having the highest V_{TH}.

In Figure 52 , now the gate signal of module C transitions states first for both turn off and turn on. Interestingly, the imbalance between current at turn-off is effectively eliminated, and module A has the highest losses. However, at turn on, module C now turns on significantly earlier than the other modules and has higher losses.

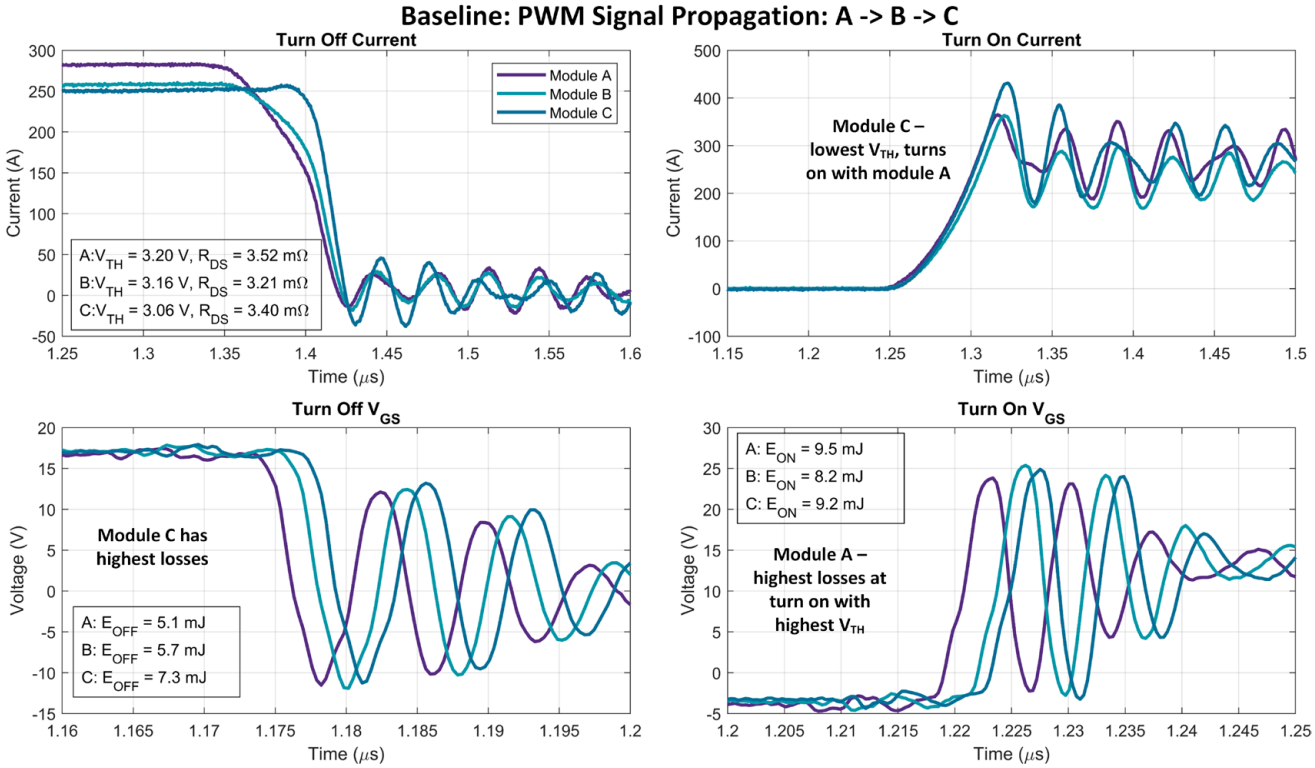


Figure 51: Comparison of drain current and gate-source voltage of paralleled modules with PWM signal propagating from A to B to C

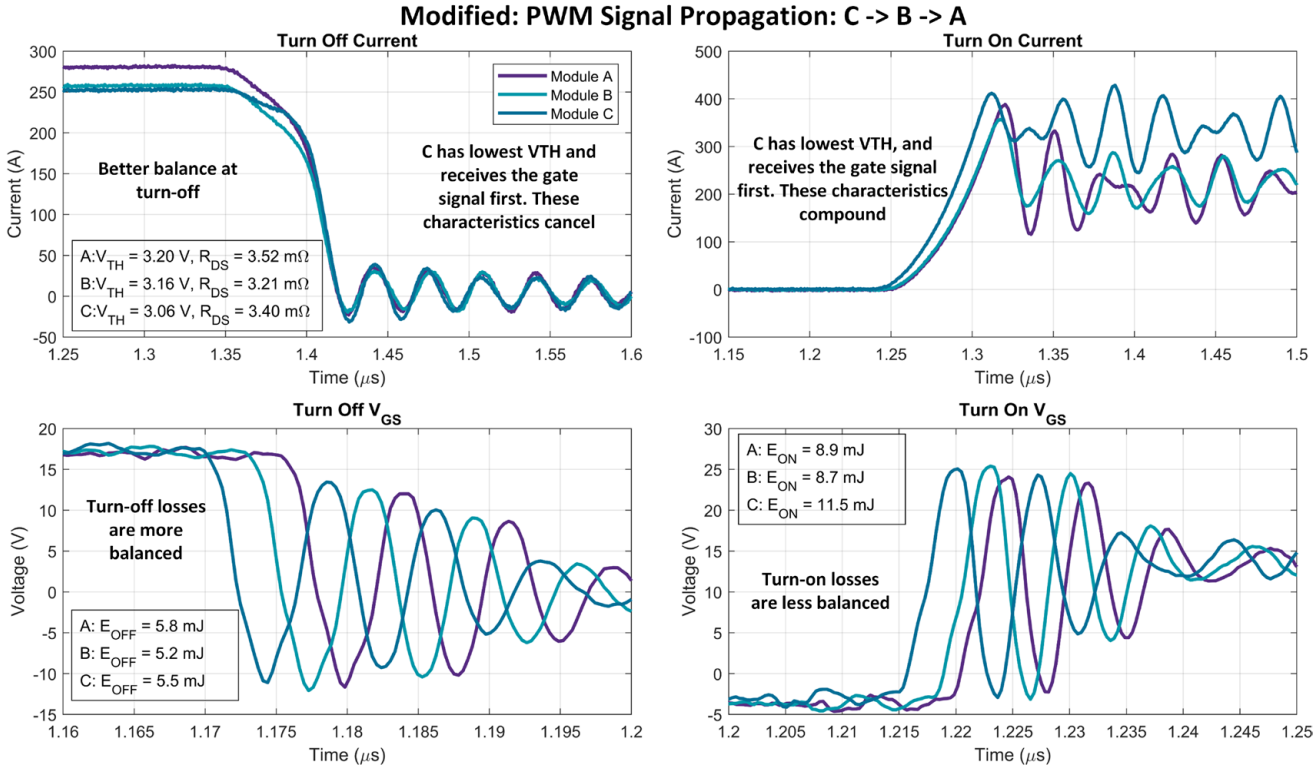


Figure 52: Comparison of drain current and gate-source voltage of paralleled modules with PWM signal propagating from C to B to A

This result is intuitive. During the turn-off event, it is the module that turns off last that is subject to the highest losses because 1) it conducts a higher share of current and 2) the other modules transition states while the voltage across the switches is very small (reminiscent of synchronous switching). During the turn-on event, it is the module that turns on first that is subject to the highest losses for these same reasons. A module driven by a gate driver with higher propagation delay will turn off later and turn on later, causing opposite effects in losses (greater turn off, lower turn on).

Implications

It is important that the gate signal to each paralleled module is initiated at the same time. Differences in propagation delay (from the controller to the gate driver) or other gate driver characteristics can have significant influences on switching losses. In the provided example, propagation delay differences on the order of nanoseconds resulted in mJ-level differences in switching losses.

- Ensure that the PWM signal from the controller has the same propagation time to each module through cable length matching or trace length matching on a PCB
- Study the variability of chosen gate driver components to implement necessary margin in a design
- Choose gate driver components with tighter tolerances
- Implement symmetry in the gate driver design

8.3.3 Gate Driver: Common vs. Multiple

In Section 5.1, the difference between a common gate driver and multiple gate driver approach was discussed. Referring to Figure 12, a common gate driver uses a single gate driver chip to drive multiple module switch positions in parallel, while a multiple gate driver approach uses a single gate driver chip per module. As shown with propagation delay, asymmetries in the gate driver implementation can have significant influences on the switching behavior of the module. A design that symmetrically drives the gates of each paralleled device is crucial for dynamic current balancing.

To study the differences between these two approaches, two configurations of modules with matching V_{TH} were measured on the empirical measurement testbed under two configurations: the standard setup with an isolated gate driver attached to each module, and a modified condition that uses a single gate driver to drive each module simultaneously. For this configuration, a PCB is used to connect from the single gate driver to the gate-kelvin pins of each XM module. The gate resistances were added at the module and split across gate/kelvin according to Figure 12.

Figure 53 and Figure 54 show the drain current and gate-source voltage waveforms for the same three modules at the same conditions. The V_{TH} of these modules is nearly equal but increases from module A to module C (this means it is expected that module A has the highest losses, followed by module B then C). Figure 53 shows the results for the multiple gate driver approach, while Figure 54 shows the results for the common/single gate driver approach. **The dynamic current sharing is significantly improved by the common/single gate driver**

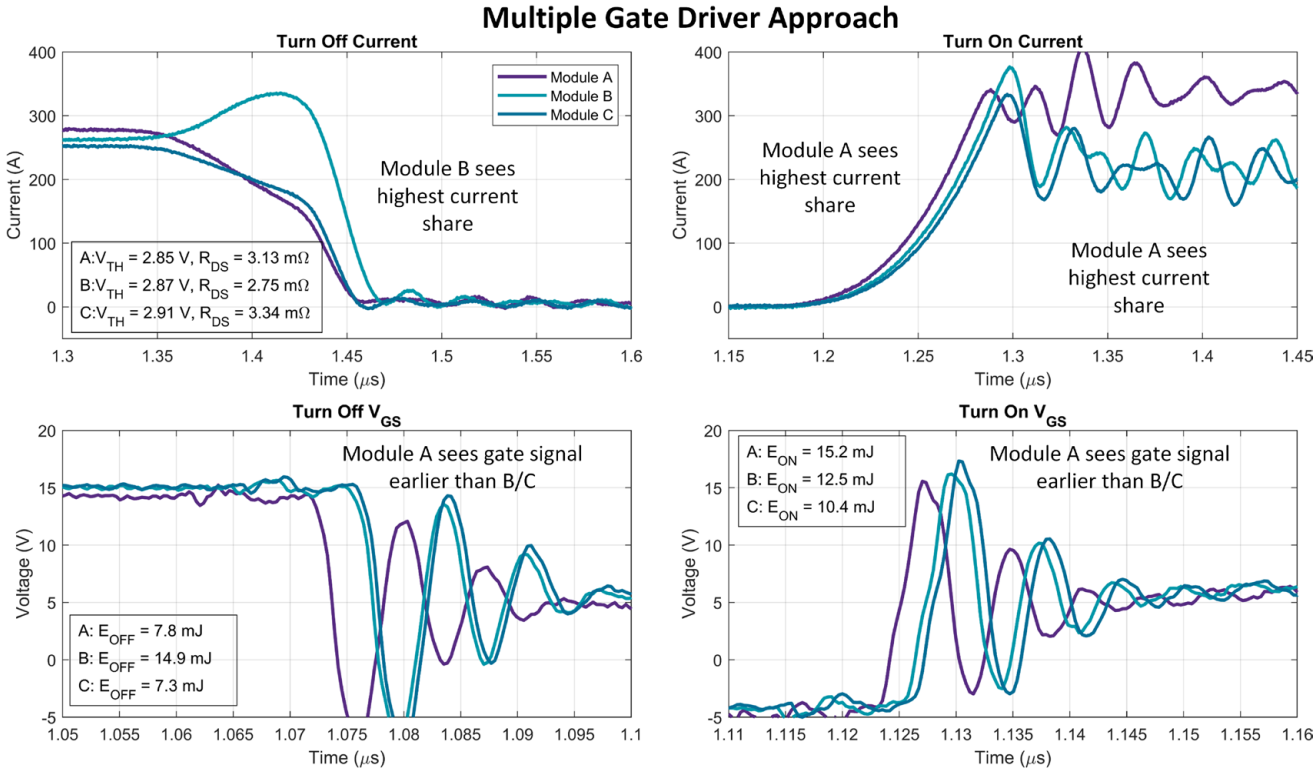


Figure 53: Comparison of drain current and gate-source voltage of paralleled modules with an isolated gate driver driving each module

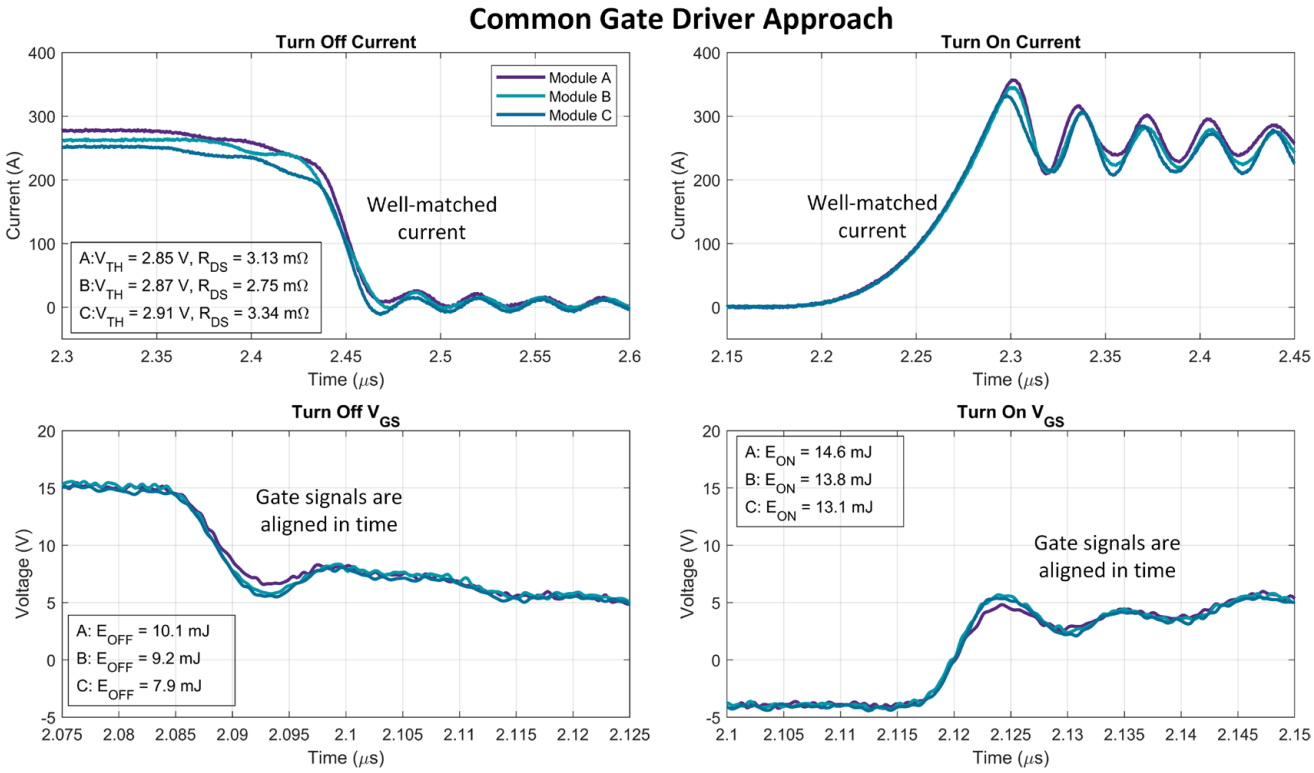


Figure 54: Comparison of drain current and gate-source voltage of paralleled modules with one gate driver driving all modules

implementation. In the multiple gate driver approach, the gate signal to module A begins turning the module off/on much sooner than the other two modules. This results in module A having lower turn-off losses than module B, despite having a lower threshold voltage. At turn-on, module A instead has the highest losses; this reversal in the expected trend from V_{TH} indicates that other system characteristics are affecting the dynamic current sharing.

The waveforms in Figure 54 using the common gate driver are significantly improved. The current mismatch between each module during the transient event is greatly reduced, and the turn-off and turn-on losses are very similar between each module. The energy loss trends expected with the V_{TH} of each module is as expected because the gate signals overlay on top of each other, and there is little to no timing mismatch between them (so any mismatch is a consequence of the module characteristics or layout, rather than the gate drivers). One unexpected improvement in the waveforms is the improvement in EMI/oscillations. In Figure 53, after the turn-on event, high-frequency multi-modal oscillations are present for each waveform and is not identical between each device. In Figure 54, the ringing after the turn-on event is at a single frequency and is identical between each module. This is important to consider when designing a system for compliance.

A second example is provided in Figure 55 and Figure 56. The configurations of the testing are identical as before, but for different modules (again with matched V_{TH}) at higher currents (~800 A for each module) and showing the instantaneous power waveforms instead of the gate-source voltage waveforms. The conclusions of this testing are identical to what was shown before: the dynamic current matching and waveform quality is

improved **significantly** with the common gate driver approach. In Figure 55, module B again has the highest

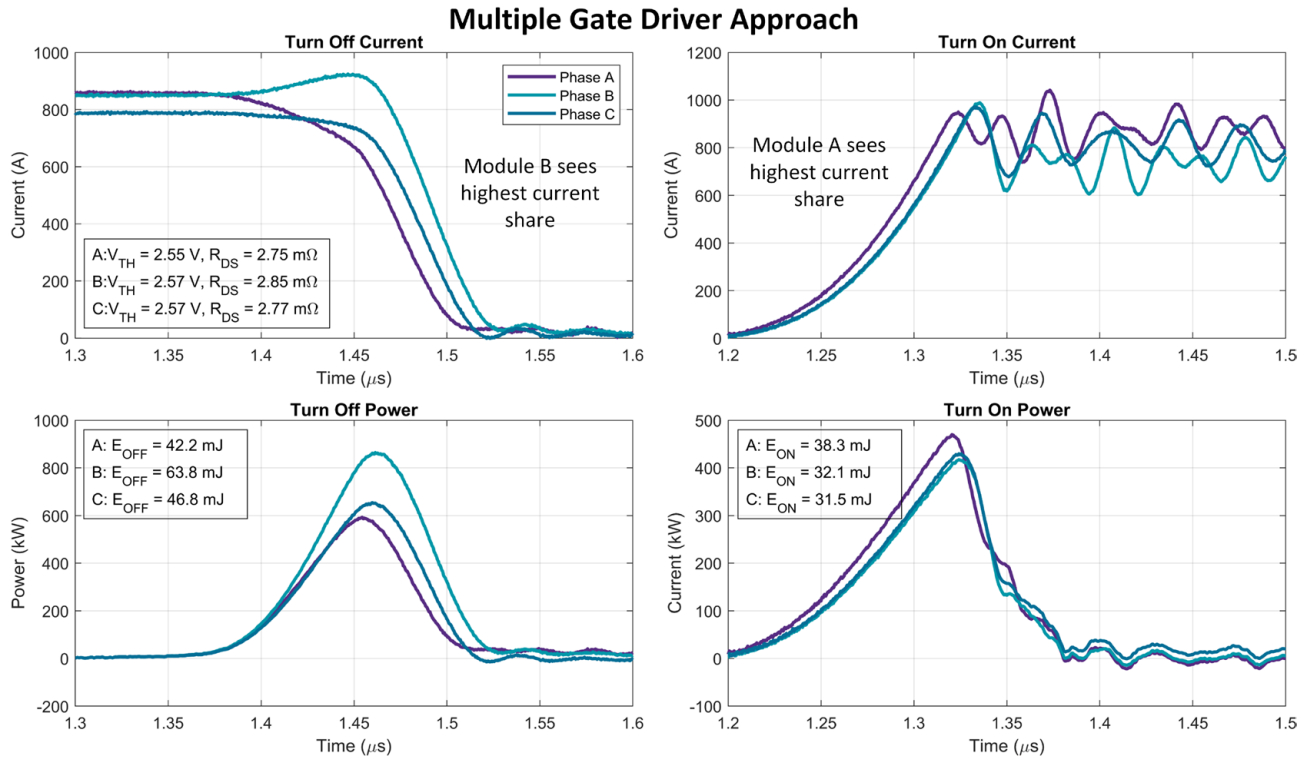


Figure 55: Comparison of drain current and gate-source voltage of paralleled modules with an isolated gate

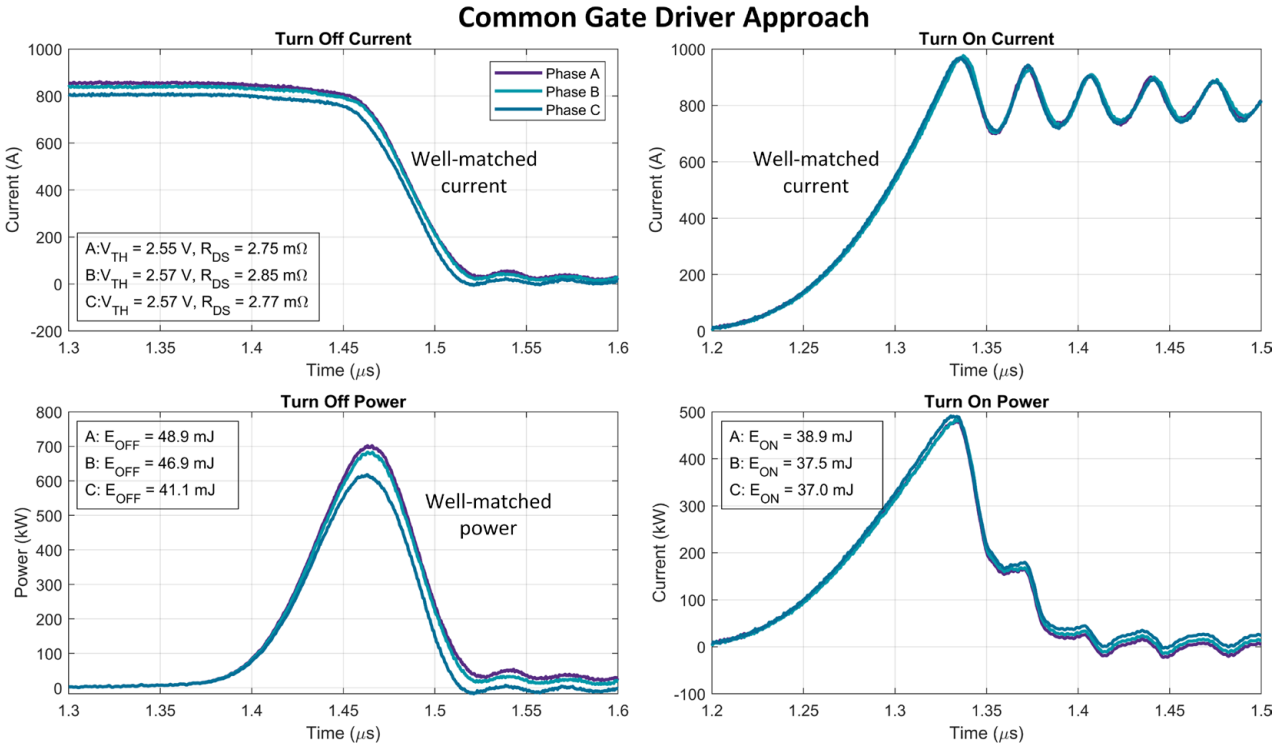


Figure 56: Comparison of drain current and gate-source voltage of paralleled modules with one gate driver driving all modules

losses at turn-off and module A has the highest losses at turn-on. This suggests that whichever layout/gate driver asymmetries in the prior example had a consistent effect on the dynamic current sharing in the system. In Figure 56, the modules show good dynamic current sharing at both turn-off and turn-on, and again the oscillations in the system are at a single frequency that is identical for each module.

Implications

While a multiple gate driver approach offers some advantages, inherent variation in signal timing and characteristics of components can cause significant imbalance between paralleled modules. When possible, it is recommended to employ a common gate driver approach to improve dynamic current balancing. However, it is important to ensure to follow the connection configuration in Figure 12 and match the gate loop inductance/propagation delay from the gate driver to each module.

It may not always be possible to implement this approach. If a gate driver or buffer is used to drive each module, consider how that component tolerance or any control signal delays will affect mismatch. These asymmetries should be minimized as much as possible and considered in the design margin.

8.3.4 V_{TH} Mismatch

The prior examples have shown that the layout and gate driver configuration can have a significant influence on the dynamic current sharing of paralleled modules. The system should be optimized as much as possible before considering the variation of module characteristics, as it has been shown that even perfectly matched modules can have mismatch if the system is not designed properly. However, the V_{TH} characteristics do affect the dynamic current sharing between devices. Figure 57, Figure 58, and Figure 59 show waveforms for three different combinations of V_{TH} with the default configuration in Figure 6 (note: each module is in series with a 10 mΩ current shunt, so $R_{DS,ON}$ differences will have a negligible influence on the system). These tests are performed using the same unoptimized layout that has mismatched load impedance, gate driver propagation delay, and uses the multiple gate driver approach. Thus, this testing will also be influenced by these asymmetries and is not reflective of how an optimized system with the provided V_{TH} mismatch would perform.

Three examples of waveforms with varying V_{TH} mismatch are provided in the following figures. These examples only populate modules A and C, while leaving module B unpopulated. Figure 57 shows an example with minimal ΔV_{TH} (0.04 V), Figure 58 shows an example with a moderate ΔV_{TH} (0.14 V), and Figure 59 shows an example with a high ΔV_{TH} (0.26 V). As the difference in V_{TH} increases, the current imbalance and subsequent energy loss imbalance increases as well. Throughout this analysis, it has been shown that the layout and gate driver surrounding module A biases it for lower turn-off and greater turn-on losses; this trend is again evident in Figure 58 and Figure 59 (in Figure 58, the module C V_{TH} is lower, but this negated by the systemically higher losses in module A, resulting in near-matching).

Implications

Higher V_{TH} imbalance between modules will generally lead to worsened switching loss imbalance. It is recommended to follow the procedures described in Section 6.2 to minimize mismatch. Binning procedures can be implemented for best performance, but it is recommended to optimize the surrounding system before implementing such measures. A properly designed system with implemented margin is sufficient for most designs.

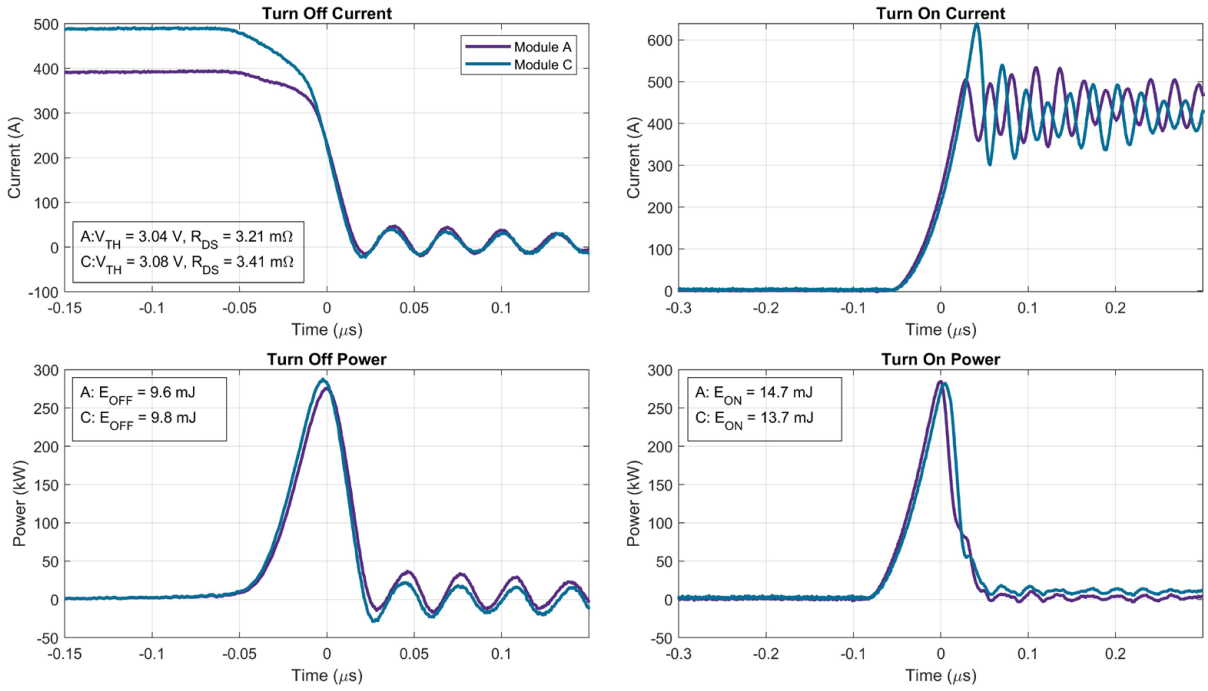


Figure 57: Module parallel example (2 modules) with minimal V_{TH} imbalance. Conditions: 25°C, 0 Ω (OFF), 0 Ω (ON), 800 V, 900 A

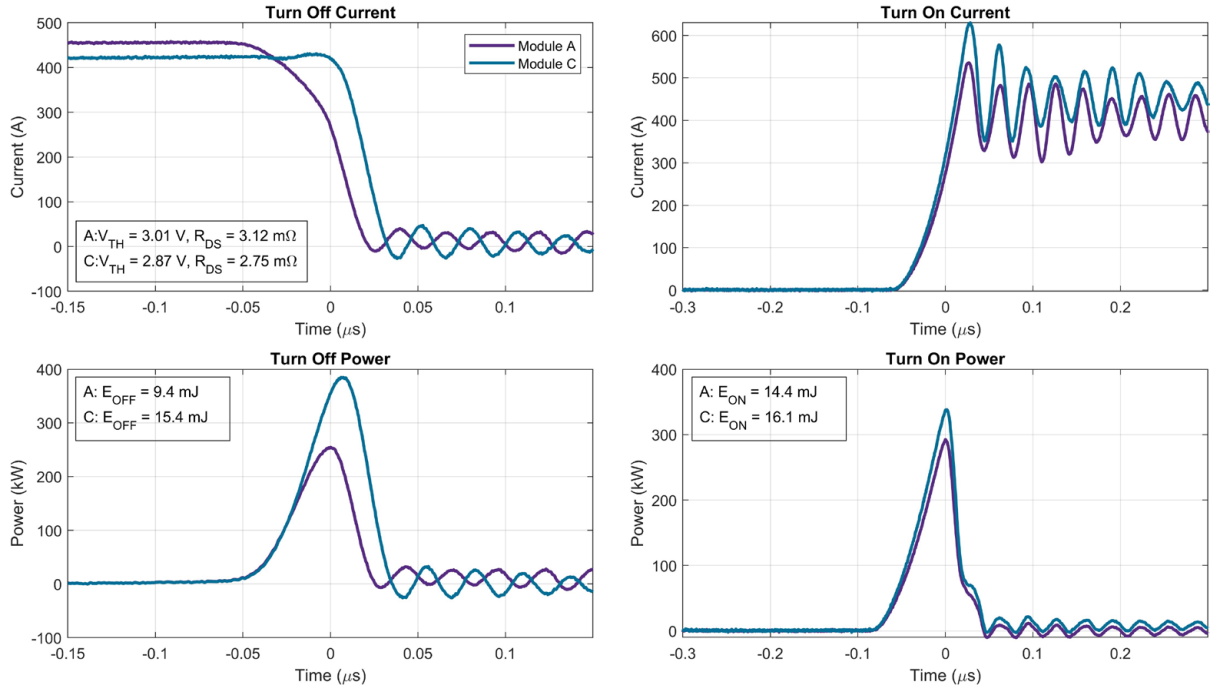


Figure 58: Module parallel example (2 modules) with V_{TH} imbalance and R_{DS} imbalance. Conditions: 25°C, 0 Ω (OFF), 0 Ω (ON), 800 V, 900 A

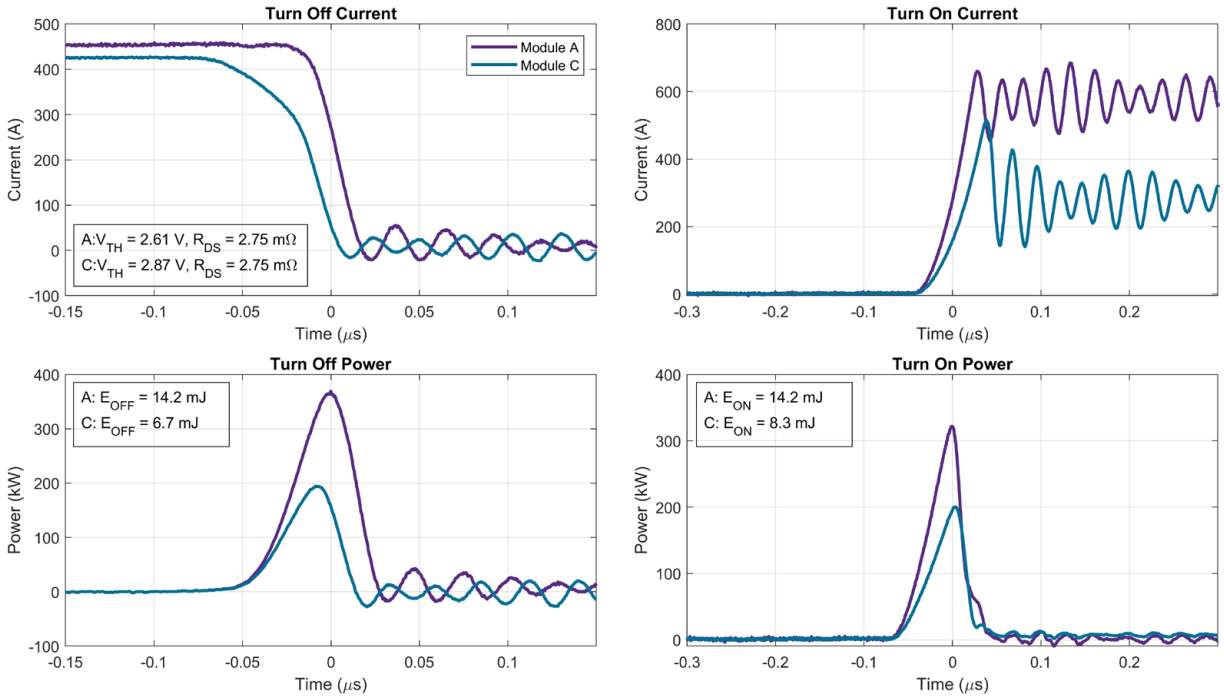


Figure 59: Module parallel example (2 modules) with V_{TH} imbalance. Conditions: 25°C, 0 Ω (OFF), 0 Ω (ON), 800 V, 900 A

8.4 Dynamic Mismatch: Operating Regions of Interest

The importance of dynamic current sharing depends on the operating conditions of the application. In general, conditions that result in higher switching losses will result in higher temperature differences between paralleled modules. For example, increasing the switching frequency, load current, or gate resistance will lead to worsened mismatch. Figure 60 shows a heatmap of temperature imbalance for two CAB450M12XM3 power

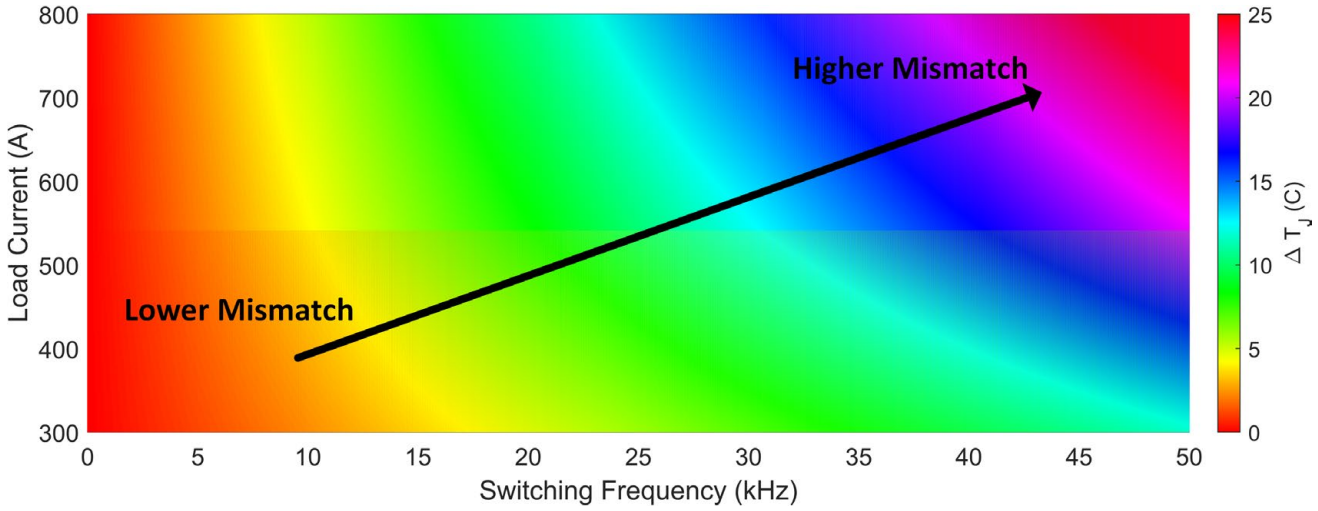


Figure 60: Heatmap of dynamic losses across load current and switching frequency: applications at higher switching frequencies are more prone to temperature imbalance caused by V_{TH}

modules using empirically measured switching loss imbalance at an 800 V bus with 0 Ω R_G. The estimated temperature mismatch increases with switching frequency and load current. In particular, systems operating at lower switching frequencies (around 20 kHz and below) are less susceptible to temperature imbalance caused by dynamic imbalance. Many systems operating in this region do not require mitigation methods beyond basic layout principles to operate within specifications.

8.5 Reverse Conduction & Reverse Recovery

The recommendations and trends provided to improve the forward conduction and switching loss imbalance for power modules applies equally to the reverse conduction and reverse recovery behavior, but with the following differences:

- Reverse conduction loss during the OFF state is determined by the body diode forward voltage, not $R_{DS,ON}$
- Reverse recovery losses do not have strong dependencies on static MOSFET parameters
- Reverse recovery losses are extremely small compared to switching losses and are negligible when considering power loss imbalance

For example, consider the reverse recovery current waveforms in Figure 61. The top plot shows the reverse recovery current for a system using a single gate driver for each module, and the bottom plot shows a

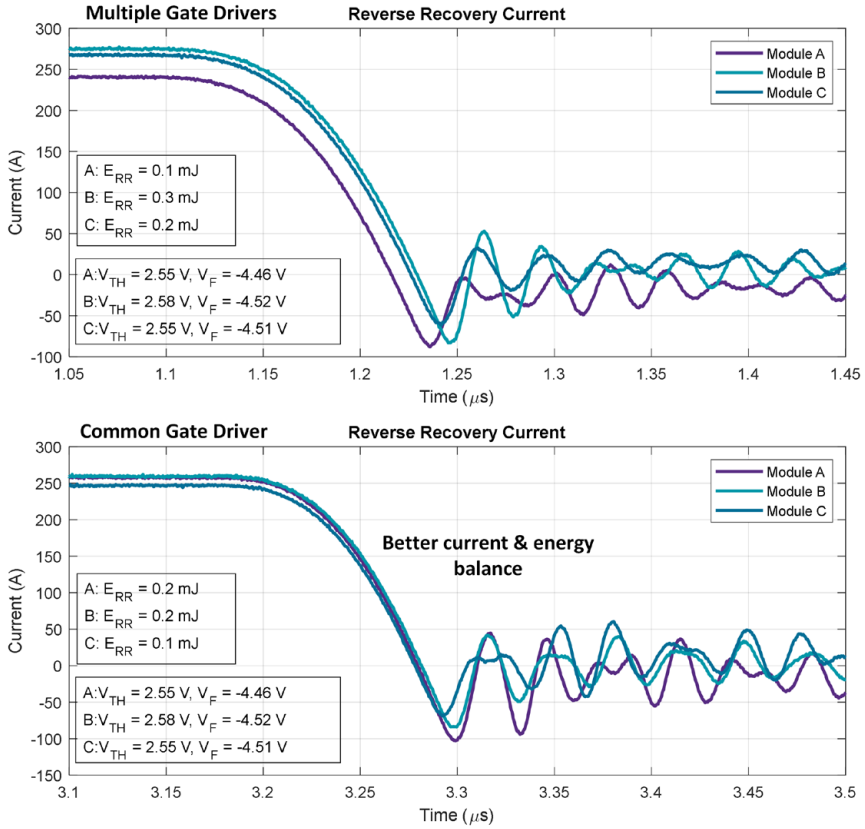


Figure 61: Reverse recovery module paralleling with multiple gate drivers (top) and a common gate driver (bottom)

measurement of the same configuration but with a common gate driver. As had been seen in normal switching waveforms, module A transitions first due to the shorter gate driver propagation delay, and the system shows much better current sharing performance with the common gate driver. However, note that the reverse recovery losses are on the order of 0.1 mJ – 0.3 mJ, which are two orders of magnitude less than has been seen with switching losses for this module.

8.6 Conclusions

Table 1: Dynamic Current Sharing Considerations

Design Parameter	Importance for Dynamic Current Sharing	Comments
Power Loop Inductance Imbalance	Low	Power loop inductance should be minimized to reduce V_{DS} overshoot, but has minimal affect current sharing
Gate Loop Inductance Imbalance	Low	Gate loop inductance should be minimized to reduce V_{GS} overshoot, but has minimal affect current sharing
Load Impedance Mismatch	High	Modules should have a symmetric attachment to the load. Inserting inductance between each module and the load can reduce mismatch. Connect midpoints at the load, instead of at the bus
Gate Driver Implementation	High	Common gate driver implementations offer significantly better current sharing than distributed gate driver approaches. Propagation delay of signals
Module Characteristics	Medium	Increased V_{TH} imbalance between modules can increase dynamic mismatch. Before addressing this issue, ensure that the layout and gate driver implementations are optimized.

9. Short-Circuit Protection

For more information on short-circuit failures and DESAT protection circuits, see PRD-08296.

The implementation of short-circuit protection (usually with a desaturation detection circuit, or DESAT) depends on the gate driver implementation (see Figure 12). When implementing short-circuit protection using the multiple gate driver approach, the protection can be implemented on each module in isolation per standard design practices. During a short-circuit event, the module with 1) the lowest impedance connection to the load and/or 2) the lowest $R_{DS,ON}$ will conduct the most current, and usually trip first. After the module trips, the current will then flow through the remaining paralleled modules, which will then trip, and the system will be protected.

Two example short circuit events for three paralleled CAB450M12XM3 power modules are shown in Figure 62. On the left, the load is shorted and connected from L_A to V_{+A} in Figure 7 (lowest inductance to module A). On the right, the load is shorted from both L_A to V_{+A} and L_C to V_{+C} (inductance balanced to module A and C, highest to

module B). The location of the shorted load has a significant effect on the current through each module. On the left, module A conducts more current than B or C, and the protection activates first. The current from module A then flows through B and C, and the protection circuits trip. On the right, all three modules conduct evenly until module C trips, in which the current then flows through A and B until they trip. This suggests that, for short-circuit events caused by a shorted load, the impedance between the load and each module plays an important role in the current they are subjected to during a short circuit.

For systems using a single gate driver, the DESAT circuit can be applied either at a single module or at a common node between the modules. If the DESAT circuit is applied to a single module, there may be a delay in detection. For example, consider if module B were configured with the DESAT circuit in the test setup shown in the left of Figure 62. If the DESAT circuit is applied to a common mode between the modules, the DESAT circuit may not work effectively. Any designs using these approaches will need to be tested and validated to ensure that they are robust and meet the system requirements.

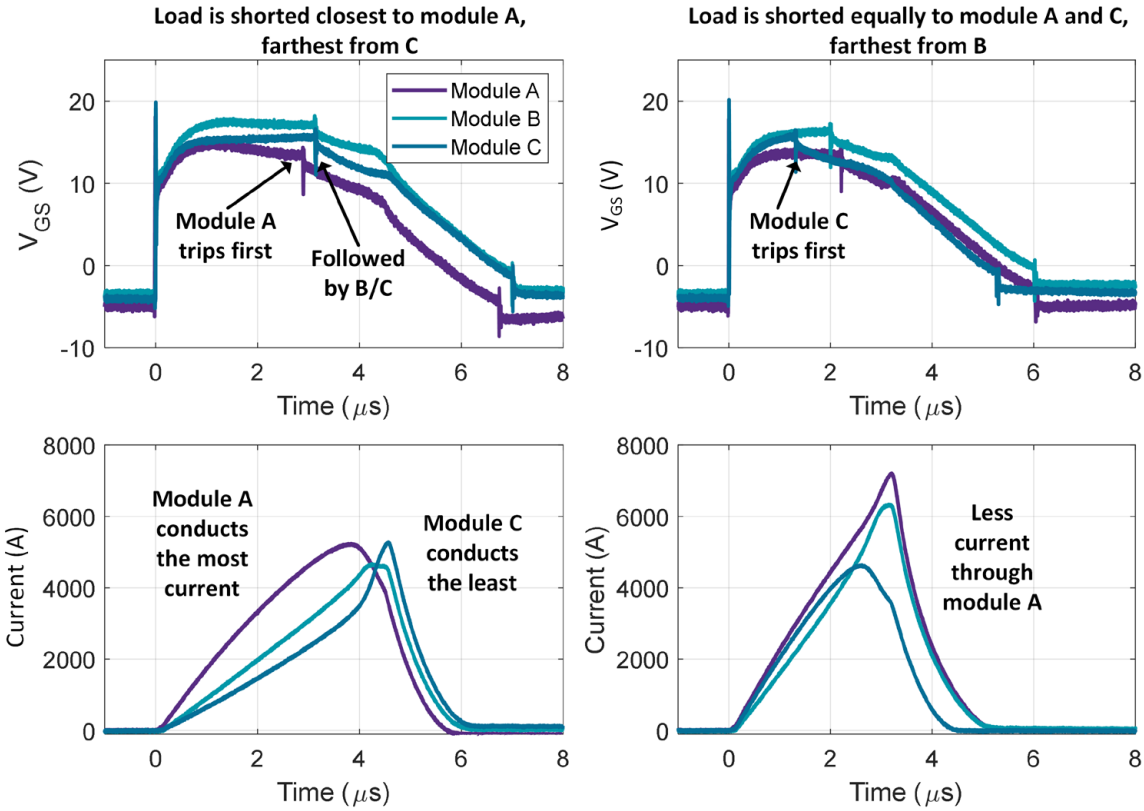


Figure 62: Short circuit event with load shorted closest to module A (left) and load shorted across both module A and C (right)

Revision History

Date	Revision	Changes
January 2025	1	Initial Release

References

[1] X. She, H. Q. Alex, L. Oscar and O. Burak, "Review of Silicon Carbide Power Devices and Their Applications," IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, 2017.

[2] K. Sheng, S. J. Finney and B. W. Williams, "Thermal stability of IGBT high-frequency operation," in IEEE Transactions on Industrial Electronics, vol. 47, no. 1, pp. 9-16, Feb. 2000, doi: 10.1109/41.824018.

[3] F. Wagner, G. Reber, M. Rittner, M. Guyenot, M. Nitzsche and B. Wunderle, "Power Cycling of SiC-MOSFET Single-Chip Modules with Additional Measurement Cycles for Life End Determination," CIPS 2020; 11th International Conference on Integrated Power Electronics Systems, Berlin, Germany, 2020, pp. 1-6.

[4] S. Liu, Y. -H. Mei, J. Li, X. Li and G. -Q. Lu, "Copper-Wire Stress Buffers for Extending Lifetime of Double-Sided Bidirectional SiC Modules," in IEEE Transactions on Power Electronics, vol. 38, no. 6, pp. 7118-7127, June 2023, doi: 10.1109/TPEL.2023.3252266.

[5] G. Romano, A. Fayyaz, M. Riccio, L. Maresca, G. Breglio, A. Castellazzi and A. Irace, "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2016.

[6] J. Liu, G. Zhang, B. Wang, W. Li and J. Wang, "Gate Failure Physics of SiC MOSFETs Under Short-Circuit Stress," IEEE Electron Device Letters, vol. 41, no. 1, pp. 103-106, 2019.

[7] B. T. DeBoi, B. W. Nelson, A. Curbow, T. McNutt and A. N. Lemmon, “Computational Efficiency Analysis of a Compact Behavioral SiC SPICE Model,” PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-9, doi: 10.30420/566091262.

[8] B. DeBoi, B. Nelson and A. Curbow, "Accuracy Evaluation and Proposed Dynamic Tuning Procedure of a Compact SiC SPICE Model," PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2024, pp. 1470-1479, doi: 10.30420/566262199.

[9] Y. Wang et al., "Investigation of Threshold Voltage Mismatch on Junction Temperature Estimation for Multichip SiC MOSFET Power Modules," 2023 IEEE 14th International Conference on Power Electronics and Drive Systems (PEDS), Montreal, QC, Canada, 2023, pp. 1-6, doi: 10.1109/PEDS57185.2023.10268827.

[10] Y. Wei, L. Du, X. Du and A. Mantooth, "Multi-level Active Gate Driver for SiC MOSFETs with Paralleling Operation," 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), Cartagena, Colombia, 2021, pp. 1-7, doi: 10.1109/COMPEL52922.2021.9645994.

[11] L. Du, X. Du, H. Cao, H. Yang and H. A. Mantooth, "A Simple Gate Driver Design for SiC MOSFET Paralleled Operation," 2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia), Jeju Island, Korea, Republic of, 2023, pp. 2026-2031, doi: 10.23919/ICPE2023-ECCEAsia54778.2023.10213699.

[12] Y. Funaki and K. Wada, "Gate Drive Circuit Configuration for Current Balancing of SiC MOSFETs Connected in Parallel," 2021 IEEE International Future Energy Electronics Conference (IFEEC), Taipei, Taiwan, 2021, pp. 1-5, doi: 10.1109/IFEEC53238.2021.9661805.

[13] Y. He, J. Zhang and S. Shao, "Dynamic Current Balancing for Paralleled SiC MOSFETs With Circuit Mismatches Considering Circulating Current in Drive Circuit," in CPSS Transactions on Power Electronics and Applications, vol. 9, no. 2, pp. 219-229, June 2024, doi: 10.24295/CPSSTPEA.2024.00004.

[14] S. Liu, G. Dong, T. Mishima and C. -M. Lai, "Over 98% Efficiency SiC-MOSFET Based Four-Phase Interleaved Bidirectional DC–DC Converter Featuring Wide-Range Voltage Ratio," in IEEE Transactions on Power Electronics, vol. 39, no. 7, pp. 8436-8455, July 2024, doi: 10.1109/TPEL.2024.3389052.
[15] H. Li et al., "Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs," in IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 621-634, Jan. 2016, doi: 10.1109/TPEL.2015.2408054.
[16] D. Peftitsis, R. Baburske, J. Rabkowski, J. Lutz, G. Tolstoy and H. -P. Nee, "Challenges regarding parallel-connection of SiC JFETs," 8th International Conference on Power Electronics - ECCE Asia, Jeju, Korea (South), 2011, pp. 1095-1101, doi: 10.1109/ICPE.2011.5944660.
[17] J. Lv, C. Chen, B. Liu, Y. Yan and Y. Kang, "A Dynamic Current Balancing Method for Paralleled SiC MOSFETs Using Monolithic Si-RC Snubber Based on a Dynamic Current Sharing Model," in IEEE Transactions on Power Electronics, vol. 37, no. 11, pp. 13368-13384, Nov. 2022, doi: 10.1109/TPEL.2022.3179829.
[18] Y. Nakamura, N. Kuroda, A. Yamaguchi, K. Nakahara, M. Shintani and T. Sato, "Influence of Device Parameter Variability on Current Sharing of Parallel-Connected SiC MOSFETs," 2020 IEEE 29th Asian Test Symposium (ATS), Penang, Malaysia, 2020, pp. 1-6, doi: 10.1109/ATS49688.2020.9301592.
[19] N. Lin, Y. Zhao and H. A. Mantooth, "An Effective Current Balancing Method for Inverters With Paralleled Silicon Carbide Power Modules," in IEEE Transactions on Industry Applications, vol. 59, no. 6, pp. 6986-7000, Nov.-Dec. 2023, doi: 10.1109/TIA.2023.3306750.
[20] J. Lv et al., "A Dynamic Current Balancing Method for Paralleled SiC MOSFETs With Gate-Branch Full-Coupled Inductors," in IEEE Transactions on Power Electronics, vol. 39, no. 10, pp. 12600-12614, Oct. 2024, doi: 10.1109/TPEL.2024.3423414.
[21] Y. Mao, Z. Miao, C. -M. Wang and K. D. T. Ngo, "Balancing of Peak Currents Between Paralleled SiC MOSFETs by Drive-Source Resistors and Coupled Power-Source Inductors," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8334-8343, Oct. 2017, doi: 10.1109/TIE.2017.2716868.
[22] N. Lin, Y. Zhao and H. A. Mantooth, "An Effective Current Balancing Method for Inverters With Paralleled Silicon Carbide Power Modules," in IEEE Transactions on Industry Applications, vol. 59, no. 6, pp. 6986-7000, Nov.-Dec. 2023, doi: 10.1109/TIA.2023.3306750.
[23] H. Li, S. Zhao, X. Wang, L. Ding and H. A. Mantooth, "Parallel Connection of Silicon Carbide MOSFETs—Challenges, Mechanism, and Solutions," in IEEE Transactions on Power Electronics, vol. 38, no. 8, pp. 9731-9749, Aug. 2023, doi: 10.1109/TPEL.2023.3278270.
[24] K. Matsubara and K. Wada, "Current Balancing for Parallel Connection of Silicon Carbide MOSFETs Using Bus Bar Integrated Magnetic Material," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 2688-2693, doi: 10.1109/APEC.2019.8721777.