WP396 (v1.2) December 12, 2017

Spartan-6 FPGAs: Performance, Power, and I/O Optimized for Cost-Sensitive Applications

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The rapid change in today's design environment requires a programmable solution that provides high performance and low power at the lowest cost to address the needs of cost-sensitive systems.

The purpose of this white paper is to describe how Spartan®-6 FPGAs address the needs of cost-sensitive systems. The ability to connect efficiently and inexpensively to commodity memories, high-performance chip-to-chip interface capability, and innovative power down modes are just a few of the problems solved by high-performance, low-power, and low-cost Spartan-6 FPGAs.

Introduction

With the dramatic shifts in the market, designers of cost-sensitive products are driven to deliver innovative systems with smaller budgets and tighter schedules. Designers need flexible, easy to use system-on-chip type solutions.

To address these demands, Xilinx integrated design innovations derived from the successful Virtex®-5 FPGA architecture into Spartan-6 FPGAs. The Spartan-6 family offers designers of cost-sensitive systems multiple advantages not found in alternative products. These advantages include:

- 45nm Process Node
  - An FPGA family on 45nm process node delivering best-in-class cost, power, and performance.
- High-speed I/O
  - Best-in-class performance chip-to-chip interfaces with 1,080Mb/s LVDS and 3.2Gb/s serial transceivers.
- Power-down Modes
  - Suspend mode with fast wake-up maintains configuration and state, reducing static power by 20–30%.
- Embedded Memory Controller
  - Offering mainstream memory interface speeds, e.g., DDR3 at 800Mb/s.
- Comprehensive Design Kit Offering
  - Complete development platform for Ethernet and embedded development.
  - MicroBlaze™ Processor Design Kit.
  - In-depth, step-by-step tutorials to facilitate design closure.

Spartan-6 FPGAs meet these requirements for cost-sensitive applications like multifunction printers, industrial and home networking, compact programmable logic controllers, automotive infotainment, motor control, portable medical and industrial instruments, D-SLR cameras and camcorders, software defined radios, and video surveillance.

Solving Key Challenges

Key technological breakthroughs have enabled the Spartan-6 family to offer a balance of power and performance in a cost-sensitive FPGA. Spartan-6 FPGAs offer designers tremendous capabilities in the areas of transceivers, DSP, high-speed I/O, clock management, security, memory capacity, and control. With Spartan-6 FPGAs, designers no longer need to choose between low-cost, low-capability FPGAs versus higher cost, feature-rich FPGAs.

As an example, Spartan-6 FPGAs provide the ideal programmable platform to optimally perform computationally intensive facial recognition, intelligent eye tracking, and ever increasing high-resolution imaging that allow digital signage applications to deliver an intuitive, adaptive, and immersive experience.

The tightly integrated programmable logic and I/O optimization enable feature-rich implementation and hardware accelerated video processing functions for the ultimate mix of performance with low BOM cost and reduced power consumption.

The benefits of Spartan-6 FPGAs for Digital Signage applications include:

- Increased system performance with hardware acceleration for computationally intensive functions such as metadata acquisition/tagging, autosense facial recognition eye contact, and object tracking.
- A fully programmable platform with Full HD image and video processing to enable customized picture quality differentiation.
- I/O optimization through integration of the latest interface technologies like SD/HD/3G-SDI, DisplayPort, and HDMI.
- Integrated video over IP bridging standards like Ethernet AVB.

The tightly integrated programmable logic and I/O optimization enable feature-rich implementation and hardware accelerated video processing functions for the ultimate mix of performance with low BOM cost and reduced power consumption. See the Spartan-6 FPGA usage in the digital signage application example in Figure 1.

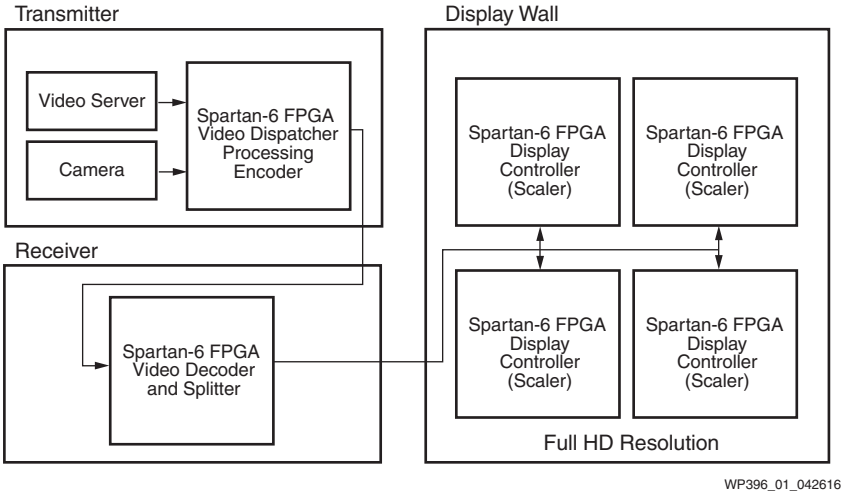

Figure 1: **Full-HD Intelligent Digital Signage Using Spartan-6 FPGAs**

Integrated High-Speed Serial Transceivers Reduce Cost

Today's systems require high bandwidth for interfacing chip-to-chip across backplanes and long distance transmission over fiber optics. Parallel I/O reaches a speed limit around 1GHz for single-ended pins and below 1.5GHz for LVDS differential pin pairs, even with the latest standards.

Wide parallel connections also consume a significant number of I/O and the receivers burn a large amount of power. These connections create skew between data lanes as well as between clock and data lanes. Ultimately, this introduces crosstalk and other signal integrity issues.The integrated high-speed serial transceivers found in Spartan-6 LXT FPGAs solve all these problems.

The Spartan-6 LXT FPGAs complement low-cost logic capability with high-speed serial connectivity, which has up to eight GTP transceivers (3.2Gb/s line rate). Capitalizing on the vast SerDes capabilities in the Virtex FPGA families, Spartan-6 LXT devices deliver protocols at 3.2Gb/s and below. See Table 1 for key transceiver protocol support comparisons.

Table 1: **Transceiver Protocol Support**

Speed	Spartan-6 FPGA High-Speed Serial Standards
3.125Gb/s	XAUI, SRIO
3.072Gb/s	OBSAI, CPRI
3.0Gb/s	SAS II, SATA II, V-by-One
2.97Gb/s	3G-SDI
2.7Gb/s	DisplayPort
2.5Gb/s	PCIe® G1.1, Infiniband
2.488Gb/s	OC-48
2.125Gb/s	2G Fibre-Channel
1.485Gb/s	HD-SDI
1.25Gb/s	1GbE

Another advantage unique to the Spartan-6 LXT FPGAs is that its logic interface is nearly identical to the interfaces of the Virtex-5 FPGA GTP transceivers, facilitating porting of designs to the lower cost Spartan-6 FPGAs. As listed in Table 1, Spartan-6 LXT FPGAs support a broad range of standards, supporting today's higher performance designs.

High Performance I/O Standards Simplify System Design

The Spartan-6 FPGA leads in I/O richness with the broadest support in its class. To meet the wide range of I/O requirements found in cost-sensitive systems, Spartan-6 FPGAs provide the fastest in class with LVDS—up to 1,080Mb/s. This offers a significant advantage compared to Altera's Cyclone IV GX at 840Mb/s. The Spartan-6 FPGA I/O enables a broad range of new applications, including but not limited to HD video, display, and other high-bandwidth interfaces. In addition to the LVDS I/O, Spartan-6 FPGAs have dedicated clock routing to reduce duty-cycle distortion and serializing/deserializing I/O, enabling up to 1:8 serial-to-parallel data conversion for easier-to-design high-speed differential interfaces. For detailed I/O standard support comparison details, see Table 2.

Table 2: **I/O Standard Support Comparison**

I/O Standards	Spartan-6 FPGA	Cyclone IV GX[1]
LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, and 1.2V)	✓	✓
LVDS and Bus LVDS	✓[2]	✓
LVPECL (2.5V, 3.3V)	✓	✓[3]
PCI	✓	✓
I2C	✓	
HSTL (1.8V, 1.5V, Classes I, II, III)	✓	
HSTL_I_12 (unidirectional only)		✓
PPDS	✓	✓
TMDS	✓	
RSDS	✓	✓
Display Port Aux Channel	✓	
SSTL (3.3V, 2.5V, 1.8V, 1.5V Classes I, II)	✓	✓
DIFF_SSTL	✓	
DIFF_HSTL	✓	
LVTTL	✓	✓

Notes:

1. Source: Cyclone IV Handbook December 2010.
2. Sub LVDS is available upon request. Contact your local Xilinx Sales Representative for more information.
3. LVPECL supported only on dedicated clock input**s.**

Spartan-6 FPGAs also support true 3.3V standards with full 4.4V overshoot support and offer full 3.3V LVCMOS and LVTTL 24 mA output drive. Supporting true 3.3V standards simplifies board design with standard tolerance components and enables design teams to design the standards into high-speed environments with minimal simulation and reduced overshoot concerns. Designers using competing FPGAs need to overcome the limited output drives and the reduction of overshoot by adding buffers for high fanout signals or line drivers for backplanes and tighter board traces, thus adding to total system complexity, cost, and design time.

Spartan-6 LX devices only require two power rails—further simplifying and lowering system design costs. Lower power-supply complexity (fewer, cheaper regulators, and reduced bypass requirements) not only makes the board less expensive and more reliable, but easier to design. Designers who are using Spartan-6 FPGAs do not need to address power-rail isolation, tantalum capacitors, and ferrite beads for every power pin. With true 3.3V I/O capability, higher drive strength, and fewer power rails, system and board design is easier and lower cost with Spartan-6 FPGAs.

To learn more about Spartan-6 FPGA SelectIO™ technology go to UG381, *Spartan-6 FPGA SelectIO Resources User Guide.*

Optimized Logic Performance and Architecture Efficiency

To meet the high-volume industry's demands of cost-sensitive applications, it is essential that FPGAs for these applications provide high performance with the lowest cost logic architecture. The optimized Spartan-6 FPGA logic architecture meets these demands by using a dual-register 6-input look-up table (LUT) structure. The traditional 4-input LUT used by other FPGA families can provide an adequate solution for simple functions, but the increased logic cell capability of the 6-input LUT (with an additional flip-flop) minimizes the required levels of logic, reducing delay and improving system through-put by up to 25%. See Figure 2 for details on the LUT architectural comparison.

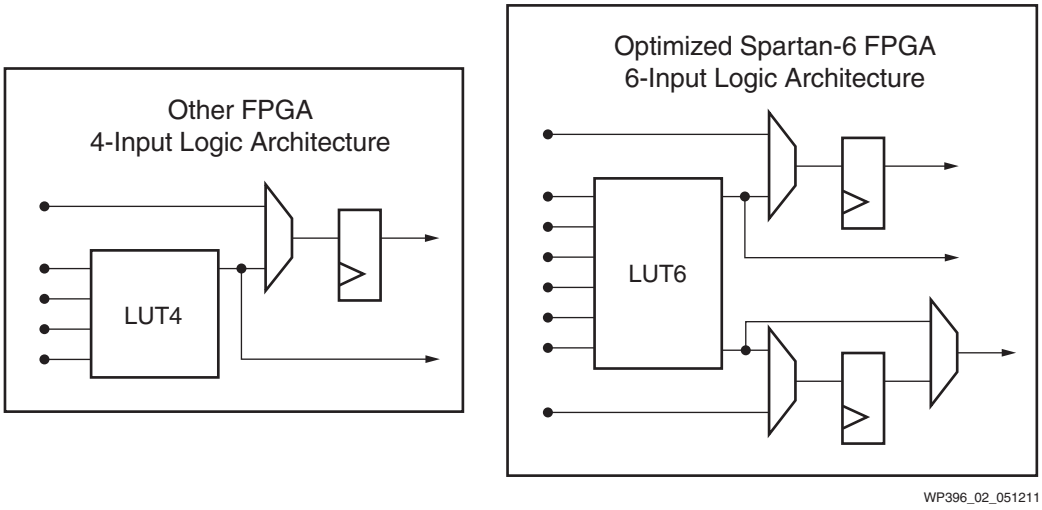

Figure 2: **6-Input LUT versus 4-Input LUT Alternative**

Design comparisons on logic performance also show a significant benefit with Spartan-6 FPGAs. Table 3 is the result of running a suite of benchmark designs using tools from both Xilinx and Altera. Against all three speed grades, Spartan-6 FPGAs are faster versus the equivalent Cyclone IV devices.

Table 3: **FPGA Performance Benchmarking**

Speed Grade Benchmark[1]	Spartan-6 FPGA Advantage
Spartan-6 FPGA -2 speed grade vs. Cyclone IV -8	20%+ faster
Spartan-6 FPGA -3 speed grade vs. Cyclone IV -7	19% faster
Spartan-6 FPGA -3 speed grade vs. Cyclone IV -6	12% faster

Notes:

1. Using Xilinx ISE® 13.1 software and Quartus 10 Altera tools across a suite of 392 designs.

Integrated Memory Controller for 2X Greater Performance

Spartan-6 FPGAs offer hard memory controller blocks (MCBs) for the lowest power and highest performance. All but the smallest Spartan-6 device include dedicated MCBs, with each MCB supporting DRAM standards (LPDDR, DDR, DDR2, and DDR3). The integrated MCBs have predictable timing and allow designers to quickly and easily design and implement DDR3-800 memory interfaces. Spartan-6 FPGAs with MCBs support access rates of up to 800Mb/s compared to Cyclone IV GX DDR2 400Mb/s soft controller capability. See the memory interface capability comparison in Figure 3.

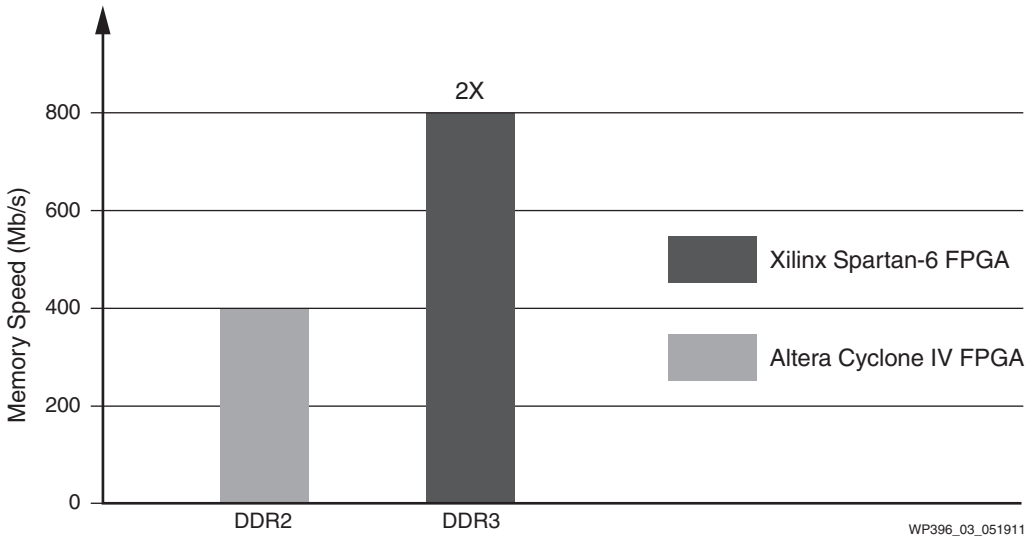

Figure 3: **DDR3 Memory Interface Speed Comparison**

Integrated Digital Signal Processing

To maximize performance while minimizing power consumption and silicon utilization, Spartan-6 devices support math-intensive applications with a high ratio of DSP48A1 slices to general-purpose logic. These DSP48A1 slices support many independent functions, including multiplier, multiplier-accumulator (MACC), pre-adder/subtracter followed by a multiply accumulator, multiplier followed by an adder, wide bus multiplexers, and wide counters. Multiple DSP48A1 slices can be cascaded together to implement wide math functions, DSP operations, filters, and complex arithmetic without wasting any general FPGA logic. Figure 4 shows the efficiency of the DSP48A1 slice.

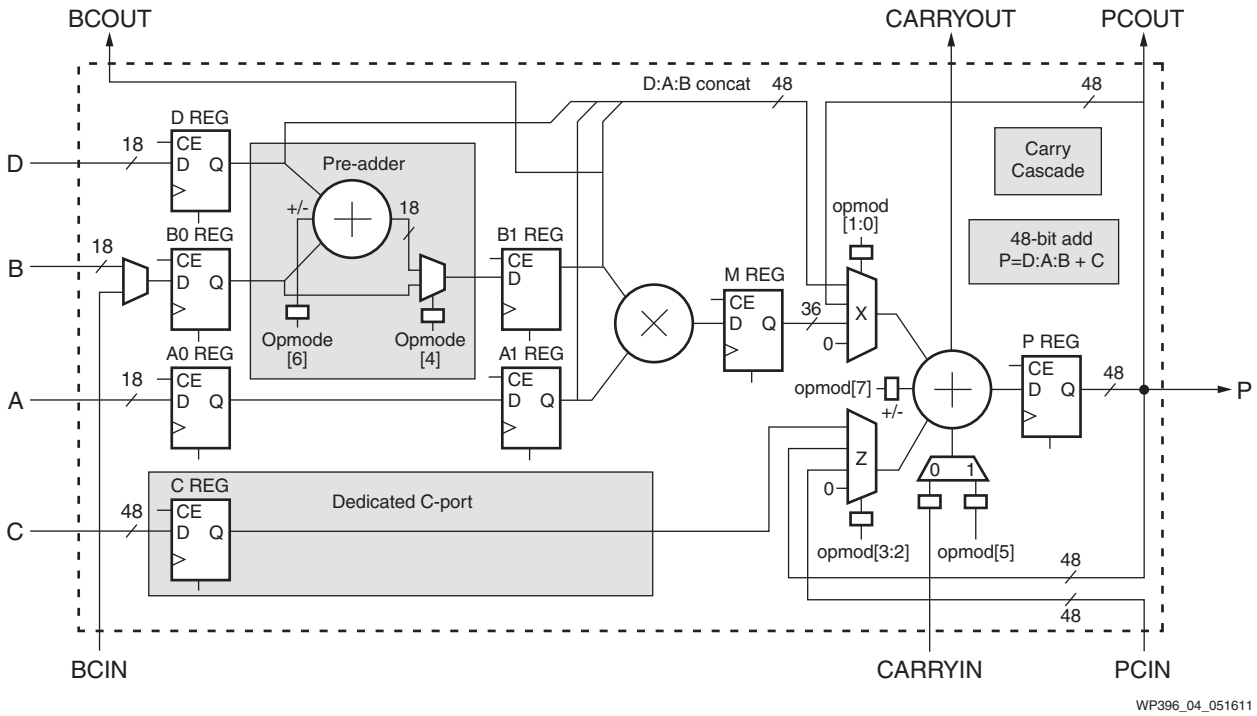

Figure 4: **Spartan-6 FPGA DSP48A1 Slice**

The enhanced DSP48A1 structure found in Spartan-6 devices includes the highly efficient pre-adder. The pre-adder provides many user benefits, including:

- Reduced power consumption by 50% compared to architectures without a pre-adder.
- Implementation with the smallest amount of logic while competing devices must perform the pre-adder function in the logic.
- A smaller footprint.
- Xilinx synthesis tools (XST) support, offering easy implementation.

Figure 5 shows an implementation of the symmetrical FIR filter in a leading alternative FPGA.

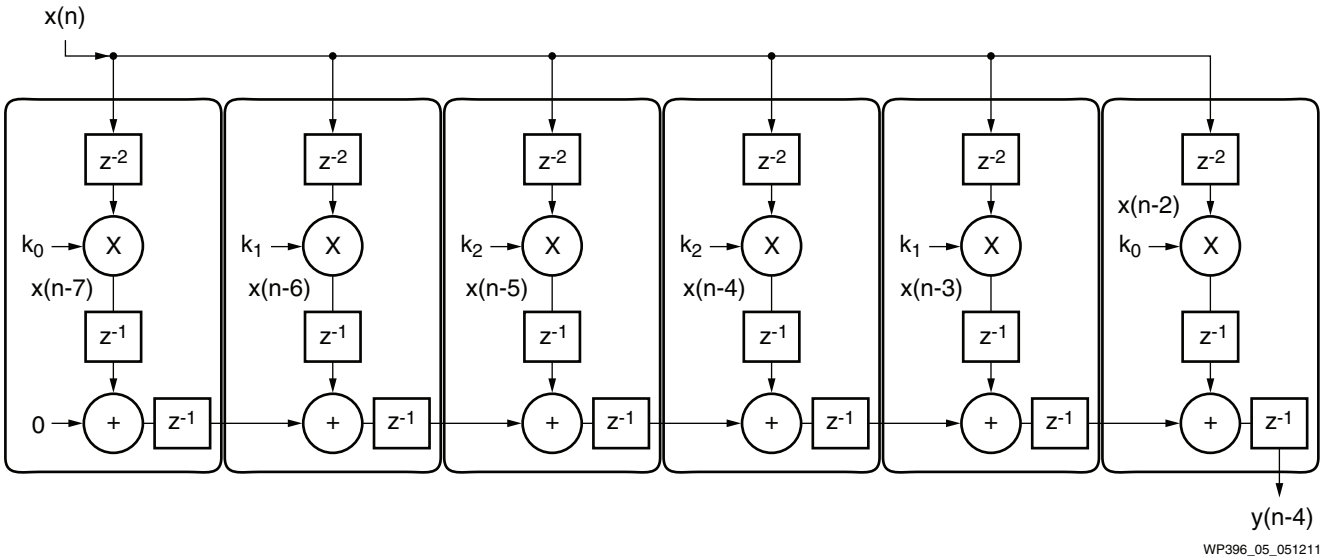

Figure 5: **Symmetrical FIR Filter in a Leading Alternative FPGA**

This same function in Spartan-6 devices requires much less logic and half the amount of DSP—and as much as 50% less power is consumed. See Figure 6. Ultimately, this enables a smaller device requirement and lower cost.

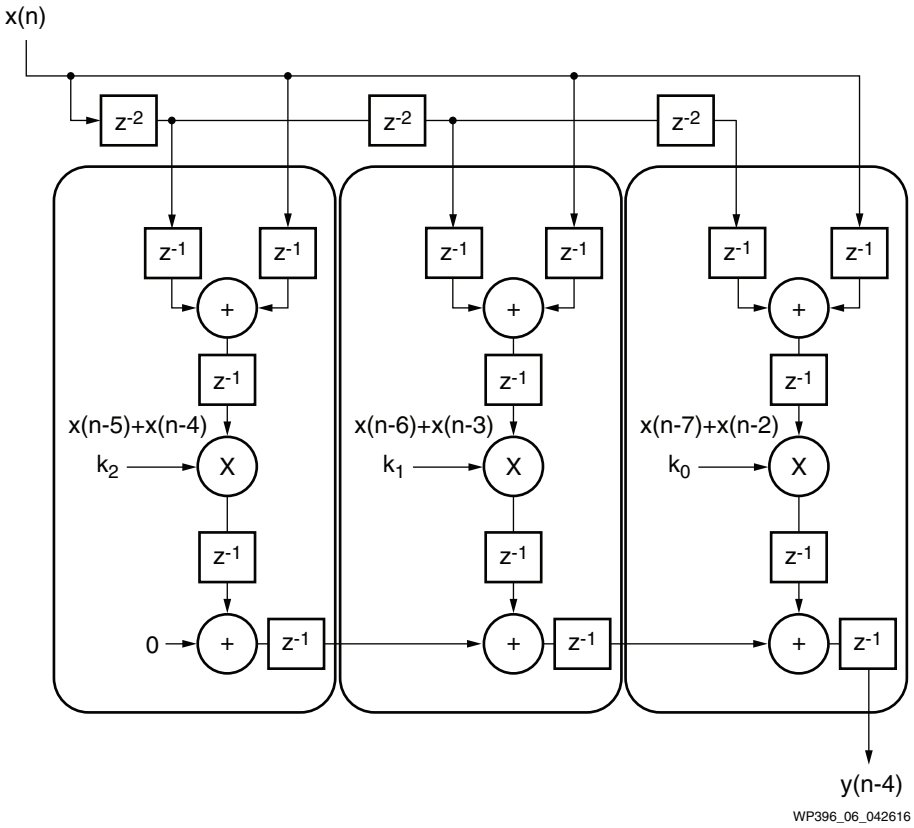

Figure 6: **Symmetrical FIR Filter in a Spartan-6 Device**

Integrated Endpoint Block for PCI Express

To streamline designs and lower development cost, the Spartan-6 FPGA includes the Integrated Endpoint Block for PCI Express® (Gen1) that interfaces seamlessly with the integrated Spartan-6 LXT FPGA serial I/O transceivers. Additionally, this integrated block is highly configurable to meet various design needs and has passed compliance testing performed at the PCI-SIG®. Spartan-6 FPGA hard block implementations not only save approximately 6,000 logic cells, allowing designs to fit into smaller Spartan-6 LXT FPGAs, but reduce cost, design complexity, and time to market due to the elimination of an external PHY chip.

High-Performance Clock Management

The digital clock managers (DCMs) and phase-locked loops (PLLs) in Spartan-6 FPGAs offer more flexibility than competing alternatives. The DCM adds finer phase shift capability than the PLLs available in Cyclone IV. Spartan-6 FPGAs offer up to six clock management tiles (CMTs), each consisting of two DCMs and one PLL, providing a rich clocking structure for internal and external clock distribution, maximizing system clock domain support.

Low Power with 45nm Process Technology

Using process, architectural, and software innovations, Xilinx has made major advances at the 45nm process node in Spartan-6 FPGAs, reducing static, dynamic, and I/O power significantly over previous generations of FPGAs. The closest competitor is at 60nm, which was a process shrink from an existing 65nm set of devices. Comparing Spartan-6 FPGAs to Spartan-3A FPGAs, the average static power in the Spartan-6 devices is 50% lower and dynamic power is 40% lower. Process enhancements in Spartan-6 FPGAs include a transistor selection that balances power and performance, and capacitance reductions (geometry shrink and low-K dielectric).

Spartan-6 FPGAs achieve further power reductions through architectural enhancements like efficient 6-input LUTs, optimized feature mix, clock gating, various hard blocks like DSP, Integrated Endpoint Block for PCI Express, integrated memory controller, AES, programmable I/O slew rate and drive strength capability, system-level power management, and voltage scaling.

Innovative Power Management

Similar to Spartan-3 FPGAs, Spartan-6 FPGAs provide system-level power management features, such as suspend, hibernate, and clock gating. New to Spartan-6 FPGAs, designers now have much finer control with the introduction of the Multi-Pin Wake-Up technology. This feature gives designers the flexibility of using up to eight pins to control wake-up or exit from suspend mode, which maintains configuration and state. Suspend mode offers fast wake-up to respond to external system needs. On average, these features can reduce static power up to 30%—critical for highly power-sensitive applications, such as battery-powered and consumer applications, which can take advantage of dynamically controlled shutdown and wakeup.

Figure 7 shows the comparison of an equivalent Spartan-6 FPGA and Cyclone IV GX device. As illustrated, the example is a heavily utilized device with logic, DSP, and block RAM. In this example, the higher the frequency the greater the benefit, up to 25%, to the total power.

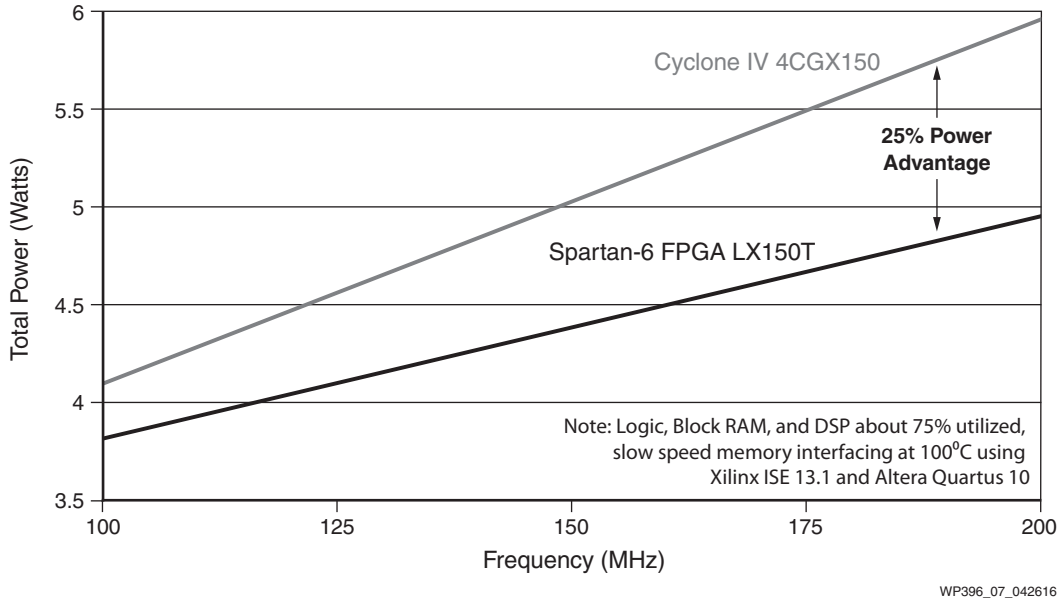

Figure 7: **Total Power Consumption Comparison**

Clock Gating and Voltage Scaling for Further Power Reduction

For additional power savings, designers can use Spartan-6 FPGA's fine-grained clock gating, which eliminates unnecessary clock activity while maintaining functionality and performance. With clock gating, local slice clock drivers or block RAM are dynamically turned off, or gated, when logic is not in use, enabling an excellent opportunity to further reduce dynamic power by up to 30%.

For designers of battery-operated systems who need the lowest possible power consumption, all Spartan-6 LX FPGAs offer the voltage-scaled -1L option, which lowers core voltage from 1.2V to 1.0V, reducing core power an additional 30–40%.

For additional Spartan-6 FPGA power management details, see WP298, *Power Consumption at 40 and 45 nm*.

Quick Design Differentiation with Design Kits

With the broad offering of design kits, designers are provided a "kick-start," eliminating the need to develop all applications from the ground up, enabling a focus on innovation and product differentiation as soon as their development cycle begins.

These integrated platforms of hardware, software, IP, and targeted reference designs deliver productivity gains that greatly exceed the sum-of-the-parts of conventional evaluation boards and design examples. Xilinx and its partners offer a complete set of design kits. See Table 4.

Table 4: **Available Design Kits**

Logic Evaluation Kits
Atlys Spartan-6 FPGA Development Kit
Spartan-6 FPGA SP605 Evaluation Kit
Spartan-6 FPGA SP601 Evaluation Kit
Avnet Spartan-6 LX9 MicroBoard
Connectivity Kits
Spartan-6 FPGA Connectivity Kit
Embedded Kits
Spartan-6 FPGA Embedded Kit
Market-Specific Kits
Spartan-6 FPGA Broadcast Connectivity Kit
Spartan-6 FPGA Consumer Video Kit
Spartan-6 FPGA Industrial Ethernet Kit
Spartan-6 FPGA Industrial Video Processing Kit
Transceiver Characterization Kits
Spartan-6 FPGA SP623 Characterization Kit

No competing FPGA family offers this total solution combination, and Altera Cyclone IV currently offers only a few development kits. For a complete listing of available kits, go to: http://www.xilinx.com/products/boards-and-kits/device-family/nav-spartan-6.html

Cost Efficient Configuration Memories

Programmable devices typically require storage for device configuration just as processors require storage for their program instructions. This means system designers must factor in components such as configuration memory.

While some currently available programmable solutions have integrated nonvolatile memory (NVM) within the device, they are typically designed on older processing technologies. Therefore, they often cannot deliver the signal processing capabilities, high clock speeds, and gigabit transceiver rates required by many of today's equipment manufacturers. In addition, storage requirements for many applications (e.g., protocol stacks) often exceed the capacity of these integrated NVMs.

Other programmable solutions support only their own configuration device, forcing system designers to use proprietary, often very expensive, configuration memories.

Spartan-6 FPGAs support the most popular open-market flash interfaces, ensuring that a low-cost, commonly used configuration device can be chosen. Also supported are many options for remote configuration via an external processor, making use of a centrally located NVM that is shared across the complete system.

Robust Security

Extending low-cost security leadership, Spartan-6 FPGAs provide proven Device DNA for protection from cloning and overbuilding. Spartan-6 FPGAs also include hard readback-disabling circuitry, internal configuration clearing (IPROG), and in the larger densities, advanced 256-bit AES support is available, previously only available in Virtex devices. For more information on Xilinx advanced FPGA security, see WP365, *Solving Today's Design Security Concerns*.

Comparing the Alternatives

The integrated blocks in Spartan-6 FPGAs provide greater efficiency, ease-of-use, lower total power, lower cost, and adept connectivity and memory capabilities. The I/O richness and robust clocking in the 45nm Spartan-6 FPGA family extends its low-cost FPGA market leadership. Table 5 lists the detailed competitive comparison between Spartan-6 FPGAs and Altera Cyclone IV GX FPGAs.

Table 5: **Spartan-6 FPGA versus Cyclone IV GX Capability Comparison**

Xilinx	Altera
Spartan-6 FPGAs	**Cyclone IV**
Low-cost, low-power 45nm Process	60nm Process
Efficient 6-input LUT architecture	4-input LUT
3.2Gb/s transceivers with dedicated PLL	3.125Gb/s
1Gb/s+ LVDS capability	840Mb/s
Integrated DDR3-800 memory controller	DDR2-400
Advanced power management	No
Integrated DSP blocks	Multipliers only
Robust clock management	No
Robust security	No
Comprehensive design kits	No

The Spartan-6 family is a foundational member of the Xilinx Cost-Optimized Portfolio of devices, shown in Figure 8. Spartan-6 FPGAs deliver I/O rich solutions to cost-sensitive applications. To see the entire Cost-Optimized Portfolio, visit https://www.xilinx.com/products/silicon-devices/cost-optimized-portfolio.html

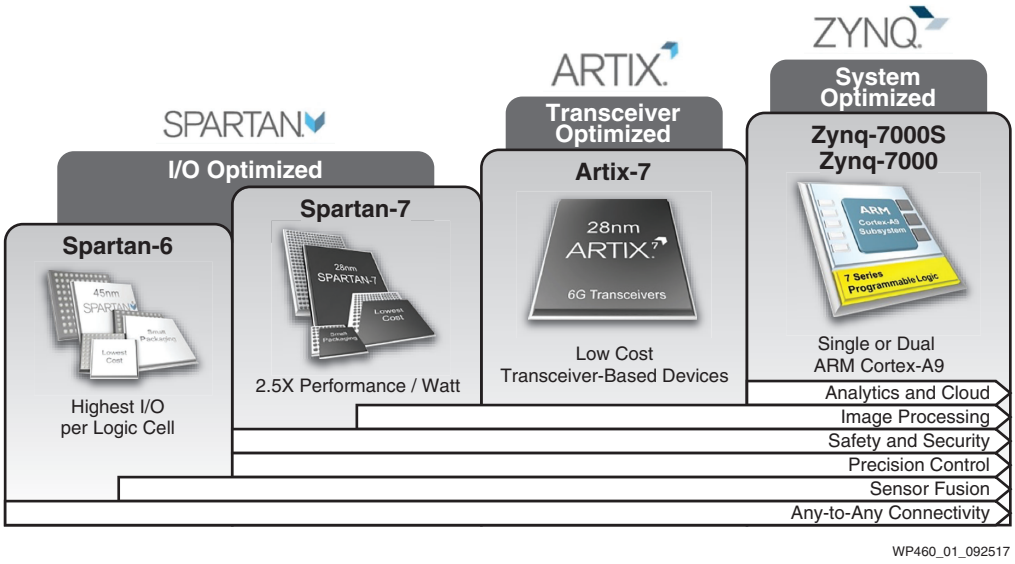

Figure 8: **Xilinx's Cost-Optimized Portfolio Value**

Conclusion

Xilinx understands the problems designers are trying to solve, and offers the low-cost, low-power Spartan-6 family, to fill the performance gap found in alternative low-cost FPGA families. Spartan-6 FPGAs are supported by the Xilinx ISE® Design Suite and free ISE WebPACK™ tools, now available on Windows 10, offering better power efficiency, increased productivity, and higher performance.

For specific Spartan-6 FPGA feature summaries by device, see DS160, *Spartan-6 Family Overview*. And for more Spartan-6 family application details, go to: http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/12/2017	1.2	Updated Figure 8 and Conclusion.
06/01/2016	1.1	General update of white paper, including title, to reflect current market and trends. Updated Figure 6.
05/19/2011	1.0	Initial Xilinx release.

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