AMD
XILINX

VEK280 Evaluation Board User Guide (UG1612)

Introduction

Overview

The VEK280 evaluation board features the AMD Versal™ XCVE2802 device. The VEK280 board enables the demonstration, evaluation, and development of the applications listed here, as well as other customer applications. Many features found on the VEK280 board are subsets of existing Versal adaptive SoC boards (for example, the VCK190 and VMK180 boards).

- Fiber optic
- Communications
- Automotive
- Data center compute acceleration
- Aerospace and defense
- Test and measurement

The VEK280 evaluation board is equipped with many of the common board-level features needed for design development, including:

- HDMI support
- PCIe® support
- CAN support
- PMOD support
- SFP28 optical transceiver support
- LPDDR4 component memory
- USB
- Ethernet networking interfaces
- One FMC+ expansion port

Models of Boards

The following table lists the models for the VEK280 evaluation board. See the VEK280 Evaluation Board product page for details.

Table: Models of VEK280 Evaluation Boards

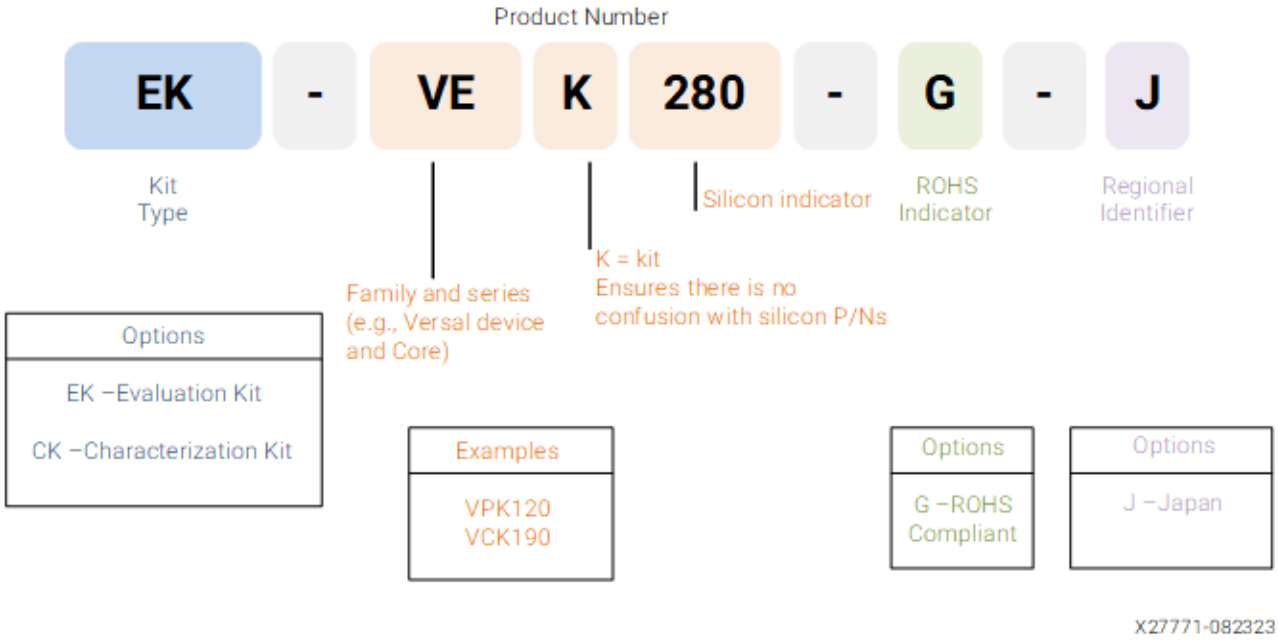
Kit	Description

Kit	Description
EK-VEK280-G	AMD Versal adaptive SoC VEK280 evaluation kit
EK-VEK280-G-J	AMD Versal adaptive SoC VEK280 evaluation kit, Japan specific

Versal Device Kit Numbering

The Versal device kit numbering is illustrated in the following figure.

Figure: Kit Numbering



Navigating Content by Design Process

AMD Adaptive Computing documentation is organized around a set of standard design processes to help you find relevant content for your current development task. You can access the AMD Versal™ adaptive SoC design processes on the Design Hubs page. You can also use the Design Flow Assistant to better understand the design flows and find content that is specific to your intended design needs.

Board System Design

Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. For more information, see Versal Adaptive SoC Design Process Documentation Board System Design.

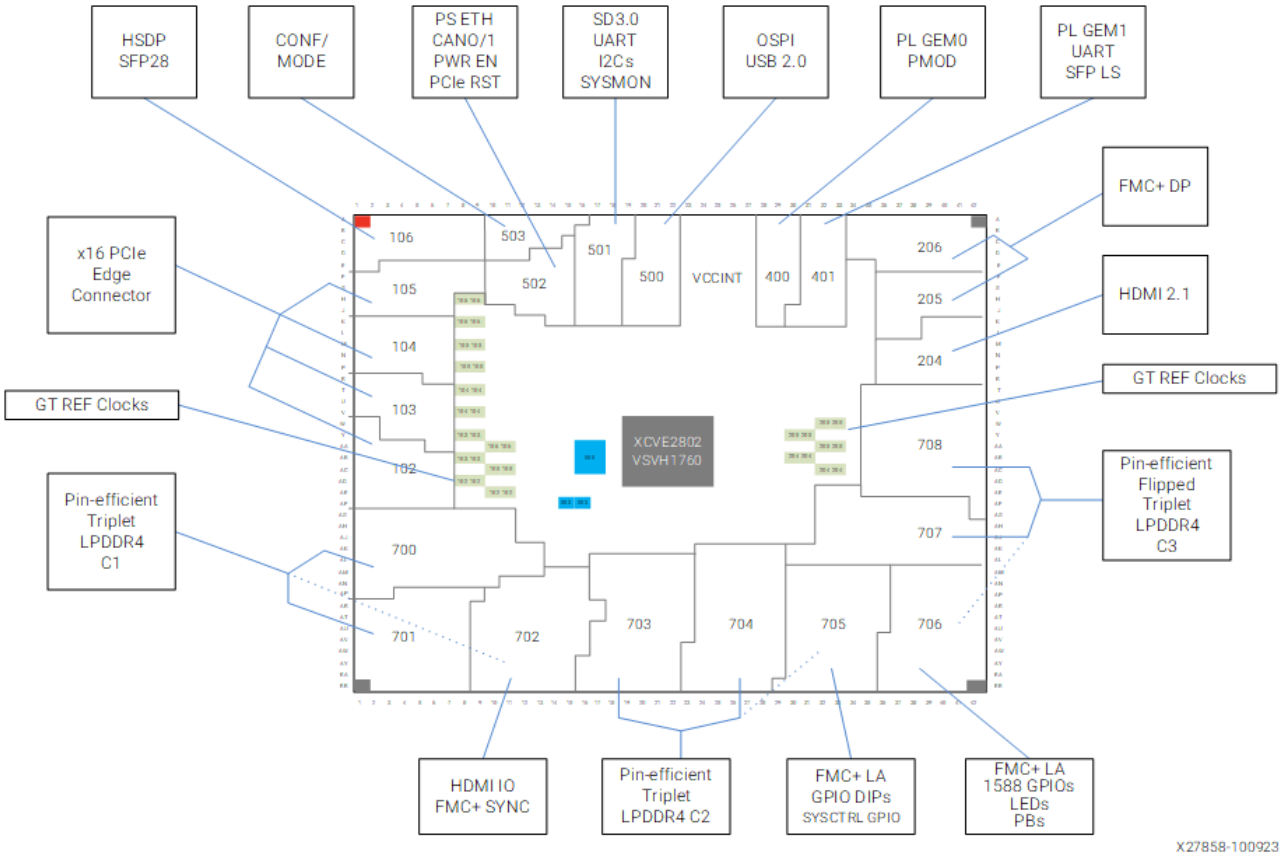
Additional Resources

See Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VEK280 evaluation board.

Block Diagram

A block diagram of the VEK280 evaluation board is shown in the following figure.

Figure: Evaluation Board Block Diagram



Board Features

The VEK280 evaluation board features are listed here. Detailed information for each feature is provided in Board Component Descriptions.

- XCVE2802, VSVH2802 package
- Form factor: see Board Specifications
- Onboard configuration from:
  - USB-to-JTAG bridge
  - JTAG pod 2 mm 2x7 flat cable connector
  - microSD card (PS MIO I/F)
  - Quad SPI (QSPI)/eMMC (system controller I/F)
  - OSPI
- Clocks
  - Versal device bank 702/5/6 RC21008A SYS_CLK_0/1/2 (DIMM) 200 MHz
  - Versal device bank GTY205/6 RC21008A_GTCLK1_OUT6/7 100 MHz
  - Versal device bank GTY106 RC21008A RC21008A_GTCLK1_OUT8 156.25 MHz
  - Versal device bank GTY106 626L15625 HSDP_156_25_REFCLK 156.25 MHz
  - Versal device bank GTY204 8T49N241 HDMI_8T49N241_OUT design dependent
  - Versal device bank GTY204 TMDS1204 HDMI_RCLK_OUT design dependent
  - Versal device bank 503 RC21008A PS_REF_CLK 33.3333 MHz
  - Versal device bank 503 RTC Xtal 32.768 kHz
- Three pin-efficient mode LPDDR4 interfaces (2x32-bit 4 GB components each)
  - XPIO triplet 1 (banks 700, 701, 702)
  - XPIO triplet 2 (banks 703, 704, 705)
  - XPIO triplet 3 (banks 706, 707, 708)
- PL FMCP HSPC (FMC+) connectivity
  - FMCP1 HSPC full LA[00:33] bus
- PL GPIO connections
  - PL UART1 to FTDI
  - PL GPIO DIP switch (4-position)
  - PL GPIO LEDs (four)
  - PL GPIO pushbuttons (two)
  - PL SYSCTLR_GPIO[0:7]
  - PL 1588_GPIO[0:7, SMA_CLK I/O]
- 32 PL GTYP transceivers (8 quads)

    - Not used (1, bank GTYP106)
    - System controller HSDP (1, banks GTYP106)
    - USB-C HSDP (1, banks GTYP106)
    - SFP28 (1, bank GTYP106)
    - PCIe Gen 4 (16, banks GTYP102-GTYP105)
    - FMCP1 HSPC DP (8, banks GTYP205, GTYP206)
- PS PMC MIO connectivity
    - PS MIO[0:12]: boot configuration OSPI
    - PS MIO[13:25]: USB2.0
    - PS MIO[26:36, 51]: SD1 I/F
    - PS MIO[37]: ZU4_TRIGGER/CANFD0_INH (J406)
    - PS MIO[38]: CAN0_nSTB
    - PS MIO[39:41]: SYSMON_I2C
    - PS MIO[42:43]: UART0 to FTDI
    - PS MIO[44:47]: I2C1, I2C0
    - PS MIO[48], PS LPD MIO[0:11, 24:25]: GEM0 RGMII Ethernet RJ-45
    - PS MIO[11,49] and LPD MIO[12,13,20,23]: power enables
    - PS MIO[50] and LPD MIO[18:19]: PCIe status
    - PS LPD MIO [21:22]: optional fan interface
    - LPD MIO[23]: VADJ_FMC power rail
- Security: PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, POR_B, boot mode DIP switch)
- Operational status LEDs (INIT, DONE, PS STATUS, PGOOD)
    - See Power and Status LEDs
- Power management
- System controller (XCZU4EG)

The VEK280 evaluation board provides a rapid prototyping platform using the XCVE2802-2MSEVSVH device. See the *Versal Architecture and Product Data Sheet: Overview* (DS950) for a feature set overview, description, and ordering information.

Board Specifications

Dimensions

PCB

Height: 7.517 inches (19.09 cm)
Length: 9.470 inches (24.05 cm)
Thickness: 64.5 mil ±5 mil (1.64 mm ±0.13 mm)

Evaluation Board

Thickness fully assembled: 1.976 inches (5.017 cm)
Fully assembled, from table to bottom of PCB: 0.673 inches (1.710 cm)

Note: A 3D model of this board is not available.

See the VEK280 Evaluation Kit website for the XDC listing and board schematics.

Environmental

Note: The operating temperature range is not fully tested across the specified temperature range. It is for general guidelines only. Customers should use the VEK280 evaluation board for evaluation purposes only in a normal lab environment and should not operate beyond room temperature.

Temperature

Operating: 0°C to +45°C
Storage: –25°C to +60°C

Humidity

5% to 95% non-condensing

Operating Voltage

+12 V_{DC}

Mechanical

The VEK280 evaluation board includes a mechanical stiffener to help ensure success with the board under normal lab conditions and use. While it is

recommended to not remove this stiffener, it is understood that it might be necessary to remove it for continued evaluation.
The mechanical stiffener screw torque is 4.5 in-lbs. When attaching or removing the mechanical stiffener, ensure proper ESD precautions are taken. See Standard ESD Measures for suggestions on best practices.

- Removing the Stiffener
  With power and other cabling unplugged, carefully unscrew the eleven 4-40 screws in any order. Care needs to be taken with the cooling solution as the board is manipulated due to potential excessive forces.
- Attaching the Stiffener
  With power and other cabling unplugged, carefully align the PCBA standoff holes to the sheet metal tray (stiffener) standoffs. Next, it is suggested to insert two screws in opposite corners of the board/tray combination. Loosely tighten the screws to aid in alignment. Add the remaining nine screws and loosely tighten. Finally, in a left to right or right to left pattern, tighten all eleven screws to 4.5 in-lbs.

Note: The tray will only fit one direction with the transceiver connectors having cutouts below. See Board Component Descriptions for more information.

Board Setup and Configuration

Standard ESD Measures

⚠ CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

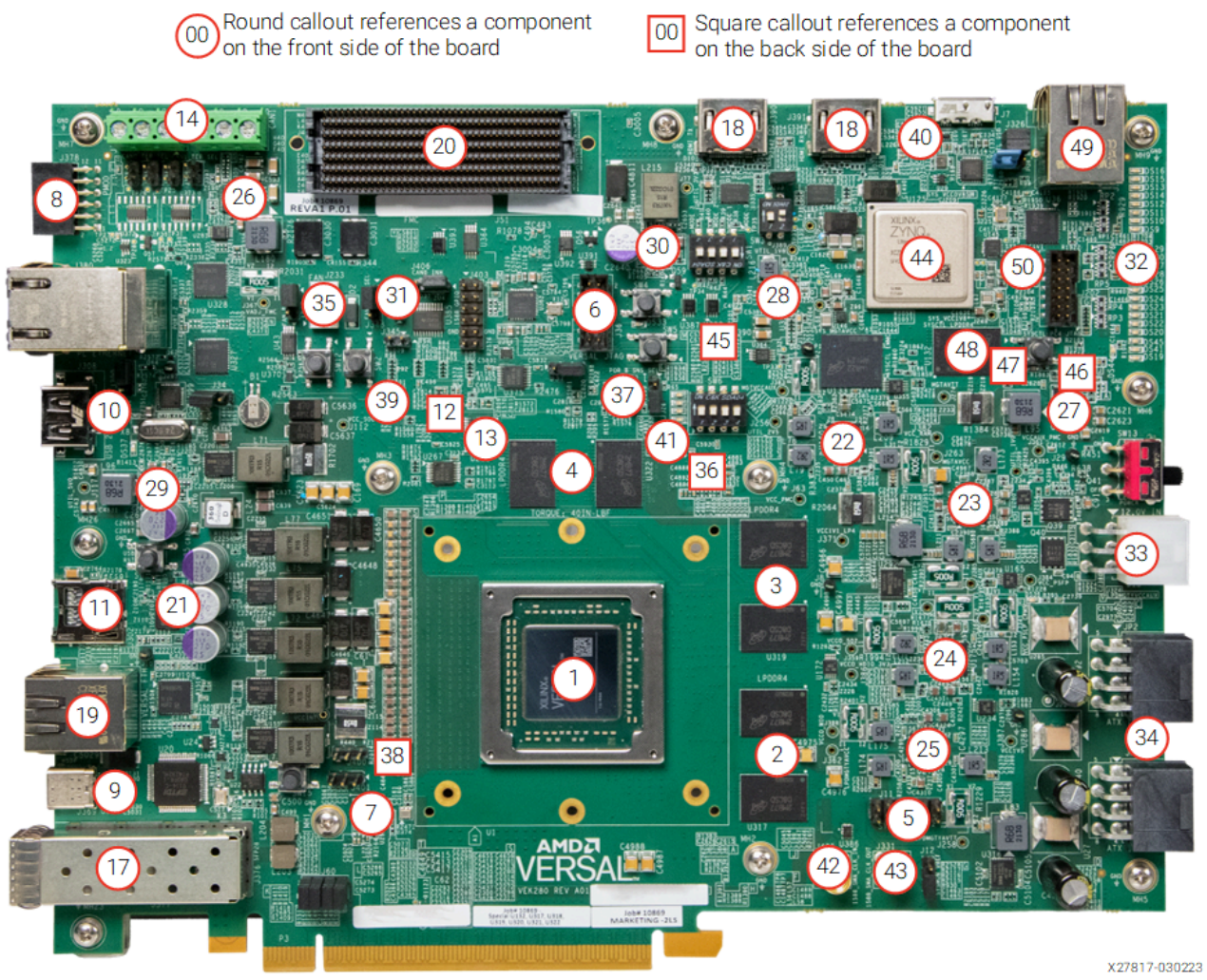
Board Component Location

The following figure shows the VEK280 board component locations. Each numbered component shown in the figure is keyed to the table in Board Component Descriptions.

!! Important: The following figure is for visual reference only and might not reflect the current revision of the board.

!! Important: There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VEK280 version of interest for such details.

Figure: Evaluation Board Component Locations



Board Component Descriptions

The following table identifies the components and references the respective schematic (038-05127-01) page numbers.

⚠ CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into the VEK280 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VEK280 board and voids the board warranty.

Table: Board Component Locations

Callout	Ref. Des.	Feature	Notes	Schematic Page
1	U1	AMD Versal™ adaptive SoC	XCVE2802-2MSELSVC4072 The heatsink[1] is not shown in Figure 1	3-16
2	U317, U318	LPDDR4 16 GBIT comp. memory	Micron MT53E512M32D1ZW-046	3,22,23

Callout	Ref. Des.	Feature	Notes	Schematic Page
		(B700-B702 IF)	IC SDRAM LPDDR4 512Mx32 2133 MHz	
3	U319, U320	LPDDR4 16 GBIT comp. memory (B703-B705 IF)	Micron MT53E512M32D1ZW-046 IC SDRAM LPDDR4 512Mx32 2133 MHz	4,24,25
4	U321, U322	LPDDR4 16 GBIT comp. memory (B706-B708 IF)	Micron MT53E512M32D1ZW-046 IC SDRAM LPDDR4 512Mx32 2133 MHz	5,26,27
5	J11	SYSMON header	Sullins PBC06DAAN Conn. hdr. vert. 12 pos. 2x6 2.54 mm pitch	10
6	J36	Adaptive SoC JTAG 2 mm 2x7 flat-cable connector	Molex 0878321420 Conn. hdr. male vert. 14 pos 2x7 2 mm	20
7	U298	PCIe® clock buffer	Renesas RC19004AGNL	49
8	J378	PMOD 2x6 connector	Sullins PPPC062LJBN-RC Conn Hdr Female RA 12 Pos 2x6 2.54 mm P TH	48
9	J369, U20	USB-UART bridge, USB Type-C connector (USB2.0)	Amphenol 12401598E4#2A FTDI FT4232HL-REEL	21
10	J308, U99	USB 2.0 type-A connector, USB ULPI transceiver	Wurth 629104190121, USB 2.0 type-A Microchip USB3320C USB 2.0 Xcvr	37
11	J302, U104	SD card socket, Versal adaptive	Molex 5025700893 Micro SD card cage	35

Callout	Ref. Des.	Feature	Notes	Schematic Page
		SoC SD 3.0 level translator circuit		
12	U33	I2C bus switches	Texas Instruments TCA9548APWR IC switch bus 1-In 8-Outs I2C 400 kHz Bottom of board	39
13	U233	I2C bus expander	Texas Instruments TCA6416APWR IC exp. GPIO 16-bit I2C 400 kHz Bottom of board	39
14	J392, J393	CAN bus connectors	Phoenix 1935174 Conn Term Blk RA 3 Pos 1x3 5 mm P 17.5A 250V Green TH 14-26AWG Screw Clamp	41
17	J376	zSFP+ connector	Molex 1703820001 zSFP+ connector and cage	29
18	J390, J391	HDMI™ TX and HDMI RX connectors	Molex 2086581061 Conn Rcpt HDMI 2.1 RA	44-45
19	J307	GEM0 SGMII Ethernet PHY, 0x01, RJ45 w/mag	Halo HFJ11-1G01E-L12RL RJ-45 Gigabit connector	36
20	J51	FMCP1	Samtec ASP-184329-01 560 pos. connector 14x40 1.27 mm	30-34
21	Various	Adaptive SoC power management	Infineon regulators	51-56

Callout	Ref. Des.	Feature	Notes	Schematic Page
		system (VCCINT, VCC_SOC)		
22	U160	VCC_PMC/UTIL_2V5/VCC_PAMC/UTIL_3V3 regulator	Infineon IR38064MTRPBF IC PMU 5-Ch step-down DC/DC	57
23	U167, U316	LPDMGTYAVTT/VCCAUX_PMC/LPDMGTYAVCCAUX/UTIL_3V3 regulator	Infineon IR38064MTRPBF IC PMU 5-Ch step-down DC/DC	58-59
24	U175	VCCO_HDIO_3V3/VCC_PSLP_PMC/LPDMGTYVCCAUX regulator	Infineon IR38064MTRPBF IC PMU 5-Ch step-down DC/DC	60
25	U279, U292	VCC1V1_LP4/VCC1V5_LPDMGTRAVCC/VCCO_HDIO regulator	Infineon IR38064MTRPBF IC PMU 5-Ch step-down DC/DC	61-62
26	U282	VADJ_FMC regulator	Infineon IR38060MTRPBF IC V. reg. step-down DC/DC sync	66
27	U295	MGTAVTT regulator	Infineon IR38164MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	67
28	U354	UTIL_1V8 regulator	Infineon IR38060MTRPBF IC REG BUCK ADJ 6A	68
29	U191	UTIL_3V3 regulator	Infineon IR3889MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	69
30	U190	UTIL_5V0 regulator	Infineon IR3889MTRPBFAUMA1 IC V. reg. step-down DC/DC sync	70

Callout	Ref. Des.	Feature	Notes	Schematic Page
31	J325	PMBus 3-pin header	Sullins PBC03SAAN Conn. hdr. vert. 3 pos. 1x3 2.54 mm	55
32	Various	Power good LEDs (see Power and Status LEDs for more details)	Various; see the Bill of Materials	72
33	J16	Power connector, 2x3, for AC-DC power adapter	Molex 0039301060 Conn. ddr. RA 6 pos. 2x3 4.2 mm	50
34	JP1, JP2	Power connector, 2x4, for ATX PCIe power	Astron 6652208-T0003T-H Conn. hdr. male RA 8 pos. 2x4 4.2 mm	50
35	J233	Fan header (keyed 4-pin)	Molex 0470533000 Keyed fan header 4 pos. 0.100" vert.	50
36	U299	MGT and system clock generators	Renesas RC21008A065GND#BB0	93
37	J374	RC21008A_GTCLK header	Molex 0878321820	93
38	U297	Adaptive SoC U1 OSPI	Micron MT35XU02GCBA1G12-0SIT IC flash Xccela 2 Gb SPI 200 MHz 1.8V	28
39	DS1	Done LED (Active-High-Z and pulled High)	Lumex SML-LX0603GW-TR LED green	12
40	DS2	Error out LED (Active-High-Z and pulled High)	Lumex SML-LX0603IW-TR LED red	12

Callout Ref. Des.	Feature	Notes	Schematic Page
41	DS3, DS4, DS5, DS6	User LEDS	Lumex SML-LX0603GW-TR LED green	48
42	J405	IEEE-1588 eCPRI CLK in SMA	Rosenberger 32K10K-400L5 Conn. rcpt. SMA vert. 50R 12.4 GHz	92
43	J331	IEEE-1588 eCPRI CLK out SMA	Rosenberger 32K10K-400L5 Conn. rcpt. SMA vert. 50R 12.4 GHz	92
44	U125	XCZU4EG system controller	AMD XCZU4EG-2SFVC784E AMD Zynq™ UltraScale+™ MPSoC	73-83
45	U301	SYSCTLR clock156.25 MHz HSDP REFCLK	CTS 626L15625I3T Osc 156.25 MHz 3.3V 25 PPM LVDS with OE	89
46	U302	SYSCTLR clock 33.33 MHz REFCLK	Renesas XUJ716033.333333I Osc 33.333333 MHz 1.8V 25 PPM LVCMOS with OE	89
47	U304	SYSCTLR clock 26 MHz USB REFCLK	Raltron XCO583IV11-26.000 Osc 26 MHz 3.3V 30 PPM LVDS with OE	89
48	U132	System controller LPDDR4 16 GBIT comp. memory	Micron MT53E512M32D1ZW-046 WT:D IC SDRAM LPDDR4 16 Gb 512Mx32 2133 MHz	86

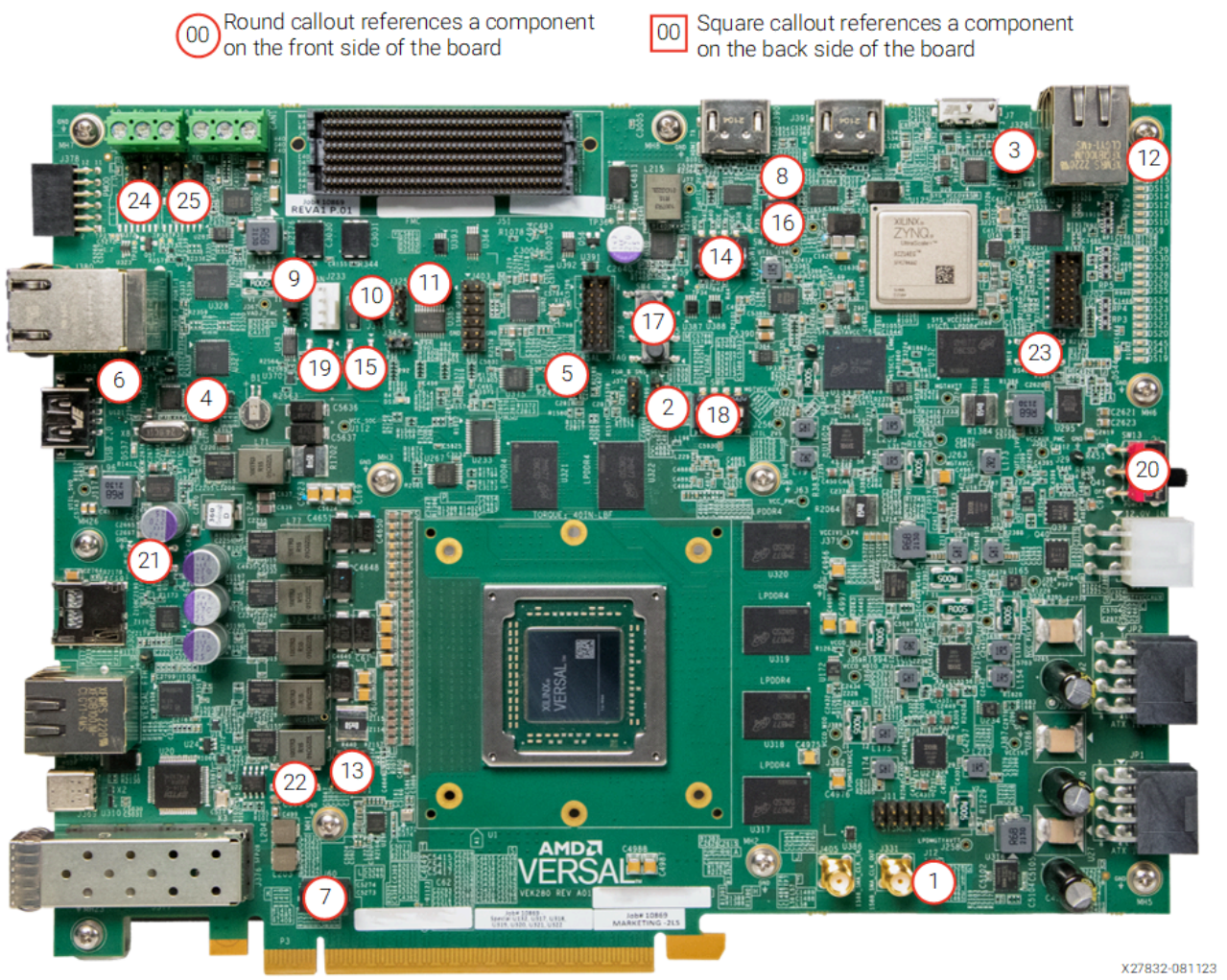
Callout	Ref. Des.	Feature	Notes	Schematic Page
49	J349	System controller SGMII Ethernet, RJ45 w/magnetics	Halo HFJ11-1G01E-L12RL RJ-45 Gigabit connector	84
50	DS34	System controller done LED (active-High)	Lumex SML-LX0603GW-TR LED green	77

1. The VEK280 evaluation board includes a heatsink with a thermal resistance of 0.46°C/W.

Default Jumper and Switch Settings

The following figure shows the VEK280 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section. Both tables reference the respective schematic page numbers.

Figure: Board Jumper Header and Switch Locations



Jumpers

The following table lists the default jumper settings.

Table: Default Jumper Settings

Callout Number	Ref Des.	Function	Default	Schematic Page
1	J12	SYSMON VREFP SEL 1-2: External VREF 2-3: Disable external VREF	1-2	10
2	J26	POR_B supervisor SENSE input 1-2: VCCO_MIO ramp-up sense (1.8V) 2-3: VCCAUX_PMC ramp-up sense (1.5V)	2-3	13
3	J326	POR_B enable header 1-2: SYSCTLR can drive POR_B	1-2, 3-4 jumpered	13

Callout Number	Ref Des.	Function	Default	Schematic Page
		3-4: PC4 can drive POR_B 5-6: FTDI can drive POR_B Open: POR_B source not connected	5-6 open	
4	J34	VCC Fuse programming enable 1-2: Fuse programming enabled 2-3: Fuse programming disabled	2-3	15
5	J37	JTAG source enable 1-2: JTAG sources disabled 2-3: JTAG sources enabled	2-3	20
6	J300	USB shield GND 1-2: USB connector DC grounded 2-3: USB connector no DC grounded	1-2	37
7	J60	PCIe PRSNT_B WIDTH SEL 1-2: x1 3-4: x4 5-6: x8 7-8: x16	1-2, 3-4, 5-6, 7-8	40
8	J203	SYSCTLR POR_B supervisor enable 1-2: SYSCTLR POR_B supervisor enabled Open: SYSCTLR POR_B supervisor disabled	1-2	77
9	J347	Fan type 1-2: System controller PWM 2-3: Versal device MIO PWM	1-2	50
10	J348	TACH type 1-2: System controller TACH 2-3: Versal device MIO TACH	1-2	50
11	J406	MIO37 selection 1-2: ZU4_TRIGGER 2-3: CANFD0_INH_B	1-2	10

Callout Number	Ref. Des.	Function	Default	Schematic Page
12	J407	SYSCTLR JTAG mode Default: QSPI32 Installed: JTAG	DNP	77
13	J400, J401	SFP RS0/1 input 1-2: Full BW RX 2-3: Low BW Rx	Open	29
24	J395, J396	CAN0 termination option	Installed	41
25	J398, J397	CAN1 termination option	Installed	41

Switches

The following table lists the default switch settings.

Table: Default Switch Settings

Callout Number	Ref. Des.	Function	Default	Schematic Page
14	SW1	U1 mode 4-pole DIP switch Switch OFF = 1 = high; ON = 0 = low Mode = SW1[1:4] = Mode[0:3] SD = ON,OFF,OFF,OFF = 0111 OSPI = ON,ON,ON,OFF = 0001 JTAG = ON,ON,ON,ON = 0000	ON, ON, ON, ON	12
15	SW2	VEK280 power-on reset (POR_B)	Open	13
16	SW3	SYSCTLR JTAG source selection Switch OFF = 1 = high; ON = 0 = low SYSCTLR JTAG SOURCE SEL = SW3[1:2] = SEL[0:1] PL JTAG = ON,ON = 00 FTDI JTAG = OFF,ON = 10	OFF, ON	20

Callout Number	Ref Des.	Function	Default	Schematic Page
17	SW4, SW5	User pushbutton inputs **Note:** Pushbutton switch default = open = logic low (not pressed).	Open	48
18	SW6	User GPIO DIP Switch OFF = 0 = low; ON = 1 = high	OFF, OFF, OFF, OFF	48
19	SW12	System controller power-on reset (SYSCTL_POR_B)	Open	77
20	SW13	Main power	OFF	50
21	SW14	User USB reset	Open	37
22	SW15	User GEM reset	Open	36
23	SW16	System controller FWUEN pushbutton (SYSCTLR_MIO12_FWUEN_C2M_B) See BEAM wiki for more information	Open	76

Versal Device Configuration

The “Platform Boot, Control, and Status” section of the *Versal Adaptive SoC Technical Reference Manual* (AM011) describes the Versal XCVE2802 device boot process. The VEK280 board supports a subset of the modes documented in the technical reference manual via onboard boot options. The mode DIP switch SW1 configuration option settings are listed in the following table.

Table: Mode Switch SW1 Configuration Option Settings

Boot Mode	Mode Pins [0:3] [2]	Mode SW1 [1:4] [2]
JTAG	`0000` [1,3]	ON, ON, ON, ON
OSPI	`0001`	ON, ON, ON, OFF

Boot Mode	Mode Pins [0:3] [2]	Mode SW1 [1:4] [2]
SD1 (SD 3.0)	0111	ON, OFF, OFF, OFF

1. Default switch setting.
2. Mode DIP SW1 poles [1:4] correspond to U1 XCVE2802 MODE[0:3].
3. Mode DIP SW1 individual switches ON=LOW (p/d to GND)=0, OFF=HIGH (p/u to VCCO)=1.

JTAG

The AMD Vivado™ , AMD SDK, or third-party tools can establish a JTAG connection to the Versal device in the two ways described in this section.

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 2.0 type-C connector (J369), which requires:
  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
  - On the 3-pin JTAG MUX, enable header J37 to enable the JTAG MUX. Move the 2-pin jumper to be installed on pins 2-3. See Default Jumper and Switch Settings for defaults and Board Component Location for location.
  - Set 2-pole DIP SW3[1:2] set to 10 (OFF, ON) for JTAG MUX channel 2 FT4232 U20 bridge.
  - Power-cycle the VEK280 evaluation board or press the power-on reset (POR) pushbutton (SW2). SW2 is near the USB-C JTAG port J369 in the figure in Board Component Location).

- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed), which requires:

  Note: In this mode, the FT4232 device (U20) UART functionality continues to be available.

  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
  - On the 3-pin JTAG MUX, enable header J37 to inhibit the JTAG MUX. Move the 2-pin jumper to be installed on pins 1-2 for high-z mode. See Default Jumper and Switch Settings for defaults and Board Component Location for location.
  - 2-pole DIP SW3[1:2] setting does not matter as the MUX is inhibited/turned off.
  - Power-cycle the VEK280 board or press the power-on reset pushbutton (SW2). SW2 is near the USB-C JTAG port J369 in the figure in Board Component Location).

OSPI

This boot mode is supported onboard and is wired to the XCVE2802 U1 bank 500 PMC_MIO[0:12] pins. The octal SPI controller can access two devices using several different methods. See the Flash Memory Controllers section of the *Versal Adaptive SoC Technical Reference Manual* (AM011) for more information. To boot from OSPI:

1. Store a valid XCVE2802 adaptive SoC boot image file in the OSPI.
2. Set boot mode SW1 for OSPI as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
3. Power-cycle the VEK280 board or press the POR pushbutton SW2. SW2 is near the USB-C JTAG port J369 in the figure in Board Component Location.

SD1_3.0

To boot from a SD card installed in microSD card socket J302:

1. Store a valid XCVE2802 device boot image file on a microSD card. Plug the SD card into the VEK280 evaluation board SD socket J302 connected to the XCVE2802 U1 bank 501 MIO SD interface.
2. Set boot MODE SW1 for SD1_3.0 as indicated in the table in Versal Device Configuration.
3. Power-cycle the VEK280 board or press the POR pushbutton SW2. SW2 is near the USB-C JTAG port J369 in the figure in Board Component Location.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. The "Board Component Locations" table in Board Component Descriptions identifies the components and references the respective schematic page numbers. Component locations are shown in the "Evaluation Board Component Locations" figure in Board Component Location.

Component Descriptions

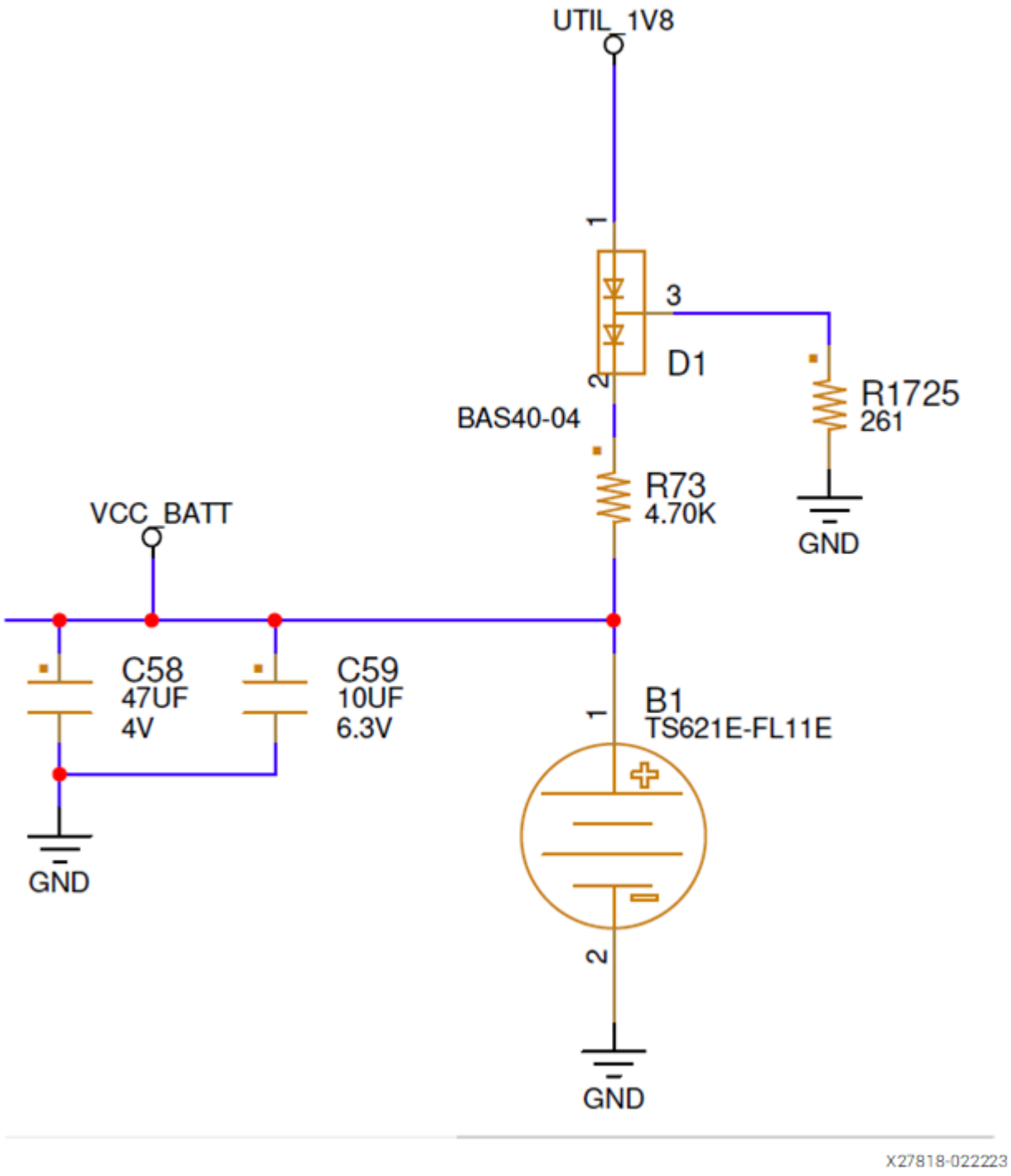
Versal Device

[Figure 1, callout 1]
The VEK280 evaluation board is populated with the AMD Versal™ XCVE2802-2MSEVSVH2802 device, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Versal device features the Arm® flagship Cortex®-A72 64-bit dual-core processor and Cortex-R5F dual-core real-time processor. For additional information on the Versal XCVE2802-2MSEVSVH2802 device, see the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959). See the *Versal Adaptive SoC Technical Reference Manual* (AM011) for more information about Versal device configuration options.

Encryption Key Battery Backup Circuit

The XCVE2802 device U1 implements bitstream encryption key technology. The VEK280 board provides the encryption key backup battery circuit shown in the following figure.

Figure: Encryption Key Backup Circuit



The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVE2802 device U1 VCC_BATT bank pin AN20. The battery supply current IBATT specification is 150 nA maximum when board power is off. Battery B1 is charged from the VCC1V8 1.8V rail through a 2 series diode with the first forward drop to yield between 0.24V to 0.46V over temperature per fixed 5 mA load, R1725, and limiting 1.56V max at the device pin, PSVBATT. The second diode and 4.7 kΩ current limit resistor allows the battery to trickle charge and prevent battery B1 from back powering R1725.

I/O Voltage Rails

The XCVE2802 device PL I/O bank voltages on the VEK280 board are listed in the following table.

Important: See LPD MIO[23]: VADJ_FMC Power Rail for more details on the VADJ_FMC power rail.

Note: See the *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959) for more information. See the *Versal Adaptive SoC Technical Reference Manual* (AM011) for more information about Versal device configuration options.

Table: I/O Voltage Rails

Versal Device (U1)	Power Supply Rail Name	Voltage	Description
XPIO Bank 700	VCC1V1_LP4	1.1V	LPDDR4 TRIP1 CH0
XPIO Bank 701	VCC1V1_LP4	1.1V	LPDDR4 TRIP1 CH1
XPIO Bank 702	VCC1V5_LP4	1.5V	LPDDR4 TRIP1 CH0/1 reset, HDMI control signals, GPIO LEDs
XPIO Bank 703	VCC1V1_LP4	1.1V	LPDDR4 TRIP2 CH0
XPIO Bank 704	VCC1V1_LP4	1.1V	LPDDR4 TRIP2 CH1
XPIO Bank 705	VADJ_FMC [1]	1.5V	LPDDR4 TRIP2 CH0/1 reset, HDMI control signals, GPIO DIP,PB0/1, SYSCTLR GPIO[0:7], SYS_CLK_1, FMCP1_LA[00:01]_CC, FMCP1_LA[02:16],FMCP_CLK0
XPIO Bank 706	VADJ_FMC [1]	1.5V	FMCP1_SYNC_M2C/C2M, LPDDR4 TRIP3 CH0/1 reset, SYS_CLK_2, 1588_GPIO[0:5], FMCP1_REFCLK_C2M, FMCP1_LA[17:18]_CC,

Versal Device (U1) Bank	Power Supply Rail Net Name	Voltage	Description
			FMCP1_LA[19:33], FMCP1_CLK1_M2C
XPIO Bank 707	VCC1V1_LP4	1.1V	LPDDR4 TRIP3 CH1
XPIO Bank 708	VCC1V1_LP4	1.1V	LPDDR4 TRIP3 CH0
XPIO Bank 400	VCCO_HDIO_3V3	3.3V (default)	PL_GEM0 MDIO/MDC, PMOD_IO[0:7], PL_GEM0_RX/TX
XPIO Bank 401	VCCO_HDIO_3V3	3.3V (default)	PL_GEM1_MDIO/MDC, PL_GEM[0:1]_RST, SFP_TX_FAULT, SFP_RX_LOS, UART1_TXD/RXD, SYSCTLR_UART0, PL_GEM1_RX/TX
PMC MIO 500	VCCO_MIO	1.8V	SYSMON, USB ULPI 2.0 interface, OSPI interface
PMC MIO 501	VCCO_MIO	1.8V	SD bus power, PCIe controls, I2C0/21, UART0, CAN0_nSTB, System Controller I2C/[trigger OR CANFD0_INH], SD card controls, GEM reset
LPD MIO 502	VCCO_502	1.8V	GEM interface/controls, power enables, PCIe PERST, fan tach, fan PWM

1. The VEK280 board is shipped with VADJ_FMC set to 1.5V. This value cannot be changed. Care must be taken when using FMC accessories.

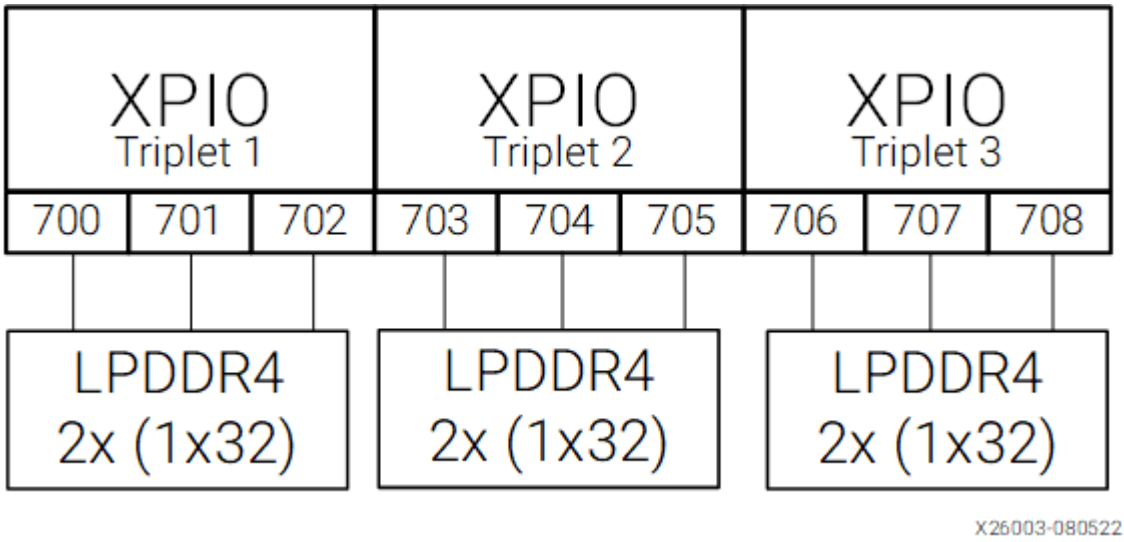
See LPD MIO[23]: VADJ_FMC Power Rail for more details.

LPDDR4 Component Memory

[Figure 1, callout 2, 3, 4]
The VEK280 XCVE2802 device PL DDR memory interface performance is documented in the *Versal Premium Series Data Sheet: DC and AC Switching*

Characteristics (DS959). The VEK280 board LPDDR4 component memory interfaces adhere to the constraints guidelines documented in the "PCB guidelines for Memory Interfaces" section of the *Versal Adaptive SoC PCB Design User Guide* (UG863). The VEK280 DDR4 component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Versal Adaptive SoC Memory Resources Architecture Manual* (AM007). For more memory component details, see the Micron MT53E512M32D1ZW data sheet on the Micron website. For the most current part number, see the Bill of Materials (BOM) located on the VEK280 Evaluation Board website. The detailed device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.
The VEK280 evaluation board hosts three LPDDR4 memory systems, each with a component configuration of 2x (1x32-bit component).

Figure: LPDDR4 Component Memory



XCVE2802 U1 has been configured with three triplet banks.

- XPIO triplet 1 (banks 700/701/702)
- XPIO triplet 2 (banks 703/704/705)
- XPIO triplet 3 (banks 706/707/708)

Each support two independent 32-bit 2 GB component interfaces (4 GB per triplet). The VEK280 evaluation board uses the LPDDR4 memory components as follows:

- Manufacturer: Micron
- Part number: MT53E512M32D1ZW-046 WT:B (dual die LPDDR4 SDRAM)
- Component description
  - 16 Gb (512 Mb x 32)
  - 1.1V 200-ball TFBGA
  - LPDDR4-2133

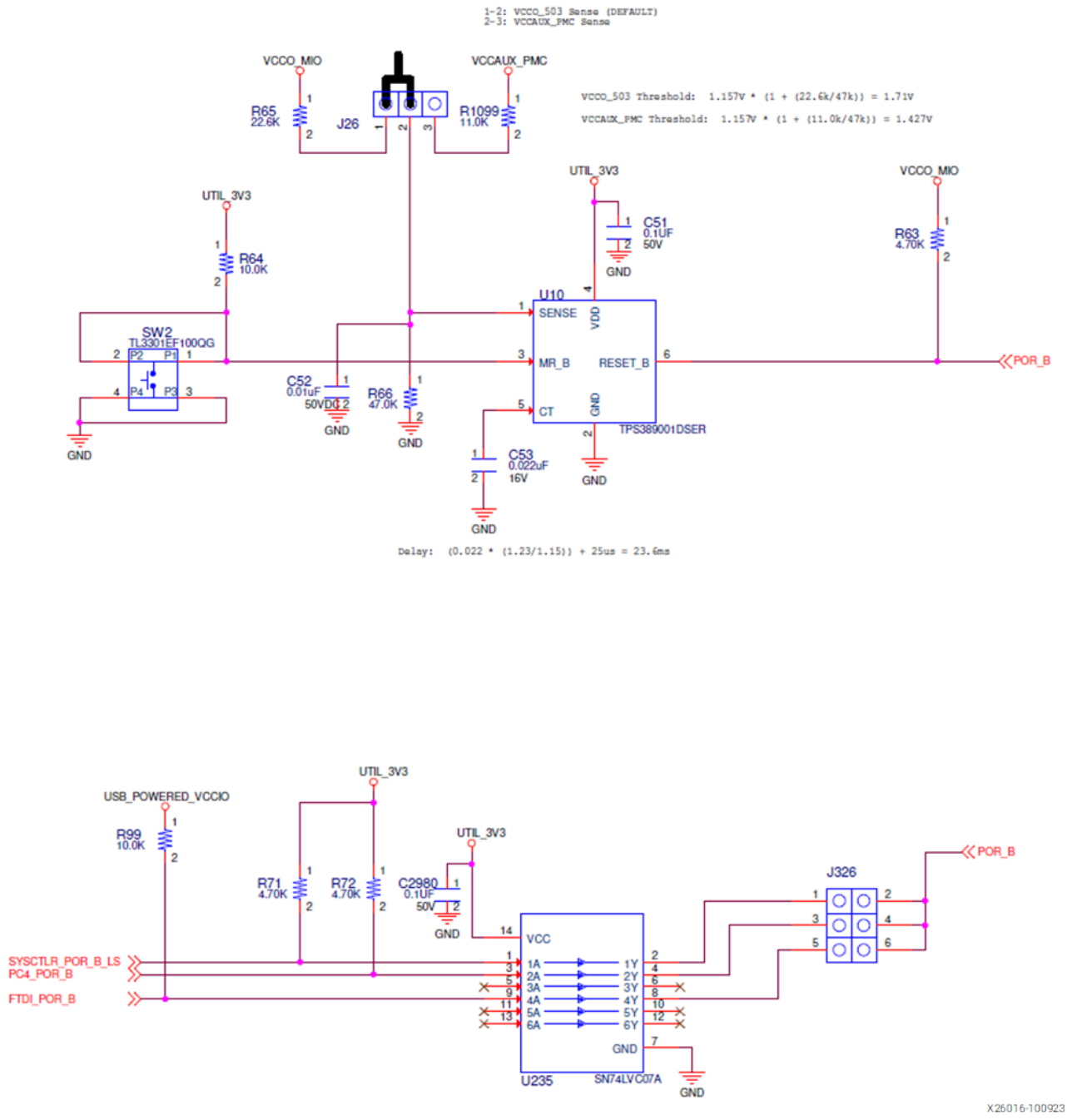
System Reset POR_B

[Figure 1, callout 2]
POR_B is the Versal device processor reset, which can be controlled by:

- SYSCTLR (U125)
- PC4 header (J36)
- FTDI USB JTAG chip (U20)

The VEK280 board POR circuit is shown in the following figure. U235 allows directional open drain level shifting for all of these masters, and J326 allows them to be bused together if desired. The TPS389001 U10 supervisor chip holds POR_B off until power is valid.

Figure: POR_B Reset Circuit



PMC and LPD MIO

The following sections provide the MIO peripheral mapping implemented on the VEK280 evaluation board. See the *Versal Adaptive SoC Technical Reference Manual* (AM011) for more information on MIO peripheral mapping. Additional signal connectivity can be located in the following schematic sections:

- Bank 500: See schematic page 10
- Bank 501: See schematic page 10
- Bank 502: See schematic page 11

The following table provides MIO peripheral mapping implemented on the VEK280 evaluation board. The Versal device bank 500, 501, and 502 mappings are listed in the following table.

Table: MIO Peripheral Mapping

Bank	MIO #	Device	Signal	I/O	Notes
500	0	OSPI	PMC_MIO0_OSPI_CLK	O	
	1		PMC_MIO1_OSPI_DQ0	I/O	
	2		PMC_MIO2_OSPI_DQ1	I/O	
	3		PMC_MIO3_OSPI_DQ2	I/O	
	4		PMC_MIO4_OSPI_DQ3	I/O	
	5		PMC_MIO5_OSPI_DQ4	I/O	
	6		PMC_MIO6_OSPI_DQS	I/O	
	7		PMC_MIO7_OSPI_DQ5	I/O	
	8		PMC_MIO8_OSPI_DQ6	I/O	
	9		PMC_MIO9_OSPI_DQ7	I/O	
	10		PMC_MIO10_OSPI0_CS_B	O	
	11	Regulator Enable GPIO	PMC_MIO11_VCC_AUX_1V2_EN	O	See Table 1
	12	OSPI	PMC_MIO12_OSPI_RST_B	O	
	13	USB	PMC_MIO13_USB_RST_B	O	
	14		PMC_MIO14_USB_DAT0	I/O	
	15		PMC_MIO15_USB_DAT1	I/O	
	16		PMC_MIO16_USB_DAT2	I/O	
	17		PMC_MIO17_USB_DAT3	I/O	

Bank	MIO #	Device	Signal	I/O	Notes
	18		PMC_MIO18_USB_CLKOUT	O	
	19		PMC_MIO19_USB_DAT4	I/O	
	20		PMC_MIO20_USB_DAT5	I/O	
	21		PMC_MIO21_USB_DAT6	I/O	
	22		PMC_MIO22_USB_DAT7	I/O	
	23		PMC_MIO23_USB_DIR	I/O	
	24		PMC_MIO24_USB_STP	O	
	25		PMC_MIO25_USB_NXT	I/O	
501	26	SD	PMC_MIO26_SD_CLK	O	
	27		PMC_MIO27_SD_DIR1	O	
	28		PMC_MIO28_SD_DET	I	
	29		PMC_MIO29_SD_CMD	I/O	
	30		PMC_MIO30_SD_DAT0	I/O	
	31		PMC_MIO31_SD_DAT1	I/O	
	32		PMC_MIO32_SD_DAT2	I/O	
	33		PMC_MIO33_SD_DAT3	I/O	
	34		PMC_MIO34_SD_SEL	I/O	
	35		PMC_MIO35_SD_DIR_CMD	O	
	36		PMC_MIO36_SD_DIR0	O	
	37	Factory/CANFD0 See CAN Interface	PMC_MIO37_COMBINED	I/O	Selectable J406, Factory/CANFD0_INH_B
	38	CANFD0	PMC_MIO38_CAN0_nSTB	O	Standby mode control input

Bank	MIO #	Device	Signal	I/O	Notes
		See CAN Interface			
	39	SYSMON I2C	PMC_MIO39_SYSMON_I2C_SCL	I/O	
	40		PMC_MIO40_SYSMON_I2C_SDA	I/O	
	41		PMC_MIO41_SYSMON_I2C_ALERT	I/O	
	42	UART	PMC_MIO42_501_RX_IN	I	
	43		PMC_MIO43_501_TX_OUT	O	
	44	I2C1	PMC_MIO44_501_LP_I2C1_SCL	I/O	
	45		PMC_MIO45_501_LP_I2C1_SDA	I/O	
	46	I2C0	PMC_MIO46_501_I2C0_SCL	I/O	
	47		PMC_MIO47_501_I2C0_SDA	I/O	
	48	GEM0	PMC_MIO48_GEM_RST_B	O	
	49	Regulator Enable GPIO	PMC_MIO49_VCC_PSLP_EN	O	See Table 1
	50	PCIe	PMC_MIO50_PCIE_WAKE_B	I	
	51	SD	PMC_MIO51_SD_BUSPWR	O	
502	0	GEM0	LPD_MIO0_GEM_TX_CLK	O	
	1		LPD_MIO1_GEM_TX_D0	I/O	
	2		LPD_MIO2_GEM_TX_D1	I/O	
	3		LPD_MIO3_GEM_TX_D2	I/O	
	4		LPD_MIO4_GEM_TX_D3	I/O	
	5		LPD_MIO5_GEM_TX_CTL	I/O	
	6		LPD_MIO6_GEM_RX_CLK	I	

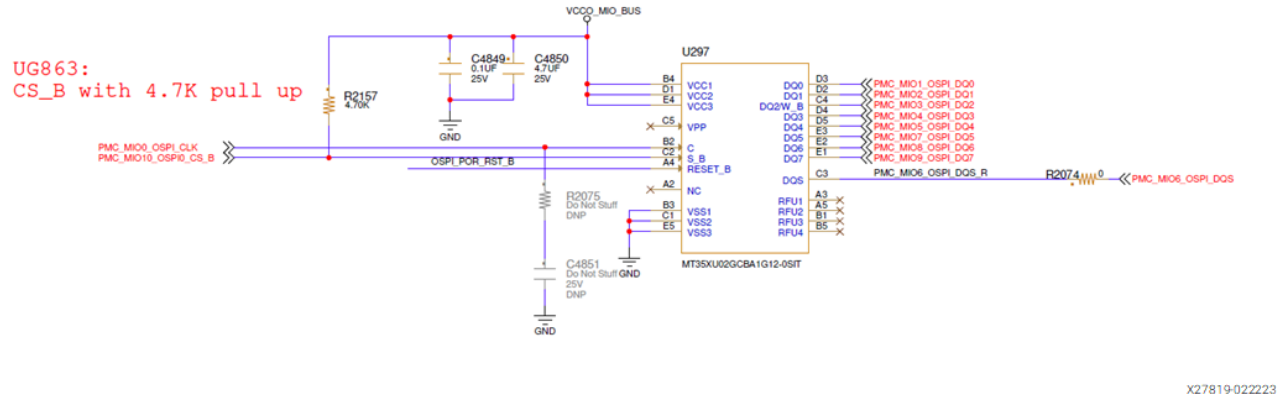
Bank	MIO #	Device	Signal	I/O	Notes
	7		LPD_MIO7_GEM_RX_D0	I/O	
	8		LPD_MIO8_GEM_RX_D1	I/O	
	9		LPD_MIO9_GEM_RX_D2	I/O	
	10		LPD_MIO10_GEM_RX_D3	I/O	
	11		LPD_MIO11_GEM_RX_CTL	I/O	
	12	Regulator Enable GPIO	LPD_MIO12_VCC_PSFP_EN	O	See Table 1
	13	Regulator Enable GPIO	LPD_MIO13_VCC_SOC_EN	O	See Table 1
	14	CANFD0 See CAN Interface	LPD_MIO14_CANFD0_RX	I	
	15		LPD_MIO15_CANFD0_TX	O	
	16	CANFD1 See CAN Interface	LPD_MIO16_CANFD1_TX	O	
	17		LPD_MIO17_CANFD1_RX	I	
	18	PCIe	PCIE_PERST_B	I	
	19		PCIE_PERST_B	I	
	20	Regulator Enable GPIO	LPD_MIO20_VCC_PL_EN	O	See Table 1
	21	Fan	MIO21_FAN_PWM_VERSAL	O	Versal device fan PWM
	22		MIO22_FAN_TACH_VERSAL	I	Versal device fan tach
	23	Regulator Enable	LPD_MIO23_VADJ_FMC_EN	O	VADJ_FMC enable

Bank	MIO #	Device	Signal	I/O	Notes
		GPIO			
	24	MDIO	LPD_MIO24_GEM_MDC	O	GEM MD clock
	25		LPD_MIO25_GEM_MDIO	I/O	GEM MD I/O

PMC MIO[0–10,12] Bank 500: OSPI U297

[Figure 1, callout 38]
The VEK280 evaluation board uses one Micron MT35XU02GCBA1G12-0SIT 8-bit serial peripheral interface (octal SPI) flash device. This 2 Gb NOR flash device can be used as onboard boot, as well as non-volatile storage memory. When used as a boot source, it is selectable from SW1. See Switches for more information.
See schematic page 28.

Figure: Dual Parallel OSPI Circuit



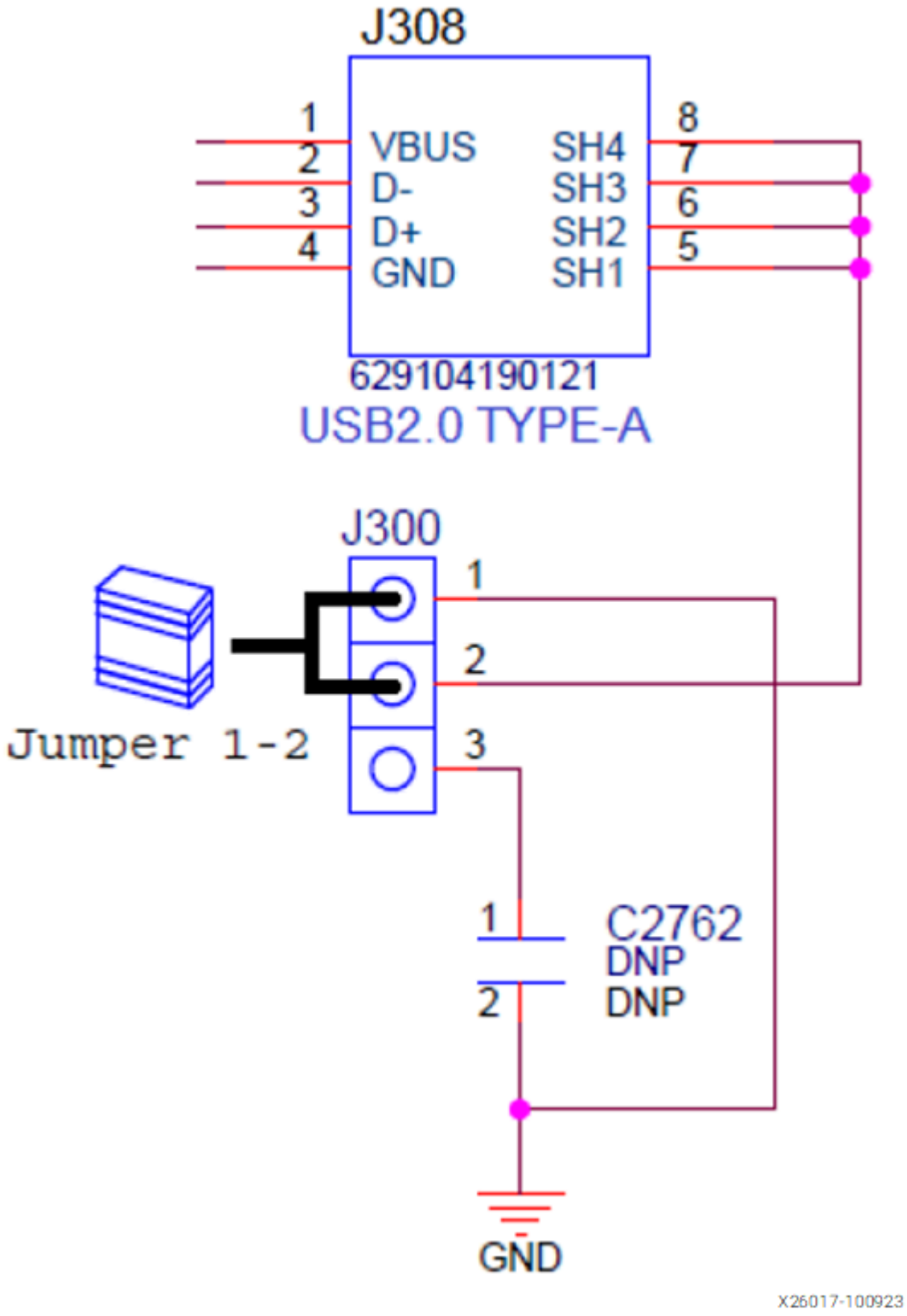
PMC MIO[13:25] Bank 500: USB 2.0 ULPI PHY

The VEK280 evaluation board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI transceiver (U99) to support a USB 2.0 type-A connector (J308). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB signaling. Using the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.
The USB3320 is clocked by a 24 MHz crystal (X8). See the Standard Microsystems Corporation (SMSC) USB3320 data sheet for clocking mode details. The interface to the USB3320 PHY is implemented through the IP in the XCVE2802 device PS.

The USB3320 ULPI transceiver circuit has a Micrel MIC2544 high-side programmable current limit switch (U100). This switch has an open-drain output fault flag on pin 2, which turns on red LED DS37 if over current or thermal shutdown conditions are detected.

Note: As shown in the following figure, the shield for the USB 2.0 type-A connector (J308) can be tied to GND by a jumper on header J300 pins 1-2 (see Default Jumper and Switch Settings). The USB shield can optionally be connected through a series capacitor to GND by installing a capacitor (body size 0402) at location C2762 and inserting a jumper across pins 2-3 on header J300.

Figure: USB3320 USB2.0 Connector J308 Shield Connection Options

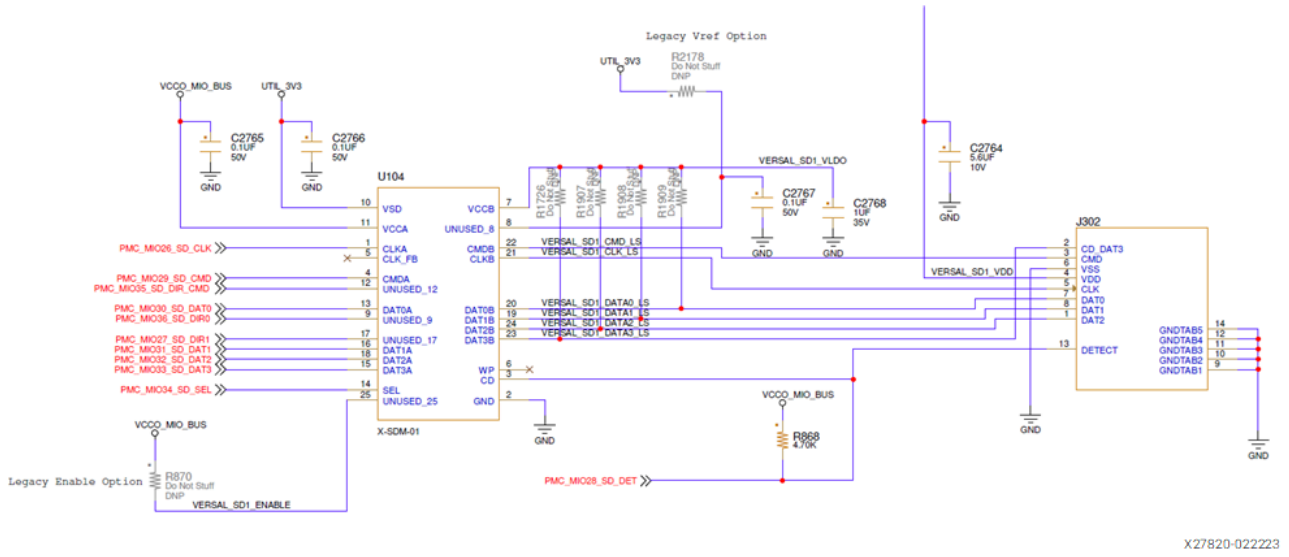


PMC MIO[26:36, 51] Bank 501: Secure Digital (SD) Card IF

[Figure 1, callout 11]
The VEK280 evaluation board includes a secure digital input/output (SDIO) interface to provide access to general purpose non-volatile SDIO memory cards and

peripherals. This interface is used for the SD boot mode and supports SD2.0 and SD3.0 access.
The SDIO interface signals PMC_MIO[26:36, 51] are connected to XCVE2802 device bank 501, which has its VCCO set to 1.8V. Six SD interface nets PMC_MIO[26, 29, 30:33] are passed through a NXP NVT4857UK SD 3.0-compliant voltage level-translator U104. This translator is present between the Versal device and the SD card connector (J302). The NXP NVT4857UK U104 device provides SD3.0 capability with SDR104 performance. The following figure shows the connections of the SD card interface on the VEK280 evaluation board.

Figure: SD Card Interface Connections



The following table lists the NVT4857UK U104 adapter pinout.

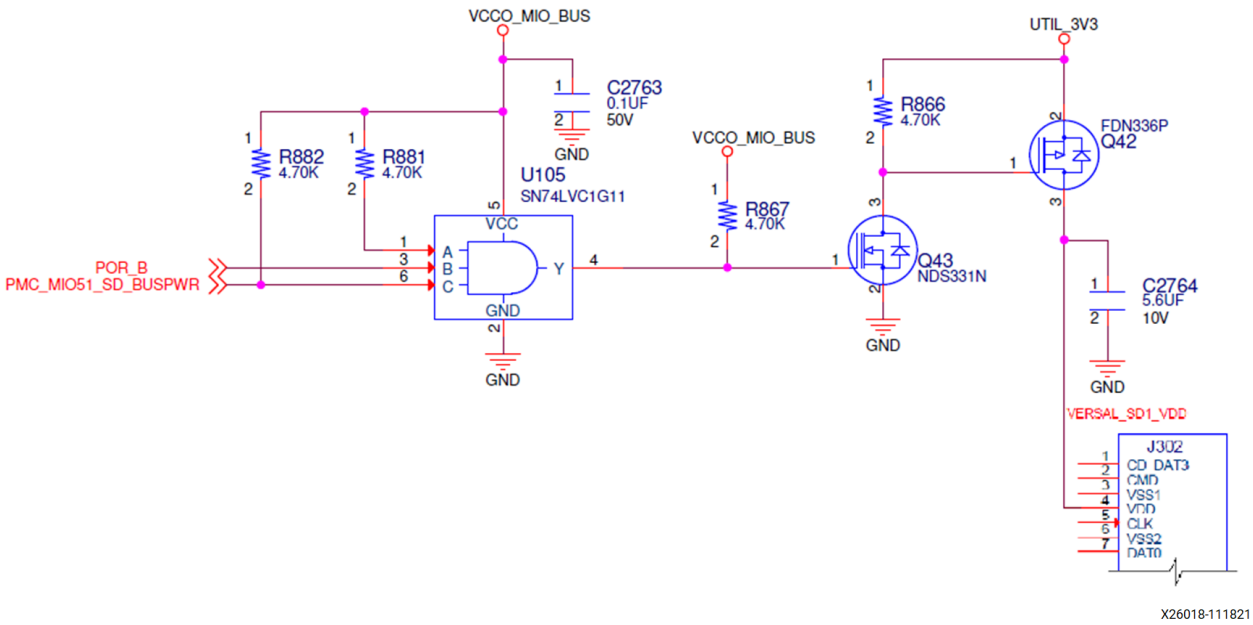
Table: NVT4857UK U104 Adapter Pinout

Aries Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
1	D2	CLKA
2	C3, C2	GND
3	B2	CD
4	C1	CMDA
5	E2	CLK_FB
6	Unused	Unused
7	B3	VCCB

Aries Adapter Pin Number	NVT4857UKAZ Pin Number	NVT4857UKAZ Pin Name
8	Unused	Unused
9	Unused	Unused
10	A3	VSD
11	A2	VCCA
12	Unused	Unused
13	D1	DATA0
14	E3	SEL
15	B1	DAT3A
16	E1	DAT1A
17	Unused	Unused
18	A1	DAT2A
19	E4	DAT1B
20	D4	DAT0B
21	D3	CLKB
22	C4	CMDB
23	B4	DAT3B
24	A4	DAT2B
25	Unused	Unused

The Versal device (U1) also has control over the power for the SDCARD, which allows the Versal device to remove power to the SD card as needed.

Figure: SD Socket J302 Power Control



Information for the SD I/O card specification can be found at the SanDisk Corporation or SD Association websites. The VEK280 SD card interface supports the SD1 (2.0) and SD2 (3.0) configuration boot modes documented in the *Versal Adaptive SoC Technical Reference Manual* (AM011). See schematic page 35 for more details.

For NVP NVT4857UK component details, see the NVT4857UK data sheet on the NXP website.

The detailed Versal device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.

PS MIO[37] Selectable

The Versal device PS bank 501 MIO37 is jumper selectable as factory reserved [1:2] or as CANFD0_INH_B [2:3]. The default is [1:2].

PS MIO[38] CAN0 Standby Mode

The Versal device PS bank 501 MIO38 controls the CAN0 standby mode. This control is an output from the Versal device and an input to the CAN transceiver.

PMC MIO[39:41] System Monitor I2C

The Versal device PS bank 501 MIO39 (PMC_MIO39_SYSMON_I2C_SCL), MIO40 (PMC_MIO40_SYSMON_I2C_SDA), and MIO41 (PMC_MIO41_SYSMON_I2C_ALERT) are connected to the system controller for use with the system controller related applications and alerts.

PMC MIO[42:43] UART0

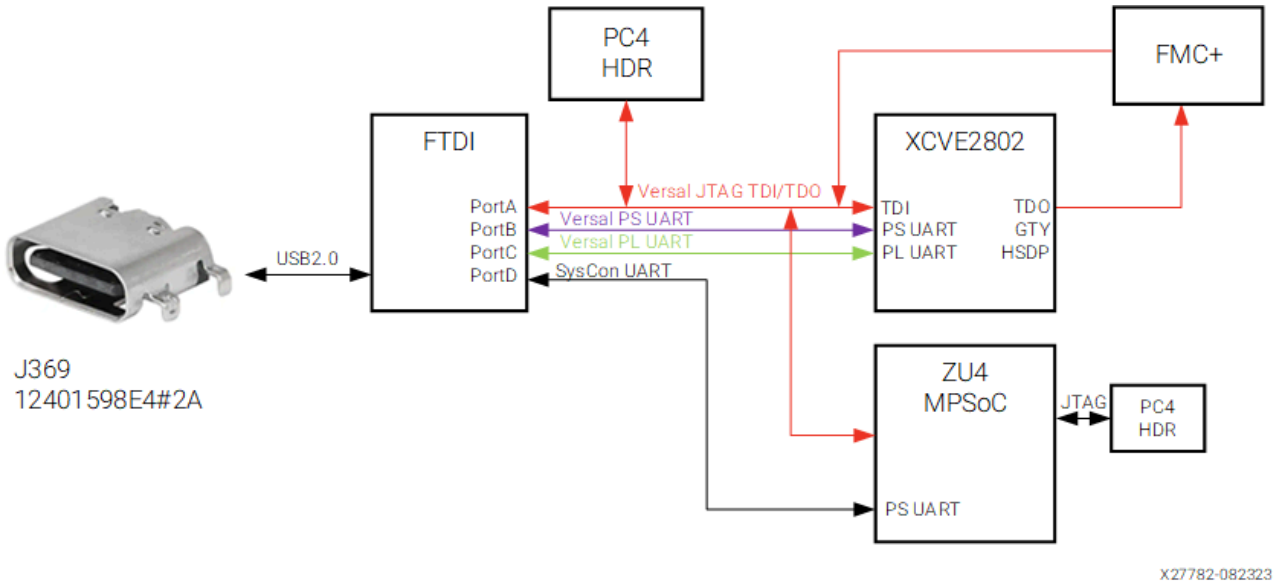
[Figure 1, callout 9]
This is the primary Versal device PS-side UART interface. MIO42 (RX_IN) and MIO43 (TX_OUT) are connected to FTDI FT4232HL U20 USB-to-Quad-UART bridge port BD through TI SN74AVC4T245 level-shifters U18 and U271. The FT4232HL U20 port assignments are listed in the following table.

Table: FT4232HL Port Assignments

FT4232HL U34	Versal Device U1
Port AD JTAG	VEK280 JTAG chain
Port BD UART0	PS_UART0 (MIO 42-43)
Port CD UART1	PL_UART1 bank 401
Port DD UART2	U20 system controller UART

The FT4232HL UART interface connections are shown in the following figure.

Figure: FT4232HL UART Connections



For more information on the FT4232HL, see the Future Technology Devices International Ltd. website.

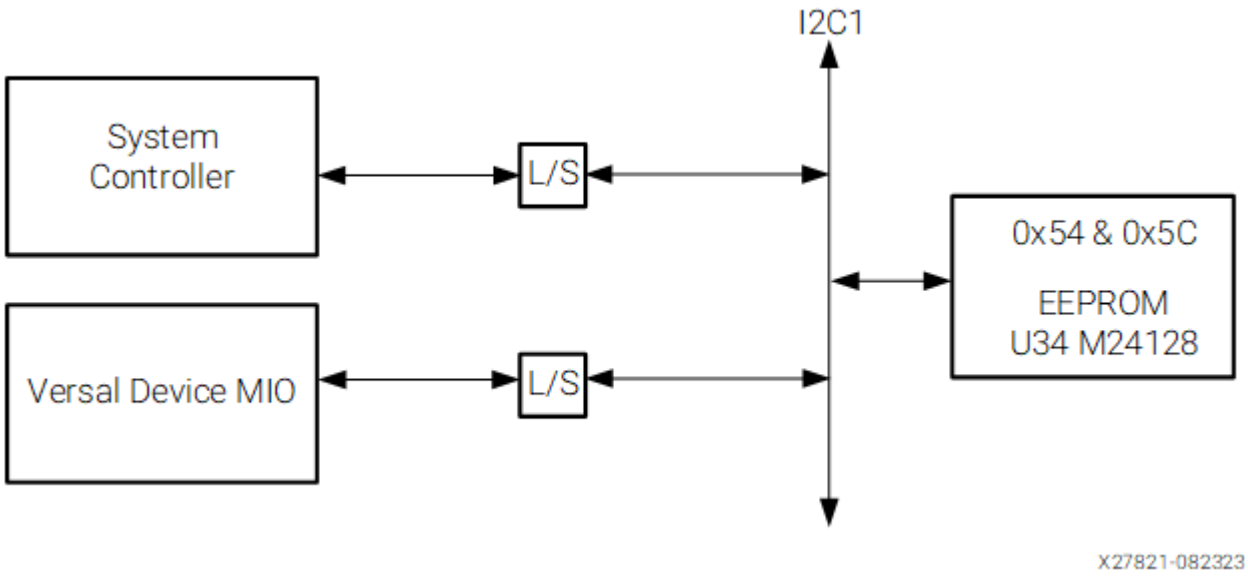
Note: The FTDI configuration image can be programmed with the Vivado tools. See the Programming FTDI Devices for Vivado Hardware Manager Support section in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908). Alternatively, a JTAG-SMT2 or similar from Digilent is recommended.

The detailed device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.

PMC MIO[44:45] I2C1 Bus

[Figure 1, callout 12]
Bus I2C1 connects the XCVE2802 U1 PS bank 501 and the XCZU4EG system controller U125 PS bank 501.
The detailed device connections for the feature described in this section are documented in the VEK280 evaluation board XDC file, referenced in Xilinx Design Constraints.

Figure: I2C1 Bus Topology



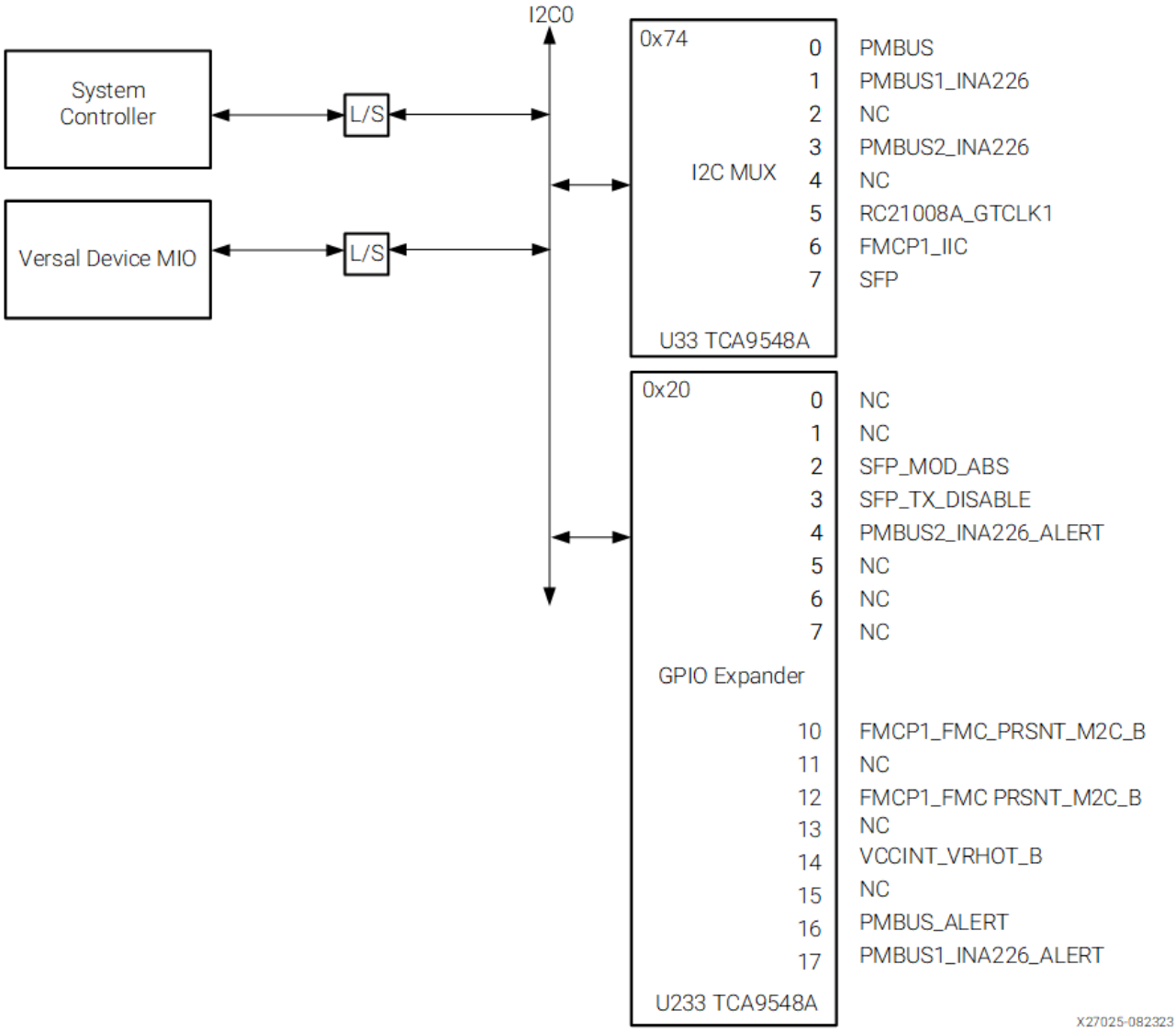
U34 is an I2C addressable 128-Kbit serial I2C bus EEPROM. It has two addresses associated with it. Address `0x54` is used when the memory array is accessed. When using `0x5C`, the identification page is accessed.

PMC MIO[46:47] I2C0 Bus

[Figure 1, callout 12]
Bus I2C0 connects the XCVP1802 U1 PS bank 501 and the XCZU4EG system controller U125 PS bank 501 to a GPIO 16-bit port expander (TCA6416A U233) and I2C switch (TCA9548A U33). The port expander enables accepting various SFP, FMCP connector, and power system status inputs and outputs. Bus I2C0 also provides access to power system PMBus power controllers and INA226 power monitors, as well as RC21008A clock components via the U33 TCA9548A switch. TCA6416A U233 is pin-strapped to respond to I2C address `0x20`. The TCA9548A

U33 switch is set to 0x74. Details for controlling the U33 TCA9548A switch can be located in the data sheet located on the Texas Instruments website.
The detailed device connections for the feature described in this section are documented in the VEK280 board schematic and XDC file, referenced in Xilinx Design Constraints.

Figure: I2C0 Bus Topology



The devices on each port of the I2C0 U233 TCA6416A port expander and on each bus of the I2C0 U33 TCA9548A switch are listed in the following tables.

Table: I2C0 Port Expander TCA6416A U233 Address 0x20 Connections

I2C0 Port Expander TCA6416A U233 Address 0x20 Connections			
I2C Devices	Port	Direction	Device
NC	P00-P01	N/A	N/A

I2C0 Port Expander TCA6416A U233 Address 0x20 Connections			
I2C Devices	Port	Direction	Device
SFP_MOD_ABS	P02	Out	J376 SFP+ connector
SFP_TX_DISABLE	P03	Out	J376 SFP+ connector
PMBUS2_INA226_ALERT	P04	In	U125 (ZU4), U166, U168, U172, U174, U176, U177, U188, U234, U264, U265, U281, U306, U309
NC	P05-P09	N/A	N/A
FMCP1_FMC_PRSNT_M2C_B	P10	In	J51 FMCP HSPC
NC	P11	N/A	N/A
FMCP1_FMCP_PRSNT_M2C_B	P12	In	J51 FMCP HSPC
N/A	P13	N/A	N/A
VCCINT_VRHOT_B	P14	In	U152 IR35215
N/A	P15	N/A	N/A
PMBUS_ALERT	P16	In	U125 (ZU4), U152, U160, U167, U175, U275, U282, U295, U354
PMBUS1_INA226_ALERT	P17	In	U65, U125 (ZU4), U161, U163, U165 U260, U355, U356

Table: I2C0 Multiplexer TCA9548A U33 Address 0x74 Connections

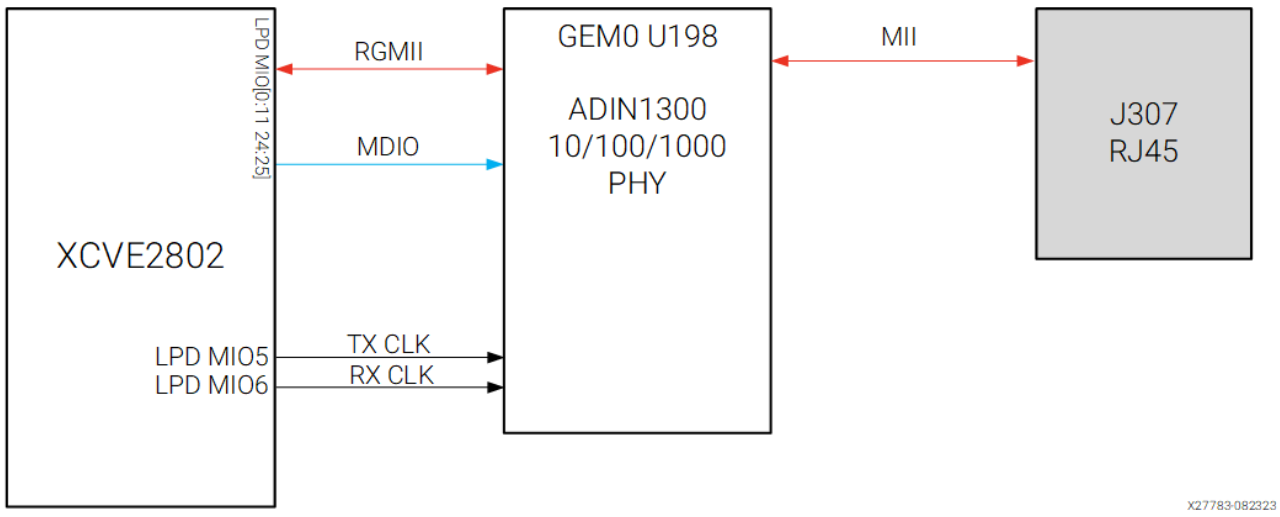
I2C Devices	I2C Switch Pos.	I2C Address	Devices
PMBUS	0	See Schematic, PMBus Regulators Map	
PMBUS1_INA226	1	See Schematic, PMBus Regulators Map	
No connect	2	N/A	
PMBUS2_INA226	3	See Schematic, PMBus Regulators Map	

I2C Devices	I2C Switch Pos.	I2C Address	Devices
No connect	4	N/A	
RC21008A_GTCLK1	5	0x09	
FMCP1_IIC	6	0x##	
SFP	7	0x##	

PMC MIO[48] and LPD_MIO[0:11, 24:25]: GEM0 Ethernet

[Figure 1, callout 19]
A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mbps Ethernet interface. In the following figure, the device (U1) is connected to ADI ADIN1300 U198 Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector J307. The RGMII Ethernet PHY is boot strapped to PHY address (`0x01`) and Auto Negotiation is set to Enable.

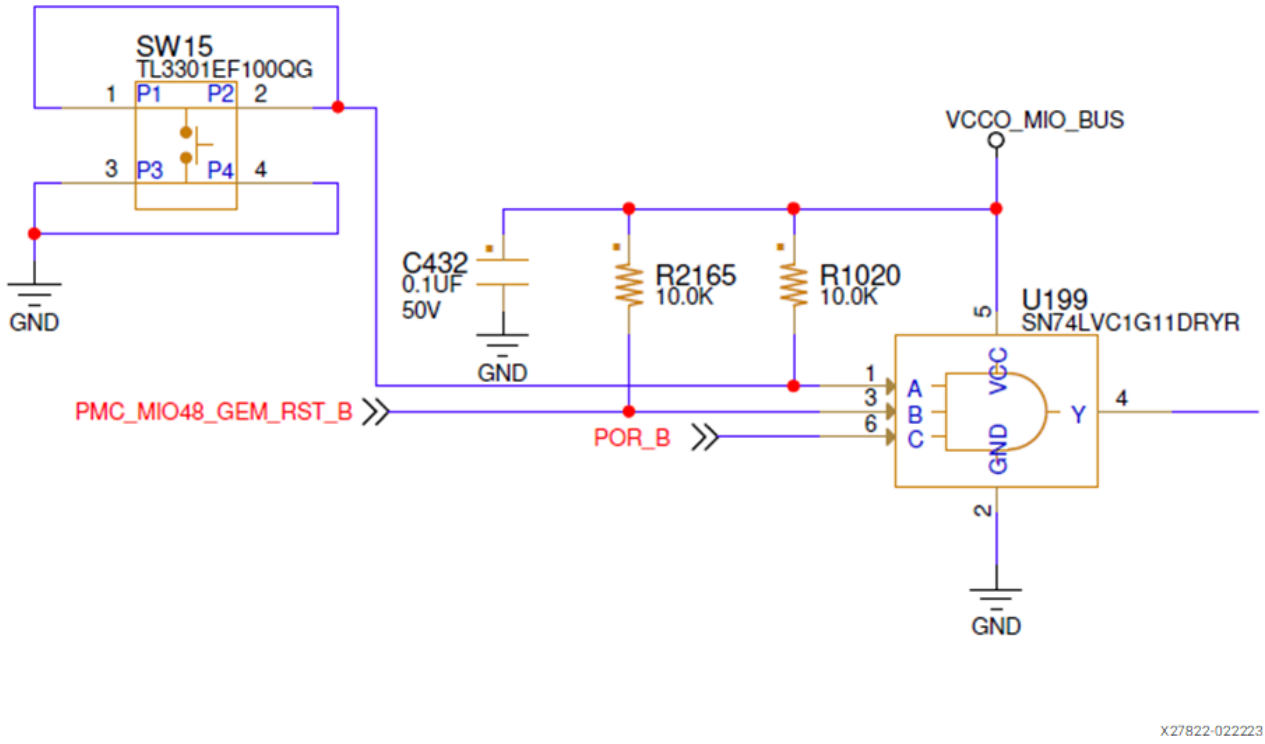
Figure: RGMII Ethernet



Ethernet PHY (Three Resets)

[Figure 1, callout 19]
The ADIN1300 PHY (GEM0 U198) is reset by its GEM0_RESET_B generated by dedicated pushbutton switch (SW15) and PMC_MIO signals as shown in the following figure. The POR_B signal generated by the TPS389001DSER U10 POR device is wired in parallel to each Ethernet PHY reset circuit. The POR device is activated by pushbutton SW2. See System Reset POR_B for more details.

Figure: Ethernet PHY Reset Circuit



Ethernet PHY LED Interface

[Figure 1, callout 19]
The ADIN1300 PHY (GEM0 U198) controls two LEDs in the J307 two port connector bezel. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED functional description is listed in the following table.

Table: Ethernet PHY LED Functional Description

ADIN1300 PHY Pin		Description
Name	Number	
LED_1	26	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits. The LINK_ST pin is a general-purpose output used to indicate to the MAC whether a valid link has been established.
LED_0	21	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

ADIN1300 PHY Pin		Description
Name	Number	
		The LED_0 can be used to indicate the speed of operation, link status, and duplex mode. By default, LED_0 illuminates when a link is established and blinks when there is activity. The default LED operation can be overwritten in software using the PHY LED control registers, LED_CTRL_1, LED_CTRL_2, and LED_CTRL_3 (Register Address 0x001B, Register Address 0x001C, and Register Address 0x001D, respectively).

The LED functions can be repurposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC.
See the ADI ADIN1300 RGMII PHY data sheet at the Analog Devices website for component details.
The detailed device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.

PMC MIO[11,49] and LPD MIO[12,13,20,23]: Power Enable

[Figure 1, callout 22-30]
The VEK280 allows the Versal device to control the power to the various power domains. This is an active-High signal. It is connected to the components that are controlled using an open-drain buffer. Signals are listed in the following table with their associated power domains. The output of the buffers are pulled up with a 4.7K resistor to aid in the default boot state being set properly. When J345 is installed, the associated power enables and, consequently, power supplies are disabled. This can be useful when changing the programmable power supply default programming. When not installed, the Versal device shares control with UTIL_5V0_PGOOD, which is an output from the 5.0V power supply (U191). See schematic page 71 for more information (see Jumpers for defaults).

Table: PMC MIO[49] and LPD MIO[12,13,20,23] Power Domains

Versal Device Pin	Signal	Power Domains

Versal Device Pin	Signal	Power Domains
PMC MIO 11	VCC_AUX_1V2_EN	VCCAUX_PMC, VCC_PSFP, VCCAUX, UTIL_0V9, VCC1V1_LP4, VCC1V5, LPDMGTYAVCC, VCCO_MIO,
PMC MIO 49	VCC_PSLP_EN	LPDMGTYAVCC, LPDMGTYAVTT
LPD MIO 12	VCC_PSFP_EN	VCC_PSFP
LPD MIO 13	VCC_SOC_EN	VCC_SOC
LPD MIO 20	VCC_PL_EN	VCCINT, VCCO_HDIO_3V3, VCC1V5, MGTAVTT, VCC_RAM, MGTAVCC, MGTVCCAUX
LPD MIO 23	VADJ_FMC_EN	VADJ_FMC

Note: See LPD MIO[23]: VADJ_FMC Power Rail for more information.

LPD MIO[21:22] Fan PWM

The Versal device PS bank 502 MIO21 (MIO21_FAN_PWM_VERSAL) is connected to J347 pin 3. When J347 is selected as 2-3 (see Jumpers for defaults), the Versal device is able to control the fan PWM speed. A controller application must be created to drive this logic. The Versal device PS bank 502 MIO22 (MIO22_FAN_TACH_VERSAL) is connected J348 pin 3. This signal is fed by a 2N7002 MOSFET (Q46), which is in turn connected to the 12V fan tachometer feedback. The 2N7002 is a N-Channel 60 V MOSFET. For more details, see Cooling Fan Connector.

LPD MIO[23]: VADJ_FMC Power Rail

Warning: The VEK280 board can only be used with FMC cards that can support 1.5V. The VEK280 board exposes FMC add-on cards requiring lower than 1.5V levels to this higher voltage.

The VITA 57.4 FMC+ Industry Standard calls out not only specific connectors, but behaviors of the devices being connected. This creates a highly adaptable and flexible interface allowing a best fit for many industries and prototyping needs. While AMD strives to adhere to all standards providing customers with the best

possible experience, in the case of the VEK280 evaluation and prototyping board, a compromise had to be made. Due to the I/O limitations on the XCVE2802-2MSEVSVH1760 package, there is limited VITA 57.4 compatibility. As the targeted use case for the VEK280 requires LPDDR4, a large quantity of I/O pins is used for the memory. This prevents the use of other features and capabilities for the designated feature set. To resolve this, pin-efficient layout and routing was selected for use with the LPDDR4. As a result, Banks 705 and 706 are tied to VADJ_FMC. VADJ_FMC_BUS is the non-adjustable voltage for the FMC connector (J51). VADJ_FMC and VADJ_FMC_BUS for the VEK280 is fixed to 1.5V at boot and, consequently, is non-compliant to the VITA 57.4 FMC+ Industry Standard. The power control of the VADJ_FMC power rail is managed by the power good and enable connection to U282.

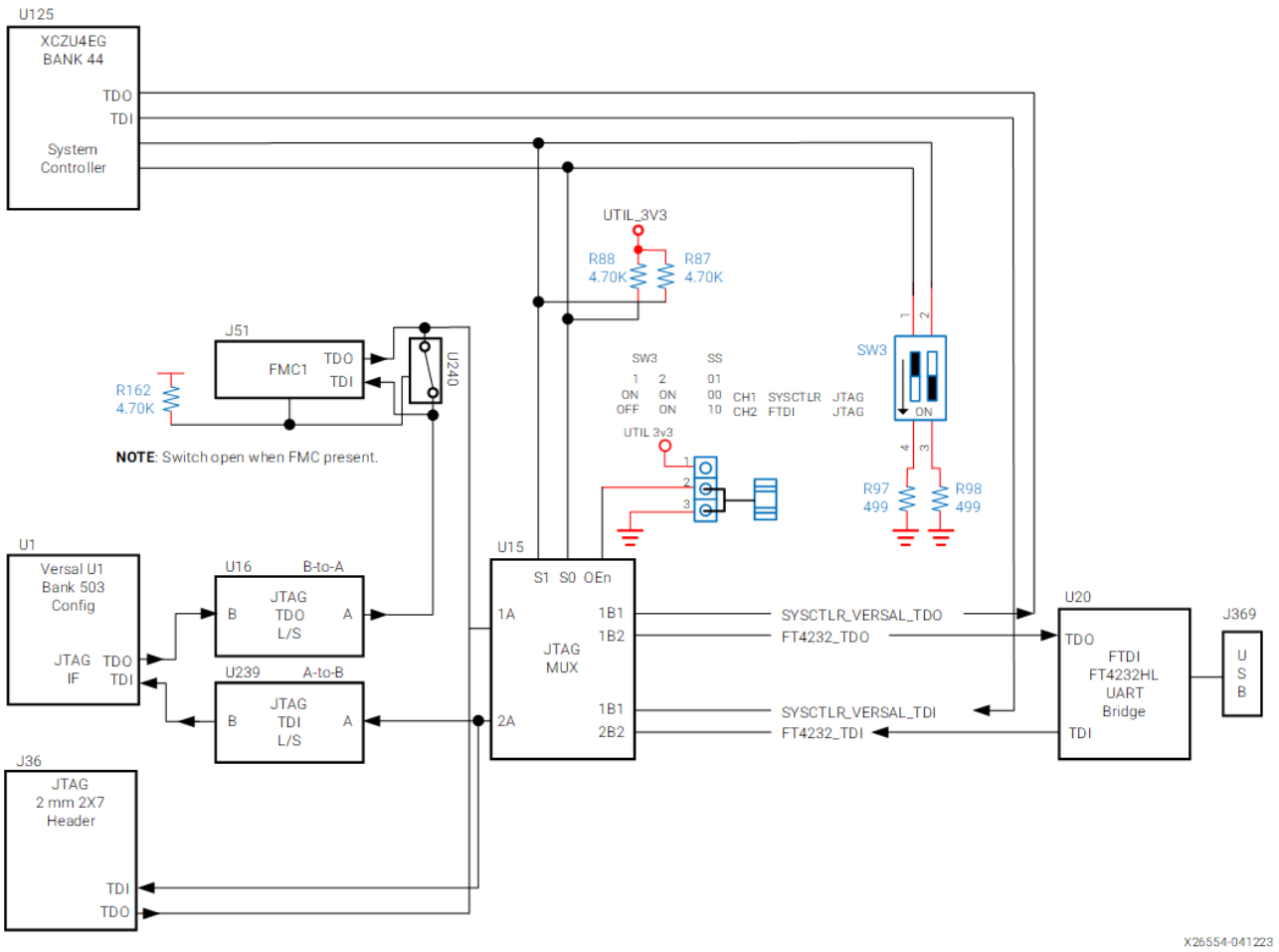
Note: While banks 705 and 706 can be power monitored by an INA226 (U281), the J51 VADJ pins are not monitored

JTAG Chain

[Figure 1, callout 6, 9, Figure 1, callout 14, 16]
The JTAG chain includes:

- J36 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J369 USB3 type-C connector connected to U20 FT4232HL USB-JTAG bridge
- U125 XCZU4EG System Controller bank 44

Figure: JTAG Chain Block Diagram



See Versal Device Configuration for information on JTAG programming via:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U20) connected to USB 3.1 type-C connector (J369)
- JTAG pod flat cable connector J36 (2 mm 2x7 shrouded/keyed)

See the "FT4232HL UART Connections" figure in PMC MIO[42:43] UART0 for an overview of FT4232 U20 JTAG and USB-UART connectivity.

Clock Generation

The VEK280 board provides fixed and variable clock sources for the XCVE2802 U1 device and other function blocks. The following table lists the source devices for each clock.

Table: Clock Sources

Ref. Des.	Feature	Notes	Schematic Page
U299	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x09	Renesas output 1RC21008A	93

Ref. Des.	Feature	Notes	Schematic Page
U299	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x09	Renesas output 2 RC21008A	93
U299	DDR4 DIMM CLK, 200 MHz, 3.3V LVDS, 0x09	Renesas output 3 RC21008A	93
U299	Adaptive SoC U1 GTYP (FMC+) CLK, 100 MHz, 3.3V LVDS, 0x09	Renesas output 6 RC21008A	93
U299	Adaptive SoC U1 GTYP (FMC+) CLK, 100 MHz, 3.3V LVDS, 0x09	Renesas output 7 RC21008A	93
U299	Adaptive SoC U1 GTYP (zSFP+) CLK, 156.25 MHz, 3.3V LVDS, 0x09	Renesas output 8 RC21008A	93
U299	Adaptive SoC U1 processing system (PS) reference CLK, 33.33 MHz, 1.8V LVCMOS, 0x09	Renesas output 10 RC21008A	93
U299	Master mode Ethernet CLK, 25 MHz, 1.8V LVCMOS, 0x09	Renesas output 11 RC21008A	93
U374	Adaptive SoC U1 HSDP CLK, 156.25 MHz, 3.3V LVDS	CTS 626L15625I3T	8
U344	HDMI RX RCLK, various, 3.3V differential, 0x5B	TI TMDS1204	45
U344	HDMI RX OUT CLK, various, 3.3V differential, 0x5B	TI TMDS1204	45
U1	IEEE-1588 eCPRI CLK, various, 3.3V, 0x5B	Adaptive SoC XCVE2802	3, 92

The detailed device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.

Programmable MGT RC21008A REF Clocks

[Figure 1, callout 36]

The VEK280 evaluation board has one I2C programmable RC21008A high-performance frequency synthesizer (U299) that provides excellent phase jitter on reference clocks. The output has been configured in various outputs. See the *Clock Sources* table in the Clock Generation section for more details.
At power-up, this clock defaults to an output frequency of 200 MHz for the LPDDR4, 100 MHz for the transceivers attached to the FMC+, 156.25 MHz for the transceivers attached to the zSFP+, and 25 MHz for the onboard Ethernet. User applications or the system controller can change the output frequency within the range of 0.001 MHz to 650 MHz through the I2C bus interface. Power cycling the VEK280 evaluation board reverts this user clock to the default frequencies listed previously.

- Programmable frequency synthesizer: Renesas RC21008A097#BB0
- 0.001 MHz-650 MHz range, 156.25 MHz default
- I2C address `0x09`
- LVDS differential output

Fixed HSDP REF Clock

[Figure 1, callout 45]
The VEK280 evaluation board has a fixed frequency very low jitter 3.3V LVDS oscillator (U374). The 156.25 MHz HSDP_156_25_REFCLK clock signal is connected to the XCVE2802 device U1 bank 106. At power-up, this clock defaults to an output frequency of 156.25 MHz.

- Fixed oscillator: CTS 626L15625I3T
- 156.25 MHz default
- LVDS differential output, total stability: ±25 ppm

Transceivers

The Versal device has 32 PL GTYP transceivers. The following table contains the mapping to hardened features, quads, channel locations, as well as general features.

Table: Transceiver Mapping

		XCVE2802							
FMC+	FMCP1_DP24	CH0	GTYP Quad	PCIe X1Y2	PCIe X0Y2	GTYP Quad	CH0	Versal_HSDP	HSDP/ SFP28

		XCVE2802								
	FMCP1_DP_C2M_P_5	CH1	206 X1Y4 CC [L]			106 X0Y4 BE [RN] (RCAL)	CH1	HSDP_VERSAL_SYSCTL		
	FMCP1_DP_C2M_P_6	CH2					CH2	[UNUSED]		
	FMCP1_DP_C2M_P_7	CH3					CH3	SFP28		
	RC21008A_GTCLK1_OUT7	REF0					REF0	HSDP_156_25_REFCLK		
	FMCP1_GBTCLK1_M2C	REF1					REF1	RC21008A_GTCLK1_OUT8		
	FMCP1_DP_C2M_P_0	CH0	GTYP Quad 205 X1Y3 CB [L] (RCAL)	PCIe X1Y1	CPM5	GTYP (CPM5) Quad 105 X0Y3 BD [RS] (RCAL)	CH0	PCIe Lane3	PCIe Gen4x16	
	FMCP1_DP_C2M_P_1	CH1					CH1	PCIe Lane2		
	FMCP1_DP_C2M_P_2	CH2					CH2	PCIe Lane1		
	FMCP1_DP_C2M_P_3	CH3					CH3	PCIe Lane0		
	RC21008A_GTCLK1_OUT6	REF0					REF0	PCIe_CLK0		
	FMCP1_GBTCLK0_M2C	REF1					REF1	[UNUSED]		
HDMI 2.1	HDMI_CH0	CH0	GTYP Quad 204 X1Y2 CA [L]	MRMAC X0Y1		GTYP (CPM5) Quad 104 X0Y2 BC [RS]	CH0	PCIe Lane7		
	HDMI_CH1	CH1					CH1	PCIe Lane6		
	HDMI_CH2	CH2					CH2	PCIe Lane5		
	HDMI_TX_CLK_C / HDMI_RX_CLK_C	CH3					CH3	PCIe Lane4		
	HDMI_RCLK_OUT_C	REF0					REF0	PCIe_CLK1		
	HDMI_8T49N241_OUT_C	REF1					REF1	[UNUSED]		

		XCVE2802							
			VDU	PCIe X1Y0		GTYP (CPM5) Quad 103 X0Y1 BB [RS]	CH0	PCIe Lane11	
							CH1	PCIe Lane10	
							CH2	PCIe Lane9	
							CH3	PCIe Lane8	
							REF0	PCIe_CLK2	
							REF1	[UNUSED]	
			VDU	MRMAC X0Y0		GTYP (CPM5) Quad 102 X0Y0 BA [RS]	CH0	PCIe Lane15	
							CH1	PCIe Lane14	
							CH2	PCIe Lane13	
							CH3	PCIe Lane12	
							REF0	PCIe_CLK3	
							REF1	[UNUSED]	
			VDU	HDIO Bank 401 AA	PMCDIO Bank 503	LPDMIO Bank 502			
			VDU	HDIO Bank 400 AB	PMCDIO Bank 501	PMCMIO/PMCDIO Bank 500			

GTYP Transceivers

[Figure 1, callout 1]
The Versal device (U1) bank 205 and bank 206 GTYP transceivers are wired to the FMCP connector (J51). See schematic pages 9 and 30 for details.
The GTY/GTYP transceivers in the Versal architecture are power-efficient transceivers, supporting line rates from 1.25 Gbps to 32.75 Gbps. The GTY/GTYP transceivers are highly configurable and tightly integrated with the programmable logic resources of the Versal architecture. For more information, see the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002).

GTYP102/103/104/105: PCI Express Card Edge Connectivity

For additional information about the Versal device PCIe functionality, see the *Versal Adaptive SoC CPM Mode for PCI Express Product Guide* (PG346) and *Versal Adaptive SoC CPM DMA and Bridge Mode for PCI Express Product Guide* (PG347). Additional information about the PCI Express standard is available on the PCI-SIG website. See the *Versal Architecture and Product Data Sheet: Overview* (DS950) for more information about this feature.
See schematic pages 7 and 40, as well as the VEK280 Evaluation Board website for more details on connectivity. See schematic page 49 for details on the clocking configuration.

GTYP200/201: FPGA Mezzanine Card Interface

[Figure 1, callout 20]

Warning: The VEK280 board can only be used with FMC cards that can support 1.5V. The VEK280 board exposes FMC add-on cards requiring lower than 1.5V levels to this higher voltage. See LPD MIO[23]: VADJ_FMC Power Rail.

The detailed Versal device connections for the feature described in this section are documented in the VEK280 board XDC file, referenced in Xilinx Design Constraints.

FMC+ Connector Type

The Samtec SEAF series 1.27 mm (0.050 in) pitch mates with the SEAM series connector. For more information about the SEAF series connectors, see the Samtec, Inc. website. The 560-pin FMC+ connector defined by the FMC specification (see VITA 57.4 FMCP Connector Pinouts) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver (GBTCLK) differential clocks
- 4 differential (CLK) clocks
- 1 differential (REFCLK) clock (both C2M and M2C pairs)
- 1 differential (SYNC) clock (both C2M and M2C pairs)
- 239 ground and 17 power connections

For more information about the VITA 57.4 FMC+ specification, see the VITA FMC Marketing Alliance website.

HDMI

[Figure 1, callout 18]
The VEK280 has one HDMI™ 2.1 source and one HDMI 2.1 sink that are provided by HDMI 2.1 compatible redrivers and miscellaneous control signals. A separate high quality programmable clock is provided for driving this entire circuit to allow flexibility and tuning.

Note: The first release of the EA VEK280 has an FRL data rate limit of 8 Gbps /lane.

HDMI Video Input/Output

The VEK280 evaluation board generates HDMI video output using the TI TMDS1204 HDMI redriver chip. This video output is fed to a Molex HDMI™ 2.1 receptacle. The board also accepts HDMI video input on another Molex HDMI2.1 receptacle to another TI TMDS1204 HDMI™ redriver on the receiving.

Note: The TDMS1204 supports lane swapping. The transmit side takes advantage of this for improved layout and needs to be configured appropriately. For more information, see the TDMS1204 datasheet, section Swap (8.2.5 in SLLSF57 – AUGUST 2022 datasheet revision) and VEK280 schematic page 44.

The TMDS1204 HDMI 2.1 redriver supports data rates up to 12 Gbps. It is backwards compatible with HDMI 1.4b and HDMI 2.0b. The TMDS1204 can support both three and four lane HDMI 2.1 FRL at 3, 6, 8, 10, and 12-Gbps.
More information on the TI TMDS1204 is available on the TI website.

Note: The first release of the EA VEK280 board has a FRL data rate limit of 8 Gbps / lane

The series capacitor-connected HDMI TX and RX data signals from TMDS1204 are routed to the VE2802 GTYP Bank 204.

HDMI Control I2C Bus

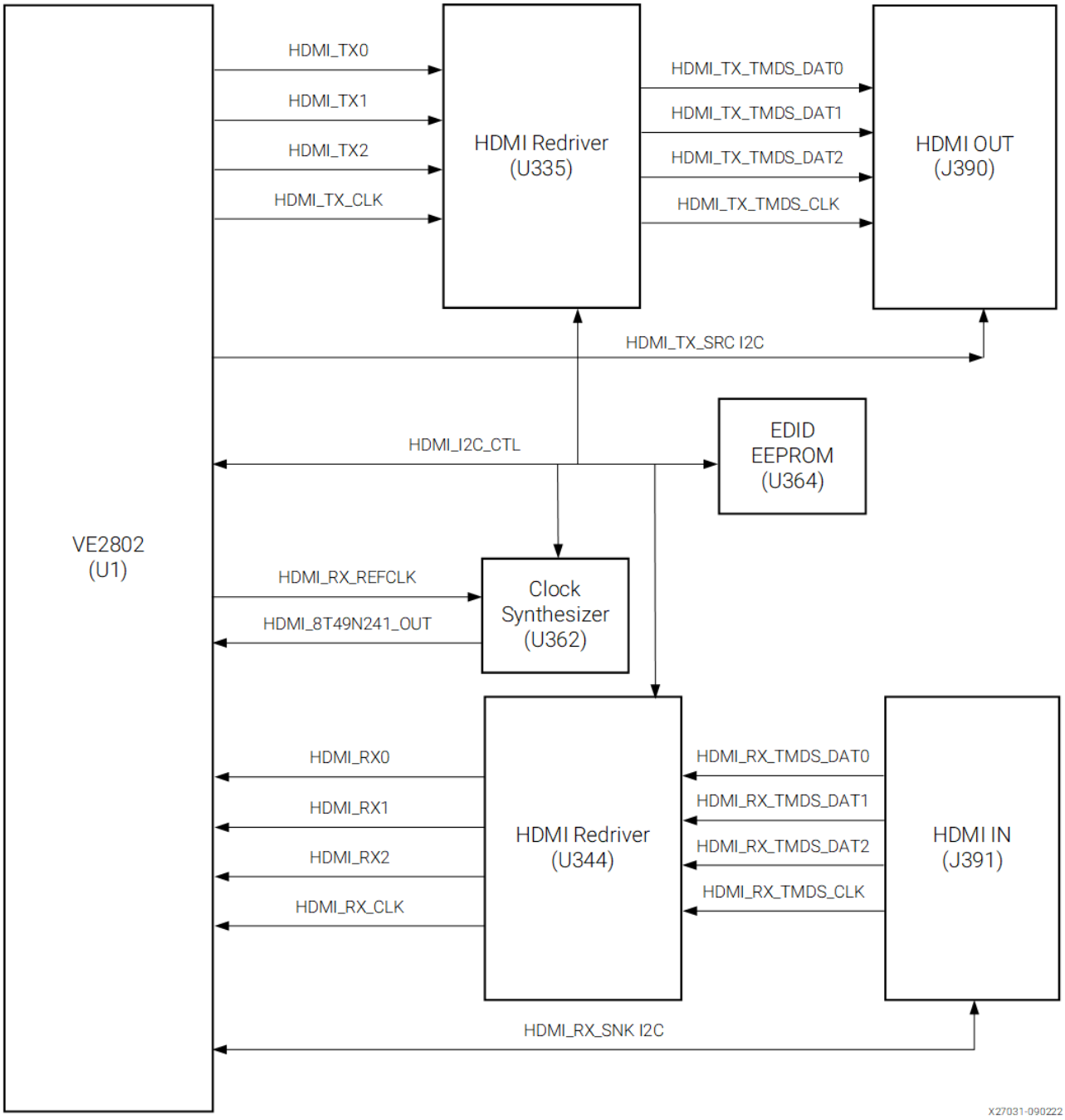
The HDMI_CTL I2C bus connects the XCVE2802 U1 bank 702 to two HDMI TDMS1204 redrivers (U335, U364), a M24128 128-Kbit EDID Serial EEPROM (U364), and a Renesas 8T49N241 FemtoClock NG Universal Frequency Translator (U362). See the VEK280 evaluation board schematic pages 3, 44, 45, and 46 for more information. The following table lists the control I2C bus devices and addresses.

Table: HDMI Control I2C Bus

Ref. Des.	I2C Devices	I2C Address
U335	TDMS1204 HDMI TX redriver	0x5E
U344	TDMS1204 HDMI RX redriver	0x5B
U362	8T49N241-994 FemtoClock	0x6C
U364	M24128 EEPROM	0x50

The HDMI video and control I/O block diagram is shown in the following figure.

Figure: HDMI Video and Control I/O Block Diagram



HDMI Clocking

HDMI Source Clock

The VEK280 evaluation board includes a Renesas RC21008A (U299). This chip is used to source the 400 MHz FRL/DRU clock used as the reference for driving the Versal device (U1) logic and related circuitry for HDMI.

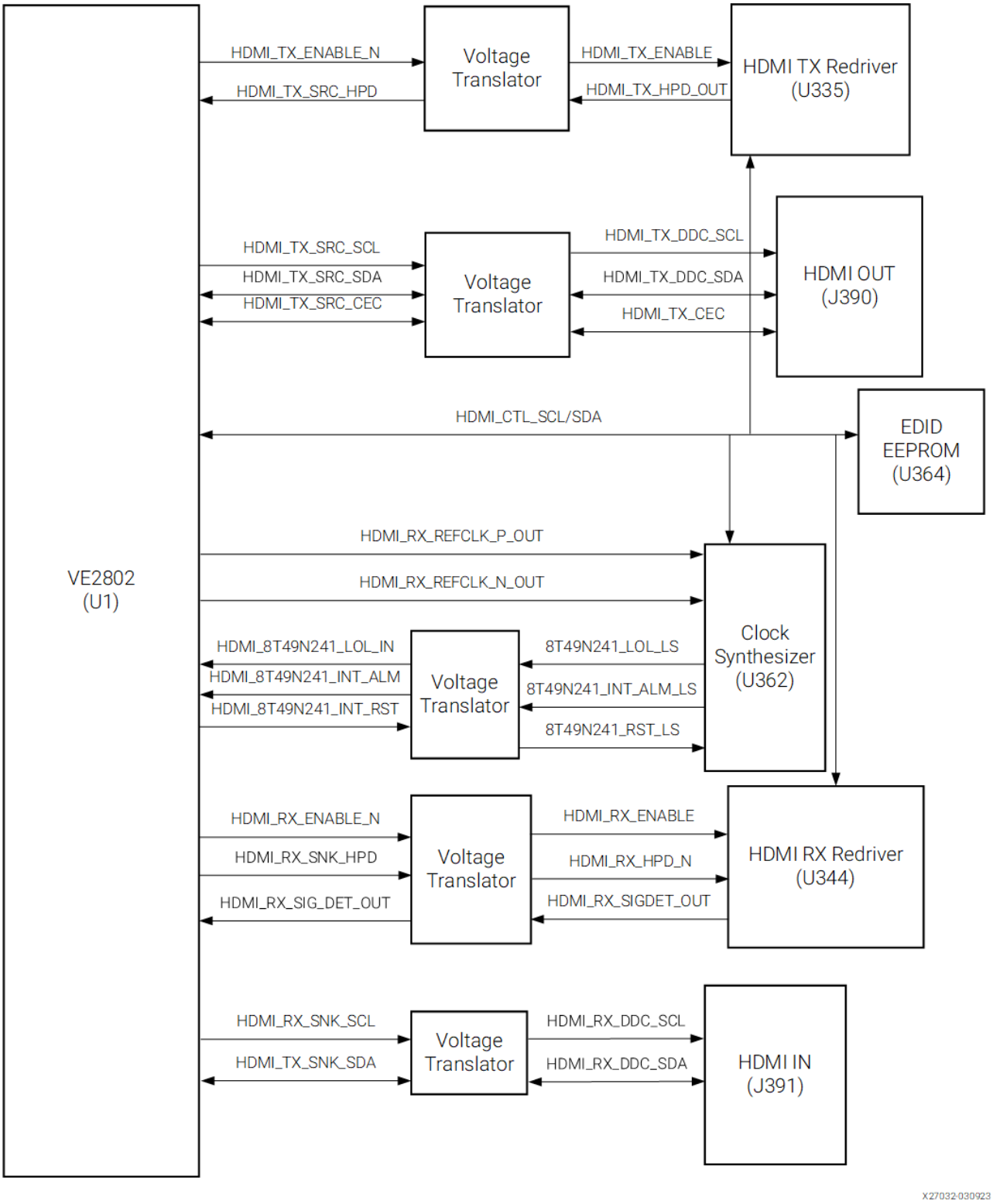
HDMI Clock Recovery

The HDMI circuitry includes a Renesas 8T49N241 frequency translator as a jitter attenuator. VE2802 can output a differential RX recovered clock (HDMI_RX_REFCLK) for jitter attenuation. The jitter-attenuated clock (HDMI_8T49N241_OUT) is routed as a reference clock to GTYP Bank 204. The 8T49N241 is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used standalone mode (FRL/TMDS) or pass-through mode (FRL), the 8T49N241 clock synthesizer (U362) operates in free running mode and uses an external oscillator as the reference. When the HDMI operation is in pass-through mode (TDMS), the 8T49N241 generates a jitter-attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI RX subsystem TMDS clock, so that they are phase aligned. The 8T49N241 is controlled by the HDMI 2.1 IP via I2C bus, HDMI_I2C_CTL.

HDMI I/O Interface

The HDMI TX and RX I/O signals are assigned to VE2802 XPIO Bank 702. Some of these signals such as I2C buses, HDMI_TX_SRC, and HDMI_RX_SNK have voltage translation to 5V connected to the HDMI receptacle. The block diagram in the following figure shows the I/O signal connections for HDMI TX and RX. A 128-Kbit EEPROM is provided for storing HDMI EDID metadata in the circuitry.

Figure: HDMI SRC and SNK Control I/O Block Diagram



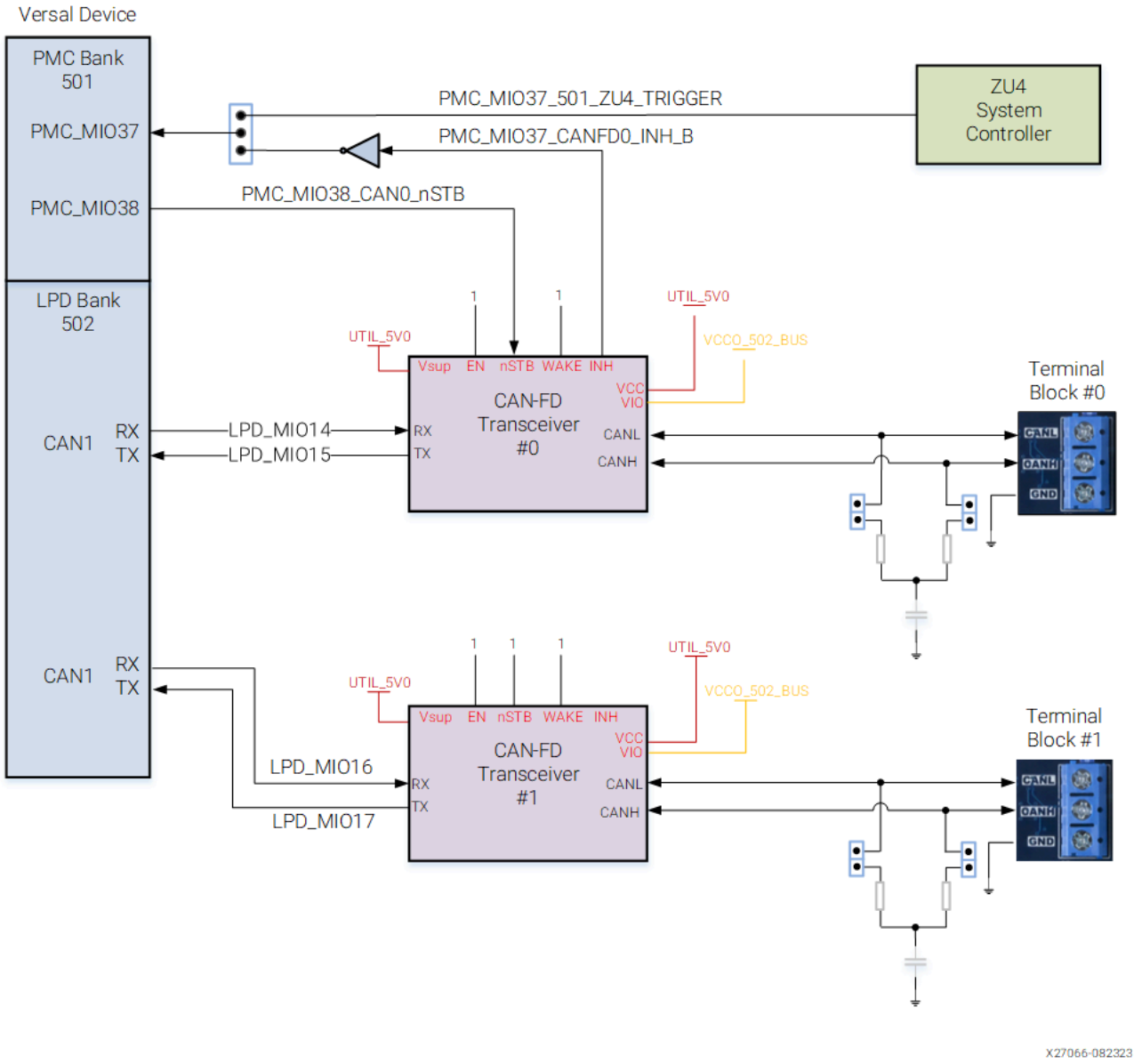
CAN Interface

The VEK280 board provides two CAN-FD buses. These can be used for prototyping and support classic CAN and CAN FD up to 8 Mbps. While many configurations are available, the design intention is for the VEK280 board to be a device on the bus.

LPD MIO[14:17] PMC MIO[37:38] CAN I/O interface

The two provided CAN-FD capable buses are identical, with the exception that CAN0 supports sleep mode and CAN1 does not. Sleep mode is connected such that when the VEK280 is a device, it can be put to sleep through CAN functions provided for in the transceiver. For more information, see the TI TCAN1043A datasheet and the VEK280 schematic page 41.
Buses are connected from the VE2802 through LPD_MIO pins. LPD_MIO[14:15], PMC_MIO[37:38] make up CAN0 and LPD_MIO[16:17] makes up CAN1. CAN0 has additional pins allocated to enable sleep mode.
CAN0 connects to a TI TCAN1043A CAN FD transceiver (U372). The output bus connects to screw terminal J392 for easy prototyping. Separate 60.4Ω resistors can be added to CAN0_CANL and CAN0_CANH using J395 and J396, respectively. CAN0 also has the INH output from U372 connected back to the VE2802 (U1) to aid in sleep mode control. See the VEK280 schematic pages 11 and 41 for details.
CAN1 connects to a TI TCAN1043A CAN FD transceiver (U373). The output bus connects to screw terminal J393 for easy prototyping. Separate 60.4Ω resistors can be added to CAN1_CANL and CAN1_CANH using J398 and J397, respectively. See the VEK280 schematic pages 11 and 41 for details.

Figure: CAN Buses



zSFP+ Control Signals

The zSFP+ control signals can be asserted in multiple ways. The zSFP+ has an I2C connection to the I2C0 bus through the I2C multiplexer (TCA9548PWR U33) as shown in the PMC MIO[46:47] I2C0 Bus section.
The following table lists the transceiver module control signals.

Table: Transceiver Module Control Signals

Signal Name	Feature	Notes	Schematic Page
SFP_SDA	Two-wire interface data	U33 I2C MUX	29, 39
SFP_SCL	Two-wire interface clock	U33 I2C MUX	29, 39

Signal Name	Feature	Notes	Schematic Page
SFP_TX_FAULT	Module to U1 - fault condition detected	U1 Bank 401	6, 29
SFP_TX_DISABLE	U1 to module - transmitter disable	U233 I2C GPIO expander	29, 39
SFP_MOD_ABS	Logic High when module absent	U233 I2C GPIO expander	29, 39
SFP_RX_LOS	Module to U1 - RX signal loss	U1 Bank 401	6, 29

High-speed Debug Port

The PS includes an integrated Aurora 64B/66B block that is dedicated for accessing the debug packet controller (DPC) via a high-speed GT-based interface. This protocol to access the DPC is the high-speed debug port (HSDP) protocol. The HSDP provides bidirectional access to the device from an external host debug/trace module, allowing for high-speed debug and trace operations. The SmartLynq+ module can be connected to the Aurora interface to access the HSDP in the Versal device. For more information, see the *SmartLynq+ Module User Guide* (UG1514). For information on the HSDP quad availability, see the *Versal Adaptive SoC Technical Reference Manual* (AM011)).

Note: The VEK280 evaluation board has additional HSDP lanes provided for future System Controller use.

Note: The integrated HSDP Aurora interface is not available in all Versal devices, which might support HSDP using a soft Aurora solution. This interface requires additional configuration in the Control, Interfaces, and Processing (CIPS) IP, a PL aurora implementation, and the use of additional gigabit transceivers.

User I/O

[Figure 1, callout 17, 18 and Figure 1, callout 41]
See Switches for default values.
The following table lists the net names, reference designators, and schematic pages for the user I/O.

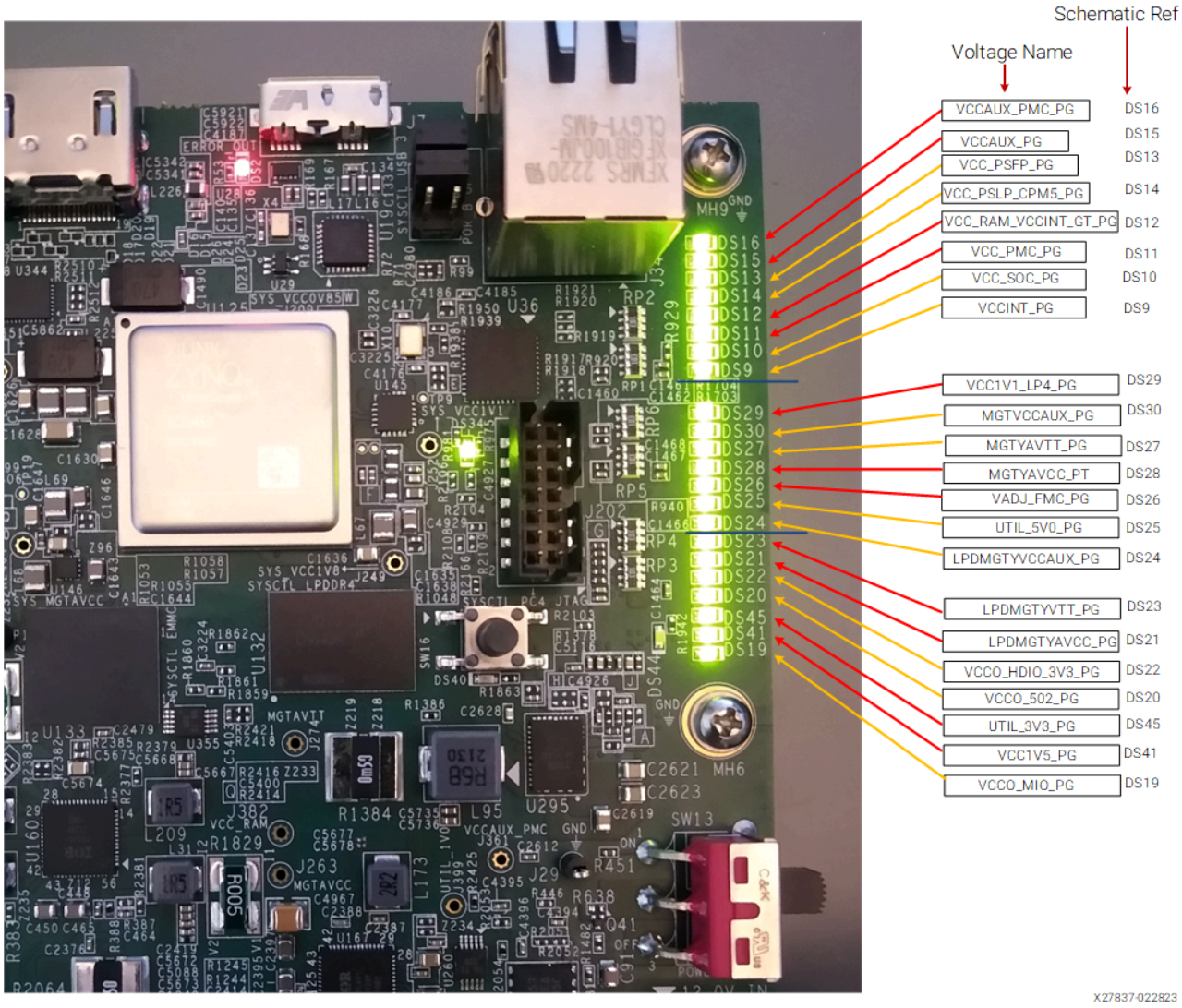
Table: User I/O

Net Name	Ref. Designator	Schematic Pages
GPIO_PB0	SW4	4, 48
GPIO_PB1	SW5	4, 48
GPIO_DIP_0	SW6	4, 48
GPIO_DIP_1	SW6	4, 48
GPIO_DIP_2	SW6	4, 48
GPIO_DIP_3	SW6	4, 48
GPIO_LED0	DS6	3, 48
GPIO_LED1	DS5	3, 48
GPIO_LED2	DS4	3, 48
GPIO_LED3	DS3	3, 48

Power and Status LEDs

[Figure 1, callout 32]
The following figure shows the power and status LEDs.

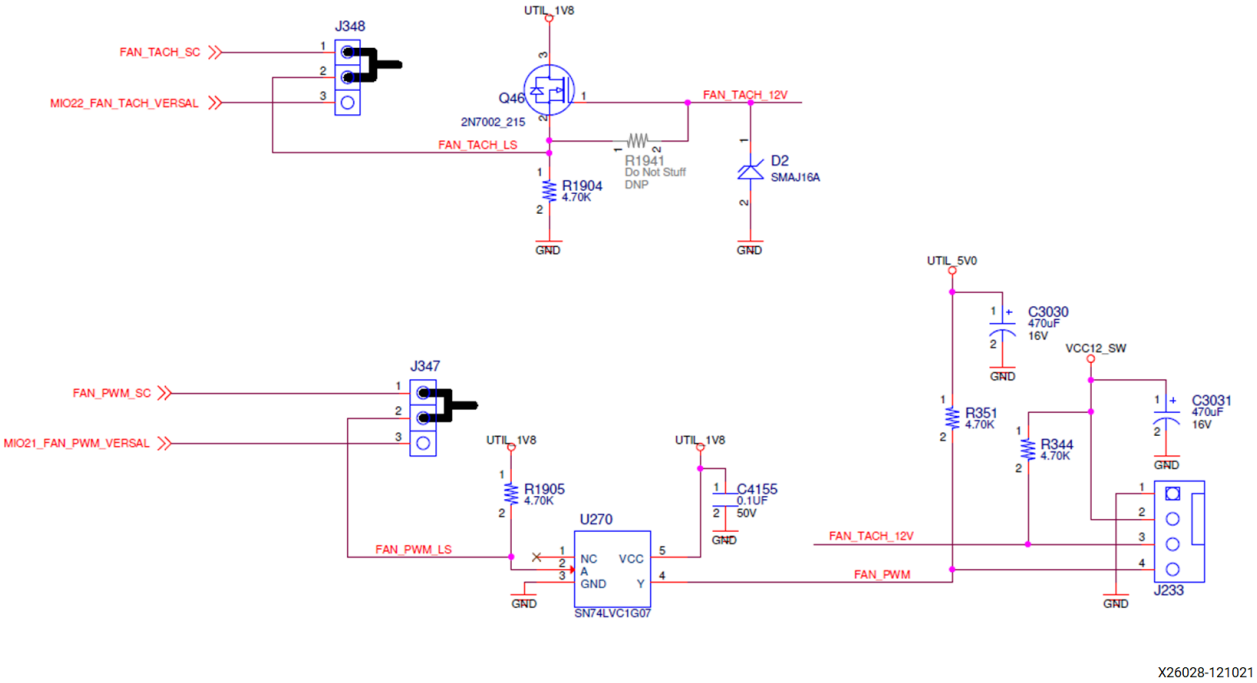
Figure: Power and Status LEDs



Cooling Fan Connector

[Figure 1, callout 35]
The VEK280 cooling fan connector is shown in the following figure. The VEK280 uses the system controller to autonomously control the fan speed by controlling the pulse width modulation (PWM) signal to the fan. The fan rotates slowly (acoustically quiet) when the Versal device's U1 is cool and rotates faster as the device heats up (acoustically noisy).
The VEK280 board provides a fan controller bypass header J347 and J348 to permit control by the Versal device. See the Default Jumper and Switch Settings for more details.

Figure: 12V Fan Header

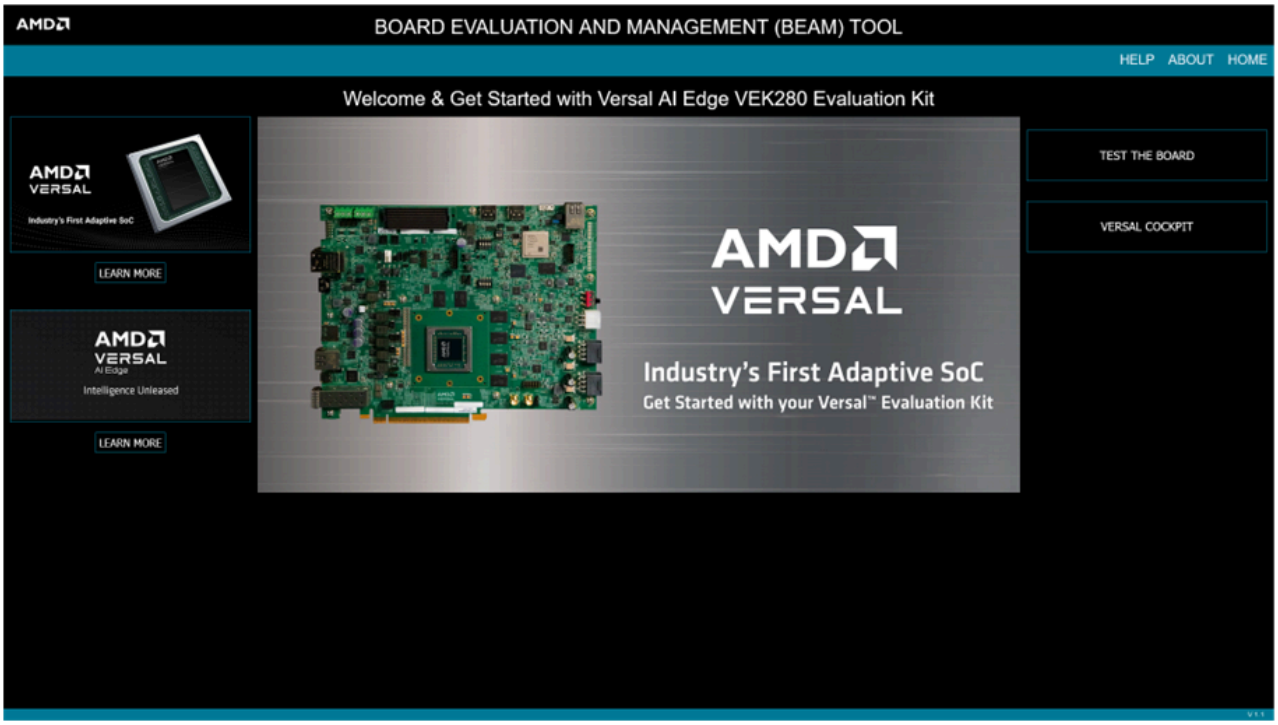


System Controller

[Figure 1, callout 44]

The VEK280 board includes an onboard system controller. The system controller hosts a website that allows for various controls over aspects of the evaluation board. This web-based interface enables the query and control of select programmable features such as clocks, FMC functionality, and power system parameters. Users should not change the default system controller image as that could potentially cause damage to the board if proper procedures are not followed. If this image needs to be updated and for more information on the system controller web interface, see the Versal Evaluation Board System Controller Wiki. The web application is shown in the following figure.

Figure: System Controller Web User Interface



X27825-100523

Power On/Off Slide Switch

[Figure 1, callout 20]
The VEK280 board power switch is SW13. Sliding the switch actuator from the off to the on position applies 12 VDC power from the 2x3 6-pin mini-fit power input connector J16 (power from an external 120 VAC-to-12 VDC power adapter).

!! Important: Power to the VEK280 is mutually exclusive and only one of the two power connections should be powered. Either J16 or both JP1 and JP2 should be used to provide board power.

The two 2x4 8-pin (6+2) ATX power supply PCIe-type connectors JP1 and JP2 are provided for higher power use cases.

- The customer ATX supply chosen must support at least two PCIe (6+2) GPU connections to support powering the evaluation board.
- Only use a single ATX supply to support delivery of 12V to two PCIe GPU (6+2) connectors or damage might occur.
- When ATX PCIe GPU 6+2 connections are made, the 6 pin mini-fit Jr power brick connection and onboard on/off power switch is disabled.

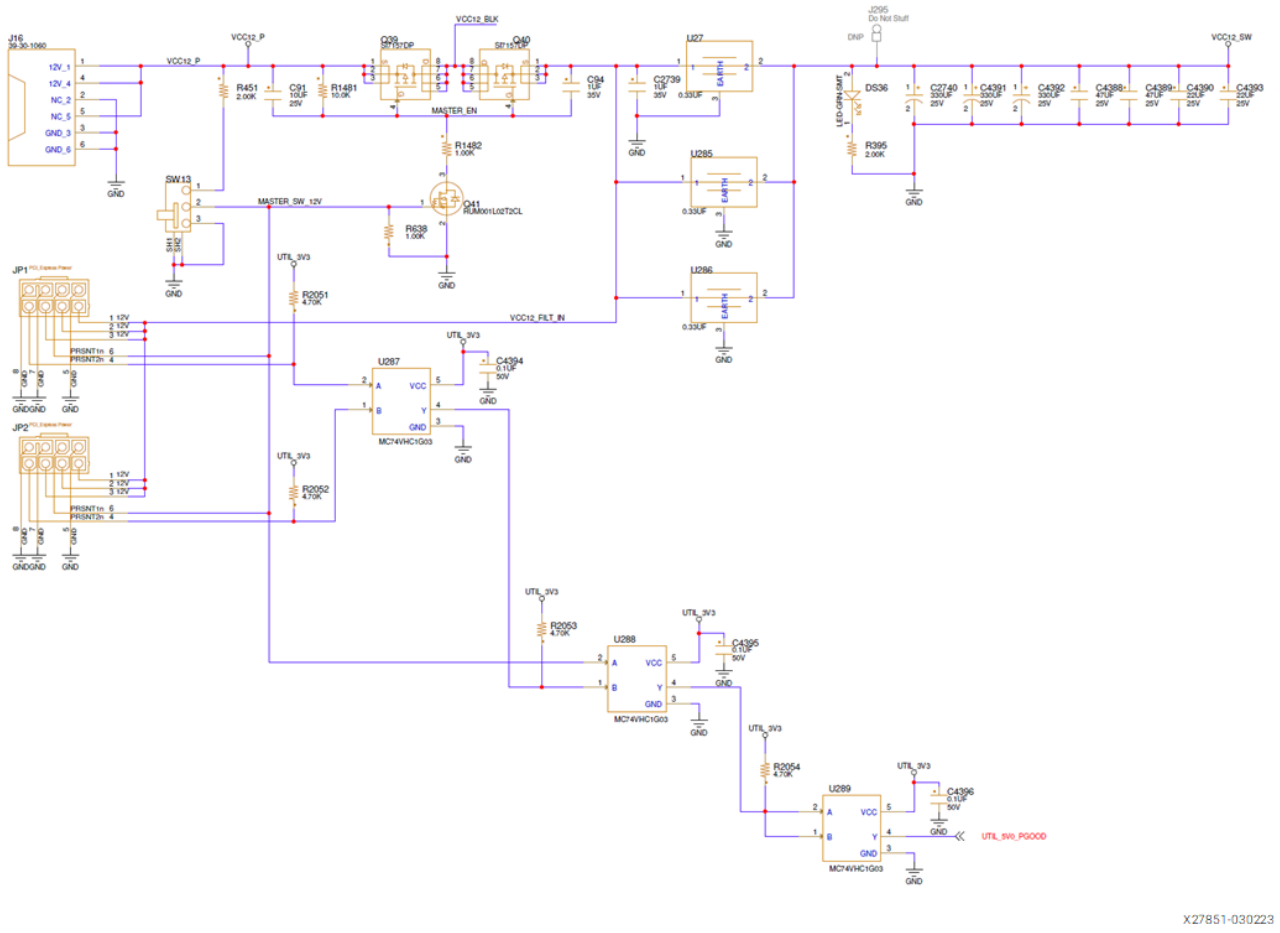
The green LED DS36 illuminates when the VEK280 board power switch is on. See Board Power System for details on the onboard power system.

⚠ CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into the VEK280 board power connector J16. The ATX 6-pin connector has a different pinout than

J16. Connecting an ATX 6-pin connector into J16 damages the VEK280 board and voids the board warranty.

The following figure shows the power connector J16, power switch SW13, and LED indicator DS36.

Figure: Power Input



Board Power System

[Figure 1, callout 21]
The VEK280 evaluation board uses power management ICs (PMIC) and power regulators from Infineon Integrated Circuits to supply the core and auxiliary voltages listed in the following tables. The detailed device connections for the feature described in this section are documented in the VEK280 board schematic.

Table: Power System - PMBus Regulators and INA226 Map

Rail	Rail Name	Nominal Voltage (V)	Max Current (A)	Device	PMBUS Addr	INA226 Addr
1	VCCINT	0.80	150	U152 L1, U154, U155, U157, U159,	0x46	0x40 BUS1

Rail	Rail Name	Nominal Voltage (V)	Max Current (A)	Device	PMBUS Addr	UCD226 Addr
				U277		
2	VCC_PMC	0.88	1	U160 A	0x47	0x42 BUS1
3	VCC_RAM	0.80	2	U160 C	0x47	0x43 BUS1
4	VCC_PSLP_CPM5	0.88	6	U175 C,D	0x4D	0x44 BUS1
5	VCC_PSFP	0.88	4	U167 C	0x4C	0x45 BUS1
6	VCC_SOC	0.80	25	U152 L2, U153	0x46	0x41 BUS1
7	VCCAUX	1.50	4	U167 D	0x4C	0x40 BUS1
8	VCCAUX_PMC	1.50	1	U167 B	0x4C	0x41 BUS2
9	VCCO_MIO	1.80	2	U279 D	0x48	0x45 BUS2
10	VCCO_502	1.80	1	U175 B	0x4D	0x47 BUS2
11	VCC1V1_LP4	1.10	6	U279 A, U292	0x48	0x49 BUS2
12	VCC1V5	1.50	2	U279 B	0x48	0x43 BUS2
13	VADJ_FMC	1.50	6	U282	0x4E	0x4A BUS2
14	LPDMGTYAVCC	0.92	4	U279 C	0x48	0x4B BUS2

Rail	Rail Name	Nominal Voltage (V)	Max Current (A)	Device	PMBUS Addr	INA226 Addr
15	LPDMGTYAVTT	1.20	6	U167 A, U316	0x4C	0x4C BUS2
16	LPDMGTYVCCAUX	1.50	0.5	U175 LDO	0x4D	0x4D BUS2
17	MGTAVCC	0.92	4	U160 D	0x47	0x42 BUS2
18	MGTAVTT	1.20	6	U295	0x49	0x46 BUS2
19	MGTVCCAUX	1.50	0.5	U160 LDO	0x47	0x48 BUS2
20	VCCO_HDIO_3V3	3.3	2	U175 A	0x4D	0x46 BUS1
21	UTIL_1V8	1.80	2	U354	0x4F	N/A
22	UTIL_2V5	2.50	2	U160 B	0x47	N/A
23	UTIL_1V0	1.00	0.4	U167 LDO	0x4C	N/A

✎ **Note:** Bus short names are decoded as:

- I2C Address – PMBUS_SDA/SCL
- BUS1 - PMBUS1_INA226_SDA/SCL
- BUS2 - PMBUS2_INA226_SDA/SCL

See PMC MIO[46:47] I2C0 Bus for I2C diagrams and more details.
The FMCP HSPC (J51) VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.50V by default. The VADJ_FMC rail also powers the XCVE2802 FMCP interface banks 709 and 710 (see the table in I/O Voltage Rails). Documentation describing PMBus programming for the Infineon power controllers is available on the Infineon Integrated Circuits website. The PCB layout and power system design meet the recommended criteria described in the *Versal Adaptive SoC PCB Design User Guide* (UG863).

Table: Power System – Non-PMBus Regulators

Rail Name	Regulator Type	Ref. Des.	Vout (V)	Iout (A)
VCC12_SW		SW13	12	Up to 50A
UTIL_3V3	IR3889	U190	3.3	12
UTIL_5V0	IR3889	U191	5	6
SYS_VCC0V85	TPS62480	U143	0.85	5
SYS_MGTAVCC	TPS62097RWKR	U146	0.9	1
SYS_VCC1V1	TPS7A8300ARGRR	U145	1.1	1
SYS_VCC1V2	TPS62097RWKR	U147	1.2	2
SYS_VCC1V8	TPS62097RWKR	U144	1.8	1

Note: VCC12_SW is disabled when using ATX 12V (6+2) input. Refer to the description in the Power On/Off Slide Switch introduction.

More information about the power system regulator components can be found at the Infineon Integrated Circuits website.

Monitoring Voltage and Current

Nineteen rails have a TI INA226 PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA226 to report the sensed parameters separately on the PMBus. The rails equipped with the INA226 power monitors are shown in the power system table in Board Power System. As described in PMC MIO[46:47] I2C0 Bus, the I2C0 bus provides access to the PMBus power controllers and the INA226 power monitors via the U33 TCA9548A bus switch. All PMBus controlled Infineon regulators are tied to the PMBUS_SDA/SCL PMBus, while the INA226 power monitors are split across PMBUS1_INA226_SDA/SCL and PMBUS2_INA226_SDA/SCL.
The I2C0 bus topology figure and I2C0 port expander TCA6416A U233 address `0x20` connections table in PMC MIO[46:47] I2C0 Bus document the I2C0 bus access path to the Infineon PMBus controllers and INA226 power monitor op amps. For connectivity details, see the schematic, which can be accessed through the VEK280 Evaluation Board website. These power system components are also accessible to the ZU4 U125 system controller (bank 501) and the Versal device U1 (bank 501).

VITA 57.4 FMCP Connector Pinouts

Overview

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification. For a description of how the VEK280 evaluation board implements the FMCP specification, see GTYP200/201: FPGA Mezzanine Card Interface.

Figure: FMCP HSPC Connector Pinout

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

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Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the VEK280 board provides for designs targeting the VEK280 evaluation board. Net names in the constraints listed correlate with net names on the latest VEK280 evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL.
See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.
The HSPC FMCP connector J51 is connected to the AMD Versal™ device U1 banks powered by the variable voltage VADJ_FMC. Because different FMC cards

implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer. See LPD MIO[23]: VADJ_FMC Power Rail for more details on the VADJ_FMC power rail.

Important: See the VEK280 board documentation ("Board Files" check box) for the XDC file.

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.
For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*
2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*
EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*
EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings

In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life. AMD has met its national obligations to the EU WEEE Directive by registering in those countries to which AMD is an importer. AMD has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.
If you have purchased AMD-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. AMD has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Finding Additional Documentation

Documentation Portal

The AMD Adaptive Computing Documentation Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Documentation Portal, go to https://docs.xilinx.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select Help > Documentation and Tutorials.
- On Windows, click the Start button and select Xilinx Design Tools > DocNav.
- At the Linux command prompt, enter `docnav`.

Note: For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the Design Hubs View tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

The most up to date information related to the VEK280 board and its documentation is available on this website:
VEK280 Evaluation Kit
VEK280 Evaluation Kit — Answer Record 000034937
These documents provide supplemental material useful with this guide:

1. *Versal Architecture and Product Data Sheet: Overview* (DS950)
2. *Versal Premium Series Data Sheet: DC and AC Switching Characteristics* (DS959)
3. *Versal Adaptive SoC Technical Reference Manual* (AM011)
4. *Versal Adaptive SoC SelectIO Resources Architecture Manual* (AM010)
5. *Versal Adaptive SoC PCB Design User Guide* (UG863)
6. *Versal Adaptive SoC Memory Resources Architecture Manual* (AM007)
7. *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002)
8. *VEK280 System Controller Tutorial* (XTP766)
9. *Tera Term Terminal Emulator Installation Guide* (UG1036)
10. *Vivado Design Suite User Guide: Using Constraints* (UG903)
11. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
12. *Versal Adaptive SoC System Monitor Architecture Manual* (AM006)
13. *Versal Adaptive SoC Clocking Resources Architecture Manual* (AM003)
14. *Versal Adaptive SoC GTM Transceivers Architecture Manual* (AM017)
15. Micron Technology (MTA9ADF1G72AZ-3GE1, MT53E512M32D1ZW)

16. Standard Microsystems Corporation (SMSC) (USB3320)
17. SanDisk Corporation
18. SD Association
19. Texas Instruments (TCA9548A, TCA6416A, DP83867, PCA9306)
20. PCI-SIG
21. Samtec, Inc. (SEAF series connectors, LPAF connectors)
22. VITA FMC Marketing Alliance (FPGA Mezzanine Card (FMC) VITA 57.1, 57.4 specifications)
23. Maxim Integrated Circuits (MAX6643)
24. Infineon Integrated Circuits (IR35215, IRPS5401, IR38164, IR3897)
25. Future Technology Devices International Ltd. (FT4232HL)
26. Integrated Device Technology, Inc. (IDT) (8A34001, RC21008A)
27. NXP Semiconductors (NVT4857UK)
28. Versal Evaluation Board - System Controller BEAM Wiki
29. Analog Devices

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
1/31/2024 Version 1.1	
Jumpers	Revised default value for J395, J396, J397, J398, J400, and J401.
1/22/2024 Version 1.0	
Initial release	N/A

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