Introduction

This application note will demystify some important jitter units used in quantifying clock jitter for high-speed applications. While the voltage and current parameters of a clock device are well understood, the units of timing jitter can lead to confusion. This is because there is no universally accepted definition of jitter for all applications.

Jitter can have units in the time and frequency domains; sometimes peak-to-peak values are stated, while other times RMS jitter is given. When datasheets for competing timing products use different units, it can prove challenging to do side-by-side performance comparisons.

This note will focus on the most common jitter units used today and describe the relationships between them. Much of the math and equations have been simplified. This note will focus on the reader's ability to:

- Compare the jitter performance of various timing products even when different units are used (e.g. RMS jitter versus peak-to-peak jitter).
- Relate the datasheet jitter parameters for a clock generator or transceiver to the application jitter specification (e.g. PCIe Gen3, Gigabit Ethernet etc).
- Appreciate the relationship between jitter and phase noise.

What is Jitter and Phase Noise?

Phase noise and jitter are different ways of quantifying the same phenomenon: signal timing error. In the time domain, common jitter measurements are *period jitter*, *cycle-to-cycle jitter* and *accumulated jitter*. Among these types of jitter, **period jitter** (see Figure 1 below) is generally given in datasheets.

In the frequency domain, oscillator quality is characterized by *phase noise* measurements which examine the spectrum of side-band noise frequencies in a clock signal. To keep things simple, assume that the ideal clock is a perfect sine wave with a frequency F_C. Such a pure clock will have all its power concentrated at F_C (see Figure 2). The effect of phase noise is to spread the power into sidebands causing slight variations in frequency. So that instead of the oscillator always producing a pure clock signal at FC, it is sometimes a bit faster: $F_C + \Delta f$, or sometimes a bit slower: $F_C - \Delta f$ (see Figure 3). These small changes in clock speed translate into jitter in the time domain.

Various random and deterministic noise sources in an electrical system cause jitter. For an excellent explanation of the types and components of jitter, please refer to the white paper IDT_Jitter-Timing_WHP_20080901. This guide will focus on explaining those unusual jitter and phase noise units seen in high performance timing specifications.

Figure 1. Jitter in the Time Domain
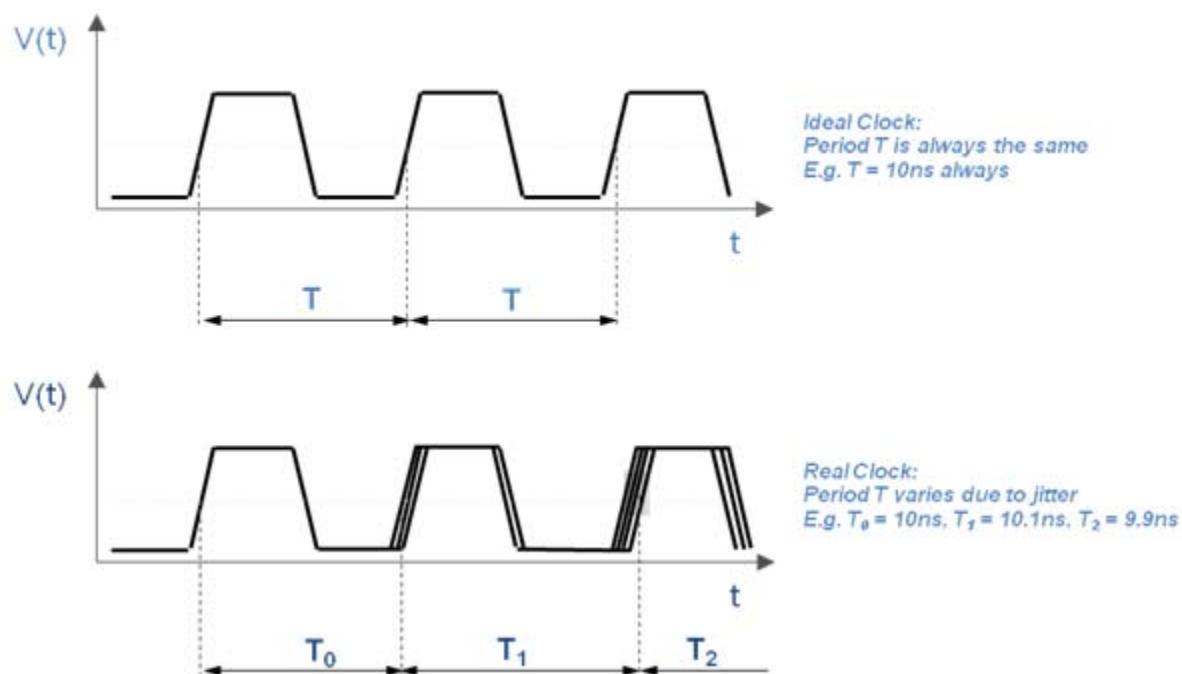
**Figure 2. Jitter in the Frequency Domain – Phase Noise**

Spectrum of Perfect Clock

$V(t) = A \sin(2\pi F_C t)$
Power concentrated in single infinitely
thin line at F_C on graph
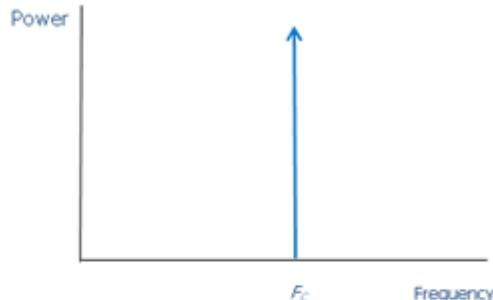
Real-World Clock

$V(t) = [A + a(t)]\sin[2\pi F_C t + \Delta\phi(t)]$
$a(t)$ is random variation of signal amplitude
$\Delta\phi(t)$ is random variations of signal phase,
usually called *phase noise*. In oscillators $\Delta\phi(t)$
is the dominant contributor to jitter.
Phase noise broadens the signal spectrum
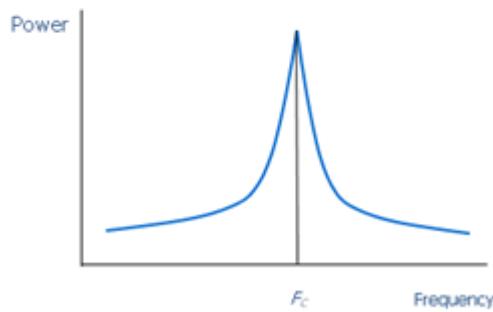
Figure 3. Vector Representation of Phase Noise

Phasor Diagram of Perfect Oscillator

Carrier vector rotates at a constant frequency F_c

Perfect Oscillator (Carrier Vector)

F_c

Rotating noise vector V_N
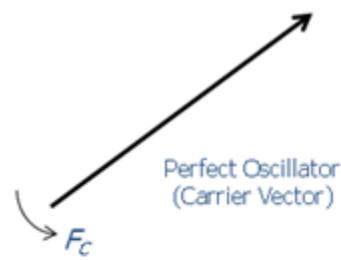
Phasor Diagram showing phase noise $\Delta\phi$ caused by a noise vector V_N

The solid black line is the original carrier vector in its ideal position.
The dotted red lines show how the rotating noise vector can displace the carrier vector from its ideal position causing phase noise.
Resultant signal (Carrier + Noise) has a modulated frequency.

$\Delta\phi$

Carrier + Noise

$F_c +/- \Delta f$
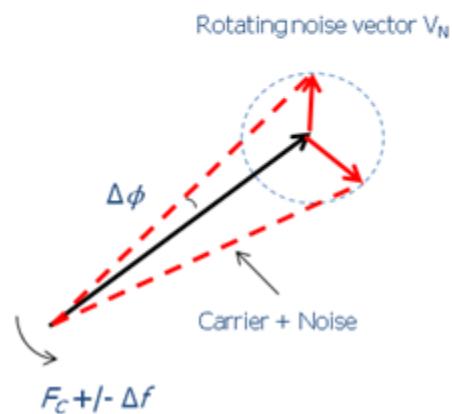
Quantifying Jitter in the Time Domain

Total jitter (TJ) equals the sum of deterministic jitter (DJ) plus random jitter (RJ). Common sources of deterministic jitter are cross-talk and simultaneous outputs switching. The peak-to-peak value of DJ is finite and can be minimized by careful design (e.g. good PCB routing).The effect of DJ is to add an offset to the value of RJ.

Random jitter (usually due to thermal noise and other uncorrelated noise sources) is unpredictable and typically follows a Gaussian or Normal distribution (see Figure 4). It is highly process dependent. Unlike DJ, the peak-to-peak value of RJ is unbounded; the more samples measured, the wider the variation of RJ_{pk-pk} observed (see Figure 5).

**Figure 4.   Gaussian Distribution Reveals Random Nature of Period Jitter**
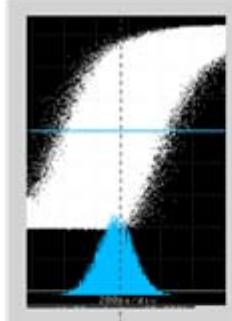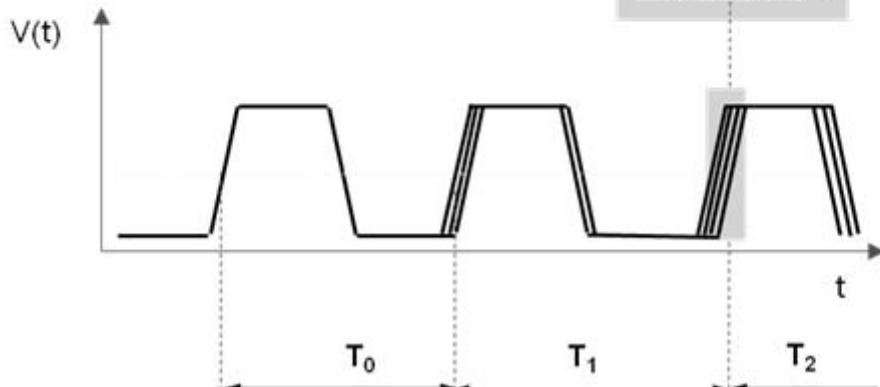
Figure 5.   Random Jitter is Unbounded. The Peak-to-Peak Value of Jitter Depends on the Number of Samples.
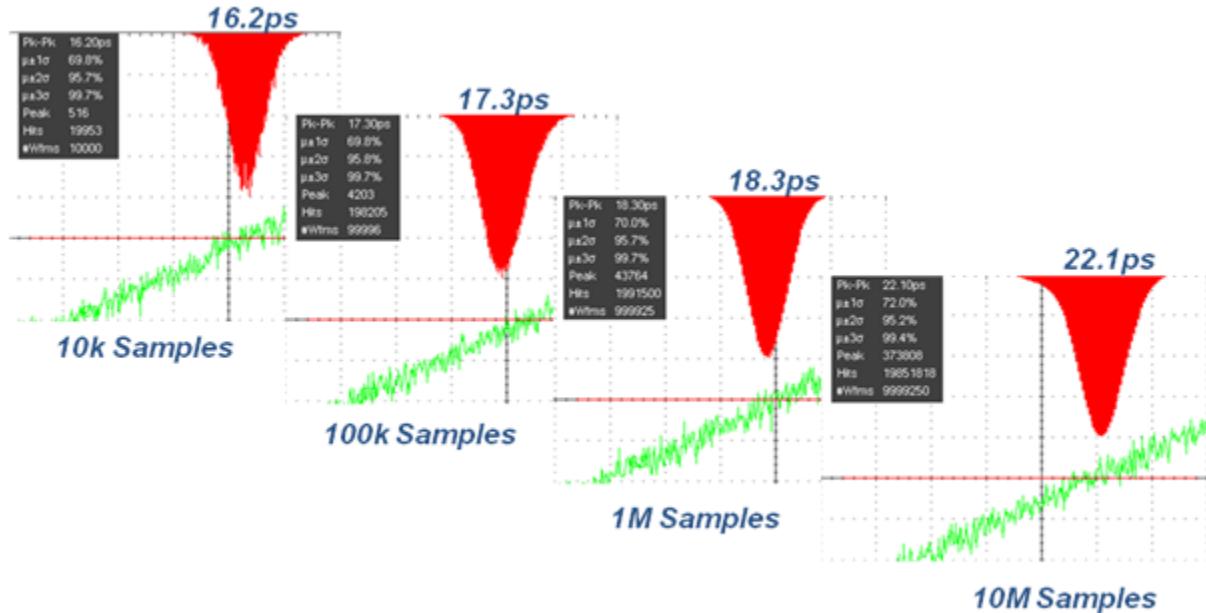
Two Ways of Quantifying Random Jitter: RMS and Peak-to-Peak

Period jitter is the short term variation in clock period compared to the average (mean) clock period. If the average or reference period is To (see Figure 1 above), then we take samples of period jitter as $T_1 - T_o$, $T_2 - T_o$, $T_3 - T_o$, ... and so on until we reach 10,000 samples (JEDEC standard JESD65B).

Plotting these jitter samples as a histogram may well result in a Normal distribution (see Figure 6).

Figure 6.   Gaussian (Normal) Distribution

1σ = standard deviation = RMS jitter. Mean value = μ
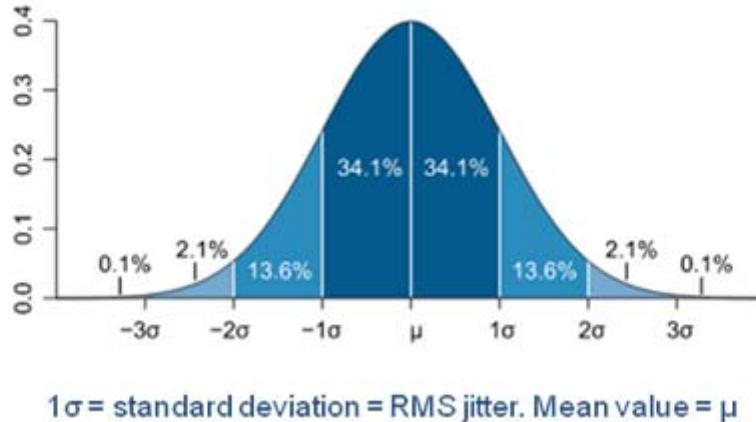
Ideally the mean value μ of jitter is zero. Values to the left of μ represent clock periods smaller than the reference period, and values to the right are larger than the reference clock period.

One standard deviation 1σ each side from μ (dark blue) accounts for about 68% of the jitter samples. While $\pm 2\sigma$ from μ (medium and dark blue) account for about 95%, and $\pm 3\sigma$ (light, medium, and dark blue) account for about 99.7%.

The Normal distribution yields two common jitter specifications:

- **Root Mean Squared** jitter (RJ_{RMS}) or the value of one standard deviation σ. Since this value hardly changes as the number of samples increases, it is considered a more meaningful measurement. However it is only valid in pure Gaussian distributions (no deterministic jitter).

- **Peak-to-peak** jitter or the distance from the smallest to the largest measurement on the normal curve. In most circuits this value increases with the number of samples taken (see Figure 5). To arrive at a meaningful value of peak-to-peak jitter, the bit error ratio (BER) also needs to be specified.

How RMS Jitter Relates to Peak-to-Peak Jitter and BER

In Figure 6, we can see that inside a peak-to-peak range of 6σ ($\pm 3\sigma$ from the mean) or $6 \times RJ_{RMS}$, about 99.7% of jitter samples are accounted for. To account for 100% of the jitter samples is impossible - the tales of the Gaussian distribution stretch to infinity. What decides that the peak-to-peak jitter is $6 \times RJ_{RMS}$, or $7 \times RJ_{RMS}$, or $12 \times RJ_{RMS}$?

A useful way to accomplish this is based on the bit error ratio (BER) required by the system. It is assumed that any samples that fall outside the peak-to-peak range will cause bit errors. Therefore, if a BER target of 10^{-12} is demanded, it is necessary to select a range that will contain the jitter for all except 0.0000000001% of the time.

To convert from RMS jitter to peak-to-peak jitter using this method, simply multiply RJ_{RMS} by the value N corresponding to the appropriate BER in Table 1 below:

Table 1: BER and RMS Multiplier N

BER	N
10^{-3}	6.18
10^{-4}	7.438
10^{-5}	8.53
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069
10^{-113}	14.698
10^{-14}	15.301
10^{-15}	15.883
10^{-16}	16.444

For example RJ_{RMS} = 4ps, and the system BER requirement is 1 x 10^{-12}, the corresponding peak-to-peak jitter (rounded up) is:

$$RJ_{pk-pk} = 4 \times 14.069 = 56.4ps$$

This figure gives us an idea of the allowable jitter budget. Roughly speaking, if the various random jitter sources in a communication link add up to less than 56.4ps, then the bit errors should be less than 1 x 10^{-12}.

Predicted versus Measured Peak-to-Peak Jitter

Peak-to-peak jitter is often described in two ways:

- It can be calculated as shown previously using the RMS multiplier. This is predicted peak-to-peak jitter based on a defined BER (usually 1 x 10^{-12}).

- It can be measured using test equipment. In this case the minimum period sampled is subtracted from the maximum period measured. As we have seen before this will depend on how many samples are taken.

The predicted and measured values will not be the same. The measured value will give a feel for the jitter in the system, but is somewhat meaningless in relation to BER. For example, the peak-to-peak jitter measured from 10,000 samples will not tell you the peak-to-peak jitter needed for BER = 1 x 10^{-12}. You would need at least 1,000,000,000,000 samples to accomplish that! Therefore RJ_{pk-pk} is usually calculated from RJ_{RMS} at a defined BER.

Quantifying Jitter in the Frequency Domain: Phase Noise

As mentioned in the introduction, phase noise describes jitter in the frequency domain. Later we will see that, from the phase noise information, we can extract the RMS Phase Jitter value which is often given in datasheets as a measure of quality and spectral purity.

Figure 7. Constructing a Phase Noise Plot (from IDT white paper *RMS Phase Jitter*)
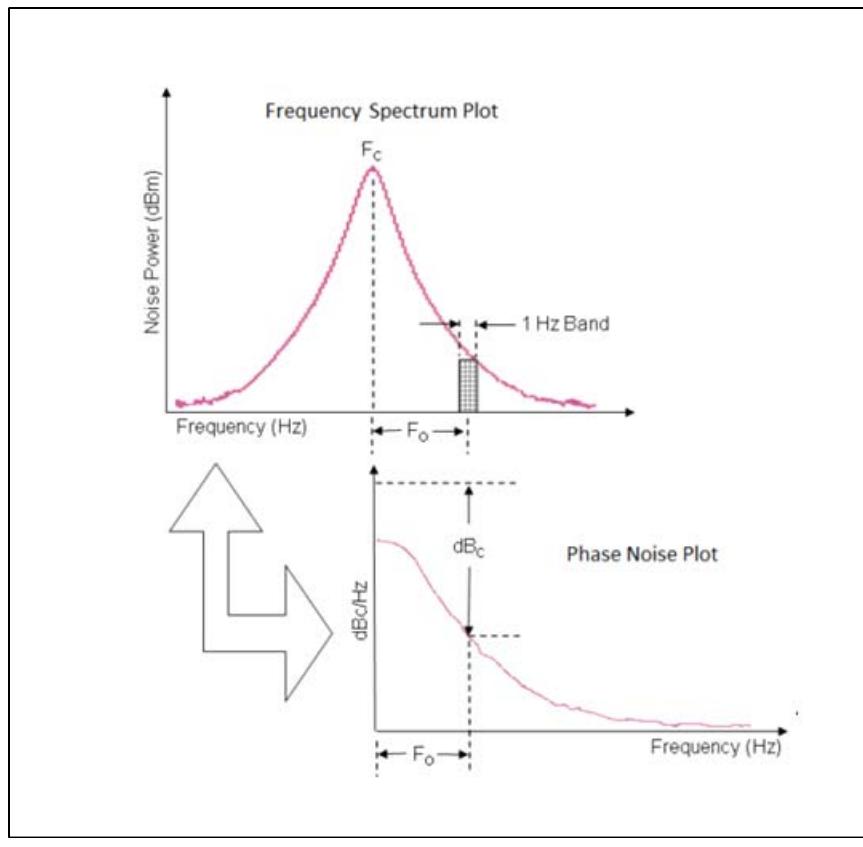
The frequency spectrum plot in Figure 7 is of a real sinusoidal clock with nominal frequency F_C (also called the **carrier** frequency) plus sideband offset noise frequencies F_O. That means, sometimes the clock will have a slightly larger frequency $F_C + F_O$ and sometimes it will have a slightly lower frequency $F_C - F_O$. The small changes in frequency appear as phase shifts in the clock waveform, hence the name phase noise.

The noise power in a 1Hz band at an offset frequency FO compared to the power of the carrier frequency F_C is called the **dBc Phase Noise** (dBc = power in dB relative to *carrier*).

$$\text{dBc Phase Noise} = \frac{\text{Power level of a 1Hz band at offset } F_O}{\text{Power level of carrier frequency } F_C}$$

The actual units of Phase Noise are dBc/Hz because the power is normalized to a 1Hz bandwidth.

Constructing a Phase Noise Plot

Referring to Figure 7 above, by sweeping a 1Hz band from the center of the Frequency Spectrum Plot to the right hand end of the frequency axis, the dBc power level can be calculated at each offset F_O. The resulting values are then plotted on a Phase Noise plot as shown in Figure 7. Table 2 below highlights the main differences between the Frequency Spectrum and Phase Noise plots. Figure 8 shows a typical oscillator phase noise plot.

Table 2: Differences between Frequency Spectrum and Phase Noise Plots

Frequency Spectrum Plot	Phase Noise Plot
Power levels are in absolute units dB	Noise power levels are relative to carrier, calculated in 1Hz bandwidths. Units are dBc/Hz.
Frequency axis shows all the frequencies in the signal	Frequency axis only shows the offset (sideband) frequencies. For example, if $F_{CARRIER} = 25\text{MHz}$, then when the frequency is 25.01MHz: $F_{OFFSET} = 0.01\text{MHz} = 10\text{kHz}$
Carrier frequency is the nominal clock frequency	Offset frequency is the modulation rate of the clock (*because the clock is frequency modulated by the noise*).
	Single side – only one side of the spectrum is plotted. The assumption is that the noise profile is symmetrical.

Figure 8. Phase Noise Plot of a 311MHz Oscillator (from Thomas Fischer TI). Offset (modulation) Frequencies are shown on a Logarithmic Scale.
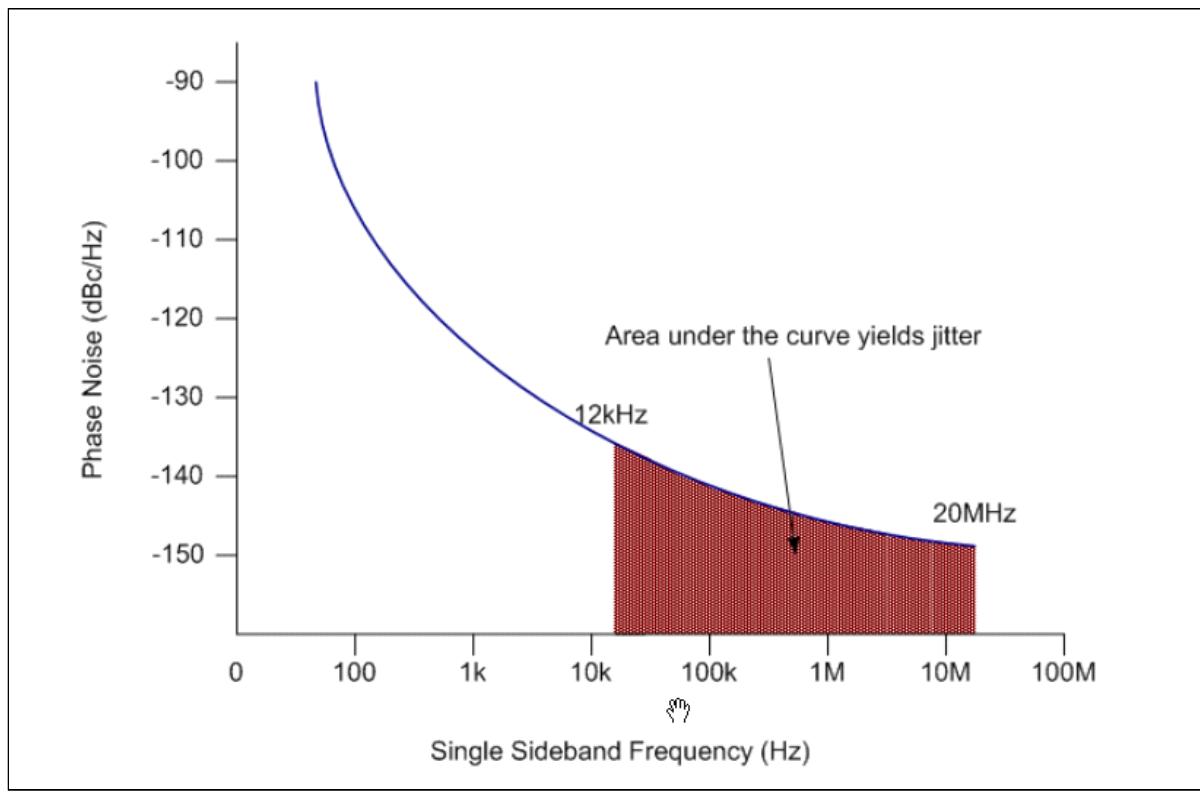
RMS Phase Jitter

When looking at oscillator phase noise plots, certain sideband frequency ranges are of interest. In telecommunications, the noise power in the range 12kHz to 20MHz is very important for timing performance. Referring to Figure 8 above:

Noise Power (dBc) = Area under curve from 12kHz to 20MHz = -63dBc

From the noise power **N** we can calculate the RMS phase jitter value in radians using the following formula:

$$\text{RMS Phase Jitter (radians)} = 2 \times \sqrt{10^{N/10}}$$

$$\text{RMS Phase Jitter} = 2 \times \sqrt{10^{-63/10}} = 0.001416 \; radians$$

The jitter value in radians can be converted to RMS jitter in time units of seconds:

$$\text{RMS Jitter (secs)} = \frac{Jitter\,(radians)}{2 \times \pi \times f}$$

In this example, the oscillator frequency f = 311MHz. So we get:

$$\text{RMS Jitter} = \frac{0.001416}{2 \times \pi \times 311MHz} = 0.72 \; pico \; seconds \; RMS$$

When jitter is derived from phase noise plots, the sideband frequency interval over which it is calculated must always be specified.

Summary

This note has described the following:

- How RMS jitter (time domain) is quantified based on standard deviation of a Gaussian distribution.
- How peak-to-peak jitter (time domain) can be predicted from the RMS jitter using multipliers related to BER requirements.
- How RMS phase jitter in frequency domain is calculated using phase noise plots.

The following appendix gives examples of how to check jitter specifications and system requirements.

Appendix: Checking Jitter Specifications and System Requirements

Example 1: Based on the FPGA specifications below, is it possible to use the clock output from the StratixV to clock a Broadcom 1GE Phy?

Phy clock input specified at 1.5ps RMS max.

Altera FPGA	PLL Type	Input Frequency	PLL BW	Output Frequency Range	Jitter
StratixV E, GX, GS, GT	Fractional or Integer VCO 600-1300/1600MHz (speed grade dependent)	Min 5 MHz Max 650 MHz to 800 MHz (speed grade dependent)	From 300KHz to 4MHz	Max from 553 MHz to 800 MHz (speed grade dependent)	Max from Dedicated Clock Output: 175ps to 250ps max pk-pk jitter Max from GPIO: 600ps max pk-pk jitter

The BER requirement for 1GE (gigabit Ethernet) is 1×10^{-12}. From Table 1 previously (*BER and RMS Mutliplier N*), pk-pk jitter is approximately equal to 14 x RMS jitter. Therefore we have:

StratixV jitter (min) = 175/14 = **12.5ps RMS**

StratixV jitter (max) = 250/14 = **17.9ps RMS**

As can be seen this is much larger than can be tolerated by the Broadcom Phy, and another clock source will be required.

Example 2: Can the StratixV clocks be used to provide timing for PCIe Gen2 systems?

PCIe Gen2 Clock Requirements

Transmitter REFCLOCK Phase Noise (622MHz)	100Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLOCK Phase Jitter (100MHz)	10kHz to 1.5MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)

- PCIe Gen2 100MHz reference clock is **3ps** RMS jitter max from 10KHz to 1.5MHz.
- The 622.08MHz TX reference clock is **1.44ps** RMS jitter max from 100Hz to 1MHz.

From the previous example, best case, the internal PLLs of the StratixV generate a clock with max RMS jitter of **12.5ps**.

As the reference clocks of the StratixV transceivers require 1.44ps or 3ps in the above examples, the internal StratixV PLLs are not able to clock them.

Sources

Figure 4 and Figure 5 are from an internal IDT training presentation ***Jitter - Theory and Measurements*** by Alberto Urbieta

Figure 7 is from an IDT white paper ***RMS Phase Jitter*** by Alberto Urbieta

Figure 8 is from the paper titled ***Phase Noise and Jitter Characterization in Oscillator Applications*** by Thomas Fischer at Texas Instruments

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