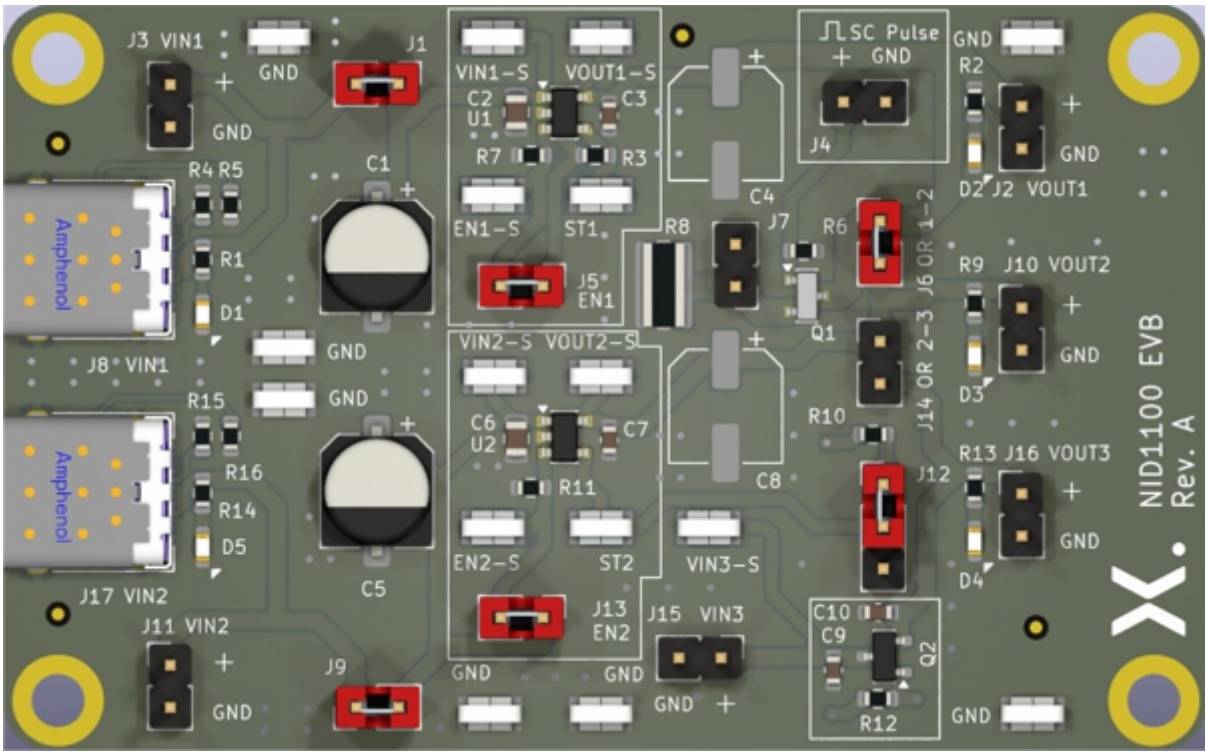
UM90044

Rev. 1 — 17 January 2025

user manual

NID1100, 1.5 V to 5.5 V, 1 A, ideal diode with forward voltage blocking evaluation board



Abstract: The NEVB-NID1100 evaluation board is a two-layer PCB equipped with two NID1100 ideal diodes and one PMOS transistor. It allows users to explore the device's behavior under various application conditions.

Keywords: Ideal diode, Schottky replacement, OR-ing, evaluation board (EVB), forward voltage blocking, power multiplexing

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1. Introduction

The NID1100 is a low-forward voltage integrated ideal diode, designed to replace traditional diodes in low-voltage systems that cannot tolerate the high voltage drops of conventional rectifier components. This device supports a continuous current of 1 A and operates over an input voltage range of 1.5 V to 5.5 V. Unlike standard diodes, it offers forward voltage and reverse current blocking, short-circuit protection, controlled inrush current and thermal protection.

This evaluation Printed Circuit Board (PCB) incorporates two NID1100 ideal diodes and one PMOS transistor, enabling the assessment of performance and behavior across various use cases, such as OR-ing and OR-ing with an external PMOS transistor. The NEVB-NID1100 offers convenient access to multiple power supply inputs, as well as probe hook-ups for evaluation. Additionally, it includes an NMOS transistor at the output to test short circuit behavior.

2. Evaluation board key parameters

- Input operating voltage range (V_{IN}) 1.5 V to 5.5 V
- Continuous output current 1 A
- Three supply inputs V_{IN1}, V_{IN2}, V_{IN3}
- Two optional USB-C supply inputs for V_{IN1} and V_{IN2}
- Access to all device pins
- Use case selection by means of jumpers
- Short circuit testing

3. Schematic

Fig. 1 shows the schematic of the NEVB-NID1100UL evaluation board. Explanation of the test pins, jumpers and other features can be found in the next sections.

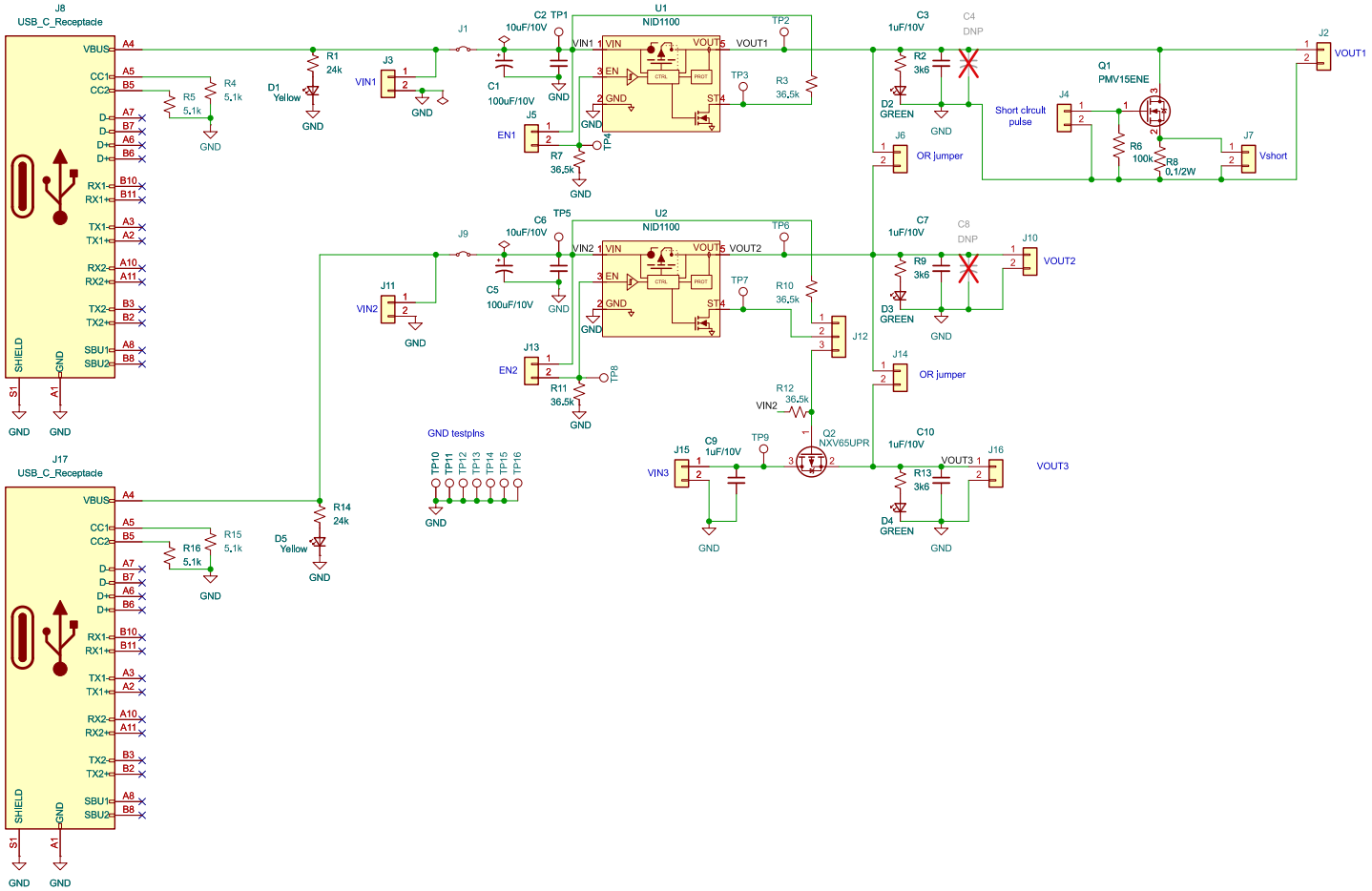

Fig. 1. NEVB-NID1100UL EVB schematic

4. PCB layout

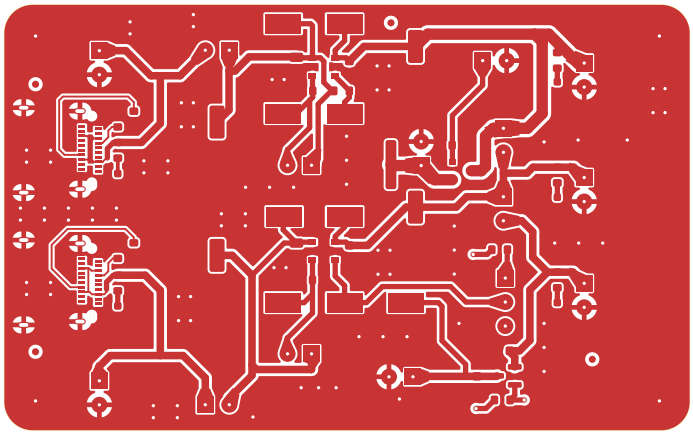

Fig. 2. NEVB-NID1100UL EVB top copper layer

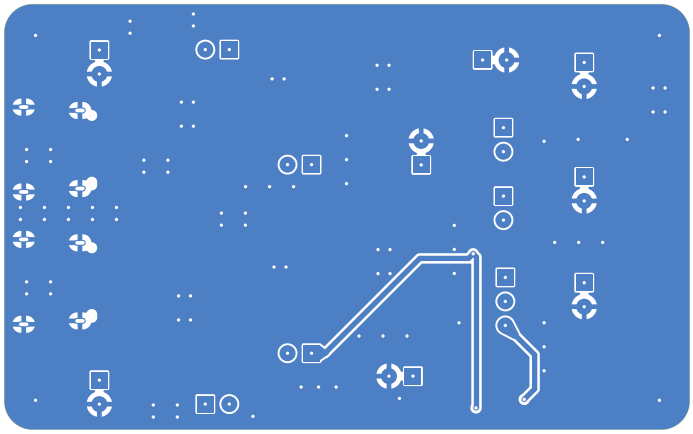

Fig. 3. NEVB-NID1100UL EVB bottom copper layer

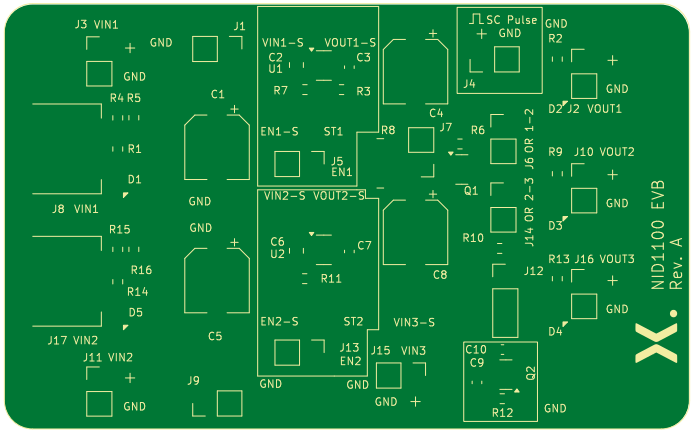

Fig. 4. NEVB-NID1100UL EVB silkscreen top layer

5. Bill of material

Table 1. Bill of Material (BOM)

Reference	Quantity	Value	Manufacturer	Component
C1, C5	2	100 µF/10 V	KEMET	EDK107M010A9GAA
C2, C6	2	10 µF/10 V	Murata Electronics	GRM21BR71A106KA73L
C3, C7, C9, C10	4	1 µF/10 V	KEMET	C0603C105K8RACTU
C4, C8	2	DNP	DNP	DNP
D1, D5	2	Yellow	Kingbright	APTD1608LSYCK/J3-PF
D2, D3, D4	3	GREEN	Kingbright	APTD1608LCGCK
J1, J2, J3, J4, J5, J6, J7, J9, J10, J11, J13, J14, J15, J16	14	Conn_01x02	Wurth Elektronik	61300211121
J8, J17	2	USB_C_Receptacle	Amphenol Commercial Products	12401610E4#2A
J12	1	Conn_01x03	Wurth Elektronik	61300311121
Q1	1	PMV15ENE	Nexperia	PMV15ENER
Q2	1	NXV65UPR	Nexperia	NXV65UPR
R1, R14	2	24 kΩ	YAGEO	RT0603DRE0724KL
R2, R9, R13	3	3.6 kΩ	YAGEO	RT0603DRE073K6L
R3, R7, R10, R11, R12	5	36.5 kΩ	KOA Speer	RK73H1JTTD3652F
R4, R5, R15, R16	4	5.1 kΩ	Bourns	CR0603-FX-5101ELF
R6	1	100 kΩ	Vishay / Dale	CRCW0603100KJNEAC
R8	1	0.1 Ω/2 W	Vishay / Dale	RCWE1020R100FKEA
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	16	TestPoint	Keystone Electronics	5019
U1, U2	2	NID1100	Nexperia	NID1100GV
	6	Open Top Jumper Socket RED	Harwin	M7581-46

6. Quick start

The NEVB-NID1100 EVB is by default configured in the dual OR-ing application. When connecting the two USB-C ports to a supply (for instance two different USB ports on a PC), the input with the highest voltage will be available on connectors V_{OUT1} (J2) and V_{OUT2} (J10). One can disconnect either one of the supplies and observe that still an output voltage will be available.

7. Setup and operation

Fig. 5 depicts the location of available jumpers, supply and load connections.

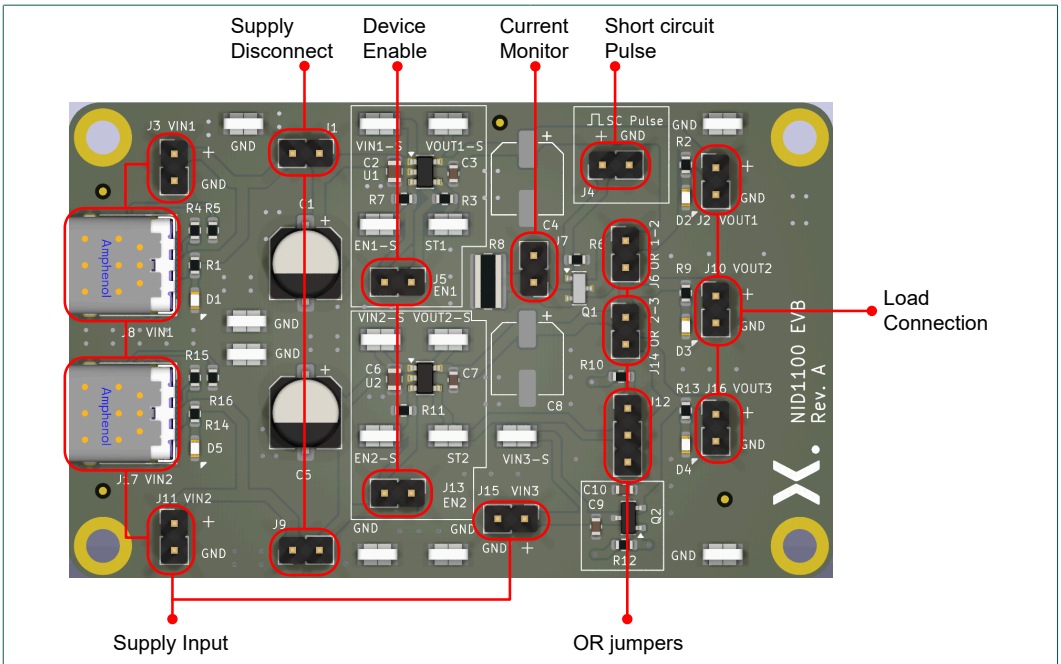

Fig. 5. NEVB-NID1100 EVB jumper positions and supply connections

There are multiple supply inputs available. Two USB-C ports (J8 and J17) and three headers (J3, J11 and J15). A yellow LED indicates the presence of an input voltage. Headers J3 and J11 are in parallel with USB-C port J8 and J17 respectively and can be used to connect a battery pack or lab supply.

Output voltages are available at J2, J10 and J16. If present a green LED will light up.

Jumpers J1 and J9 can be used to disconnect the NID1100 from the supply or measure the supply current.

Jumpers J5, J6, J12-J14 are used to set the following use cases described below.

Short circuit testing can be executed by applying a square wave pulse with an amplitude of 10 V_{PEAK} to J4. The voltage across R8 can be monitored to observe the current (10 A/V).

Both Table 2 and Table 3 summarize the usage of all jumpers and test points present on the NEVB-NID1100UL EVB evaluation board.

Table 2. Jumper settings

Jumper	Default position	Usage
J1	closed	• Disconnect V_{IN1} • Measure V_{IN1} supply current
J5	closed	• Enable U1
J6	closed	• OR V_{OUT1} - V_{OUT2}
J9	closed	• Disconnect V_{IN2} • Measure V_{IN2} supply current
J12	1-2	• 1-2 Connect U2 ST to V_{IN2} • 2-3 Enable Q1 by ST of U2
J13	closed	• Enable U2
J14	open	• OR V_{OUT2} - V_{OUT3}

Table 3. Test points and supply I/O's

Test point	Connected to
J2	Output 1 (V_{OUT1})
J3	External supply 1 (V_{IN1})
J8	USB-C supply 1 (V_{IN1})
J10	Output 2 (V_{OUT2})
J11	External supply 2 (V_{IN2})
J15	External supply 3 (V_{IN3})
J16	Output 3 (V_{OUT3})
J17	USB-C supply 2 (V_{IN2})
TP1	V_{IN} U1
TP2	V_{OUT} U1
TP3	Status indication U1
TP4	Enable U1
TP5	V_{IN} U2
TP6	V_{OUT} U2
TP7	Status indication U2
TP8	Enable U2
TP9	V_{IN3}

Table 4 shows a summary of the jumper settings for all use cases.

Table 4. Use case jumper settings

X=don't care

Use case	J1	J5	J6	J9	J12	J13	J14
Reverse Current Blocking	closed	closed	X	closed	1-2	closed	open
Single operation	closed	closed	open	open	X	X	X
Dual OR	closed	closed	closed	closed	1-2	closed	open
Dual OR with PMOS	X	X	open	closed	2-3	closed	closed

Reverse current blocking

Reverse current blocking remains active regardless of the device's enable state. This behavior can be confirmed by raising V_{OUT1} or V_{OUT2} typically 33 mV above V_{IN}. When reverse current blocking is engaged, the ST pin will be pulled low.

Single device operation

Fig. 6 illustrates the board setup for single-device operation. Fig. 7 shows the device's startup behavior. With V_{IN} (5 V) applied, as long as the enable signal remains below $V_{EN,LO}$ (0.4 V), forward voltage blocking is active, resulting in V_{OUT} = 0 V. When the enable signal crosses the $V_{EN,HI}$ threshold (1.2 V), the device enters the enabled state, and the output capacitor charges at a controlled slew rate until V_{OUT} equals V_{IN}.

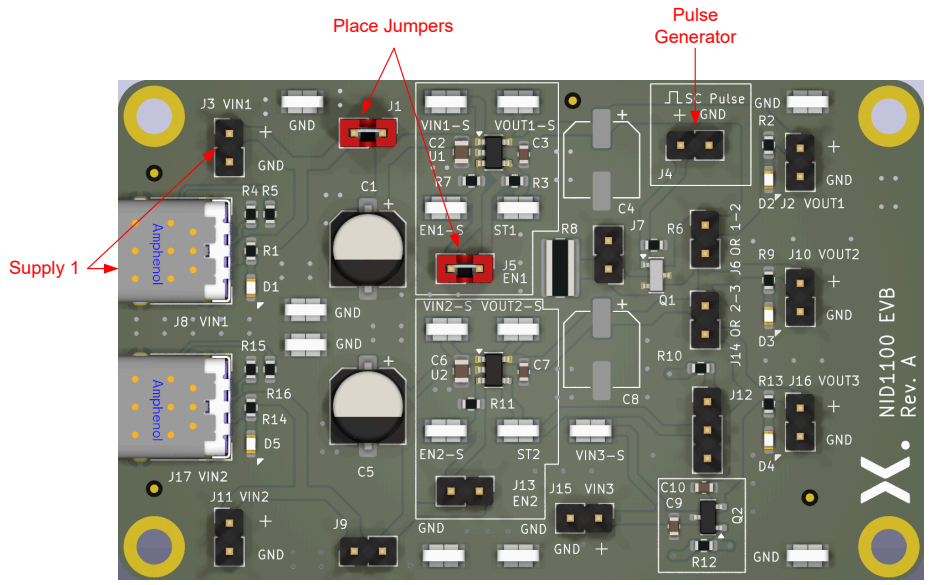

Fig. 6. Board setup for single device operation

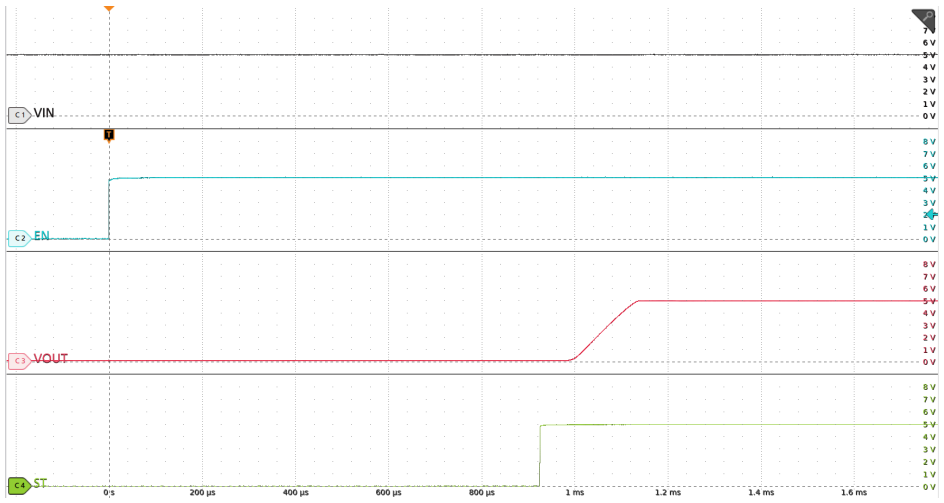

Fig. 7. Forward voltage blocking and inrush current control

In Fig. 8, the short circuit behavior of the device is shown. At t = 0 seconds, the short circuit FET is activated with a square wave pulse of 10 V_{PEAK}. The voltage across resistor R8 is monitored on channel 5, which indicates the output current of the device (10 A/V). When the device output current exceeds I_{LIM}, current limiting becomes active. If this short circuit condition persists, the device will protect itself by activating the over-temperature shutdown (T_{OTSD}) and disabling the pass-FET. When the die temperature falls below the hysteresis threshold, the FET is re-enabled until T_{OTSD} is triggered again.

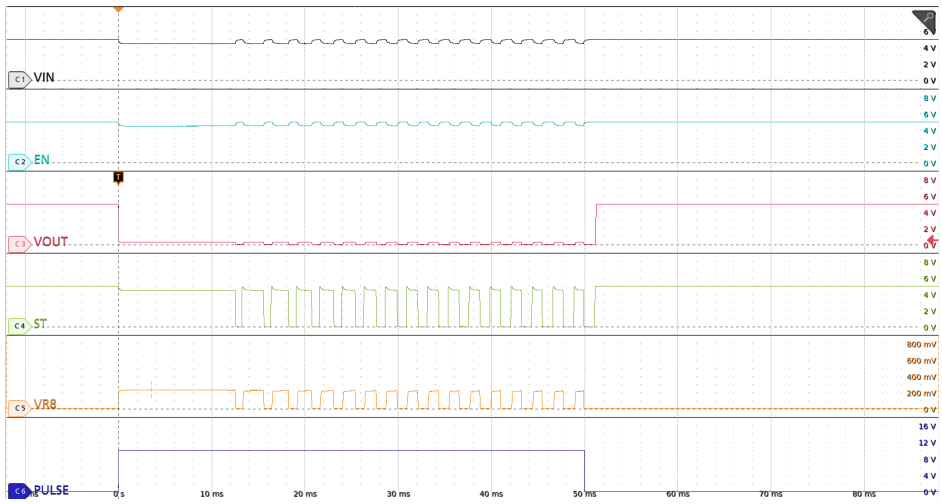

Fig. 8. Short circuit testing

Dual OR-ing

The NEVB-NID1100 evaluation board can be configured for OR-ing between V_{IN1} and V_{IN2}. To do this, both U1 and U2 must be enabled and connected in parallel. Enable both devices by placing jumpers on J5 and J13, and connect them in parallel by placing a jumper on J6. You can monitor the device state by connecting the status pin of U2 to V_{IN2} using a jumper between J12 pins 1 and 2. The status pin of U1 is permanently connected through R3. The board setup and jumper configurations are illustrated in Fig. 9.

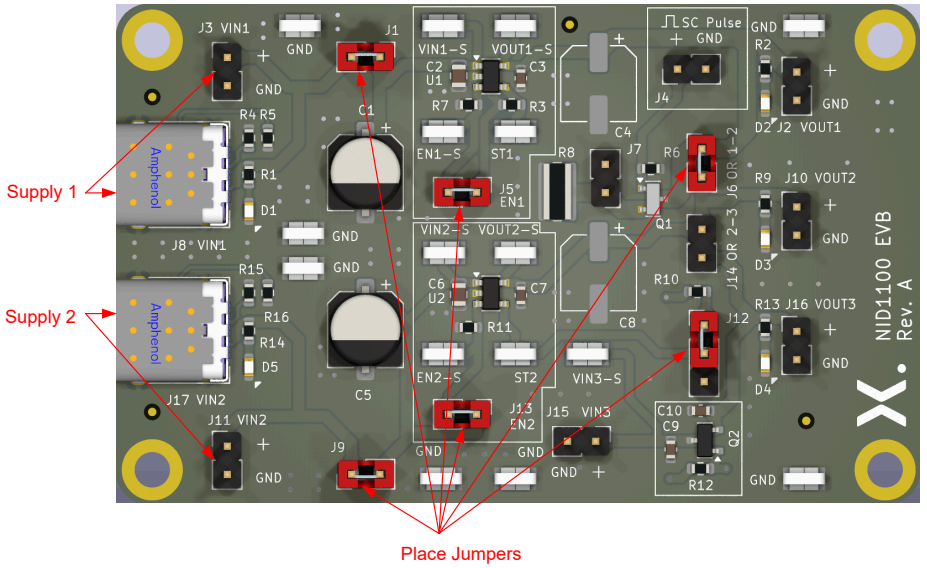

Fig. 9. Board setup for OR-ing supply 1 and supply 2

Fig. 10 shows the results when OR-ing two supplies. V_{IN1} has been connected to a 5 V source while V_{IN2} has been connected to a 3.3 V source. Initially V_{IN1} is supplying V_{OUT}. When V_{IN1} drops below V_{IN2}, V_{IN2} takes over. The status pins are active low when the device is disabled, hence one can see which device is enabled. If V_{IN1} rises again above V_{IN2}, the initial situation is restored.

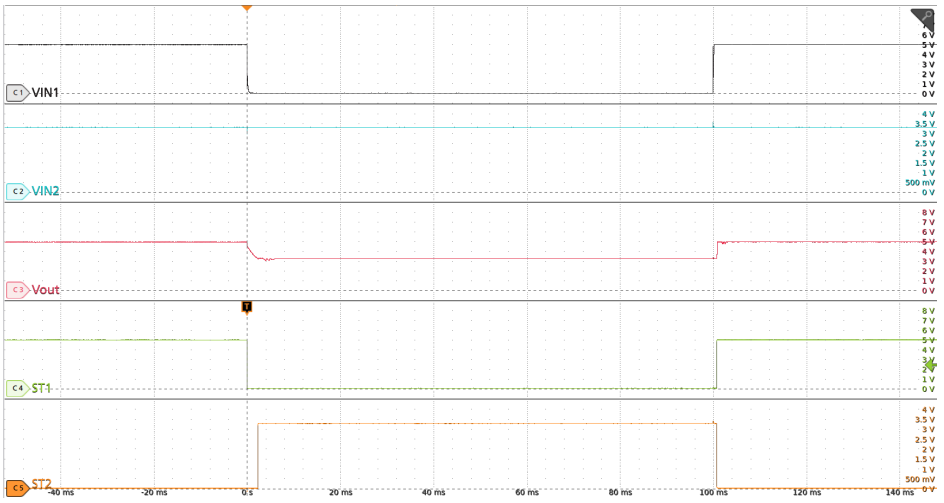

Fig. 10. Oscilloscope traces showing OR-ing between supply 1 and supply 2

OR-ing with external MOSFET

The evaluation board includes a PMOS transistor that facilitates ORing between V_{IN2} and V_{IN3} using one NID1100 at V_{IN2} and one PMOS in V_{IN3}, avoiding the use of two NID1100s. To configure this, place a jumper between pins 2 and 3 of J12, as well as a jumper on J14. Additionally, enable device U2 by placing a jumper on J13. When U2 is enabled, the ST output will be high-impedance, and the pass FET will remain non-conductive until V_{IN3} exceeds V_{IN2}.

Once V_{IN3} surpasses V_{IN2} by more than the MOSFET threshold voltage (V_{TH}), the MOSFET will begin conducting. At this point, U2's reverse current block activates, driving the ST pin low and ensuring full conductivity of the PMOS transistor. The board configuration is illustrated in Figure 11

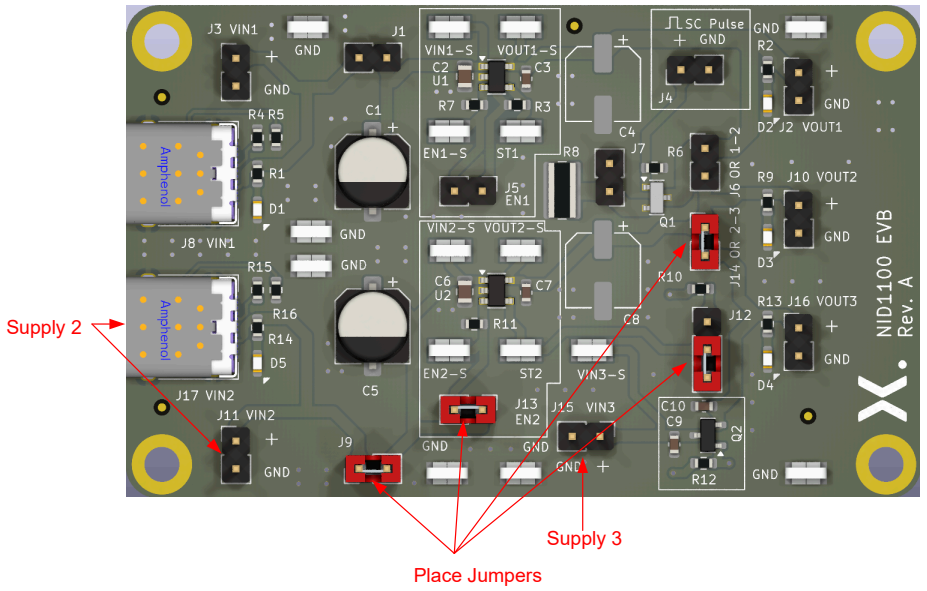

Fig. 11. Board setup for OR-ing supply 2 and supply 3 using a PMOST

Fig. 12 below shows the results when OR-ing using the PMOS transistor between 5 V and 3.3 V.

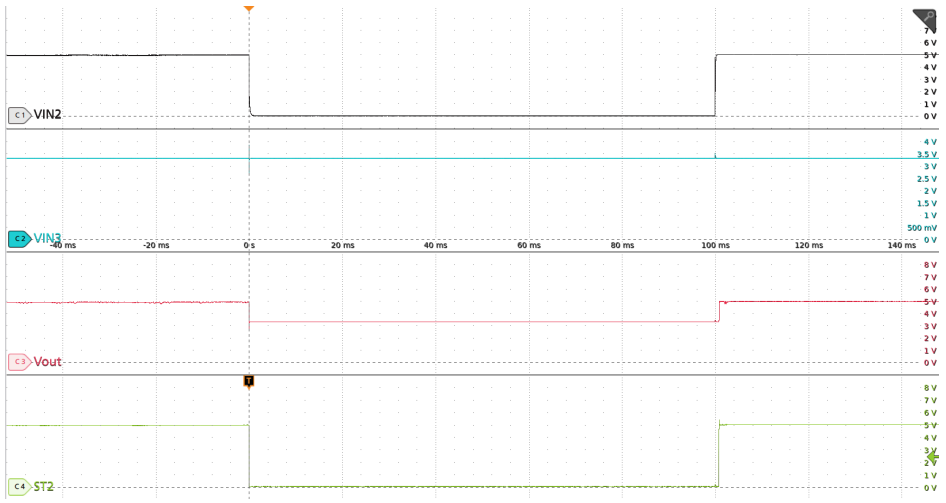

Fig. 12. OR-ing supply 2 and supply 3 using a PMOS transistor

8. Revision history

Table 5. Revision history

Revision number	Date	Description
UM90044 v.1	20250117	Initial version

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