USER GUIDE

UG521: Si82Ex-Fx Isolated Gate Driver Evaluation Board User Guide

Introduction

This user guide covers a range of Si82Ex-Fx EVB options. The Si82Ex-Fx evaluation board (EVB) is designed to evaluate and test the functionality and performance of Skyworks series of Si82Ex-Fx isolated gate drivers. The EVB can be used in standalone mode with an oscilloscope and the on-board dummy capacitive load, or it can be connected to a switch mode power supply (SMPS) controller and external power MOSFETs to conduct a system level evaluation.

The Si82Ex-Fx dual-channel isolated gate drivers feature variable current drive (VCD) and universal input in WB SOIC14 (6 kV_{RMS} isolation), NB SOIC16 (3.75 kV_{RMS} isolation), and LGA13 (2.5 kV_{RMS} isolation) packages.

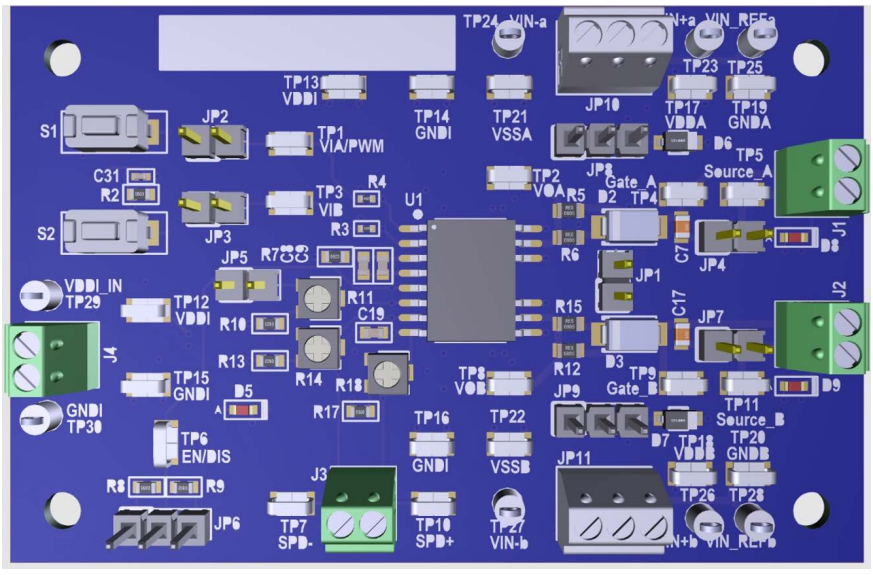
The VCD feature (only available on Si82Fx) allows adjustment of the rising/falling edge driving strength to eliminate external gate resistors. The chip also integrates input signal overlap protection and dead time insertion to simplify controller complexity.

In systems where the controller handles overlap protection and dead time control, the Si82Ex-Fx EVB universal input feature allows the chip to work as two independent drivers in any high-side + high-side, low-side + low-side, or high-side + low-side topologies.

The EVBs cover a wide variety of Si82Ex-Fx series devices. However, some features are only available on certain EVBs, depending on the driver IC on the board.

Features

- VIA/VIB inputs or PWM input
- Dead time adjustment
- Input signal overlap protection
- Variable current drive (VCD) eliminates external gate resistors
- Universal input to support dual-driver operation
- 150 kV/µs common mode transient immunity (CMTI) performance
- Reverse polarity protection
- Various power supply schemes support unipolar and bipolar gate output voltages



1. Description

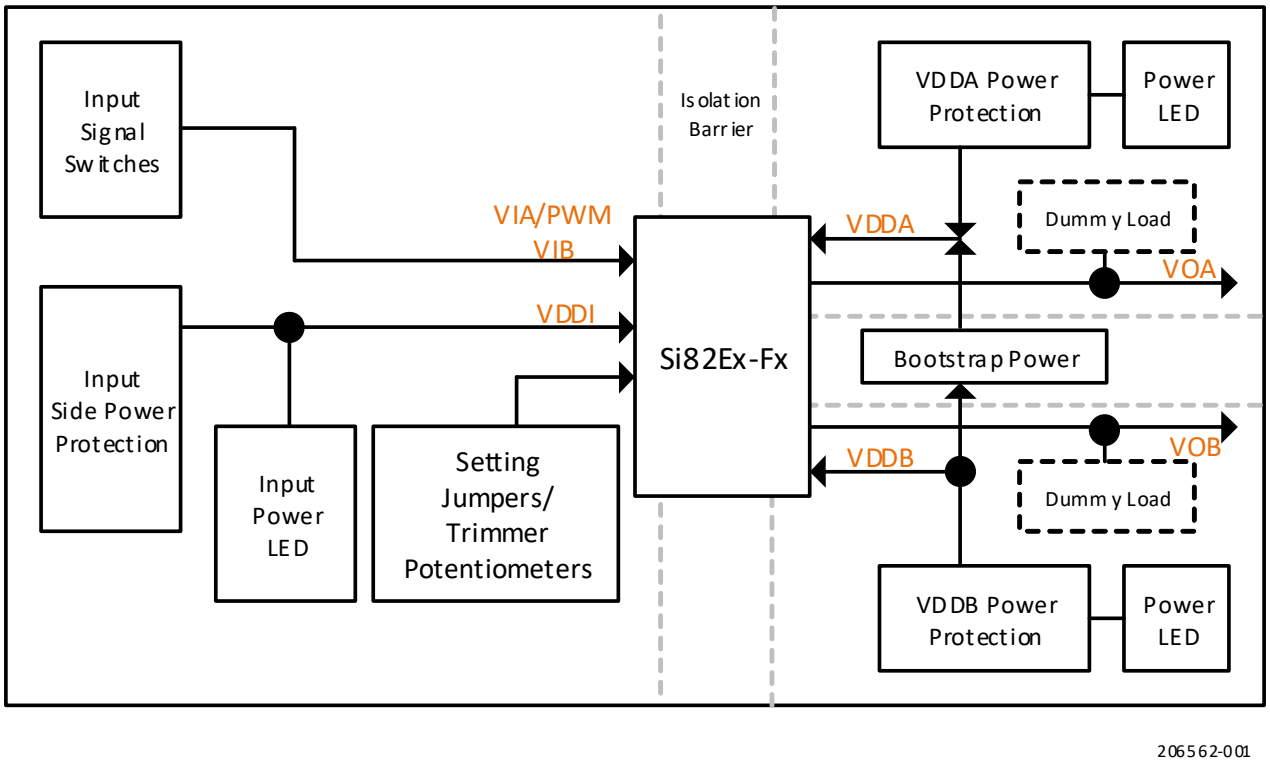


Figure 1. Si82Ex-Fx EVB Block Diagram

The EVB contains the Si82Ex-Fx chip, three power connectors, input signal connectors and switches, power supply circuit, dummy capacitive loads, two driver output connectors, setting jumper headers, setting trim potentiometers, the bootstrap power circuit, test points, and LED indicators.

The Si82Ex-FX EVB requires two to five bench power supplies and one dual-trace oscilloscope to operate in stand-alone mode. No software is required to operate the board.

The EVB can also be connected to an SMPS controller and external MOSFETs to perform a system-level evaluation.

Several different power schemes are supported. Based on the selected power scheme, the driver output voltage with respect to the MOSFET source terminal could be unipolar or bipolar. Unipolar output means the V_{GS} gate drive output toggles between 0 V and VDDA/B. In bipolar output, VGS toggles between positive and negative voltages.

Capacitive dummy loads are included at the driver output to demonstrate more realistic waveforms. The dummy load can be disabled by jumper shunts when the driver is connected to an actual MOSFET load.

2. Identify the Proper EVB Ordering Part Number (OPN)

Since there are many EVB variations, an EVB ordering part number (OPN) selection table is included below.

Table 1. Si82Ex-Fx EVB Ordering Part Number Selection Guide (EVB Labels)[1]

Ordering Part Number	Label	IC Part Number	Package	UVLO	VCD Outputs	On-board Dead Time Control	Input Type
Si82F39ABE-KIT	Si82F39ABE-EVB	Si82F39ABE-IS3	WB-SOIC14	8 V	Yes	Yes	Universal
Si82E39ABE-KIT	Si82E39ABE-EVB	Si82E39ABE-IS3	WB-SOIC14	8 V	No	Yes	Universal
Si82F39ABC-KIT	Si82F39ABC-EVB	Si82F39ABC-IS1	NB-SOIC16	8 V	Yes	Yes	Universal
Si82E39ABC-KIT	Si82E39ABC-EVB	Si82E39ABC-IS1	NB-SOIC16	8 V	No	Yes	Universal
Si82F19ABB-KIT	Si82F19ABB-EVB	Si82F19ABB-IM2	LGA-13	8 V	Yes	No	Dual driver
Si82F79AGB-KIT	Si82F79AGB-EVB	Si82F79AGB-IM2	LGA-13	5 V	Yes	No	High-side/low-side driver
Si82F79ABB-KIT	Si82F79ABB-EVB	Si82F79ABB-IM2	LGA-13	8 V	Yes	No	High-side/low-side driver
Si82E39AGB-KIT	Si82E39AGB-EVB	Si82E39AGB-IM2	LGA-13	5 V	No	Yes	Universal
Si82E39ABB-KIT	Si82E39ABB-EVB	Si82E39ABB-IM2	LGA-13	8 V	No	Yes	Universal

1. LGA-13 is a future package type, not available at this time

Figure 2. EVP OPN Label Example

The user is recommended to identify the EVB OPN before using the EVB. In the example above, the label shows the EVB OPN is Si82F39ABE-EVB and the driver part number is Si82F39ABE-IS3 in the WB-SOIC14 package.

3. Connectors, Status LEDs, and Jumper Settings

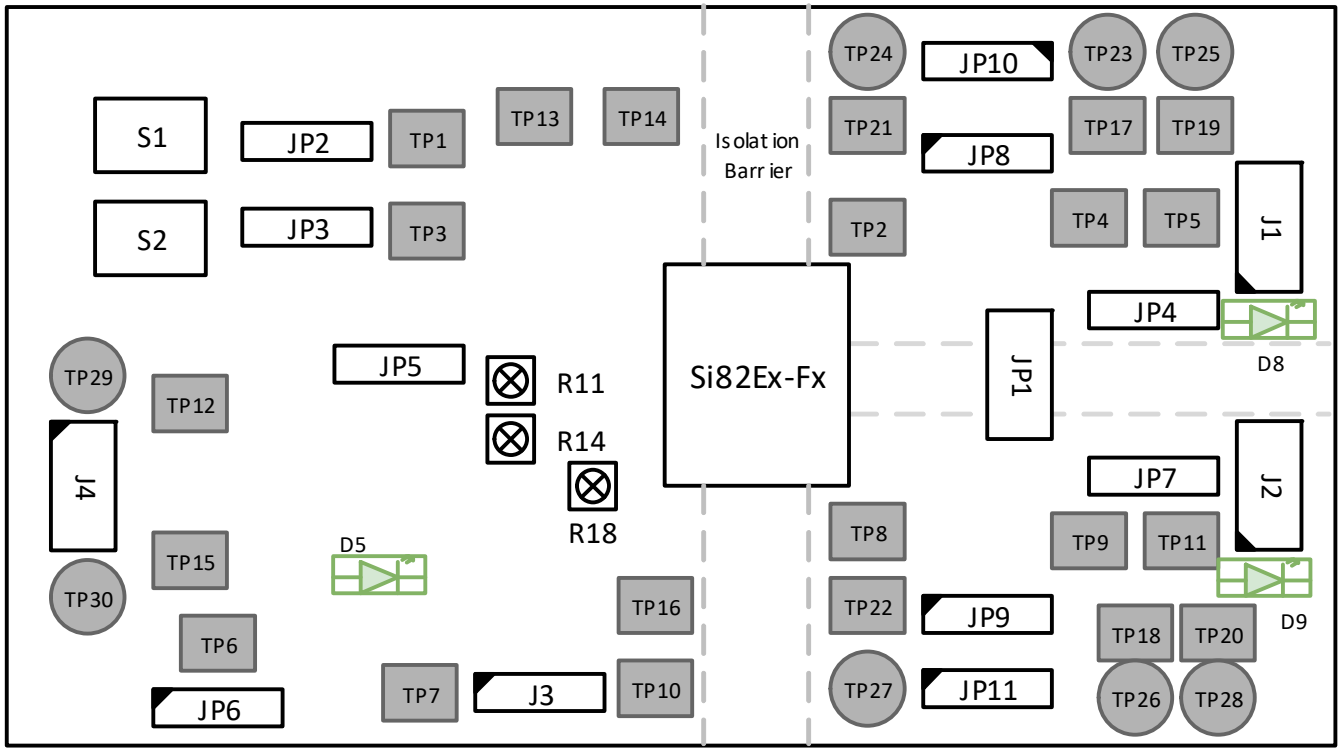


Figure 3. EVB Parts Placement, Pin 1 Positions are Marked

Table 2. Si82Ex-Fx EVB Connector Descriptions

Connector	Pin Number	Name	Description
J1	1	GATE_A	Channel A output for the extremal FET Gate and Source terminals
	2	SOURCE_A	
J2	1	GATE_B	Channel B output for the extremal FET Gate and Source terminals
	2	SOURCE_B	
J3	1	SPD–	Only available on Si82Fx EVB. The switching edge speed control pins to accept an external DAC output voltage (– for falling edge, + for rising edge)
	2	SPD+	
J4	1	VDDI	Input side power supply connector (from 3.3 V to 5.5 V)
	2	GNDI	
JP10	1	VIN+a	Driver A output power supply connector (ranging from UVLO voltage to 30 V). See Section 4 for connection details for the three power schemes External power for Driver A should connect to JP10 except when bootstrap power is used. See Section 4.4 for more detail
	2	VIN_REFa	
	3	VIN-a	
JP11	1	VIN-b	Driver B output power supply connector (ranging from UVLO voltage to 30 V). See Section 4 for connection details for the three power schemes External power for Driver B should connect to JP11. See Section 4.4 for more detail
	2	VIN_REFb	
	3	VIN+b	

Table 3. LED Indicators

LED	Color	Description
D5	Green	Lit when the input side power supply VDDI is present
D8	Green	Lit when the output side power supply VDDA is present
D9	Green	Lit when the output side power supply VDDB is present

Table 4. Switches, Jumpers, and Trimmer Potentiometer Settings

Jumper Setting	Default Setting	Description
JP1	Open	Bootstrap enable setting Short JP1 to enable the bootstrap power for Channel A When Channel A and B are configured for high-side + low-side connection, the bootstrap circuit allows Channel A (high-side) to use the Channel B (low-side) power supply so only one isolated power supply is required When the bootstrap circuit is used, remove the power supply connection for Channel A at JP10
JP2 JP3	Short	Used to disconnect switches S1 and S2 from the Si82Ex-Fx VIA/VIB/PWM input pins When JP2/JP3 is shorted (default), pressing S1/S2 produces a logic High signal to the Si82Ex-Fx input pins When external control signals are fed to VIA/VIB/PWM input pins through TP1 and TP3, the jumper shunts on JP2 and JP3 should be removed to avoid signal conflicts
JP4 JP7	Short	Channel A (JP4) and B (JP7) capacitive dummy load enable jumpers Shorting these jumpers connects the capacitive dummy load (1 nF) to the driver outputs Remove the jumper shunts to disable the capacitive dummy load when external FETs are connected to the EVB
JP5	Short	Shorting JP5 configures the Si82Ex-Fx as an independent dual driver The dual driver does not have any input overlap protection and thus the driver can be freely connected in the high-side + high-side, low-side + low-side, or any other circuit configuration Typically, in the high-side + low-side connection, input overlap protection is desired to avoid shoot-through current. The jumper shunt on JP5 should be removed to activate input overlap protection and dead time adjustment
JP6	Pin 1-2	JP6 shunt positions determine EN (enable)/DIS (disable) pin logic level Pin 1-2 position: Logic High at EN/DIS pin Pin 2-3 position: Logic Low at EN/DIS pin Open: The EN/DIS pin signal is determined by on-board R8/R9 resistor or the external control signal connected to TP6
JP8 JP9	Pin 1-2	JP8 and JP9 shunt positions determine the Si82Ex-Fx EVB power supply connection schemes on the output side. Pin 1-2 position: Single supply unipolar voltage scheme (also bootstrap power mode) Pin 2-3 position: Single supply bipolar voltage scheme Open: Dual supply bipolar voltage scheme
S1 S2	Tactile switches	S1 and S2 manually toggle Si82Ex-Fx input. See JP2, JP3 settings S1: VIA or PWM input pin S2: VIB input pin. S2 is not available for PWM input version When pressed, sends a logic High signal When released, sends a logic Low signal
R11 R14 R18	Trimmer Potentiometers	R11: Dead time (DT) adjustment. Only effective when the jumper shunt on JP5 is removed R14: Falling edge drive strength adjustment for Driver A and Driver B R18: Rising edge drive strength adjustment for Driver A and Driver B

Table 5. Test Points

Test Point	Label	Description
TP1	VIA/PWM	VIA or PWM input signal. Can be used to feed an external controller signal to the Si82Ex-Fx input pins with JP2 jumper shunt removed
TP2	VOA	Driver A output voltage at the Si82ExFx VOA pin
TP3	VIB	VIB input signal. Can be used to feed an external controller signal to the Si82Ex-Fx input pin with JP3 jumper shunt removed
TP4	Gate_A	Driver A output voltage at the load. Connect to the Channel A external FET Gate when the external FET is used
TP5	Source_A	Driver A output voltage reference at load. Connect to the Channel A external FET Source when the external FET is used
TP6	EN/DIS	Si82ExFx EN (enable) or DIS (disable) signal. This test point can be used to feed an MCU control signal to the Si82ExFx with JP6 shunt removed
TP7	SPD–	The falling edge drive strength control signal
TP8	VOB	Driver B output voltage at the Si82ExFx VOB pin

Table 5. Test Points (Continued)

Test Point	Label	Description
TP9	Gate_B	Driver B output voltage at the load. Connect to the Channel B external FET Gate when the external FET is used
TP10	SPD+	The rising edge drive strength control signal
TP11	Source_B	Driver B output voltage reference at load. Connect to the Channel B external FET Source when the external FET is used
TP12	VDDI	Input side VDDI power supply voltage
TP13		
TP14	GNDI	Input side power supply reference point
TP15		
TP16		
TP17	VDDA	Driver A positive power supply voltage VDDA
TP18	VDDB	Driver B positive power supply voltage VDDB
TP19	GNDA	Driver A power supply reference point
TP20	GNDB	Driver B power supply reference point
TP21	VSSA	Driver A negative power supply voltage VSSA
TP22	VSSB	Driver B negative power supply voltage VSSB

4. Power Up the EVB

Three isolated voltage power supplies (VDDI, VDDA, and VDDB) are required to power the Si82ExFx EVB.

However, when the bootstrap circuit is used, VDDB can provide the power for Driver A through the bootstrap circuit so only two isolated power suppliers are needed. No software is required to operate the board.

VDD1 accepts 3 V to 5.5 V. VDDA/B voltage can accept up to 30 V (reference to VSSA/B). The lowest value of VDDA/B is limited by the Si82ExFx UVLO threshold which is a chip dependent specification. (See EVB Ordering Guide)

For normal operation, set VDDA/B at least 2 V greater than the UVLO threshold. The current consumption for each supply should be less than 100 mA.

The voltage polarity protection circuit is included for each power supply connector. Power LEDs will be lit when the correct polarity power supplies are present.

The input side power supply should be connected to the EVB through J4. The pin definition and direction can be found in Table 2 and Figure 3.

The EVB supports various output side power supply connections, depending on the output voltage polarity (V_{GS}) requirement. By configuring the power supply connection, the drivers can output unipolar or bipolar gate drive voltage.

Negative V_{GS} usually results in shorter turn-off time. Turning off the MOSFET with the negative V_{GS} also provides better noise margin to avoid accidental MOSFET turn-on in harsh environments.

4.1. Single Supply Unipolar Output

This is the most straightforward power supply scheme for the output side. For each output channel, the driver is powered by one positive voltage power supply and the V_{GS} output is unipolar. See Figure 4 below.

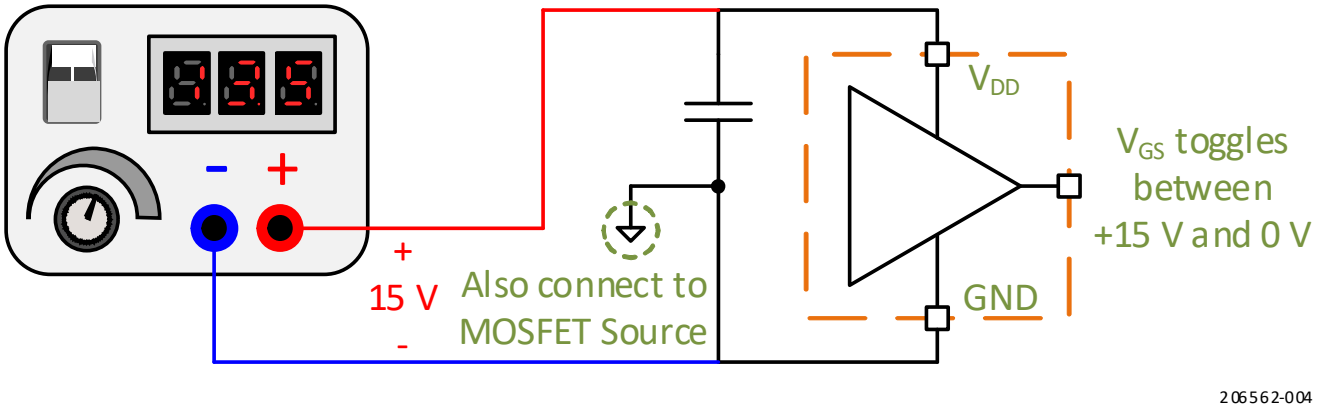


Figure 4. Single Supply, Unipolar V_{GS} Output

Table 6. Configuring for Unipolar Output

JP8/JP9 jumper	Short 1-2
JP1 jumper	Open
JP10/JP11 connector	Pin 1: Connect to the power supply positive output terminal Pin 2: Connect to the power supply reference/return (negative) terminal Pin 3: Open
Output side voltage supply range	(UVLO + 2 V) to 30 V

4.2. Dual Supply Bipolar Output

The EVB supports bipolar V_{GS} output. This requires a power supply with positive and negative voltage outputs for each channel. Below is an example using a power supply with +15 V and -5 V outputs which determines the turn-on and turn-off V_{GS} voltages respectively. Note: The common point of the +15 V and -5 V supplies (the black trace between the red and blue traces below) should be connected to the MOSFET Source pin.

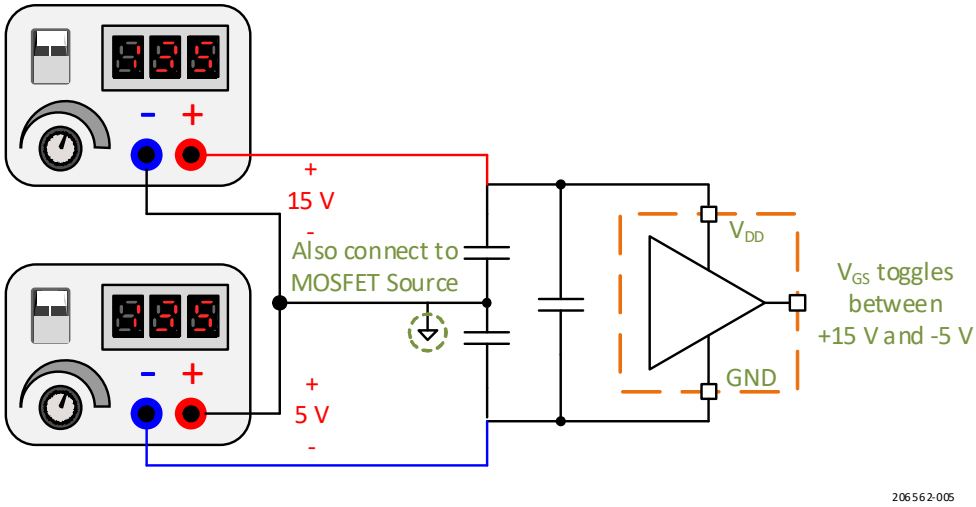


Figure 5. Dual Supply Bipolar V_{GS} Output

Table 7. Configuring for Dual Supply Bipolar Output

JP8/JP9 jumpers	Open. No jumper shunts
JP1 jumper	Open
JP10/JP11 connector	P1: Connect to the positive power supply output terminal P2: Connect to the reference/return terminals of both voltage sources P3: Connect to the negative power supply output terminal
Output side voltage supply range	|Positive supply voltage| + |negative voltage supply| between (UVLO + 2 V) to 30 V

4.3. Single Supply Bipolar Output

When bipolar output is desired but the bench power supply only has a single voltage output, the EVB includes a simple voltage splitter circuit to provide positive and negative voltages to the chip. The positive voltage level is fixed and determined by D6/D7 Zener diodes (typically 10 V, see the BOM table for more detail) on EVB.

The resulting negative voltage is the difference between the bench power supply and D6/D7 Zener voltage. In the example below, the +15 V power supply is split into +10 V and –5 V to produce the bipolar V_{GS} output.

The MOSFET Source pin should be connected to the common point of the positive and negative voltage supplies.

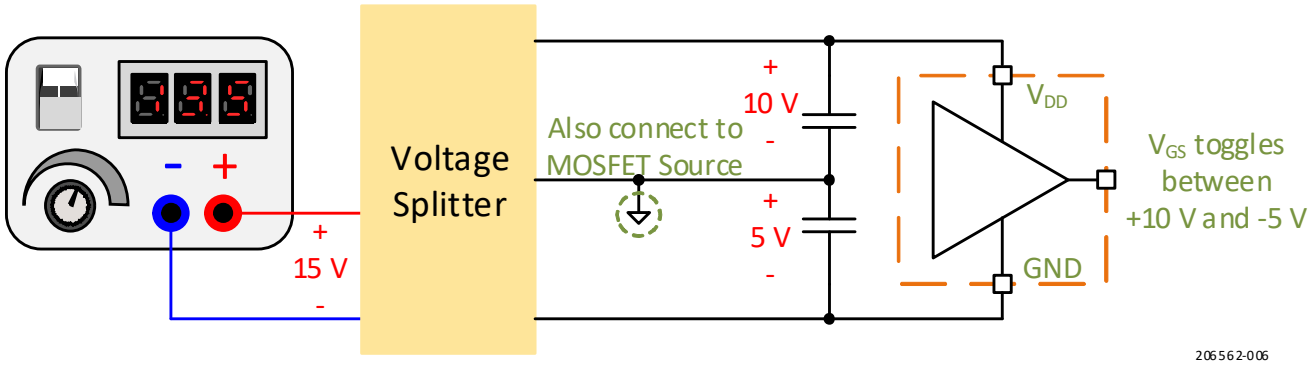


Figure 6. Single Supply Bipolar Output

Table 8. Configuring for Single Supply Bipolar Output

JP8/JP9 jumper heads	Short 2 to 3
JP1 jumper	Open
JP10/JP11 connector	Pin 1: Connect to the power supply positive output terminal Pin 2: Open Pin 3: Connect to the power supply reference/return (negative) terminal
Output side voltage supply range	10 V to 30 V

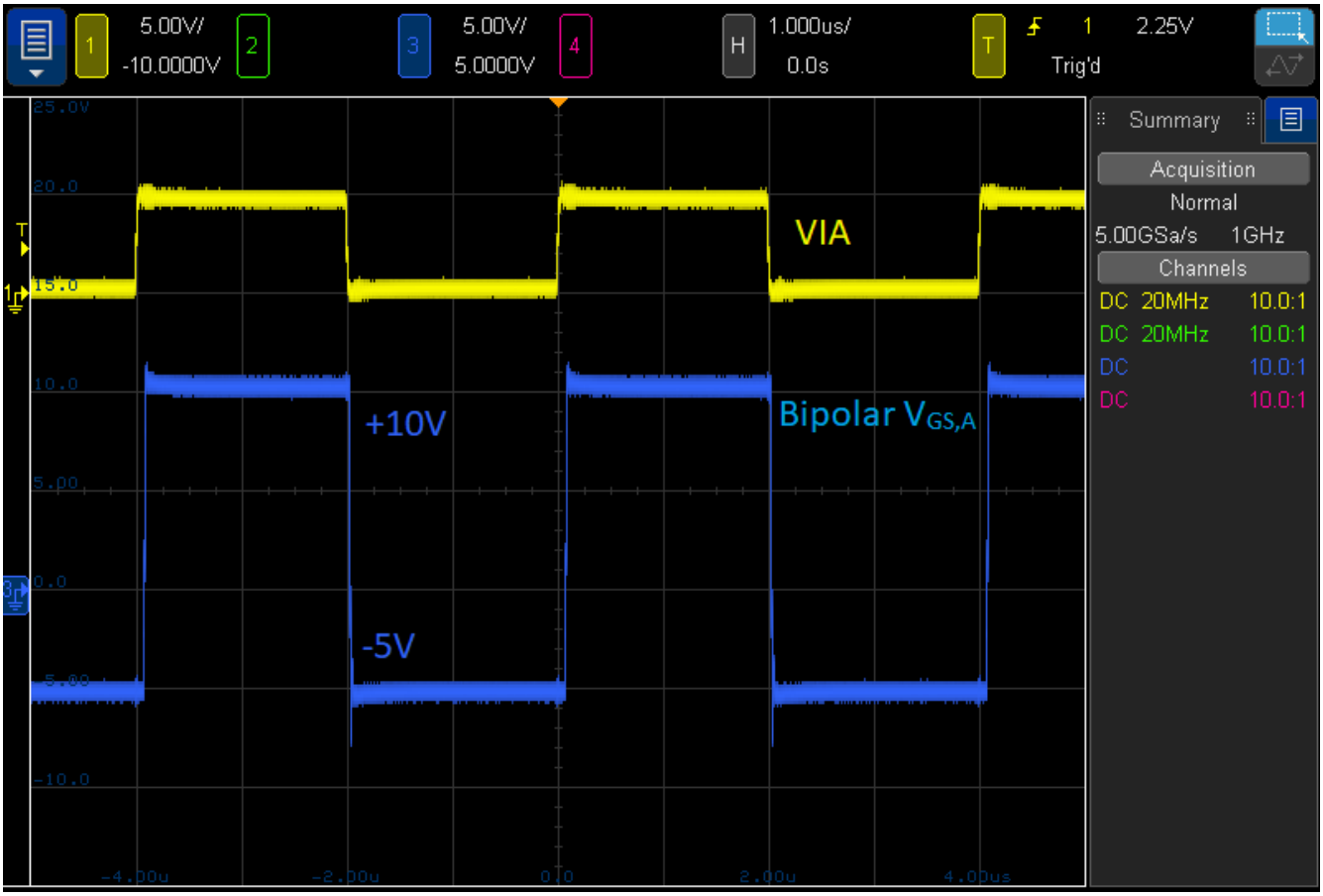


Figure 7. Single Supply Bipolar V_{GS} Output

4.4. Bootstrap Power

The Si82Ex-Fx EVB bootstrap circuit (enabled by JP1) allows Driver A and Driver B to share the same power supply (VDDB) when the drivers are connected in the high-side + low-side configuration.

Note

1. Only unipolar output is supported with the bootstrap circuit.
2. The external MOSFETs must be connected in the high-side + low-side configuration when evaluating the EVB with the bootstrap circuit. The bootstrap circuit requires the low-side MOSFET to turn on first in order to charge the high-side driver bootstrap capacitor. See Skyworks Application Note AN486 for more details.

Table 9. Configuring Bootstrap Power

JP1 jumper	Short JP1 to enable the bootstrap circuit
JP8/JP9 jumpers	Short 1 to 2
JP10 connector	Leave all pins open
JP11 connector	Pin 1: Connect to the power supply positive output terminal Pin 2: Connect to the power supply reference/return (negative) terminal Pin 3: Open
Output side voltage supply range	10 V to 30 V

5. Input Signal Interface

5.1. VIA, VIB, and PWM Input Signals

Tactile switches S1 and S2 generate the slow changing VIA/PWM and VIB signals for demonstration purposes. A debounce filter consisting of the Schmitt trigger (U2) removes the unwanted tactile switch edge noise.

When external control signals are applied through TP1 (for VIA/PWM) and TP3 (for VIB), the jumper shunts on JP2 and JP3 should be removed to avoid conflicts with the debounce Schmitt trigger.

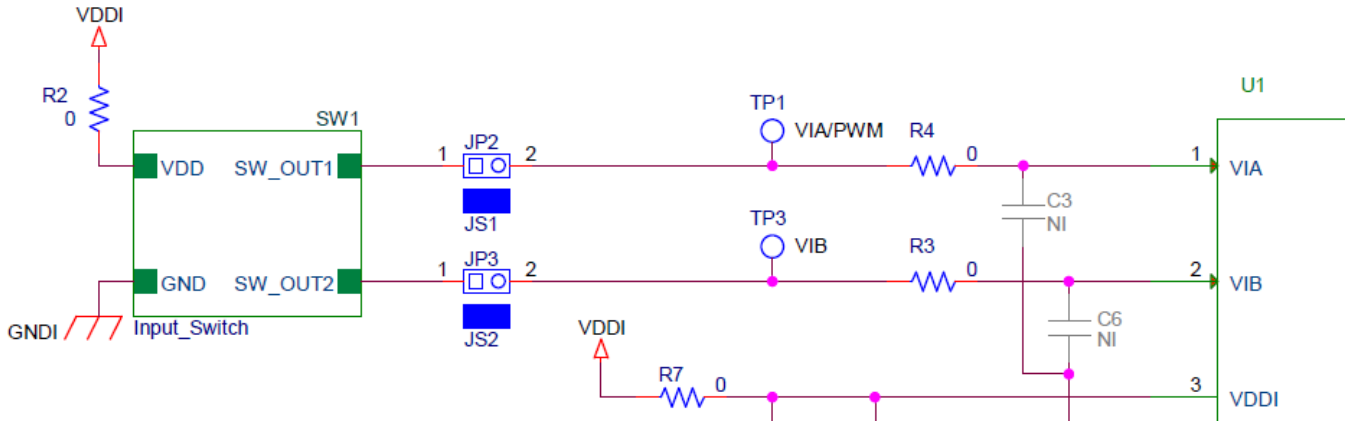


Figure 8. VIA, VIB, and PWM Input Signal Connections

5.2. Enable/Disable (EN/DIS) Signal

The EN/DIS (Enable/Disable) pin has global control to turn off both drivers regardless of the input signals. The jumper shunt position on JP6 determines the logic level at the EN/DIS pin, see Table 4. Changing the jumper shunt positions on JP6 can be used to demonstrate the EN/DIS feature. Either R8 or R9 is populated to ensure the drivers are still active even when the JP6 jumper shunt is temporarily removed during the position change.

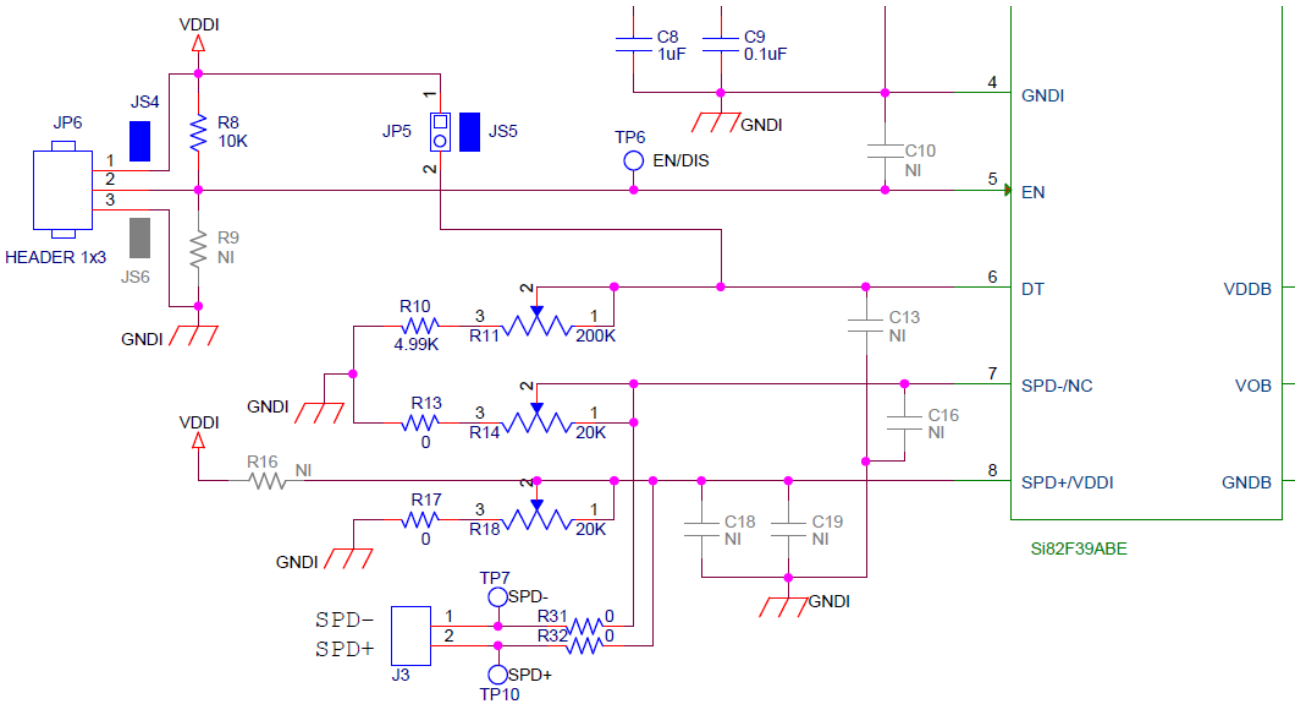


Figure 9. EN/DIS, DT, and SPD+/- Input Signal Connections

5.3. Dead Time (DT) Signal

The dead time (DT) pin is used to control the dead time between Channel A and Channel B outputs. On the EVB, DT adjustment is achieved through R11. Turning R11 clockwise increases resistance and dead time. R10 is in series with R11 to provide minimum DT resistance (4.99k ohm).

If evaluating dead time performance or variation for a given DT resistance is desired, the EVB can be reworked by replacing R10 with the desired value and turning R11 trimmer potentiometer fully counterclockwise to nullify R11.

The Si82Ex-Fx part numbers with the universal input feature has the flexibility to act as an independent dual-driver without input signal overlap protection and without dead time insertion. This leaves the dead time control to the controller and enables the Si82Ex-Fx to work in low-side + low-side, high-side + high-side, or any other configuration. By shorting the jumper shunt on JP5, the DT pin is pulled up to VDD to configure Si82Ex-Fx for dual-driver mode.

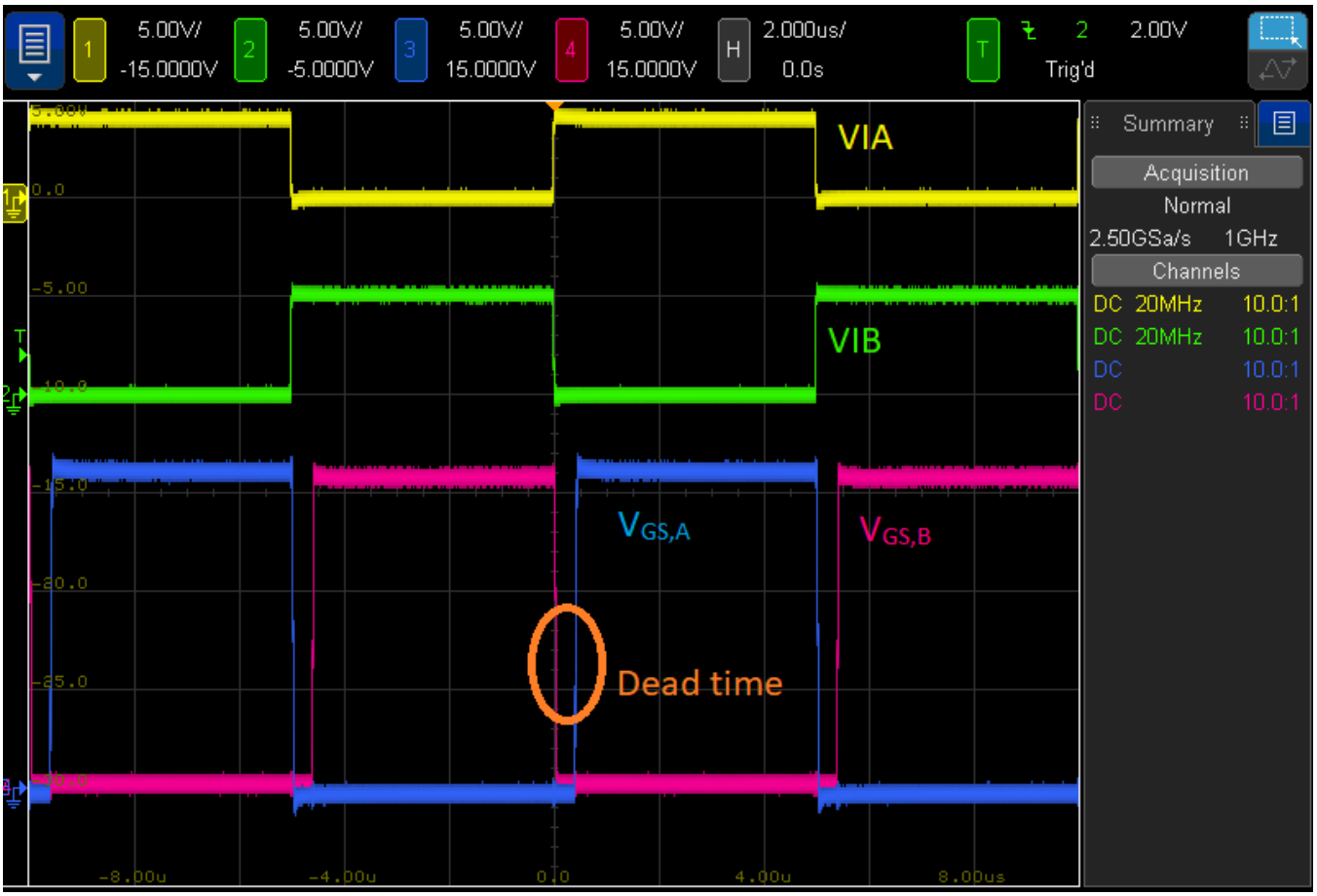


Figure 10. Dead Time Waveforms

5.4. SPD- and SPD+ Signals

The Si82Fx features variable current drive (VCD) adjustment on its outputs. By changing the pull-down resistor values at SPD+ (rising edge speed) and SPD– (falling edge speed) pins, the edge slew rate of the gate drive signals is adjusted, eliminating the need for conventional external gate resistors. Further, there is a Miller clamp feature built into the VCD. For additional details on these features, please refer to the data sheet.

Trimmer potentiometer R14 and R18 are used as pull-down resistors for SPD+ and SPD- respectively. Turning R14 and R18 clockwise increases its resistance and thus increases drive strength.

If evaluating VCD performance or variation for a given pull-down resistance is desired, the EVB can be reworked by replacing R13/R17 with the desired values and turning the trimmer potentiometers fully counterclockwise to nullify R14/R18.

6. Output Signal Interface

Si82Ex-Fx output signals can be monitored at the test points on EVB. The 1 nF capacitive dummy loads (C7 and C17) simulate the MOSFET gate charge. When an actual MOSFET is connected to the EVB, C7 and C17 can be disabled by removing the jumper shunts on JP4 and JP7. The Gate and Source terminals of the MOSFET can be connected to J1 (Driver A) and J2 (Driver B). Refer to Table 2 for more connection details. Use short, heavy-gauge wires to connect the external MOSFETs to the EVB.

For the Si82Ex which does not support the VCD feature, gate resistors are still employed for edge slew rate tuning. On the EVB populated with Si82Ex devices, R5 and R12 (default 4.7 ohm) are used for rising edge slew rate adjustment while R6 and R15 (default 1.2 ohm) are used for the falling edge slew rate adjustment. The gate resistors may be replaced to fine-tune the desired slew rates.

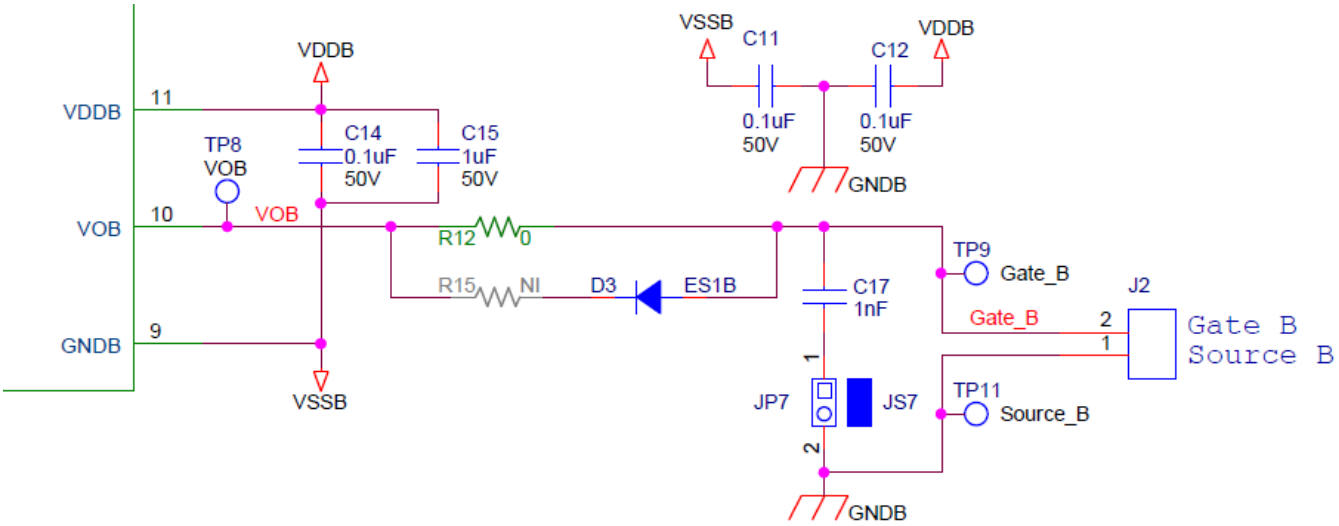


Figure 11. Output Signal Connections

7. Feature Demonstrations

7.1. Input Overlap Protection

When the driver is used in the high-side + low-side configuration, care must be taken to avoid concurrent turn-on at both high-side and low-side switching components. If this occurs, large shoot-through current flowing from the high voltage source (connected to the high-side component Drain) to ground (connected to the low-side device Source) could permanently damage the switching components.

Input overlap protection is a useful feature for the high-side + low-side circuit configuration to prevent shoot-through current. When one of the input signals is already High, the protection circuit blocks the High signal from the other input pin.

Note: The PWM input version of the Si82Ex-Fx EVB does not have input overlap protection since it has only one input signal pin.

When overlap protection is not desired, this feature can be disabled by placing a jumper shunt on JP5.

Procedure

1. Make sure there is no jumper shunt on JP5. Power up the EVB.
2. Press S1 or S2 tactile switch once at a time to send High signal to Si82Ex-Fx VIA or VIB pin. Monitor VOA and VOB waveforms (TP2 and TP8) on auto-trigger oscilloscope to confirm the output signal follows S1 or S2 switch.
3. While keeping S1 pressed, press S2. Once S2 is pressed, the overlap protection is engaged and both output signals are pulled low.
4. Repeat step 3 but this time press S2 first. The oscilloscope waveform should also show both LOW outputs due to the overlap protection.
5. Make sure no switching components are connected to EVB J1 and J2 output connectors. Next, place a jumper shunt on JP5 and repeat step 3. Now VOA and VOB can output High signals at the same time.

7.2. Dead Time Adjustment

In an ideal case, the overlap protection is sufficient to prevent shoot-through current in the high-side + low-side configuration. In reality, however, the external switching components do not turn on or off instantly. Thus, switching dead time is inserted to ensure the conducting device can be fully turned off before the opposite device is turned on. Dead time gets its name because both VOA and VOB stay Low during this time period.

The required dead time period is a system dependent parameter based on the rise and fall time of external switching components. Insufficient dead time can lead to unexpected shoot-through current while excessive dead time can lead to reduced power efficiency.

Dead time can be implemented on the VIA/VIB input signals by inserting blanking time before any signal toggles from Low to High. Some SMPS controllers have a function to adjust dead time.

R11 on the Si82Ex-Fx EVB is used to adjust the VOA and VOB dead time. Even though there is no blanking time on VIA and VIB input signals, the Si82Ex-Fx inserts adjustable dead time before the rising edge of VOA and VOB.

Procedure

1. Make sure there is no jumper shunt on JP5. Power up the EVB.
2. Press S1 or S2 tactile switch once at a time to send High signal to Si82Ex-Fx VIA or VIB pin. Monitor VOA and VOB waveforms (TP2 and TP8) on the auto-trigger oscilloscope to confirm the output High signal follows S1 or S2 switch.
3. Press and hold S1, then press S2. Both outputs become Low due to the overlap protection feature.
4. Change the oscilloscope from “auto trigger” to “normal trigger” at the VOA waveform rising edge. The suggested time base is 200 ns per division.
5. Release S2. Since only S1 is pressed, this disarms the Si82Ex-Fx overlap protection and turns the VOA signal from Low to High to trigger the oscilloscope. The inserted dead time is the time difference between VIB falling edge and VOA rising edge.
6. Adjust R11 and repeat steps 3 through 5. The waveforms should show a different dead time.

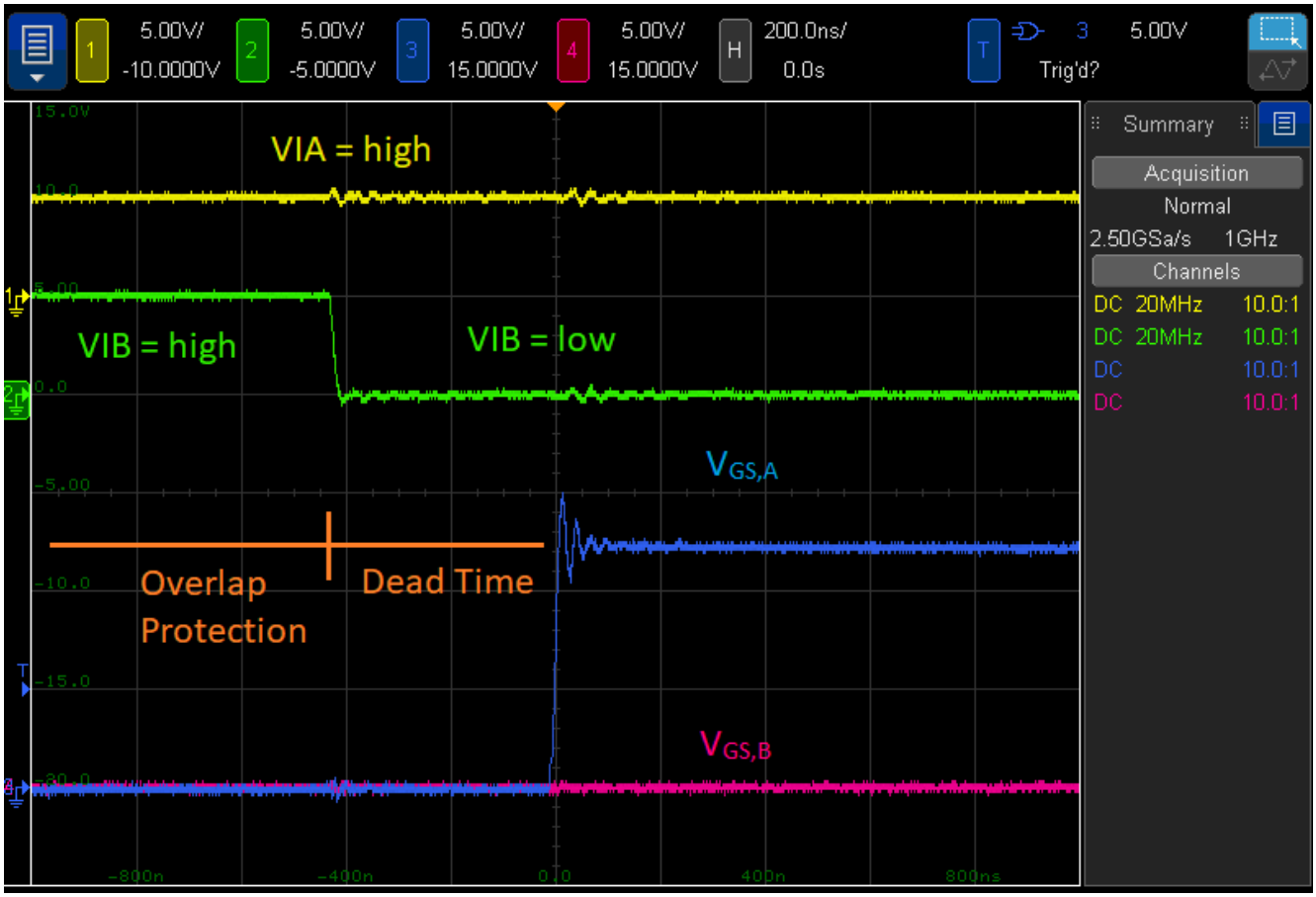


Figure 12. Dead Time After Overlap Protection is Disarmed

7.3. Driver Output Current Control

Si82Fx has output current control which is adjustable with an external resistor. The variable output current results in the different edge slew rates on a given capacitive load. R14 and R18 trimmer potentiometers on the EVB are used to demonstrate this feature.

Procedure

1. Install a jumper shunt on JP4/JP7 to enable the capacitive dummy load and power up the EVB.
2. Set the oscilloscope to normal trigger mode on either VOA or VOB waveform rising edge. The suggested time base is 100ns per division.
3. Press S1 or S2 to generate VOA or VOB output. The oscilloscope should capture the rising edge waveform.
4. Adjust R18 trimmer potentiometer for (SPD+ pin) to a different value. Repeat step 3 to see the slew rate change.
5. When the oscilloscope is set to trigger on the falling edge, it can be used to monitor the slew rate change with R14 trimmer potentiometer for (SPD– pin).

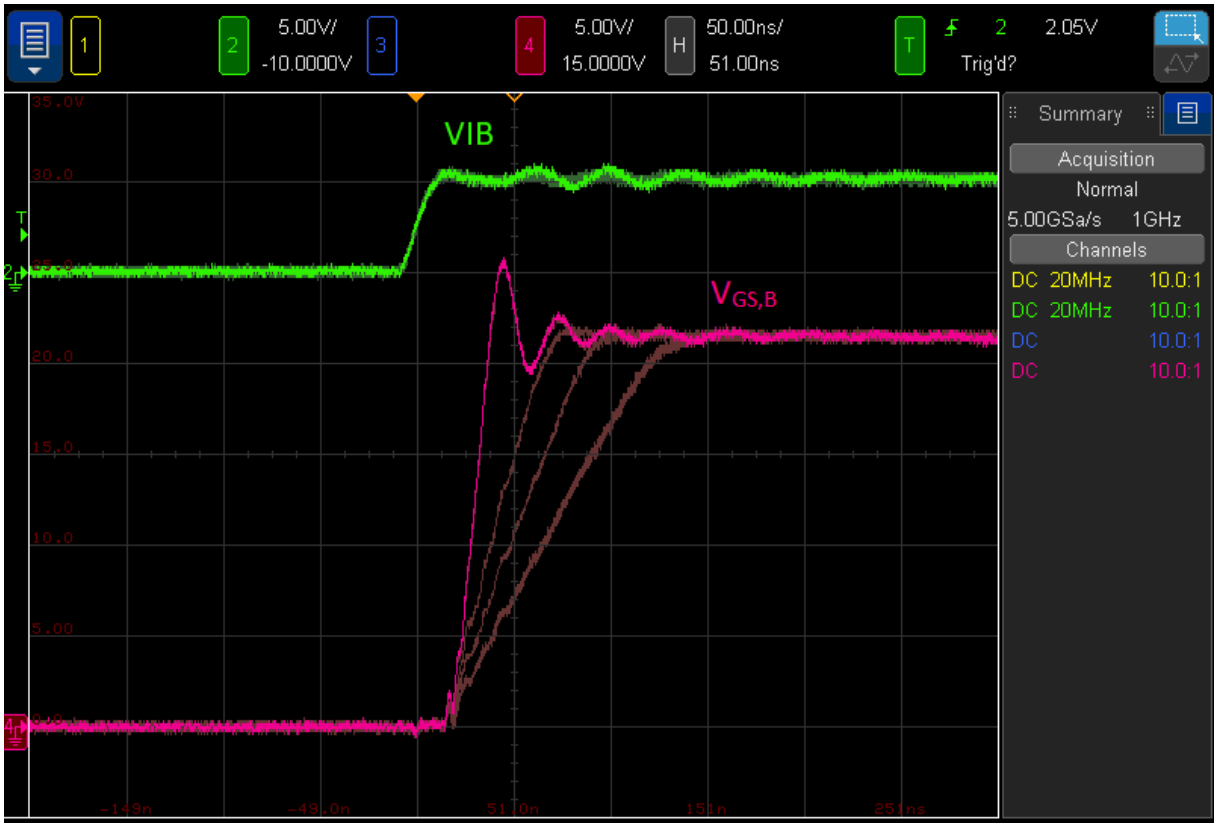


Figure 13. Rising Edge Slew Rate Adjustment

7.4. Bootstrap Power Circuit

The bootstrap power circuit allows two drivers to share one power supply based on two conditions:

- Two drivers on the EVB need to connect to two external MOSFETs in a half bridge (high-side + low-side) configuration.
- The shared power supply provides only the positive voltage. In other words, the bipolar V_{GS} output is not supported by the bootstrap power scheme.

Procedure

1. Connect the Gate and Source terminals of the external high-side MOSFET to the EVB J1 connector, and connect the Gate and Source terminals of the external low-side MOSFET to the EVB J2 connector.
2. Install a jumper short on JP1 to enable the bootstrap circuit. Follow Section 4.1 “single supply unipolar output” connection between the bench power supply and JP11.
3. Leave JP10 unconnected. Also, remove jumper shunts on JP4 and JP7.
4. Next, bring up the EVB and provide power to the external MOSFETs. Note VDDA LED D8 is off since we do not provide power to JP10.
5. Press S2 to send a High signal to the Si82Ex-Fx VIB pin.

6. VDDA LED D8 is lit when S2 is pressed. This indicates the bootstrap circuit charges the VDDA bypass capacitors when the external low-side MOSFET is conducting.

8. Si82Ex-Fx EVB Schematics

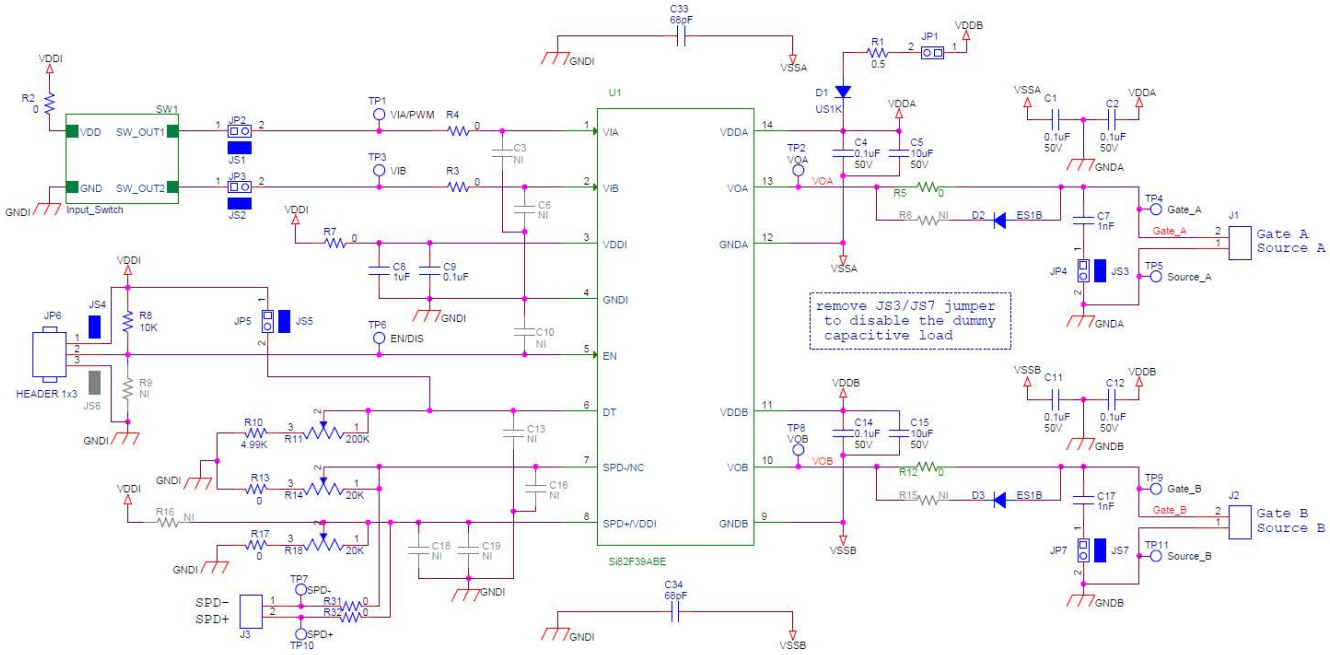


Figure 14. Si82Fx Driver (WB SOIC-14 and NB SOIC-16 Packages)

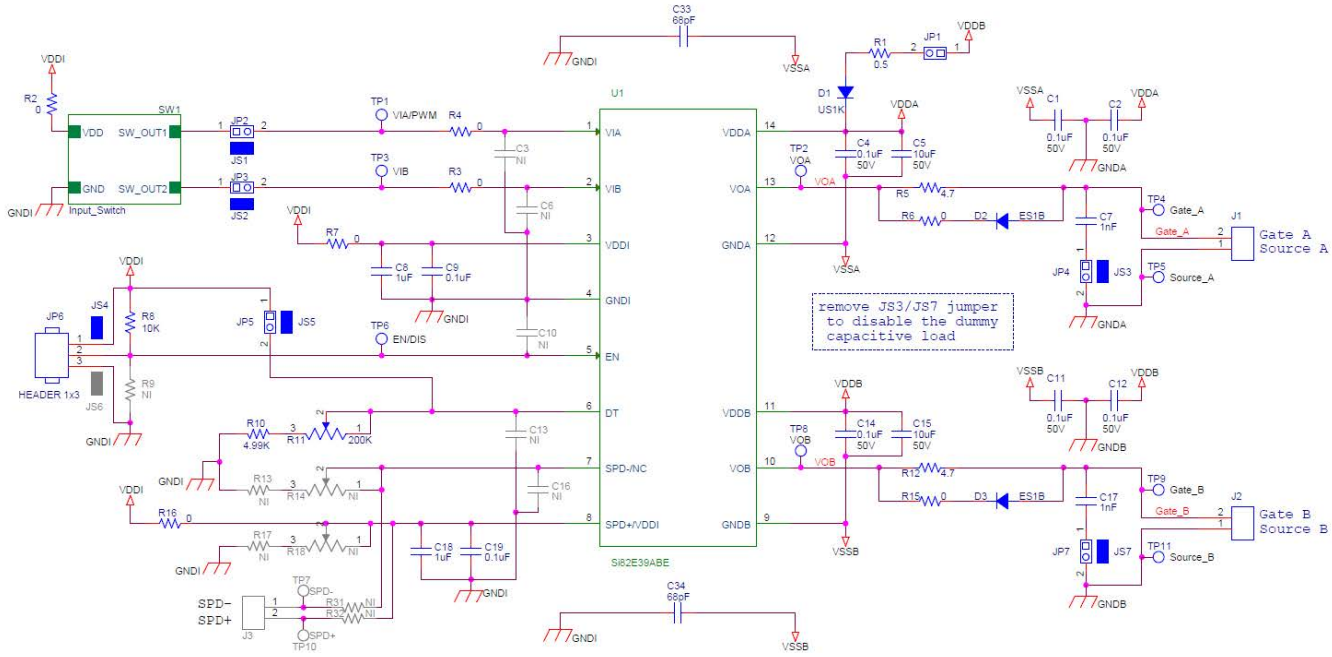


Figure 15. Si82Ex Driver (WB SOIC-14 and NB SOIC-16 Packages)

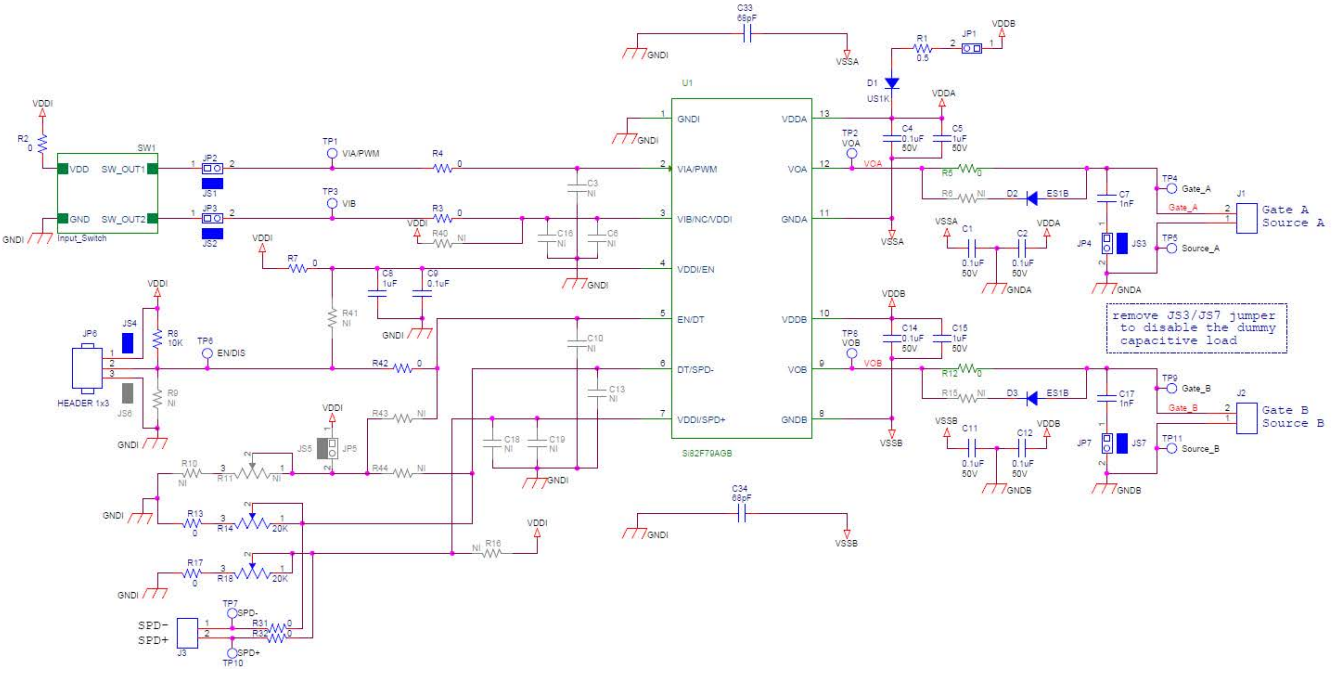


Figure 16. Si82Fx Driver (LGA-13 Package)

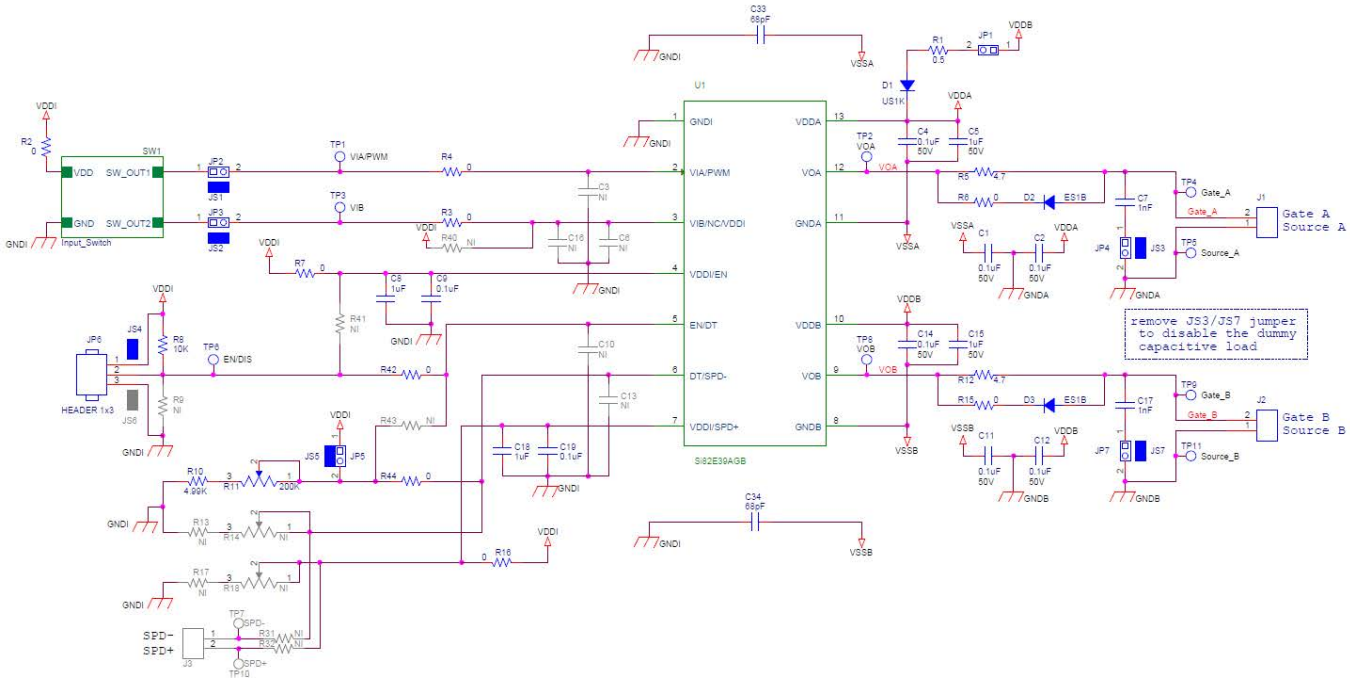


Figure 17. Si82Ex Driver (LGA-13 Package)

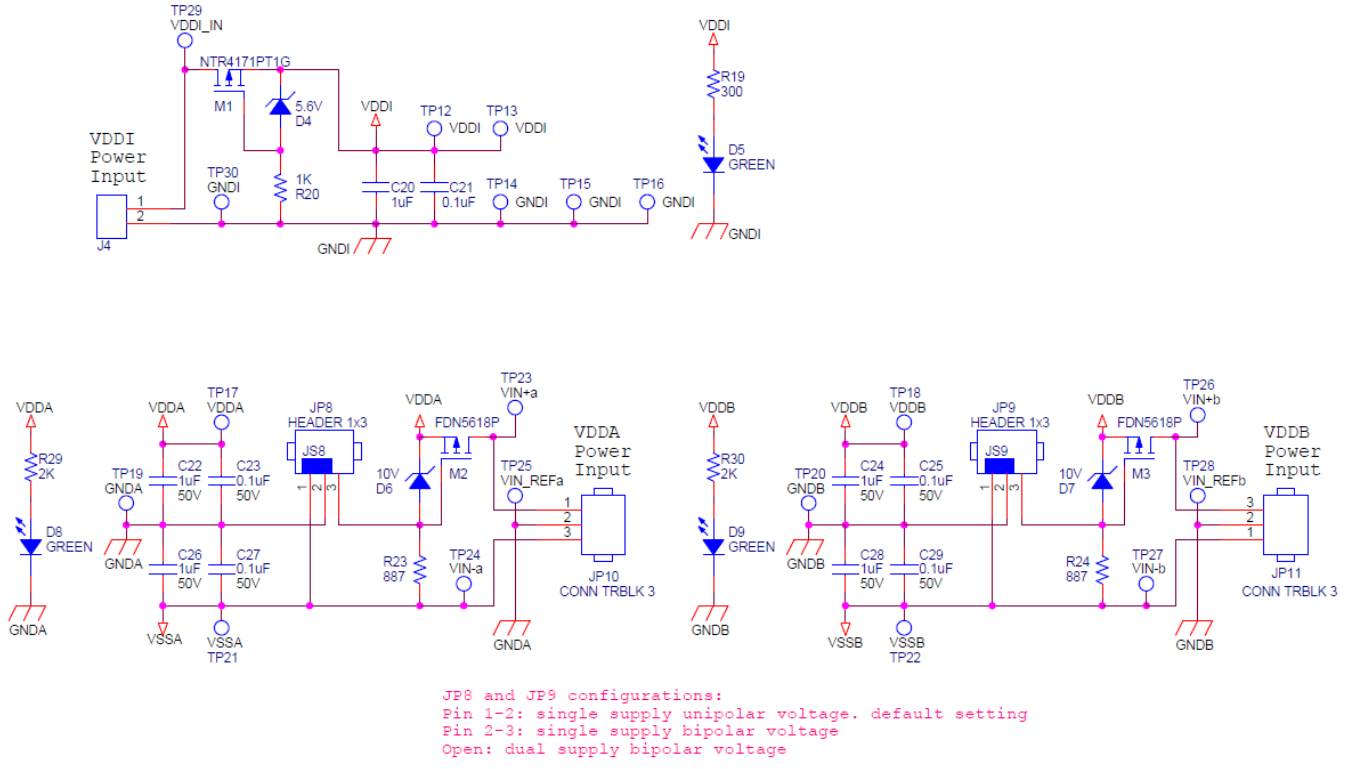


Figure 18. EVB Power Circuit (WB SOIC-14, NB SOIC-16, and LGA-13 Packages)

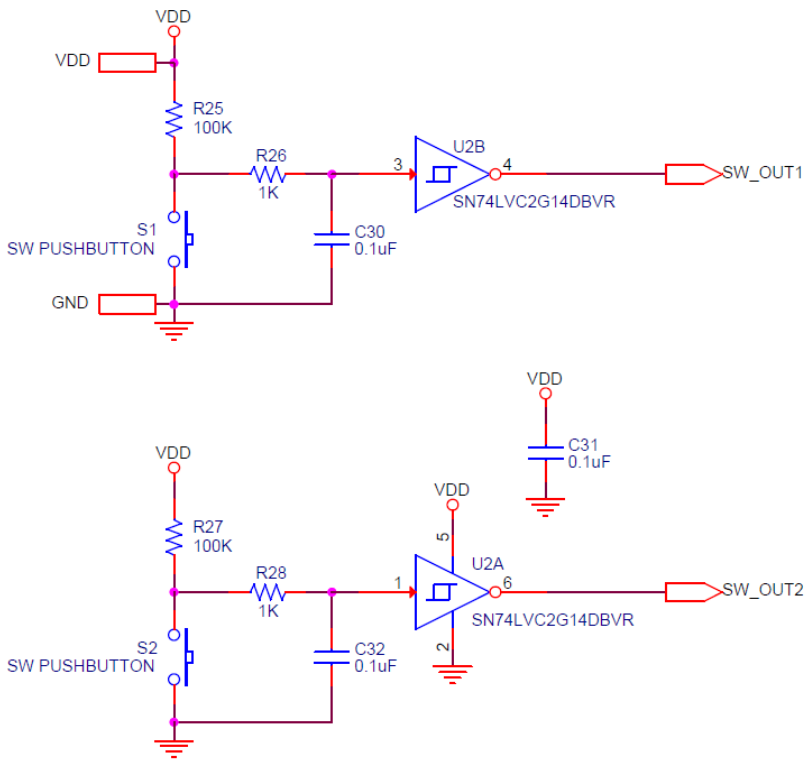


Figure 19. EVB Input Switches

Table 10. Si82Ex-Fx Bill of Materials

Reference	Value	Rating	Manufacturer Part Number	Manufacturer
C1,C2,C4, C11, C12, C14, C23, C25, C27, C29	0.1 uF		C0603X7R500-104K	Venkel
C3, C6, C10, C13, C16[1]	0.01 uF		C0402X7R250-103K	Venkel
C5, C15	10 uF		GRM21BR61H106KE43L	Murata
C7, C17	1 nF		C0805C0G500-102F	Venkel
C8, C18, C16[1]	1 uF		GCM188R71E105KA49	MuRata
C9, C19	0.1 uF		C0603X7R250-104K	Venkel
C20	1 uF		C0603X7R100-105K	Venkel
C21, C30, C31, C32	0.1 uF		C0402X7R100-104K	Venkel
C22, C24, C26, C28	1 uF		CL21B105KBFNNNE	Samsung
C33, C34	68 pF	Y2	GA342D1XGF680JY02L	MuRata
D1	US1K	1.0 A	US1K-13-F	Diodes Inc.
D2, D3	ES1B	1.0 A	ES1B	Diodes Inc.
D4	5.6 V	500 mW	SZMMSZ5232BT1G	On Semi
D5, D8, D9	GREEN	20 mA	LTST-C193TGKT-5A	Lite-On Technology Corp
D6, D7[2]	10 V	500 mW	MMSZ4697T1G	On Semi
JP1, JP2, JP3, JP4, JP5, JP7	HEADER 1X2		TSW-102-07-T-S	Samtec
JP6, JP8, JP9	HEADER 1x3		TSW-103-07-T-S	Samtec
JP10, JP11	CONN TRBLK 3		1725669	Phoenix Contact
J1, J2, J3, J4	CONN TRBLK 2		1725656	Phoenix Contact
M1	NTR4171PT1G	-3.5 A	NTR4171PT1G	ON Semiconductor
M2, M3	FDN5618P	1.25 A	FDN5618P	Fairchild
R1	0.5 Ω	1/4 W	LCR0805-R500F	Venkel
R2, R7, R13, R16, R17, R31, R32	0 Ω	1 A	CR0603-16W-000	Venkel
R3, R4, R40, R41, R42, R43, R44	0 Ω	1 A	CR0402-16W-000	Venkel
R5, R12[3]	4.7 Ω	1/10 W	CR0805-10W-4R7J	Venkel
R6, R15	1.2 Ω	1/10 W	CR0805-10W-1R2J	Venkel
R8, R9	10 kΩ	1/16 W	CR0603-16W-1002F	Venkel
R10	4.99 kΩ	1/16 W	CR0603-16W-4991F	Venkel
R11	200 kΩ	1/4 W	PVG3A204C01R00	MuRata
R14, R18	20 kΩ	1/4 W	PVG3A203C01R00	MuRata
R19	300 Ω	1/16 W	CR0603-16W-301J	Venkel
R20, R26, R28	1 kΩ	1/10 W	CR0603-10W-1001J	Venkel
R23, R24	887 Ω	1 W	ERJ-1TNF8870U	Panasonic
R29, R30	2 kΩ	1/10 W	CR0603-10W-2001F	Venkel
R25, R27	100 kΩ	1/10 W	CR0603-10W-104J	Venkel
S1, S2[4]	SW, push button	50 mA	TL3302AF180QJ	E-Switch
U2	SN74LVC2G14DBVR		SN74LVC2G14DBV	TI

1. C16 is 0.01 uF 0402 size capacitor on WB SOIC-14 and NB SOIC-16 EVBs. C16 is 1 uF 0603 size capacitor on LGA-13 EVB
2. For Si82F79AGB and Si82E39AGB EVBs, D6 and D7 are 5.6 V Zener diodes, On-semi SZMMSZ5232BT1G
3. R5 and R12 are 0 Ω for Si82Fx drivers
4. S2 is only available for dual input parts