Ultra-Broadband Capacitors in High-Speed Data Applications

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Introduction:

Ultra-broadband capacitors (UBC) have become an essential element in a line-up of devices that are essential for broadband designs. UBCs are needed for many ultra-broadband applications in the signal integrity market. They serve as ultra-broadband DC blocking, coupling, and bypassing circuit elements. Ultra-broadband capacitors are designed to maintain low loss with a relatively flat frequency response over a wide range of frequencies while providing a good match into the characteristic circuit impedance. Key application categories for ultra-broadband capacitors are listed in the table below.

Key Applications:

Application	Primary Function
Optoelectronics	High-speed data transfer over optical transmission medium
ROSA/TOSA	Receive and Transmit Optical Sub-Assembly - (Data Transfer)
SONET	Synchronous Optical Networking - (Optical carrier transmission for Data Communications, e.g., OC198, OC768)
Opto-Isolator	Creates isolation between circuits using light
Opto-Coupler	Couples light modulated signals between circuit elements
Transimpedance amplifiers	Current to voltage converter
Mach Zehnder Modulators	Electro-optic modulator
Broadband Test Equipment	Bit Error Rate Testers (BERT)
Broadband Microwave/ millimeter-wave	Microwave Communication links

High-Speed Data Transmission:

The most prominent ultra-broadband application technology is high-speed data using optoelectronics. It provides an important transitional link between RF/microwave and optical technologies. This requires UBC components to pass RF signals with minimal insertion loss and operate in such a manner as not to add any significant time-based

distortions. Both frequency domain and time domain performance characteristics are both important considerations in high-speed data designs.

Digital signal integrity has become an increasingly more important part of high-speed data systems and networks. Today's extreme demand for high-speed data is brought about by an ever-growing need for video, VoIP data communications and the Internet of things (IoT). Optoelectronics plays a key role in meeting the demands of current day high-speed data requirements. A data stream is a continuous collection of binary levels that represent a voltage state that corresponds to either one or zero. Even though these are digital signals, they are largely analog in nature while considering a single digital pulse. As such, these signals are subject to noise, distortion, and signal loss. At low bit transmission rates, propagated over short distances, a simple conductor can transmit pulses sufficiently well. At high bit transmission rates and over longer distances or through various mediums such as capacitor dielectric materials, digital signal integrity becomes a major consideration as these pulses can become degraded, thereby resulting in significant bit errors.

## Signal Integrity Considerations for Ultra-broadband Designs:

Signal integrity addresses any time and amplitude-based anomalies that are encountered in high-speed digital data systems. These irregularities have the potential to corrupt the integrity of the intended data stream, otherwise known as signal fidelity. This distortion can occur for various reasons. For example, if a broadband component exhibits excessive insertion loss (S21), or a degraded match (S11) to its 50-ohm environment, these factors can affect the height of the pulse resulting in an unacceptable amplitude level. Additionally, if a UBC adds significant time or phase delay, it will also impact signal integrity. Therefore, it is necessary to take a balanced approach and consider both frequency domain and time domain aspects of ultra-broadband designs.

Ultra-Broadband capacitors are used mostly as DC blocking devices. A smaller portion of the applications are for broadband bypassing. An ultra-broadband DC blocking capacitor is typically used as a series-through element. As such, it is important for a UBC to exhibit low insertion loss. Another consideration is how well the device matches to the transmission line in which it is placed. This can be readily determined by looking at S-Parameter forward transmission S21 and return loss S11. Data sheets will specify these parameters for a single device. As multiple UBCs are used in the design, their losses become cumulative and therefore must be carefully evaluated for any ultra-broadband design.

The following S21 curve depicts actual performance data for an AVX 550L, EIA 0402 case size UBC. As seen in the forward transmission data curve, losses are extremely low throughout the entire frequency range. Low insertion loss is especially important in design scenarios where two or more of these devices are cascaded. In this

configuration, the losses are cumulative; therefore, low loss UBC's are more desirable. The insertion loss for the 550L test sample is less than 0.4 dB throughout the entire sweep. Sadly, some component manufacturers specify insertion losses of 1 dB or more for their broadband capacitor devices. These components are almost always problematic in ultra-broadband applications as they will significantly degrade the signal. In fact, two lossy capacitors in cascade can consume almost half of the signal. Additionally, these same devices are likely to match poorly to the characteristic impedance of the circuit, thereby creating a large reflection coefficient.

### S-Parameter (S21) Forward Transmission for AVX 550L:
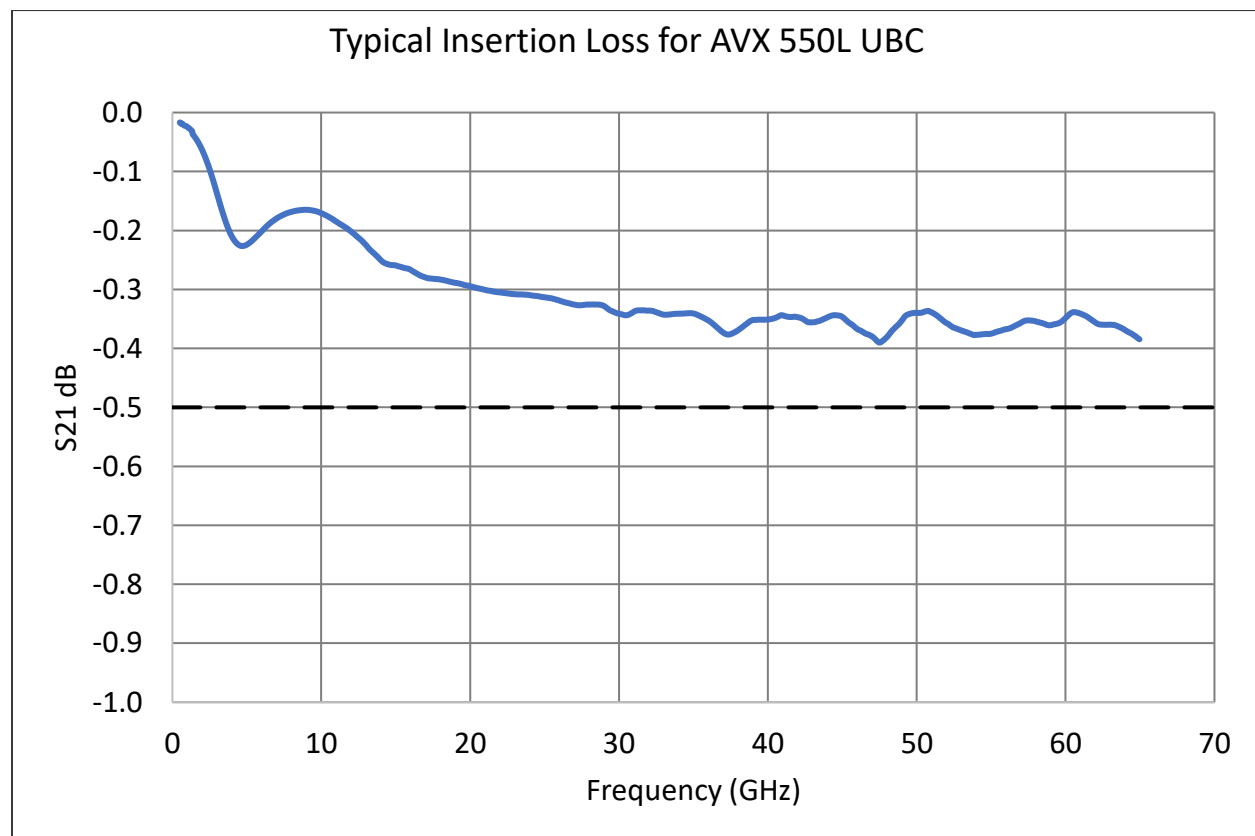
The S11 return loss curve for the same AVX 550L test sample conveys the device's match characteristics in a 50-ohm system over frequency. The return loss at 10 GHz is 33.5 dB, equivalent to a VSWR of 1.04:1; the return loss at 65 GHz is approximately 16 dB, equivalent to a VSWR of 1.37:1. From the S11 test data, it is evident that the AVX 550L device matches well over the entire frequency range.

S-Parameter (S11) Return Loss for AVX 550L:

Typical Return Loss for AVX 550L UBC
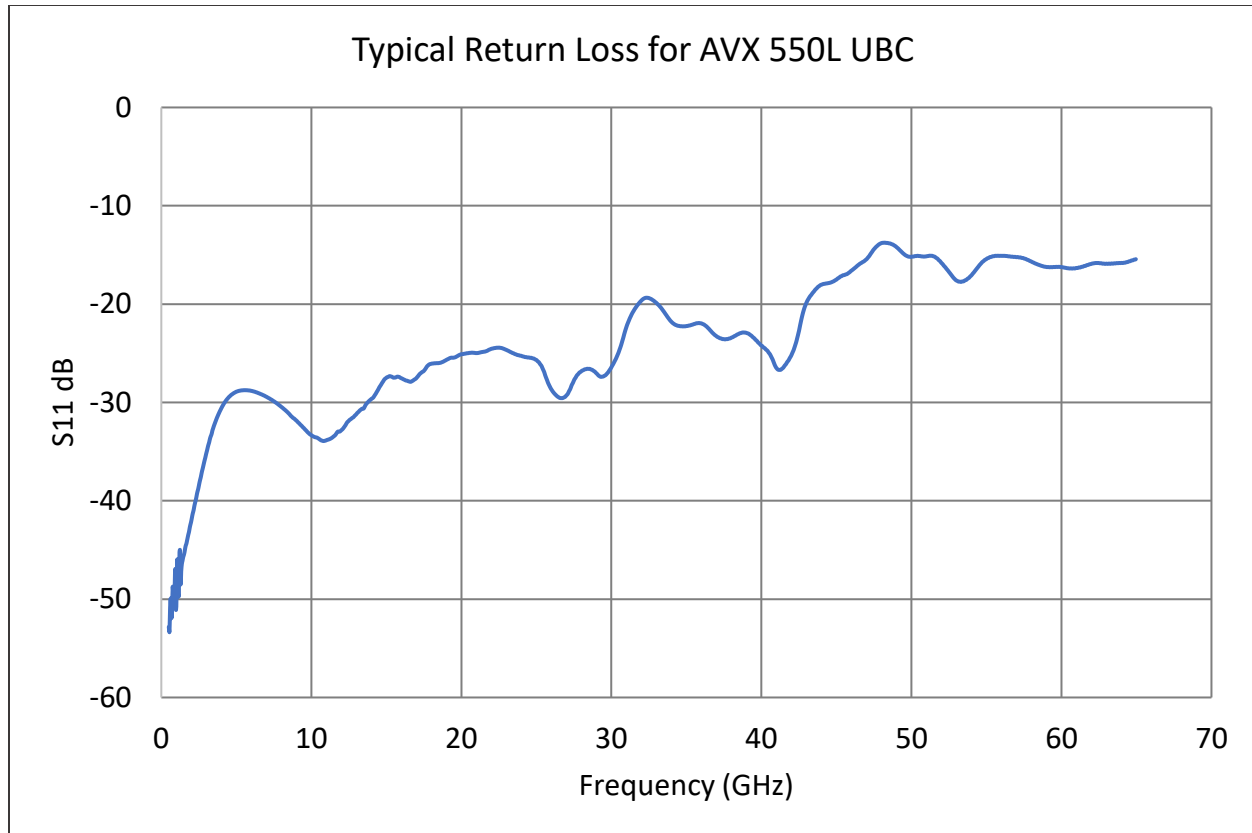
S-Parameter Test Description:

The S-Parameter test was performed on Rogers RO4350B 10-mil thick substrate with a nominal impedance of 50 ohms. The board has a 10-mil gap at the center of a 22-mil wide ½ oz copper microstrip trace. The device under test (DUT) was carefully centered over the gap of the microstrip trace, in a series-through configuration. De-embedding was accomplished using an LRL calibration method. The network analyzer used to perform these measurements was an Anritsu MS-4647B (70 GHz).
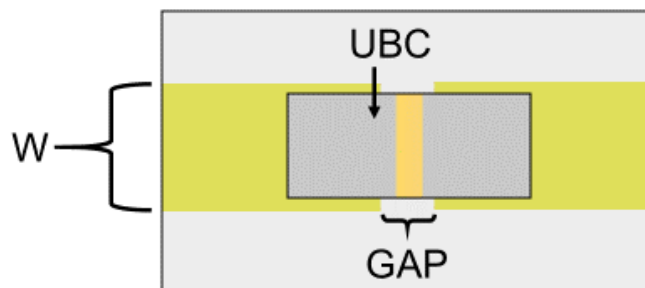
H (board thickness) = 10 mils
W (Trace Width) = 22 mils
Center Gap = 10 mils

½ Oz. Cu

H

RO4350B

Ground Plane
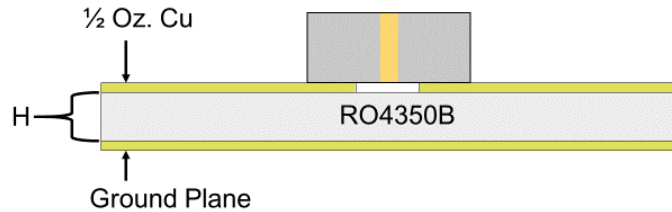
UBC Construction Variation:

Some manufactures have opted to market large two-piece ultra-broadband capacitor solutions. These devices combine a high value MLC for low frequency coverage with a smaller SLC capacitor piggybacked for high frequency coverage. Two-piece configurations are bulky and much more difficult to lay down on a PC board. While these devices may satisfy the requirements of some applications, they present definite performance limitations due to the bulky size of a two-piece construction. These limitations show up as excessive insertion loss, limits of the highest usable frequency, and response flatness. Another disadvantage of two-piece designs and even some one-piece UBC designs is their sensitivity to mounting orientation. In contrast, the AVX 550L Series UBC is a one-piece construction that is orientation insensitive with greater volumetric efficiency. This affords uniform performance in any mounting scenario making attachment more simplified.

Delay Time Anomalies and Data Transmission:

An important aspect of performance in high-speed data designs is the extent of time delay contributed by any circuit element. The eye diagram gives the designer a sense of how these circuit elements may cumulatively affect faithful reproduction of data pulses. Any circuit element in the lineup can create distortion of the original input pulse train. This occurs from a delay of input digital pulses as the data propagates through the device. An easy way to visualize this is to first look at the rise and fall time associated with a single pulse.

Rise Time Definition
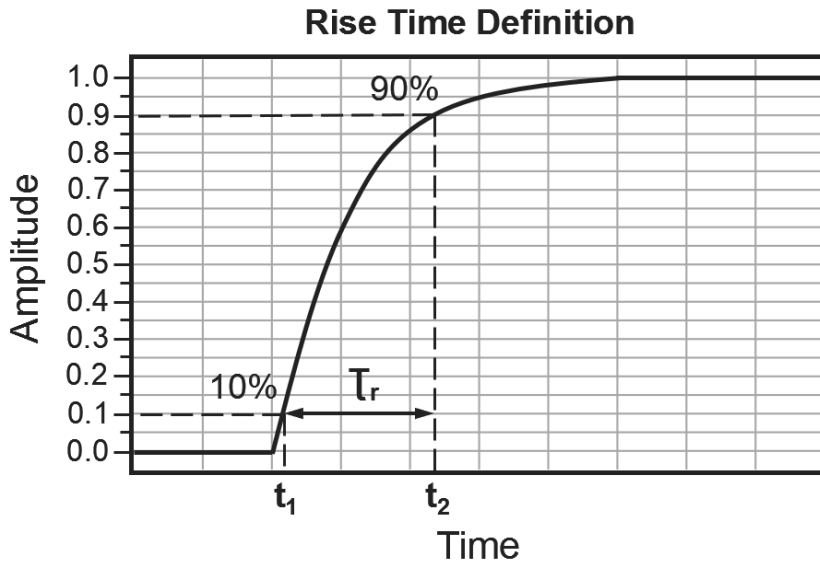
The following shows the relationship between pulse amplitude and time duration. The time interval between t1 and t2 is known as rise time. This is the interval of time required for the leading edge of a pulse to rise from 10% to 90% of the peak pulse amplitude. The larger the rise time of a digital pulse, the more problematic this becomes for passing high-speed data through a broadband network. This factor limits rate of data propagation through the system without significant loss of fidelity, i.e., bit errors. In extreme cases, the bit error rate (BER) will become unacceptably high.

Rise and Fall Time of Single Data Pulse:

The following diagram shows the rise time at the leading edge of the pulse and the fall time at the trailing edge of the pulse. These time durations are generally about the same. Pulse width and magnitude of voltage relative to a normalized pulse height of 100% is illustrated. The greater the rise time, the greater will be the limitation of the data speed that can be passed through the network. The diagram below shows a single pulse with associated rise and fall times.
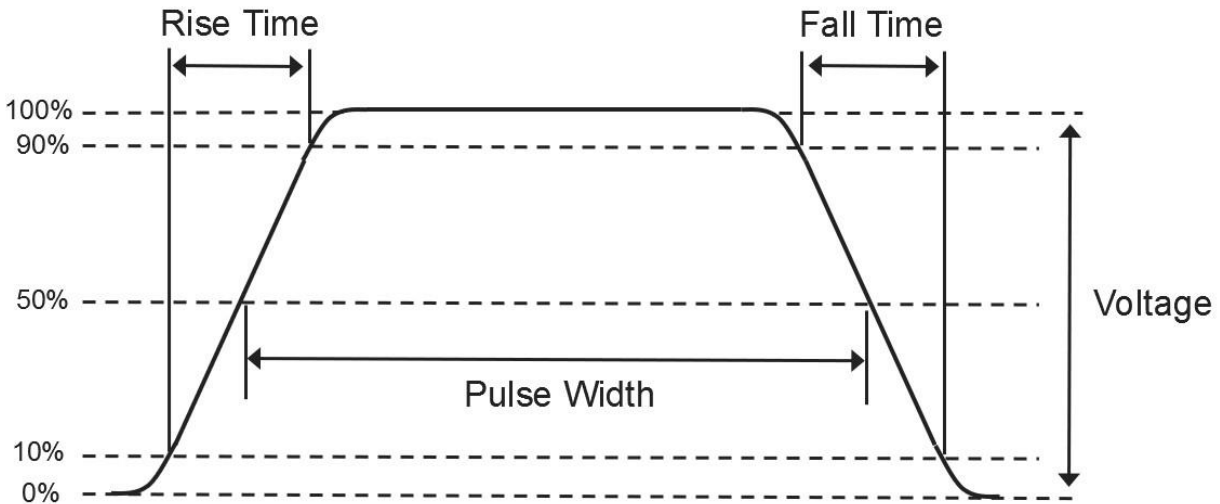
Eye Diagram:

An eye diagram is an important tool that is used to graphically display serial pulse train data. A digitally based oscilloscope at the receiver end of a digital data system Is used to display this pattern. Two or more bit time periods are shown on the horizontal axis. An eye pattern at the upper and lower signal levels are formed as a result of the bit period overlaps. The eye pattern shows the rise and fall time lengthening and rounding as well as jitter disparity. Jitter is the time deviation from the ideal timing of a data-bit event. It shows the time deviations of the transitions of rising and falling pulse edges at their crossing point. This is an important characteristic of high-speed digital data. See the eye diagram figure below.
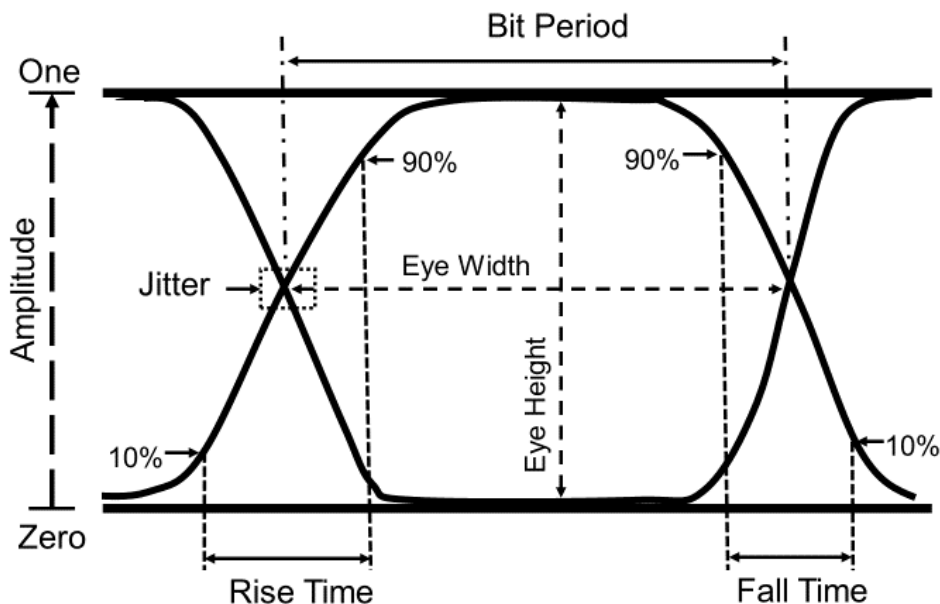
The eye diagram display pattern shows the relationship between time delay and its effect on the eye pattern. The eye should be as open as possible. The ideal textbook eye pattern resembles a rectangular box. As the eye pattern approaches this shape, faster data is achievable as the eye is more opened. If the display reveals a more closed eye pattern, the rate of data that is achievable decreases accordingly.

Conclusion:

Recent worldwide events have led to a sharp increase in video conferencing. This has bolstered the current growth in the signal integrity market and sets the stage for continued future growth. This is especially the case as new networks are created in developing regions while existing networks become more complex to facilitate the increasing bandwidth demands. Ultra-broadband components required for optoelectronics will become even more of a high-volume industry that is greatly driven by less power consumption, smaller EIA outline sizes and optimized performance.

Designing any high-speed digital system requires proper selection of all circuit elements. Maintaining signal integrity is an engineering task of analyzing and mitigating any degradations in the design. This application note points out the importance of evaluating both frequency domain and time domain aspects for specific ultra-broadband designs. It is particularly important in a high-speed data design to consider these factors during component selection.

Future UBC Application Notes:

Attachment Technique:
Eutectic di-bond
Thermo compression
Conductive epoxies
Hand soldering

EM Models:
Lumped Element
Qazi-Distributive
Distributive

Specific Applications:
Transimpedance amplifiers
Mach Zehnder Modulators

Eye Diagrams:
Showing AVX 550 Series Advantages
Compare with competition