Titan S10 EVK

User Manual

CONTENTS

Chapter 1
Overview

This chapter provides an overview of the Titan S10 EVK's Carrier board and installation guide.

1.1 General Description

The Titan S10 Evaluation Kit (EVK) consists of a Titan S10 System on Module (SOM) and a Titan S10 Carrier Board (see **Figure 1-1**). The SOM is installed onto the carrier board via two FMC+ connectors. This design ensures compatibility with Titan S10 SOMs built for either the FMC+ or the standard FMC interface.

This manual focuses primarily on the features, interface specifications, and usage of the Titan S10 Carrier Board. For detailed information regarding the Titan S10 SOM, please refer to the dedicated Titan S10 SOM User Manual.
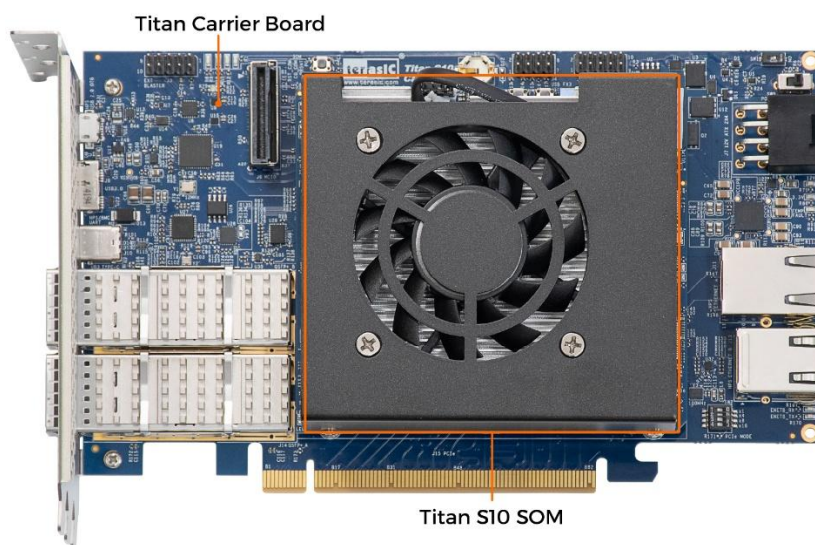

Figure 1-1 The Titan S10 Evaluation Kit

1.2 Key Features

The following hardware is implemented on the Titan S10 Carrier board:

- **Carrier Board System:**
  - PCIe Form Factor: Full Height, ¾ Length
  - On-Board USB Blaster III and 2 x5 JTAG Header
  - 2x3 ATX Power Connector

- Type-C connector for HPS terminal and Board Management
- Interface: FMC+ Connector x2 (for SOM installation)
- Active Heatsink (on SOM)

- Carrier Board FPGA Subsystem:
  - PCIe Gen3 x16
  - Two QSFPDD Ports. Up to 10.3125 Gbps per channel.
  - MCIO x8 Connector for PCIe
  - USB 3.0 Port (USB 3.0 Micro B Connector)
  - Clock source for the Si5341 on SOM
  - 4GB DDR4 (on SOM)

- Carrier Board HPS Subsystem:
  - UART Port (Type-C Connector)
  - Dual Ethernet PHY + RJ45
  - USB 2.0 OTG Port (Micro AB Connector)
  - Battery Holder for RTC
  - 4GB DDR4, 32GB eMMC, RTC, Temperature Sensor and EEPROM (on SOM)

1.3 Block Diagram

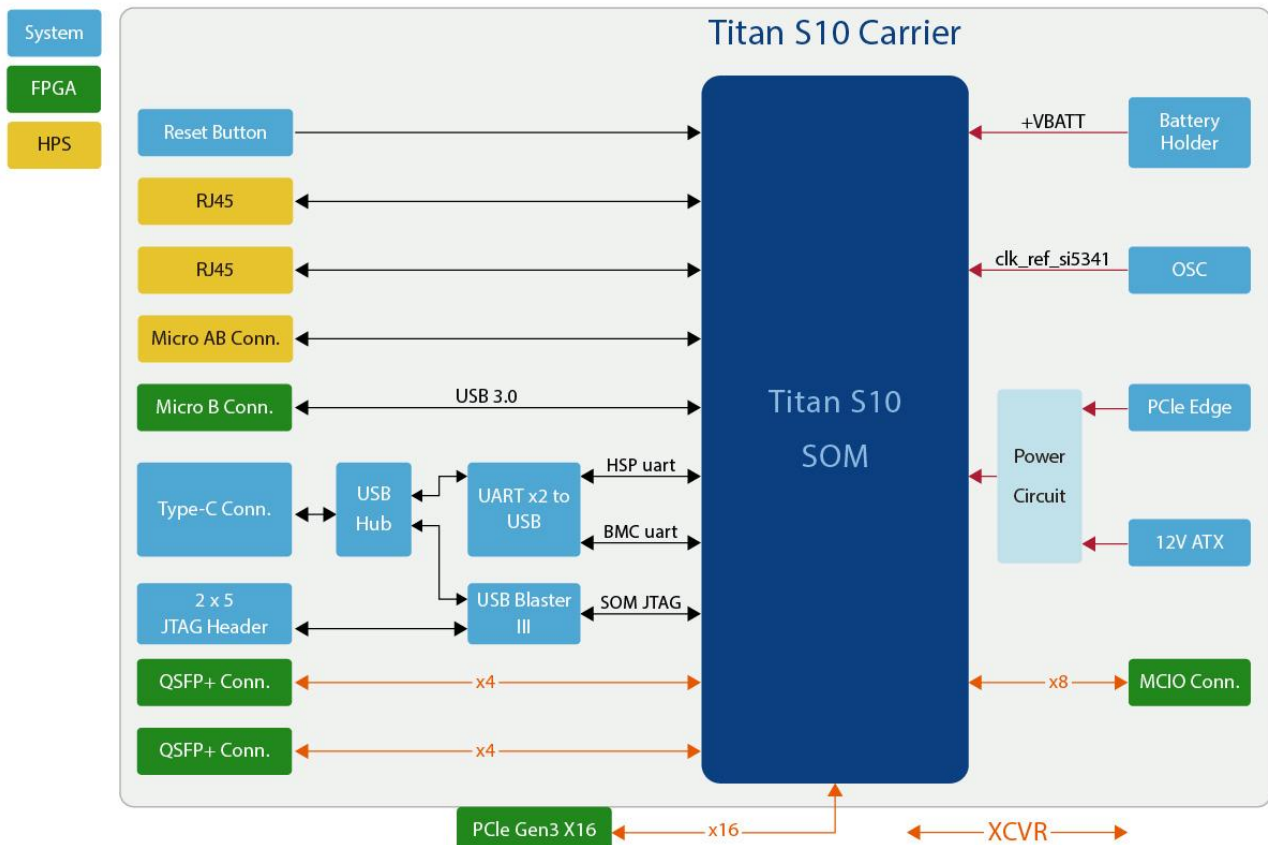**Figure 1-2** shows the block diagram of the Titan S10 Carrier board.

Figure 1-2 Block Diagram of the Titan S10 Carrier Board

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Chapter 2
Board Components

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This chapter introduces all the important components on the Titan S10 Carrier board.

2.1 Overview

Figure 2-1 is the top view of the Titan S10 Carrier board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.
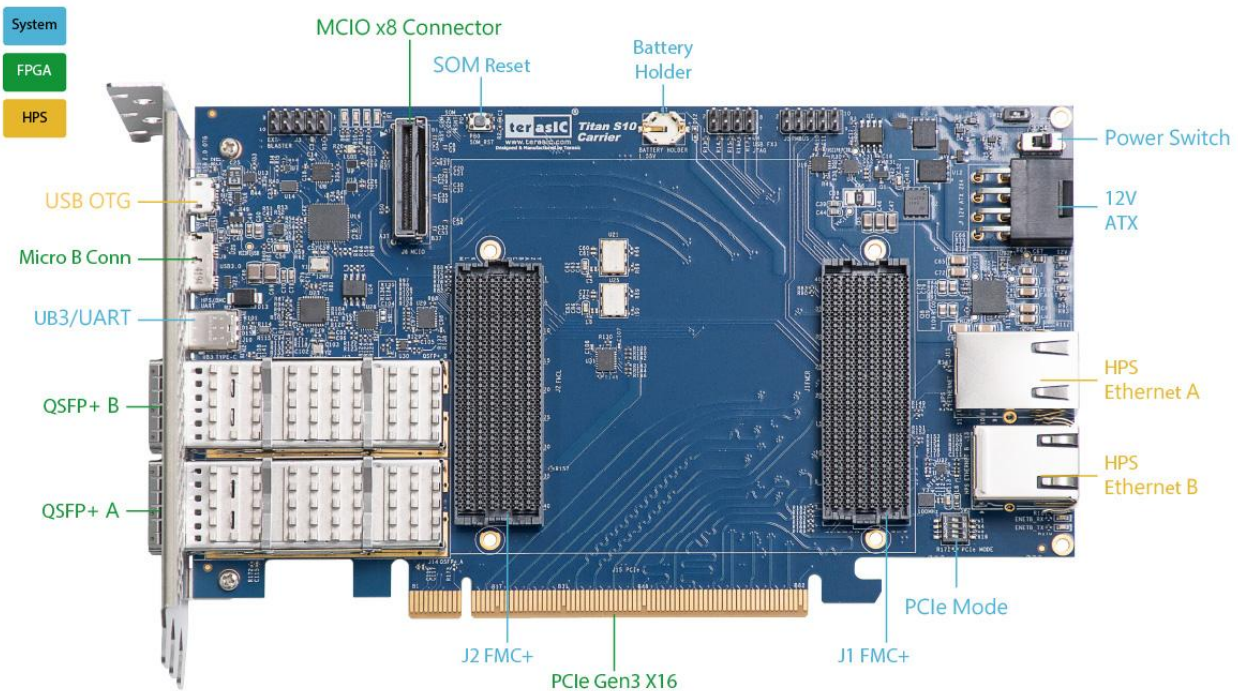

Figure 2-1 Titan S10 Carrier Board (top view)

2.2 Power Input and Switch

This carrier board supports two methods for power input:

- PCIe Slot Power: Power can be supplied directly from the host motherboard's PCIe slot via its +12V rail.

- External Power Supply: Power can be provided by connecting a standalone external power supply unit (PSU) to the onboard 2x4 ATX power connector.

Figure 2-2 illustrates the locations of the PCIe slot, external power connector, power switch, and the Force External Power Switch.

To prevent system instability caused by insufficient power from the PCIe slot, the board is equipped with a protective feature: the "**Force External Power Switch**". This switch ensures the board will not power on unless an external power supply is connected. For more details, please refer to Section 2.3, "**Force External Power Switch**".
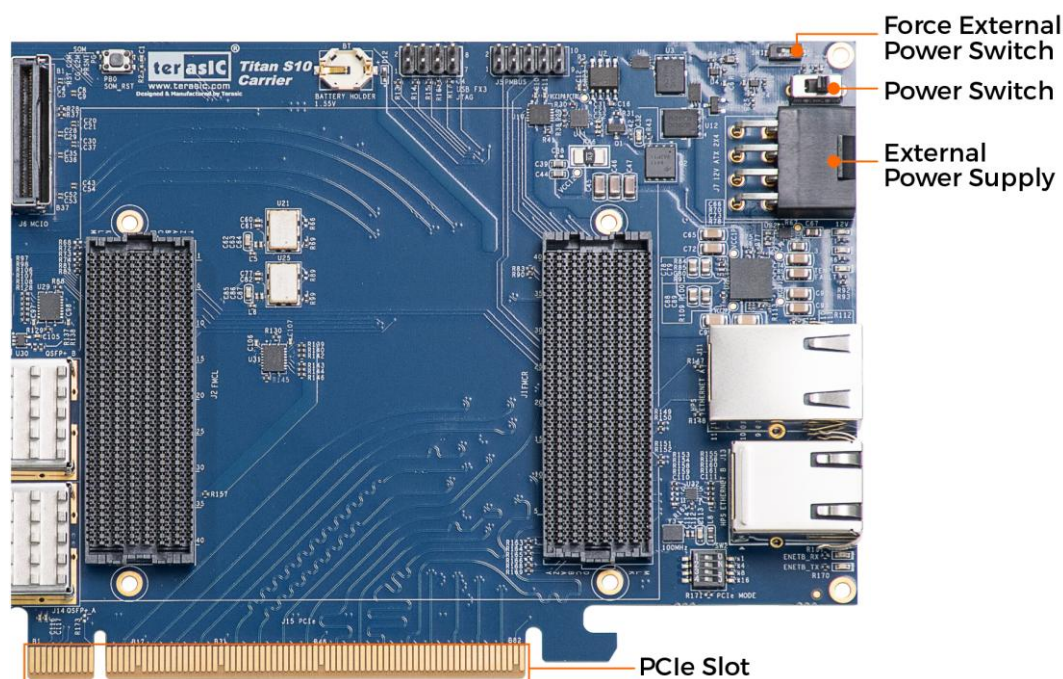
Figure 2-2 Key connectors and switches for power

2.3 Setup and Status Components

This section will introduce the use of the switch for setup on the carrier board, as well as a description of the various status LEDs.

■ **Status LED**

The FPGA development board includes board-specific status LEDs to indicate board status. **Figure 2-3** shows the location of all these status LED. Please refer to **Table 2-1** for the description of the LED indicators and **Table 2-2** for USB blaster III RGB LED

Figure 2-3 Status LED

Figure 2-4 Status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D6	12V	Illuminates when 12-V power is active.

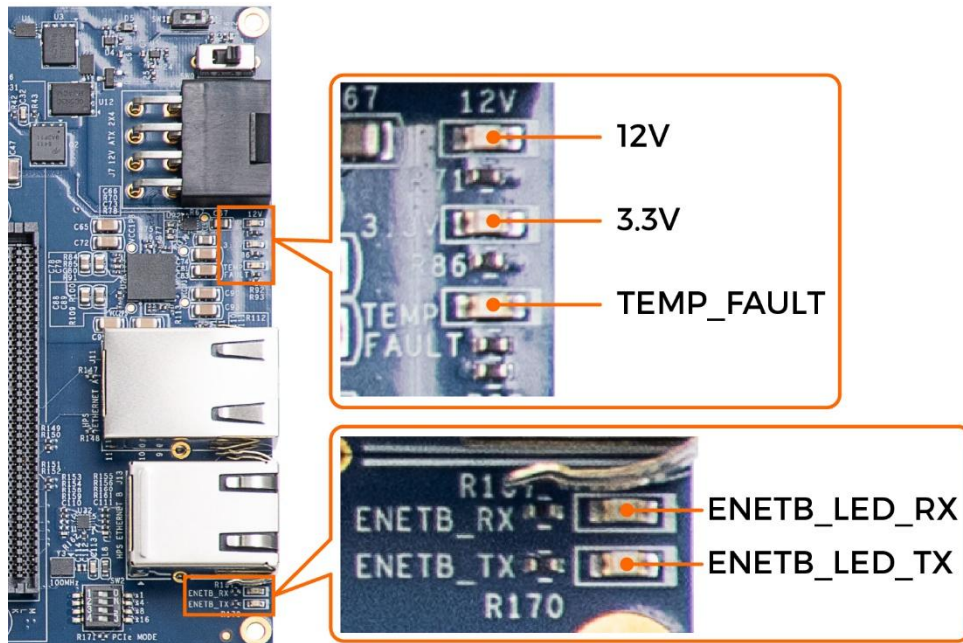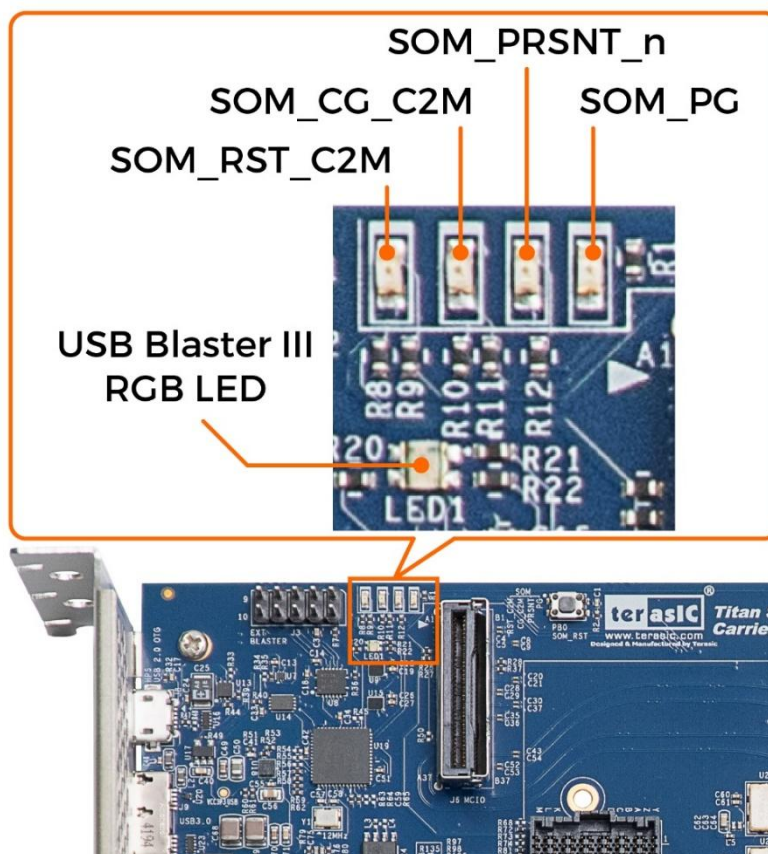| D7	3.3V	Illuminates when 3.3-V power is active.
D8	TEMP_FAULT	Indicates a temperature fault caused by a fan malfunction (e.g., fan speed is too high, too low, or stalled)
D9	ENETB_LED_RX	LED_LINK1000 pin of the Ethernet Port B (88E1111 PHY)
D10	ENETB_LED_TX	LED_LINK100 pin of the Ethernet Port B(88E1111 PHY)
D1	SOM_RST_C2M	When the SOM reset button (PB0) on the carrier board is pressed, this LED will light up.
D2	SOM_CG_C2M	Illuminates when the system MAX 10 FPGA on the SOM is successfully configured and operational.
D3	SOM_PRSNT_n	Illuminates when the SOM is correctly seated on the Carrier Board.
D4	SOM_PG	Illuminates when the SOM power supply is active.

Table 2-2 Status of USB blaster III RGB LED

Color	Meaning
Off	No power / not connected / suspend mode
Blue	Connected, not in use
Green	Connected, an application is using JTAG, no traffic
Green flickering	Connected, data is moving through the JTAG interface
Purple flashing	Identify function has been triggered on this cable

■ **Force External Power Switch**

On the Titan S10 EVK, the power supplied by the PCIe slot alone may be insufficient to meet the demands of all applications, especially when using high-performance compute modules or multiple peripheral devices. This can lead to system instability or boot failures.

To address this potential issue, the board is equipped with a "**Force External Power Switch**". Its function is as follows:

● **Enabled (ON)**: This setting requires that an external 2x4 ATX power supply must be connected for the system to power on. If the switch is enabled but no external power is detected, the system will not boot.

● **Disabled (OFF)**: This setting allows the system to power on using only the power supplied by the PCIe slot.

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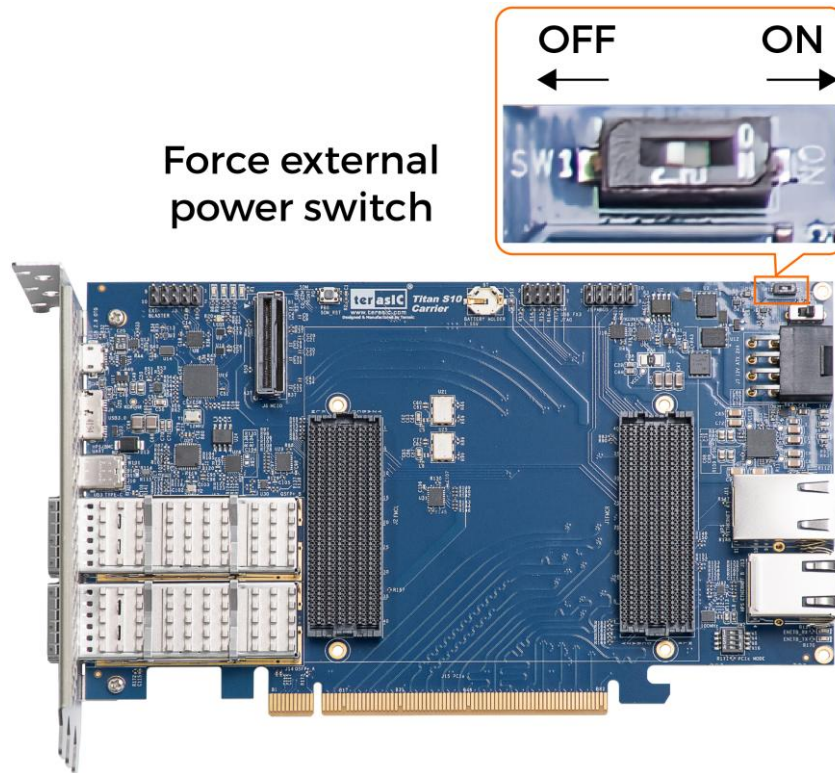
Figure 2-5 Position of the Force External Power Switch

Table 2-3 SW8 PCIe Control DIP Switch

Board Reference	Description	Default Setting
SW1	● Enabled (ON): Requires external 2x4 ATX power to boot; system won't start without it. ● Disabled (OFF): System can boot using only PCIe slot power.	ON

■ PCIe Mode switch

The PCIe Mode switch (SW2) is provided to enable or disable different configurations of the PCIe Connector (See **Figure 2-6**). **Table 2-4** lists the switch controls and description.
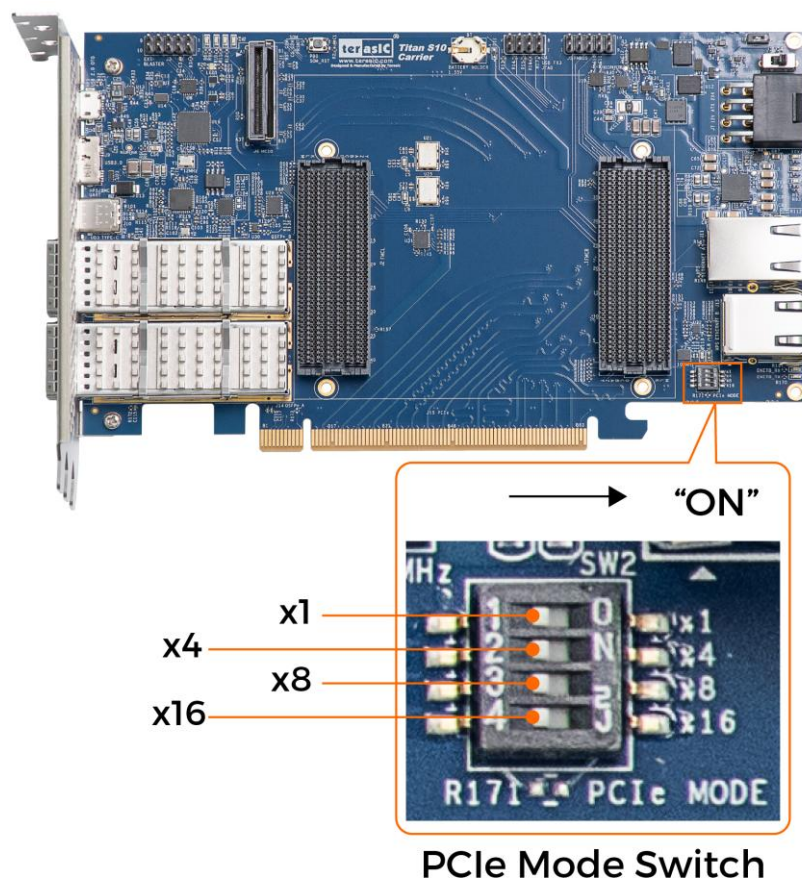
Figure 2-6 Position of the PCIe mode switch

Table 2-4 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default Setting
SW2.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW2.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW2.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	Off
SW2.4	PCIE_PRSNT2n_x16	On : Enable x16 presence detect Off: Disable x16 presence detect	On

2.4 Reset Devices

The board provides a reset button (PB0), SOM_RST, which initiates the following sequence when pressed:

First, a reset signal is sent to the System MAX 10 located on the SOM (via SOM_RST_M2C). The System MAX 10, in turn, asserts the FPGA_RST signal to reset the Stratix 10 FPGA.

Simultaneously, the System MAX 10 sends a reset status signal back to the carrier board via the SOM_RST_C2M line. This illuminates the D1 status LED to provide a visual indication that the system is in a reset state.
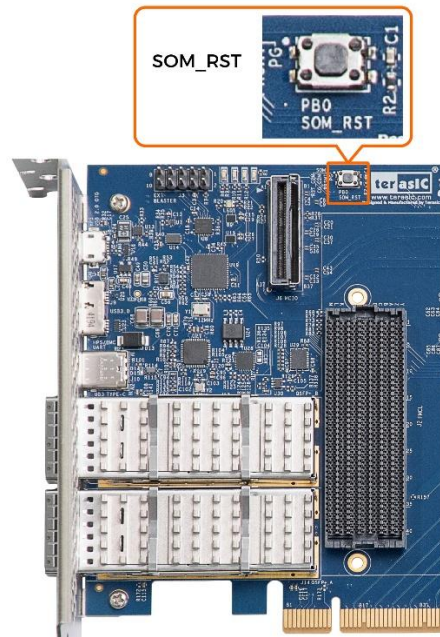
Figure 2-7 Position of the SOM_RST button

2.5 Clock Tree

The clock tree design of the Titan S10 Carrier Board is primarily composed of three onboard oscillators (see **Figure 2-8**). Its purpose is to provide precise reference clocks for the SOM module and high-speed transceiver interfaces. The function of each clock is as follows:

- **100 MHz Clock**: This clock signal (CLK_REF_Si5341_p/n) is routed through pins J2/J3 of the **FMCR** connector to the Si5341 clock synthesizer on the SOM (System on Module), serving as its primary reference clock source.

- **644.53125 MHz Clocks**: Two independent 644.53125 MHz oscillators provide reference clocks to two QSFP interfaces via the **FMCL** connector:
    - One clock signal (QSFPA_REFCLK_p/n) connects to pins L12/L13 of the FMCL to serve as the reference clock for the **QSFPA** interface.
    - The other clock signal connects to pins B20/B21 of the FMCL to serve as the reference clock for the **QSFPB** interface.
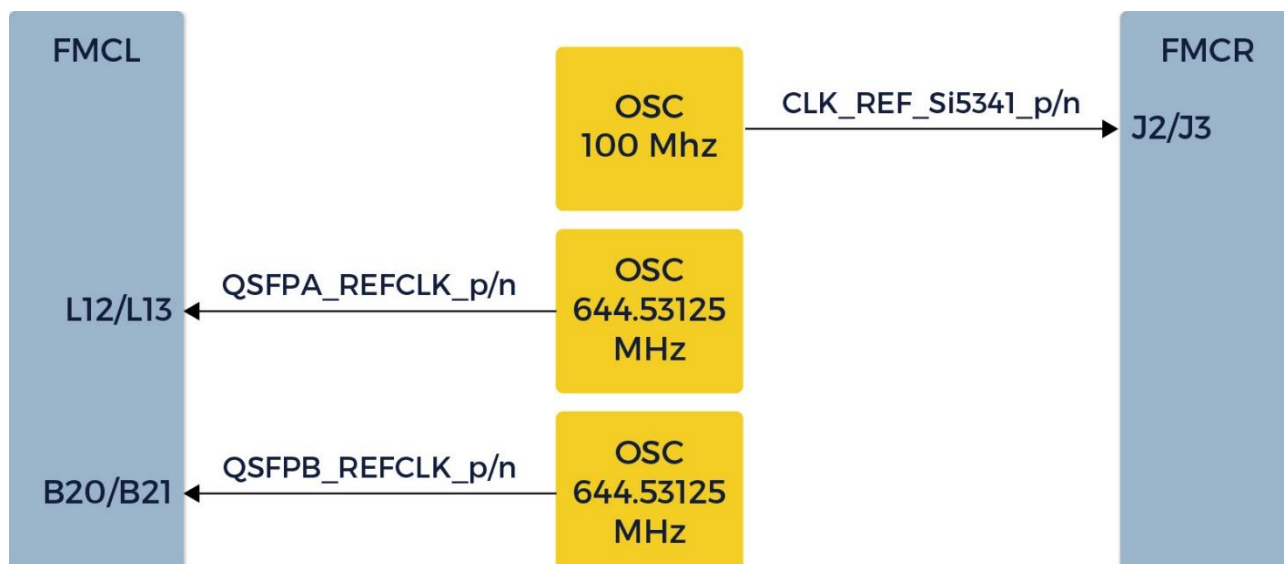
Figure 2-8 Clock tree of the Carrier Board

2.6 USB Blaster III

The board features a built-in Altera USB Blaster III debug circuit. Its USB interface is connected to the USB Type-C port via the on-board USB hub, while the JTAG signals are routed to the SOM (System on Module) through the FMC+ connector.

Please see Getting_Start_Guide_for_Titan_S10_SOM_EVK.pdf for details on installing the USB Blaster III driver.

Additionally, the board provides a 2x5 pin JTAG header for connecting an external JTAG Blaster. **Figure 2-9** provides the block diagram for the on-board USB Blaster III circuitry. **Figure 2-10** shows the physical locations of the USB Type-C connector and the external 2x5 JTAG blaster header.

Note: When an external JTAG Blaster is connected to this header, the on-board USB Blaster III circuit will be automatically disabled, and control of the JTAG bus will be taken over by the external Blaster.
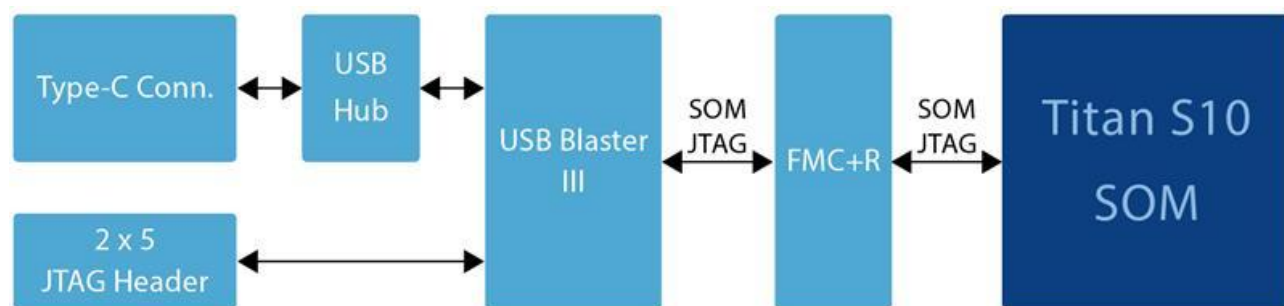
Figure 2-9 Block diagram of the USB Blaster III circuit
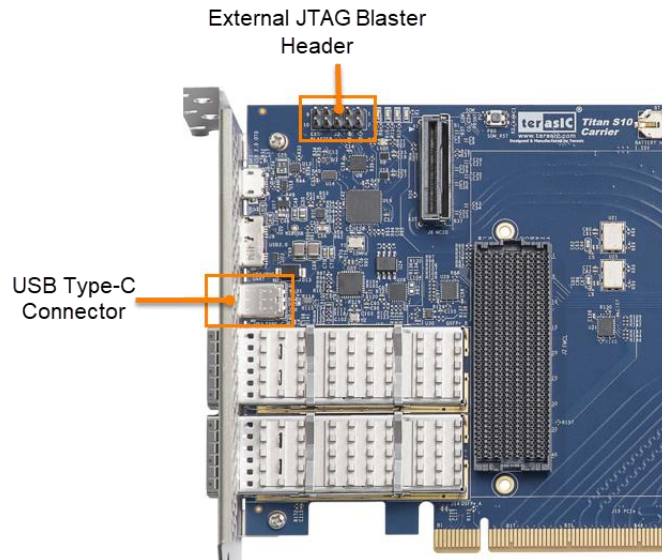
Figure 2-10 Locations of the USB type-C connector and external USB blaster header

2.7 QSFP+ Ports

The carrier board has two independent QSFP+ connectors that use four transceiver channels each from the Stratix 10 FPGA device, and they support up to 10.3125 Gbps per channel. These modules take in serial data from the Stratix 10 FPGA device and transform them to optical signals. The board includes cage assemblies for the QSFP+ connectors. **Figure 2-11** shows the connections between the QSFP+ and Stratix 10 FPGA. The pin assignment QSFP+ connectors and FPGA is listed in **Table 2-5**.

Figure 2-11 Connection between the QSFP+ A/B and Stratix 10 FPGA

Table 2-5 QSFP+ A/B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FMC+ Pin Num.	Titan S10 FPGA Pin Num.

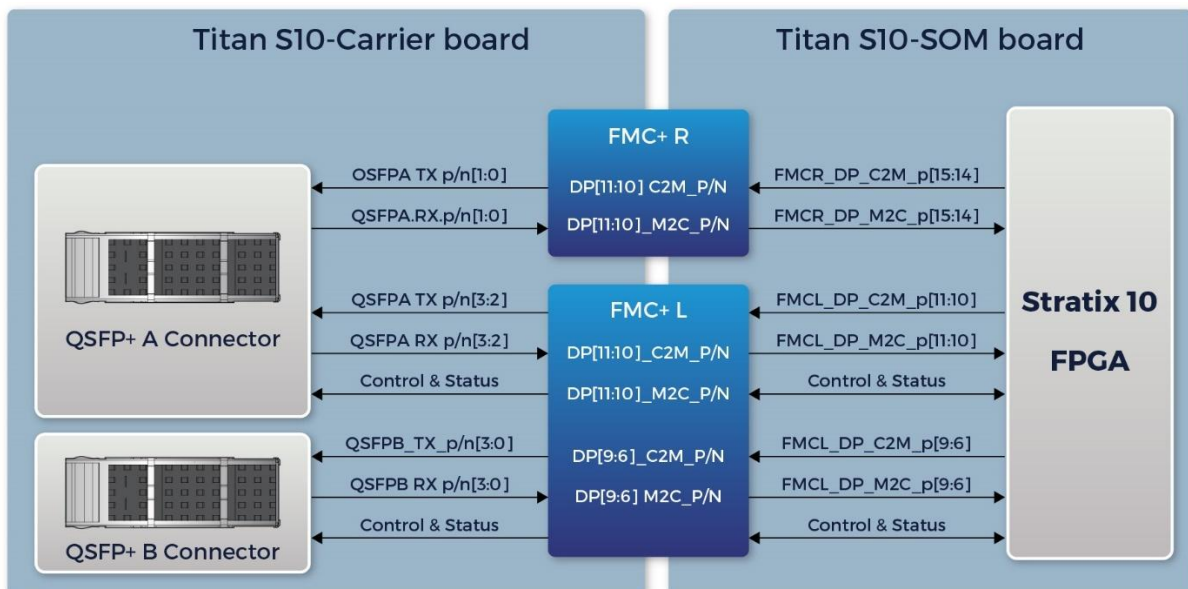| QSFPA_INTERRUPT_n	Interrupt	1.8 V	J2_H8	PIN_V8
QSFPA_LP_MODE	Low Power Mode	1.8 V	J2_H7	PIN_W8
QSFPA_MOD_PRS_n	Module Present	1.8 V	J2_G9	PIN_V12
QSFPA_MOD_SEL_n	Module Select	1.8 V	J2_G6	PIN_W1
QSFPA_RST_n	Module Reset	1.8 V	J2_G7	PIN_V1
QSFPA_SCL	2-wire serial interface clock	1.8 V	J2_D8	PIN_W6
QSFPA_SDA	2-wire serial interface data	1.8 V	J2_D9	PIN_Y6
QSFPA_REFCLK_p	QSFP A transceiver reference clock p	LVDS	J2_L12	PIN_T34
QSFPA_RX_p[0]	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	J1_Y10	PIN_M38
QSFPA_RX_p[1]	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	J1_Z12	PIN_K38
QSFPA_RX_p[2]	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	J2_Z12	PIN_L36
QSFPA_RX_p[3]	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	J2_Y10	PIN_H38
QSFPA_TX_p[0]	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	J1_Z24	PIN_N40
QSFPA_TX_p[1]	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	J1_Y26	PIN_M42
QSFPA_TX_p[2]	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	J2_Y26	PIN_L40
QSFPA_TX_p[3]	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	J2_Z24	PIN_K42
QSFPB_INTERRUPT_n	Interrupt	1.8 V	J2_C11	PIN_U7
QSFPB_LP_MODE	Low Power Mode	1.8 V	J2_C10	PIN_U8
QSFPB_MOD_PRS_n	Module Present	1.8 V	J2_H13	PIN_Y7
QSFPB_MOD_SEL_n	Module Select	1.8 V	J2_H10	PIN_V10
QSFPB_RST_n	Module Reset	1.8 V	J2_H11	PIN_V11
QSFPB_SCL	2-wire serial interface clock	1.8 V	J2_D11	PIN_U10
QSFPB_SDA	2-wire serial interface data	1.8 V	J2_D12	PIN_U9
QSFPB_REFCLK_p	QSFP B transceiver reference clock p	LVDS	J2_B20	PIN_P34
QSFPB_RX_p[0]	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	J2_B4	PIN_J36
QSFPB_RX_p[1]	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	J2_B8	PIN_G36
QSFPB_RX_p[2]	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	J2_B12	PIN_C36
QSFPB_RX_p[3]	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	J2_B16	PIN_E36
QSFPB_TX_p[0]	Transmitter data of channel 0	HSSI	J2_B24	PIN_J40

		DIFFERENTIAL I/O		
QSFPB_TX_p[1]	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	J2_B28	PIN_H42
QSFPB_TX_p[2]	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	J2_B32	PIN_G40
QSFPB_TX_p[3]	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	J2_B36	PIN_F42

2.8 MCIO Connector

This carrier board provides one 74-pin MCIO connector that can be used to connect to Stratix 10 FPGA's 8 H-tile transceiver channels for PCIe Gen3 x8 interface applications. Users can use cable to connect the board to the host and establish PCIe link.

Figure 2-12 shows the connections between the MCIO connector and Stratix 10 FPGA. The pin assignment MCIO connectors and FPGA is listed in **Table 2-6**.
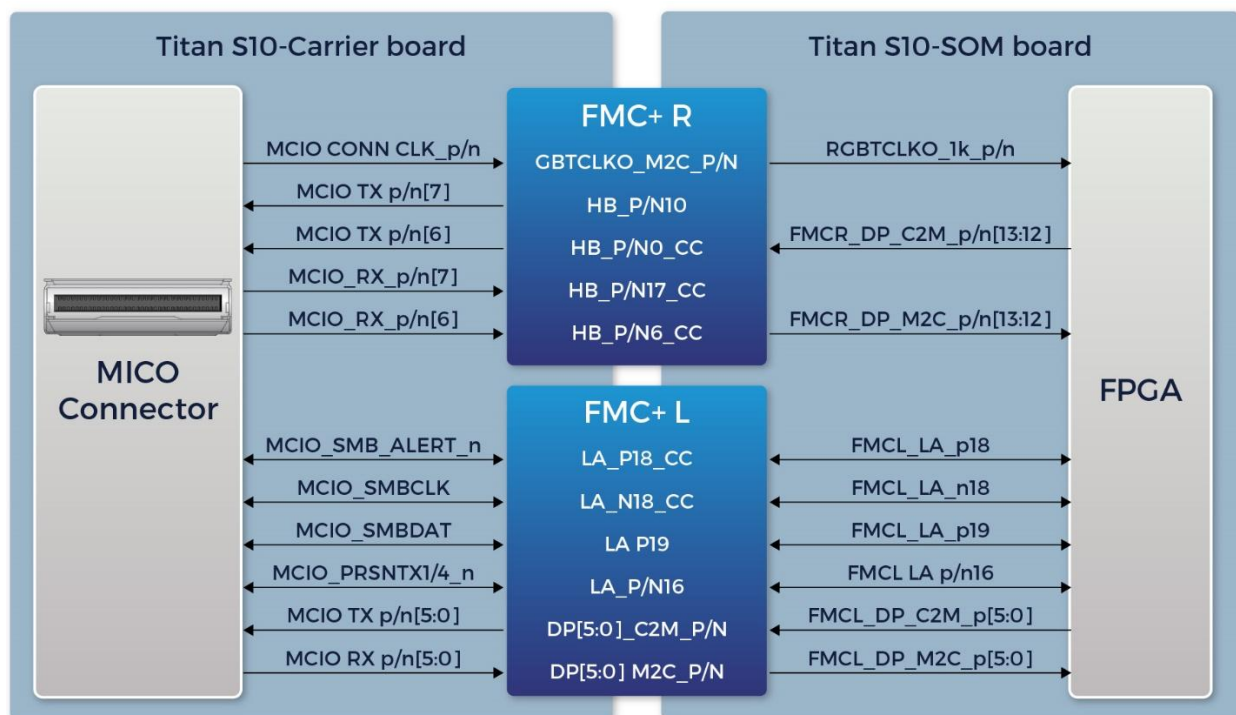
Figure 2-12 Connection between the MCIO connector and Stratix 10 FPGA

Table 2-6 MCIO connector pin assignments, schematic signal names, and functions

Schematic Signal Name	Description	I/O Standard	FMC+ Pin Num.	Titan S10 FPGA Pin Num.
MCIO_PERST_n	PCIe interface reset	3.0-V LVTTL	J2_B40	PIN_AA28
MCIO_SMB_ALERT_n	an interrupt line for devices that want to trade their ability to master	1.8 V	J2_C22	PIN_AJ6
MCIO_CONN_CLK_p	Clock for RootPort mode	HCSL	J1_D4	PIN_Y34

MCIO_SMBCLK	SMB clock	1.8 V	J2_C23	PIN_AJ5
MCIO_SMBDAT	SMB data	1.8 V	J2_H22	PIN_AK2
MCIO_TX_p[0]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_A38	PIN_AA40
MCIO_TX_p[1]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_A34	PIN_Y42
MCIO_TX_p[2]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_A30	PIN_W40
MCIO_TX_p[3]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_A26	PIN_V42
MCIO_TX_p[4]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_A22	PIN_U40
MCIO_TX_p[5]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J2_C2	PIN_T42
MCIO_TX_p[6]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J1_K24	PIN_R40
MCIO_TX_p[7]	MCIO transmit bus	HSSI DIFFERENTIAL I/O	J1_K32	PIN_P42
MCIO_RX_p[0]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_A18	PIN_W36
MCIO_RX_p[1]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_A14	PIN_Y38
MCIO_RX_p[2]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_A10	PIN_U36
MCIO_RX_p[3]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_A6	PIN_V38
MCIO_RX_p[4]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_A2	PIN_T38
MCIO_RX_p[5]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J2_C6	PIN_R36
MCIO_RX_p[6]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J1_K28	PIN_P38
MCIO_RX_p[7]	MCIO receive bus	CURRENT MODE LOGIC (CML)	J1_K36	PIN_N36

2.9 Gigabit Ethernet

The carrier board provides two RJ-45 connectors for HPS application. Micrel KSZ9031RNX PHY chip on Titan S10 SoM is used for RJ-45 A connector, it integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. Marvell 88E1111 PHY chip on Titan S10 SoM is used for RJ-45 B connector, SGMII AC coupling interface is used between PHY and FPGA transceiver.

Figure 2-13 shows the connections between the Titan S10 SoM module, FMC+ connector and RJ-45 connectors. The pin assignment of Ethernet PHYs and HPS is listed in **Table 2-7**.
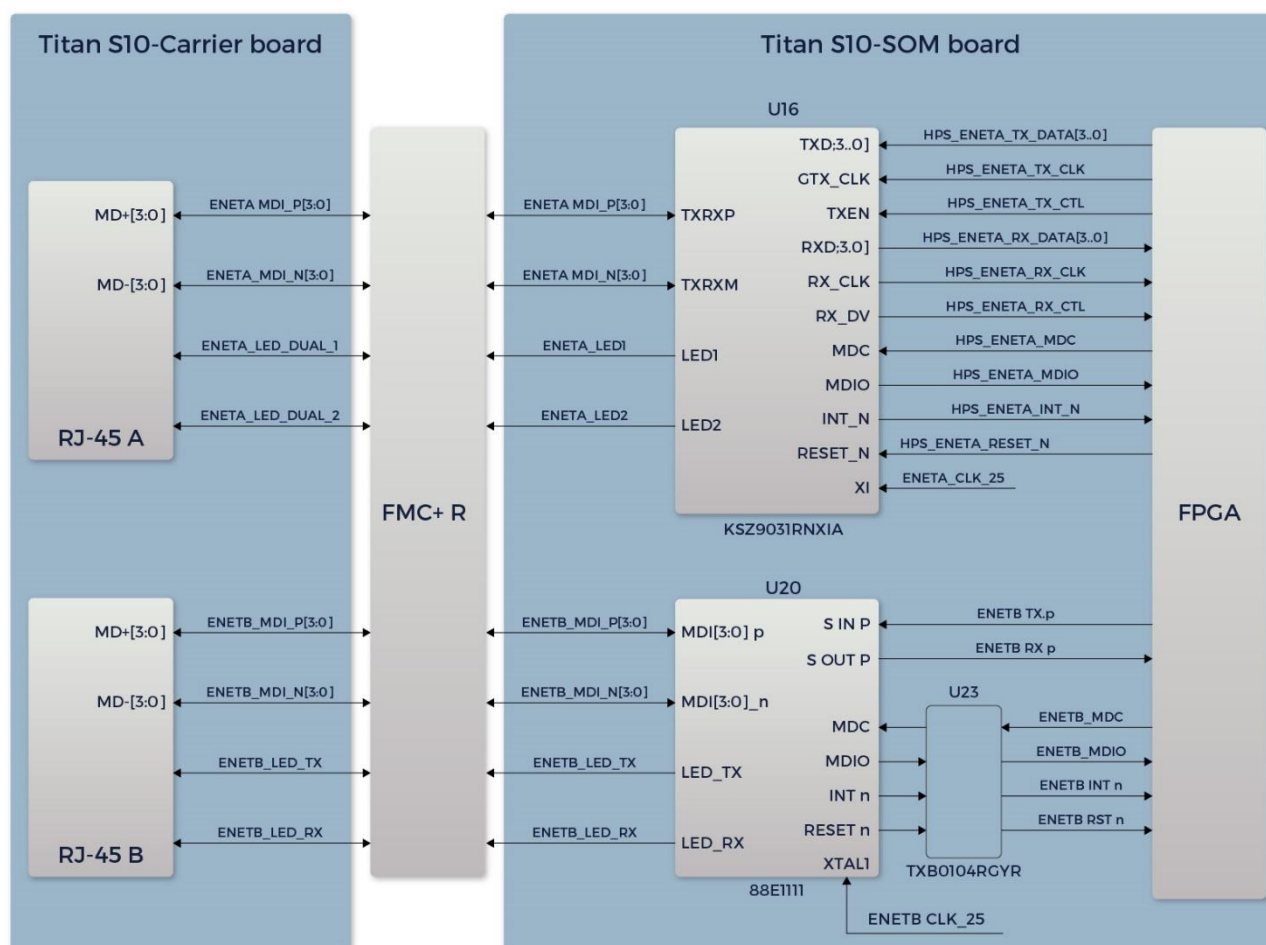
Figure 2-13 Connection between the RJ45 connectors and Stratix 10 FPGA

Table 2-7 Pin Assignment of Gigabit Ethernet PHY and HPS on Titan S10 SoM

Schematic Signal Name	Description	I/O Standard	Titan S10 FPGA Pin Num.
HPS_ENETA_MDC	Management Data Clock Reference	1.8 V	PIN_B20
HPS_ENETA_MDIO	Management Data	1.8 V	PIN_R19
HPS_ENETA_RX_CLK	GMII and MII receive clock	1.8 V	PIN_B10
HPS_ENETA_RX_CTL	GMII and MII receive data valid	1.8 V	PIN_A17
HPS_ENETA_RX_DATA[0]	GMII and MII receive data[0]	1.8 V	PIN_B9
HPS_ENETA_RX_DATA[1]	GMII and MII receive data[1]	1.8 V	PIN_A20
HPS_ENETA_RX_DATA[2]	GMII and MII receive data[2]	1.8 V	PIN_B19
HPS_ENETA_RX_DATA[3]	GMII and MII receive data[3]	1.8 V	PIN_B8
HPS_ENETA_TX_CLK	GMII and MII transmit clock	1.8 V	PIN_A19
HPS_ENETA_TX_CTL	GMII and MII transmit data valid	1.8 V	PIN_C17
HPS_ENETA_TX_DATA[0]	GMII and MII transmit data[0]	1.8 V	PIN_A9

HPS_ENETA_TX_DATA[1]	GMII and MII transmit data[1]	1.8 V	PIN_B18
HPS_ENETA_TX_DATA[2]	GMII and MII transmit data[2]	1.8 V	PIN_B12
HPS_ENETA_TX_DATA[3]	GMII and MII transmit data[3]	1.8 V	PIN_C15
ENETB_REFCLK_p	Management Data Clock Reference	LVDS	PIN_AD34
ENETB_TX_p	SGMII TX data	HSSI DIFFERENTIAL I/O	PIN_AB42
ENETB_RX_p	SGMII RX data	HSSI DIFFERENTIAL I/O	PIN_AA36
ENETB_INT_n	Management bus interrupt	1.8 V	PIN_E9
ENETB_MDC	Management bus control	1.8 V	PIN_E8
ENETB_MDIO	Management bus data	1.8 V	PIN_A6
ENETB_RST_n	Device reset	1.8 V	PIN_A7

There are four LEDs, two green LEDs(LEDG) and two yellow LEDs(LEDY), which represent the status of Ethernet PHY. The LED control signals are connected to the LEDs on the RJ45 connector. The state and definition of LEDG and LEDY are listed **Table 2-8.** For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-8 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	10 Link / Activity (RX, TX)

2.10 USB OTG Connector

The carrier board provides an USB OTG interfaces, a SMSC USB3320 device in a 32-pin QFN package device on Titan S10 SoM is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Micro-USB interface. **Figure 2-14** shows the connections between the carrier board, FMC+ connector and USB OTG connector. Table 2-9 lists the pin assignment of USB OTG PHY to HPS.
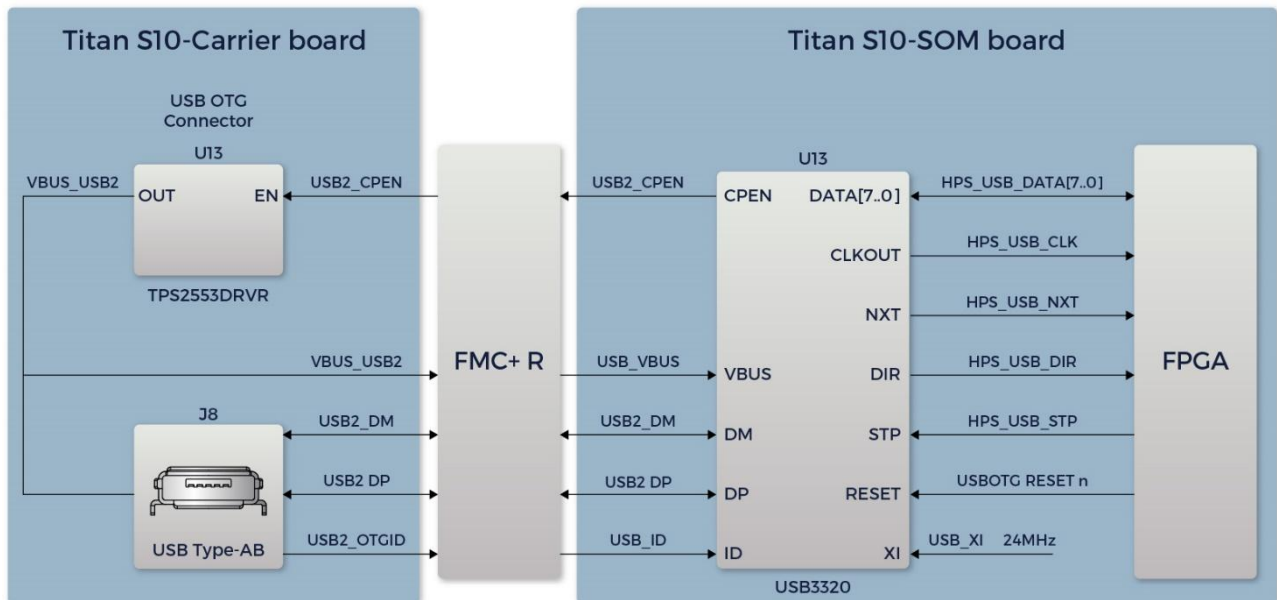
Figure 2-14 Connection between the USB OTG connector and Stratix 10 FPGA

Table 2-9 The pin assignment of USB OTG PHY to HPS on the Titan Carrier board

Schematic Signal Name	Description	I/O Standard	Titan S10 FPGA Pin Num.
HPS_USB_CLK	Reference Clock Output	1.8 V	PIN_A15
HPS_USB_DATA[0]	HPS USB_DATA[0]	1.8 V	PIN_A11
HPS_USB_DATA[1]	HPS USB_DATA[1]	1.8 V	PIN_B13
HPS_USB_DATA[2]	HPS USB_DATA[2]	1.8 V	PIN_B14
HPS_USB_DATA[3]	HPS USB_DATA[3]	1.8 V	PIN_B17
HPS_USB_DATA[4]	HPS USB_DATA[4]	1.8 V	PIN_A10
HPS_USB_DATA[5]	HPS USB_DATA[5]	1.8 V	PIN_A16
HPS_USB_DATA[6]	HPS USB_DATA[6]	1.8 V	PIN_A12
HPS_USB_DATA[7]	HPS USB_DATA[7]	1.8 V	PIN_C16
HPS_USB_DIR	Direction of the Data Bus	1.8 V	PIN_C18
HPS_USB_NXT	Throttle the Data	1.8 V	PIN_A14
HPS_USB_STP	Stop Data Stream on the Bus	1.8 V	PIN_B15

2.11 USB 3.0 Device

As shown in **Figure 2-12**, the USB 3.0 Micro-B connector on the carrier board routes its USB 3.0 signals through the FMC+ connector to the Titan S10 SOM. On the SOM, these signals connect to an Infineon EZ-USB FX3™ (CYUSB301x) SuperSpeed USB peripheral controller. This controller acts as a bridge, handling USB 3.0 communication.

Finally, the FX3 connects directly to the Stratix 10 FPGA's I/O via its 32-bit General Programmable Interface II (GPIF II), establishing a high-speed parallel data channel. **Table 2-10** list the pin assignment of Cypress USB 3.0 Controller.
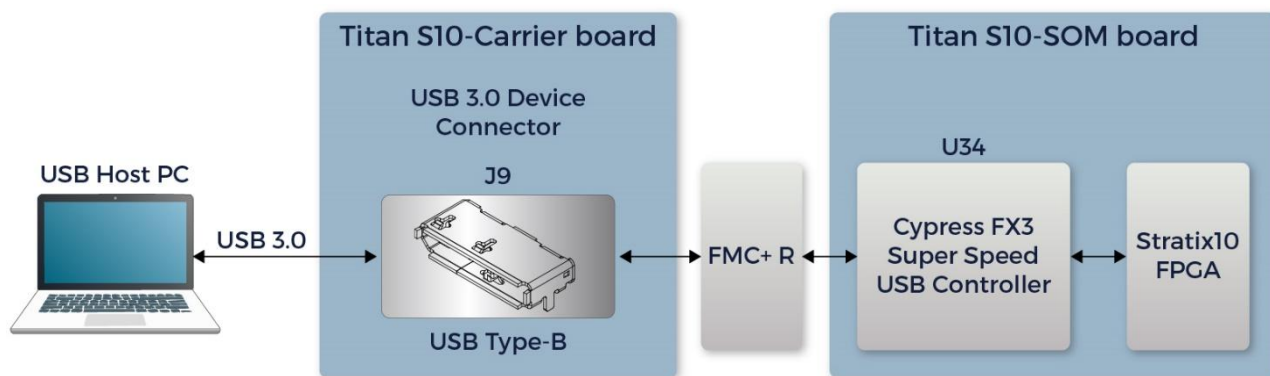
Figure 2-15 Connection between the USB 3.0 connector and Stratix 10 FPGA

Table 2-10 Pin Assignment of Cypress USB Controller and FPGA on Titan S10 SoM

Schematic Signal Name	Description	I/O Standard	Titan S10 FPGA Pin Num.
USBFX3_RESET_n	FX3 reset	1.8 V	PIN_AW11
USBFX3_PCLK	FX3 clock	1.8 V	PIN_AV6
USBFX3_CTL0_SLCS_n	GPIF II Control Bus 0	1.8 V	PIN_AR3
USBFX3_UART_TX	USB to UART transmitter	1.8 V	PIN_AW1
USBFX3_UART_RX	USB to UART receiver	1.8 V	PIN_AU2
USBFX3_CTL1_SLWR_n	GPIF II Control Bus 1	1.8 V	PIN_AW9
USBFX3_CTL2_SLOE_n	GPIF II Control Bus 2	1.8 V	PIN_AV7
USBFX3_CTL3_SLRD_n	GPIF II Control Bus 3	1.8 V	PIN_AV10
USBFX3_CTL4_FLAGA	GPIF II Control Bus 4	1.8 V	PIN_AR4
USBFX3_CTL5_FLAGB	GPIF II Control Bus 5	1.8 V	PIN_AV2
USBFX3_CTL6_FLAGC	GPIF II Control Bus 6	1.8 V	PIN_AU3
USBFX3_CTL7_PKTEND_n	GPIF II Control Bus 7	1.8 V	PIN_AV3
USBFX3_CTL8_FLAGD	GPIF II Control Bus 8	1.8 V	PIN_AW10
USBFX3_CTL9	GPIF II Control Bus 9	1.8 V	PIN_AU10
USBFX3_CTL10	GPIF II Control Bus 10	1.8 V	PIN_AV11
USBFX3_CTL11_A1	GPIF II Control Bus 11	1.8 V	PIN_AV12
USBFX3_CTL12_A0	GPIF II Control Bus 12	1.8 V	PIN_AV5
USBFX3_CTL15_INT_n	GPIF II Control Bus 15	1.8 V	PIN_AP4
USBFX3_DQ[0]	GPIF II Data Bus 0	1.8 V	PIN_BA5
USBFX3_DQ[1]	GPIF II Data Bus 1	1.8 V	PIN_BB5
USBFX3_DQ[2]	GPIF II Data Bus 2	1.8 V	PIN_BA4
USBFX3_DQ[3]	GPIF II Data Bus 3	1.8 V	PIN_BB4
USBFX3_DQ[4]	GPIF II Data Bus 4	1.8 V	PIN_AW5
USBFX3_DQ[5]	GPIF II Data Bus 5	1.8 V	PIN_AU5
USBFX3_DQ[6]	GPIF II Data Bus 6	1.8 V	PIN_AY4
USBFX3_DQ[7]	GPIF II Data Bus 7	1.8 V	PIN_AW4
USBFX3_DQ[8]	GPIF II Data Bus 8	1.8 V	PIN_AW3
USBFX3_DQ[9]	GPIF II Data Bus 9	1.8 V	PIN_AY3

USBFX3_DQ[10]	GPIF II Data Bus 10	1.8 V	PIN_AY6
USBFX3_DQ[11]	GPIF II Data Bus 11	1.8 V	PIN_AY7
USBFX3_DQ[12]	GPIF II Data Bus 12	1.8 V	PIN_AU4
USBFX3_DQ[13]	GPIF II Data Bus 13	1.8 V	PIN_BA2
USBFX3_DQ[14]	GPIF II Data Bus 14	1.8 V	PIN_AY2
USBFX3_DQ[15]	GPIF II Data Bus 15	1.8 V	PIN_AV1
USBFX3_DQ[16]	GPIF II Data Bus 16	1.8 V	PIN_AW8
USBFX3_DQ[17]	GPIF II Data Bus 17	1.8 V	PIN_AT7
USBFX3_DQ[18]	GPIF II Data Bus 18	1.8 V	PIN_AU7
USBFX3_DQ[19]	GPIF II Data Bus 19	1.8 V	PIN_AW6
USBFX3_DQ[20]	GPIF II Data Bus 20	1.8 V	PIN_AT9
USBFX3_DQ[21]	GPIF II Data Bus 21	1.8 V	PIN_AU9
USBFX3_DQ[22]	GPIF II Data Bus 22	1.8 V	PIN_AU8
USBFX3_DQ[23]	GPIF II Data Bus 23	1.8 V	PIN_AT10
USBFX3_DQ[24]	GPIF II Data Bus 24	1.8 V	PIN_AT11
USBFX3_DQ[25]	GPIF II Data Bus 25	1.8 V	PIN_AT12
USBFX3_DQ[26]	GPIF II Data Bus 26	1.8 V	PIN_AR11
USBFX3_DQ[27]	GPIF II Data Bus 27	1.8 V	PIN_AR12
USBFX3_DQ[28]	GPIF II Data Bus 28	1.8 V	PIN_AR13
USBFX3_DQ[29]	GPIF II Data Bus 29	1.8 V	PIN_AP13
USBFX3_DQ[30]	GPIF II Data Bus 30	1.8 V	PIN_AU12
USBFX3_DQ[31]	GPIF II Data Bus 31	1.8 V	PIN_AU13
USBFX3_OTG_ID	OTG ID pin	1.8 V	PIN_AP3

■ FX3 JTAG Header

The Cypress FX3 JTAG interface is used for direct, low-level programming and in-circuit debugging of the controller's internal ARM core. This requires connecting an external JTAG programmer or a compatible hardware debugger probe to the designated pins on the board.
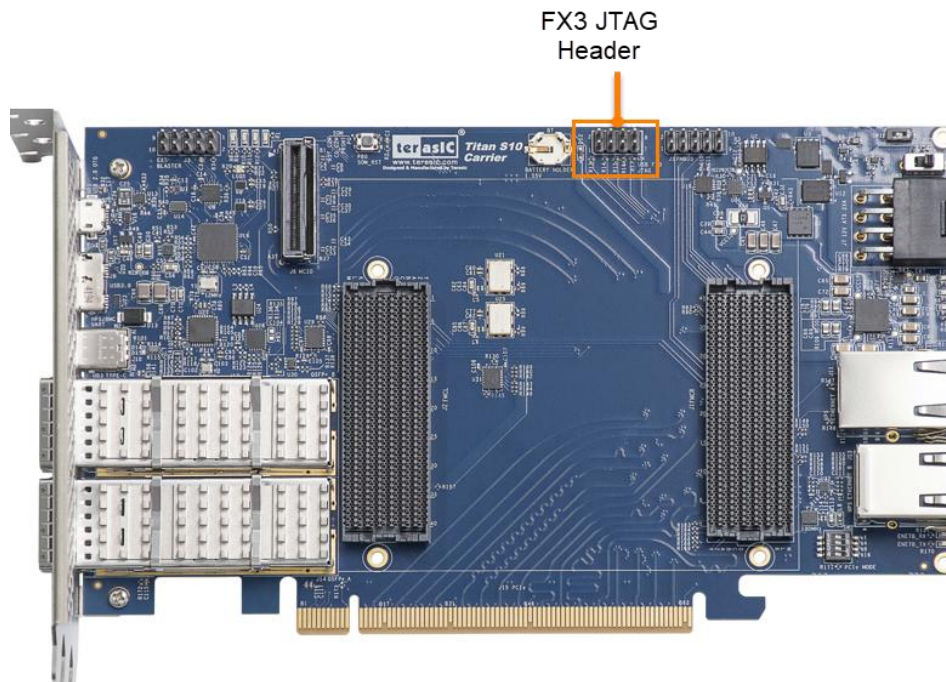
Figure 2-16 Position of the FX3 JTAG header

2.12 PCI Express

The carrier board features a PCI Express edge connector designed for a standard x16 PCIe slot on a PC motherboard. When populated with the SOM, the board provides a fully integrated, PCI Express 3.0 compliant solution by leveraging the device's built-in transceivers and dedicated Hard IP (HIP) block.

This HIP approach simplifies protocol implementation and conserves logic resources for your application. The interface supports multi-lane configurations (x1, x4, x8, and x16) and is compatible with Gen1 (2.5 Gbps/lane), Gen2 (5.0 Gbps/lane), and Gen3 (8.0 Gbps/lane) data rates. Lane width is user-configurable via a DIP switch (SW2), as detailed in Section 2.3: PCIe Mode Switch.

For power, while the board receives baseline power from the PCIe slot, it is mandatory to connect the external 2x4 ATX power connector. This auxiliary power is essential to prevent system instability or permanent FPGA damage due to insufficient power.

Figure 2-17 shows the connections between the PCIe and Stratix 10 FPGA. **Table 2-11** lists the pin assignment of PCIe and Stratix 10 FPGA.
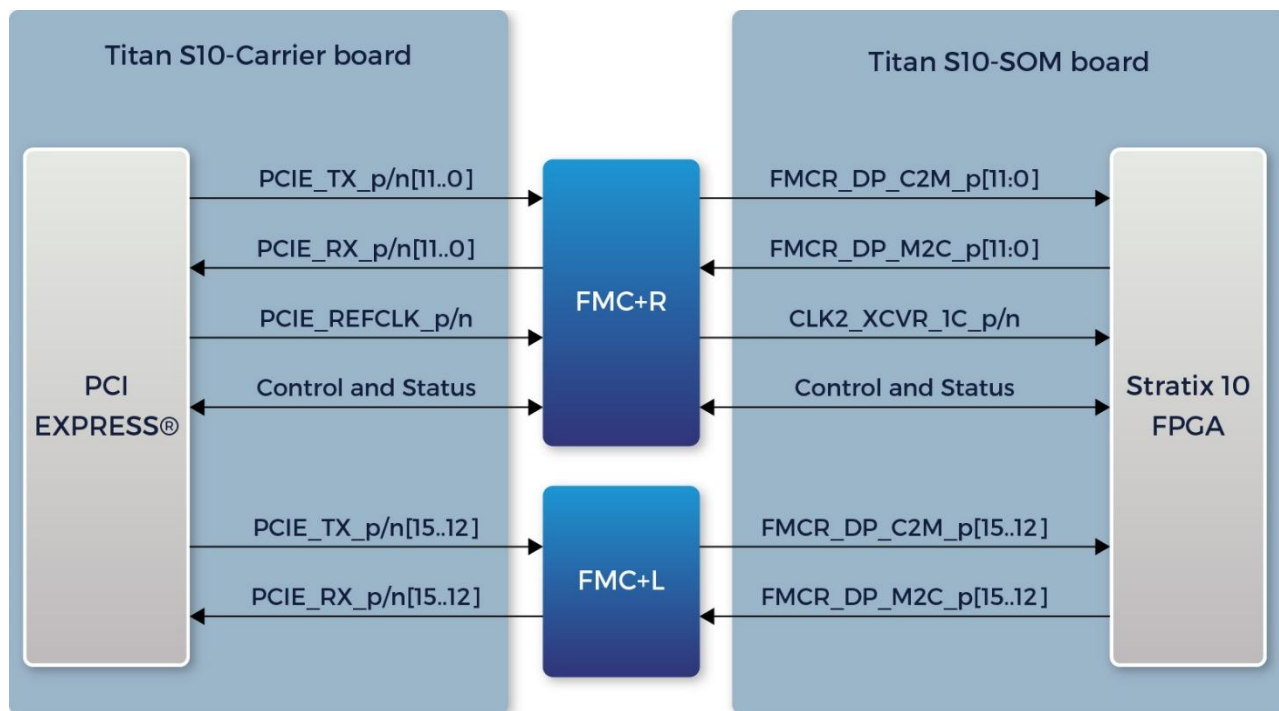
Figure 2-17 Connection between the PCIe edge connector and Stratix 10 FPGA

Table 2-11 Pin Assignment of PCIe and FPGA on Titan S10 SoM

Schematic Signal Name	Description	I/O Standard	FMC+ Pin Num.	Titan S10 FPGA Pin Num.
PCIE_TX_p0	Add-in card transmit bus	HIGH Speed Differential I/O	J1_A34	PIN_BB34
PCIE_TX_p1	Add-in card transmit bus	HIGH Speed Differential I/O	J1_A38	PIN_BA36
PCIE_TX_p2	Add-in card transmit bus	HIGH Speed Differential I/O	J1_B36	PIN_BB38
PCIE_TX_p3	Add-in card transmit bus	HIGH Speed Differential I/O	J1_B32	PIN_AY38
PCIE_TX_p4	Add-in card transmit bus	HIGH Speed Differential I/O	J1_B28	PIN_BA40
PCIE_TX_p5	Add-in card transmit bus	HIGH Speed Differential I/O	J1_B24	PIN_AV38
PCIE_TX_p6	Add-in card transmit bus	HIGH Speed Differential I/O	J1_K8	PIN_AW40
PCIE_TX_p7	Add-in card transmit bus	HIGH Speed Differential I/O	J1_K16	PIN_AV42
PCIE_TX_p8	Add-in card transmit bus	HIGH Speed Differential I/O	J1_C2	PIN_AU40
PCIE_TX_p9	Add-in card transmit bus	HIGH Speed Differential I/O	J1_A22	PIN_AT42
PCIE_TX_p10	Add-in card transmit bus	HIGH Speed Differential I/O	J1_A26	PIN_AR40

PCIE_TX_p11	Add-in card transmit bus	HIGH Speed Differential I/O	J1_A30	PIN_AP42
PCIE_TX_p12	Add-in card transmit bus	HIGH Speed Differential I/O	J2_M22	PIN_AN40
PCIE_TX_p13	Add-in card transmit bus	HIGH Speed Differential I/O	J2_M18	PIN_AM42
PCIE_TX_p14	Add-in card transmit bus	HIGH Speed Differential I/O	J2_Y30	PIN_AL40
PCIE_TX_p15	Add-in card transmit bus	HIGH Speed Differential I/O	J2_Z28	PIN_AK42
PCIE_RX_p0	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_A14	PIN_AV30
PCIE_RX_p1	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_A18	PIN_AY30
PCIE_RX_p2	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_B16	PIN_BB30
PCIE_RX_p3	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_B12	PIN_AW32
PCIE_RX_p4	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_B8	PIN_BA32
PCIE_RX_p5	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_B4	PIN_AY34
PCIE_RX_p6	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_K12	PIN_AU36
PCIE_RX_p7	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_K20	PIN_AW36
PCIE_RX_p8	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_C6	PIN_AR36
PCIE_RX_p9	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_B8	PIN_AN36
PCIE_RX_p10	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_A2	PIN_AT38
PCIE_RX_p11	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J1_A6	PIN_AP38
PCIE_RX_p12	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J2_Y22	PIN_AL36
PCIE_RX_p13	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J2_Y18	PIN_AM38
PCIE_RX_p14	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J2_Z16	PIN_AK38
PCIE_RX_p15	Add-in card receive bus	CURRENT MODE LOGIC (CML)	J2_Y14	PIN_AJ36
PCIE_SMBCLK	PCIe system management nus clock	1.8 V	J1_C30	PIN_AP8

PCIE_SMBDAT	PCIe system management Bus data	1.8 V	J1_C30	PIN_AP10
PCIE_REFCLK_p	PCIe reference clock, positive (Differential)	HCSL	J1_H13	PIN_AT34
PCIE_PERST_n	PCIe fundamental reset, cctive Low	3.0-V LVTTL	J1_J18	PIN_AC26

2.13 USB to UART

As shown in the block diagram in **Figure 2-18**, the board provides two independent UART (Universal Asynchronous Receiver-Transmitter) communication interfaces through a single USB Type-C port, allowing users to conveniently interact with the system. These two interfaces are enabled by an on-board Silicon Labs CP2105 USB-to-Dual-UART Bridge Controller.

When the development board is connected to a computer via the USB Type-C cable, two virtual COM ports will appear in the computer's Device Manager. Their functions are as follows:

- **HPS UART**: This interface is primarily used for communication with the HPS (Hard Processor System) on the SOM. It allows users to access the HPS console, view boot messages, execute Linux commands, and perform software debugging. This serves as the primary channel for interacting with the operating system.

- **BMC UART**: This interface is used for communication with the BMC (Board Management Controller) in the system MAX10 FPGA of the SOM. The BMC is responsible for monitoring and managing the board's hardware status, such as power, temperature, and fan speed.

For instructions on how to install the drivers for these two UART interfaces, please refer to Getting_Start_Guide_for_Titan_S10_SOM_EVK.pdf.

Note: The signal from the USB Type-C connector is first routed to a USB Hub. It then branches out to the CP2105 (providing the dual UART function) and the USB Blaster III circuit.
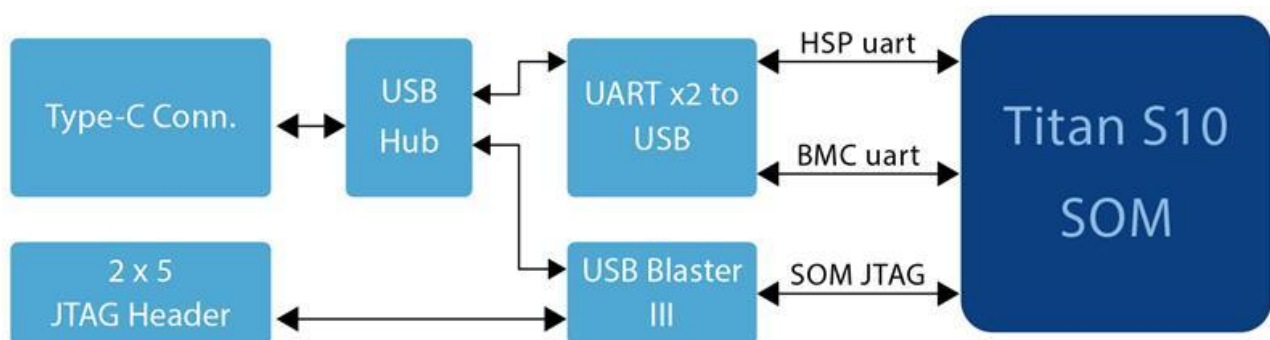

Figure 2-18 Block diagram of the USB UART interface

2.14 FMC+ Connector

This carrier board is equipped with two FMC+ connectors, FMC+R and FMC+L, for interfacing with FMC+ or FMC versions of the Titan S10 SOM. The functionality is partitioned between the two connectors to separate power/control from the high-speed data paths, optimizing for signal integrity.

■ **FMC+R Connector (Primarily for Power, Control, and HPS I/O)**

This connector primarily extends system control, HPS peripherals, and auxiliary signals from the carrier board to the SOM.

- **Power Delivery:** Serves as the primary power input for the SOM, supplying 12V and VBAT from the carrier board.
- **HPS Peripherals:** Extends interfaces from the SOM's Hard Processor System (HPS), such as UART, I2C, and SPI, making them physically accessible to the user via connectors on the carrier board.
- **System Control & Debug:** Carries the SOM JTAG interface and other board-to-board control signals.
- **Auxiliary Signals for High-Speed Interfaces:** Transmits the **reference clocks and data bus** for interfaces like USB 3.0, PCIe, MCIO, and QSFP.

■ **FMC+L Connector (Primarily for High-Speed Data)**

This connector is dedicated to routing the high-speed transceiver data lanes directly to the FPGA on the SOM.

- **High-Speed Data Lanes:** Connects the main high-speed differential pairs for the PCIe, MCIO, and QSFP interfaces.
- **Associated Control Signals:** Includes control signals directly related to the high-speed data transmission.

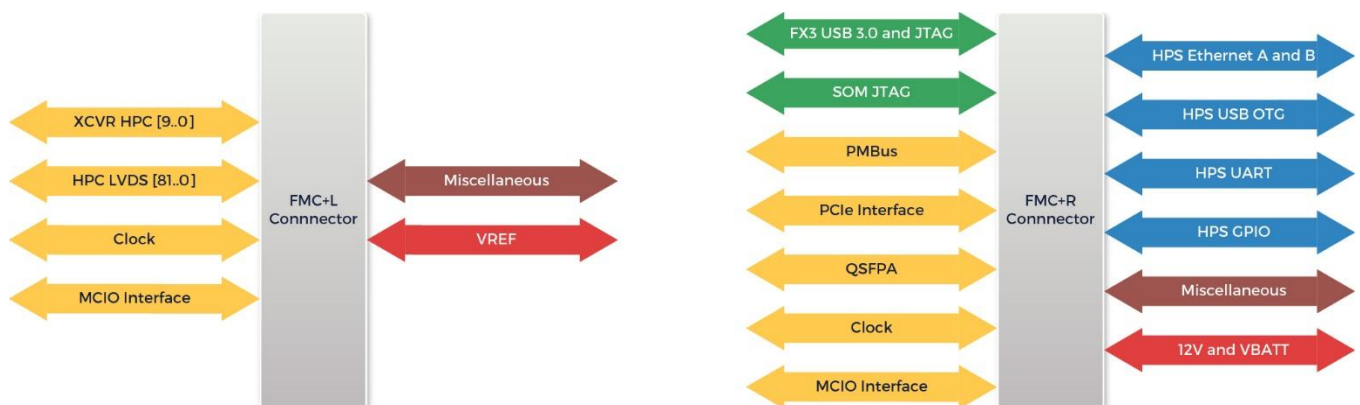Figure 2-19 shows the interfaces connected to the FMC+R and FMC+L connectors.

Figure 2-19 Interfaces connected to the FMC+R and FMC+L connectors.

Chapter 3
Board Assembly

This chapter explains how to assemble and disassemble the Titan S10 SOM and Terasic carrier board.

The video in the link below demonstrates how to install the Titan S10 SOM onto the carrier board, as well as the reverse process of removing it.
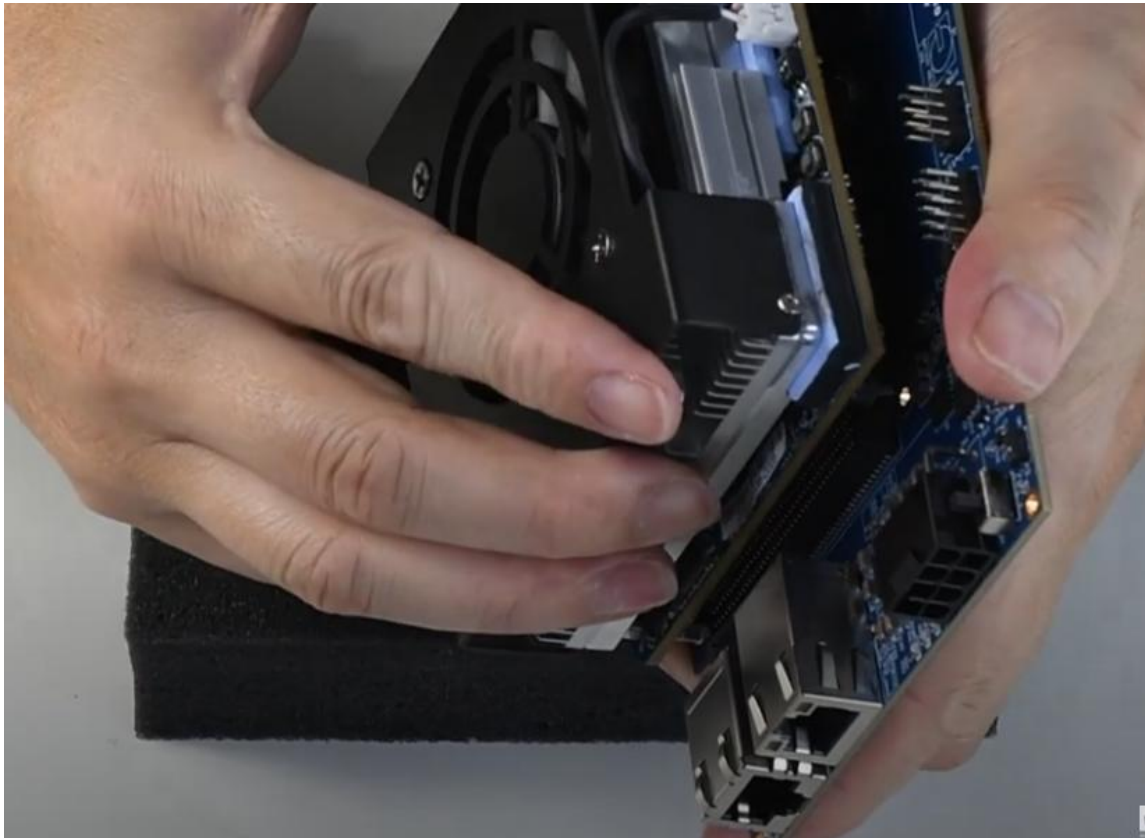https://www.youtube.com/watch?v=RbhVenAc4ps

Figure 3-1Video for installing and removing SOM and Carrier board

Additional Information

4.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ **Terasic Technologies**

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan
Email: support@terasic.com
Web: www.terasic.com

■ **Revision History**

Date	Version	Changes
2025.07	First publication	
2025.07	V1.1	Add UART/USB Blaster III/FMC+ section