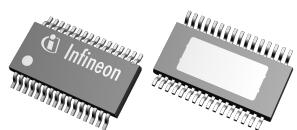


Features

- Integrated half-bridges and high-side switches
 - Overcurrent detection
 - Open load detection
 - High-side current sense
 - PWM input for half-bridges (up to 25 kHz)
 - Integrated PWM generators with phase shift for high-side switches
 - Control of capacitive loads for high-side switches
- Electrochromic mirror control
- Driver for external MOSFET for heater function
- 5 V / 3.3 V regulator with short circuit protection for off-board supply
- 32-bit SPI interface for control and diagnostic
- Overtemperature warning and protection
- Over- and under-voltage lockout
- Watchdog



Potential applications

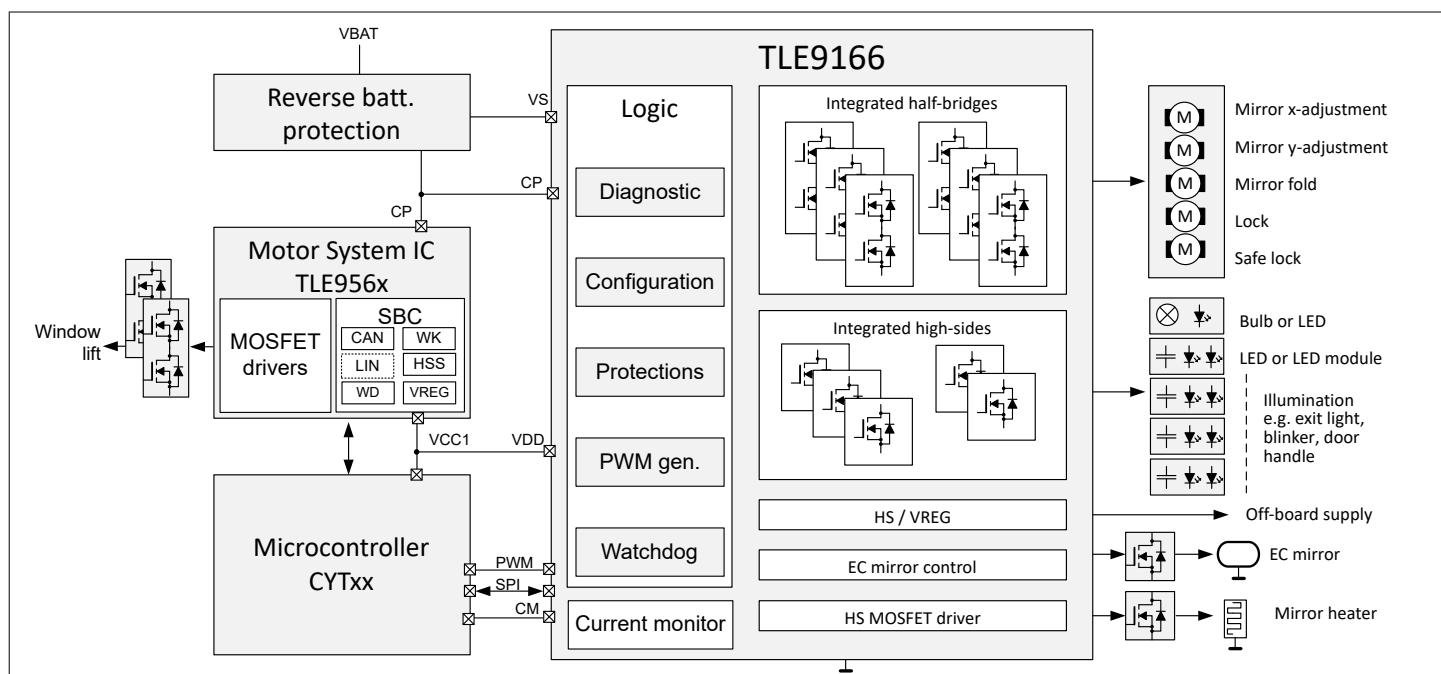
Door zone applications

Product validation

Product validation according to AEC-Q100, Grade 1. Qualified for automotive applications.

Description

The device is optimized for automotive door zone modules to control mirror functions such as mirror positioning, folding and heating, including electrochromic mirror functions. It also integrates half-bridges to control door locks and safe locks, as well as high-sides for LED control.



Product type	Package	Marking
TLE9166EQ	PG-TSDSO-32	TLE9166EQ

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1 General product characteristics

1 General product characteristics

Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

1.1 Absolute maximum ratings

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 1 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	-	40	V	-	P_GEN_01_01
Logic supply voltage	V_{DD}	-0.2	-	5.5	V	-	P_GEN_01_02
Charge pump voltage	V_{CP}	-0.3	-	Min($V_S + 17$; 52)	V	-	P_GEN_01_03
Static output voltage	V_{OUTx}	-0.3	-	$V_S + 0.3$	V	-	P_GEN_01_04
Dynamic half-bridge slew rate	$V_{OUTx_SR_MAX}$	-20	-	20	V/ μ s	Slew rate applied to OUT1 to OUT6	P_GEN_01_05
SDI, CSN	V_{SDI}, V_{CSN}	-0.3	-	$V_S + 0.3$ V	V	-	P_GEN_01_07
SDO, CM, SCLK	$V_{SDO}, V_{CM}, V_{SCLK}$	-0.3	-	$V_{DD} + 0.3$	V	-	P_GEN_01_08
ECDR voltage	V_{ECDR}	-0.3	-	$V_S + 0.3$	V	-	P_GEN_01_09
ECV voltage	V_{ECV}	-0.3	-	$V_S + 0.3$	V	-	P_GEN_01_10
VECDR - VECV	V_{EC_DIFF}	-0.3	-	V_S	V	$V_{ECDR} - V_{ECV}$	P_GEN_01_31
VSH voltage	V_{SH}	-6	-	$V_S + 0.3$	V	-	P_GEN_01_11
VGH voltage	V_{GH}	-6	-	$V_{CP} + 0.3$	V	-	P_GEN_01_12
VGH-VSH	V_{GS}	-0.3	-	12	V	-	P_GEN_01_13
VSH - VCP	$V_{SH} - V_{CP}$	-	-	0.6	V		P_GEN_01_29
PWM	V_{PWM}	-0.3	-	V_{CP}	V	-	P_GEN_01_30
Currents							
Cumulated VS current	I_{VS}	-10	-	10	A	Cumulated DC current for all 3 VS pins ¹⁾	P_GEN_01_14

(table continues...)

1 General product characteristics

Table 1 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Cumulated GND current	I_{GND}	-12	-	12	A	Cumulated DC current for all 3 GND pins ¹⁾	P_GEN_01_15
Output current, OUT1,6	$I_{OUT1,6}$	-5	-	5	A	²⁾	P_GEN_01_16
Output current OUT2,3	$I_{OUT2,3}$	-1.1	-	1.1	A	²⁾	P_GEN_01_17
Output current OUT4	I_{OUT4}	-7	-	7	A	²⁾	P_GEN_01_18
Output current OUT5	I_{OUT5}	-8	-	8	A	²⁾	P_GEN_01_19
Output current OUT7	I_{OUT7}	-3	-	3	A	²⁾	P_GEN_01_21
Output current OUT8-12, ECV	$I_{OUT8-12}$	-1.1	-	1.1	A	²⁾	P_GEN_01_22

Temperatures

Junction temperature	T_J	-40	-	150	°C	-	P_GEN_01_24
Storage temperature	T_{stg}	-50	-	150	°C	-	P_GEN_01_25

ESD robustness

ESD robustness all pins (HBM)	V_{ESD_HBM}	-2	-	2	kV	³⁾	P_GEN_01_26
ESD robustness all pins (CDM)	V_{ESD_CDM1}	-500	-	500	V	⁴⁾	P_GEN_01_27
ESD robustness corner pins (CDM)	V_{ESD_CDM2}	-750	-	750	V	⁴⁾	P_GEN_01_28

1) Absolute maximum DC current through the bond wires, without considerations for maximum power or other limits.

2) Absolute maximum DC current through the bond wires, without considerations for maximum power or other limits.

3) Human body model (HBM) robustness according to AEC - Q100-002

4) Charged device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard

1.2 Functional range

Table 2 shows the device functional range.

Note: For $V_{UV_OFF} \leq V_S \leq 5.5 \text{ V}$, $20 \leq V_S \leq 40 \text{ V}$ and $V_{DD_POFFR} \leq V_{DD} \leq 3 \text{ V}$:

- The device is operating
- Parameter deviations are possible
- For $V_S \geq V_{OV_OFF}$ the outputs are deactivated

1 General product characteristics

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VS voltage range for normal operation	$V_{S(nor)}$	5.5	–	20	V	–	P_GEN_02_01
Charge pump voltage range for normal operation	V_{CP}	$V_S + 7.5$	–	$V_S + 17$	V	–	P_GEN_02_02
Logic supply voltage range for normal operation	V_{DD}	3.0	–	5.5	V	–	P_GEN_02_03
Logic input voltages (SDI, SCLK, CSN, EN, PWM)	$V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN}, V_{PWM}$	-0.3	–	5.5	V	–	P_GEN_02_04
Junction temperature	T_j	-40	–	150	°C	–	P_GEN_02_05

1.3 Thermal resistance**Table 3 Thermal resistance**

Parameter	Symbol	Typ. value	Unit	Note or condition	P-Number
Junction to ambient (2s2p)	R_{thjA}	23	K/W	1)	P_GEN_03_01
Junction to case	R_{thjC}	3	K/W	–	P_GEN_03_02

Specified R_{thjA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board with 6 cm² cooling area; The product (chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm board with two inner copper layers (70 / 35 / 35 / 70 µm Cu). $T_a = 85^\circ\text{C}$.

2 Package outlines

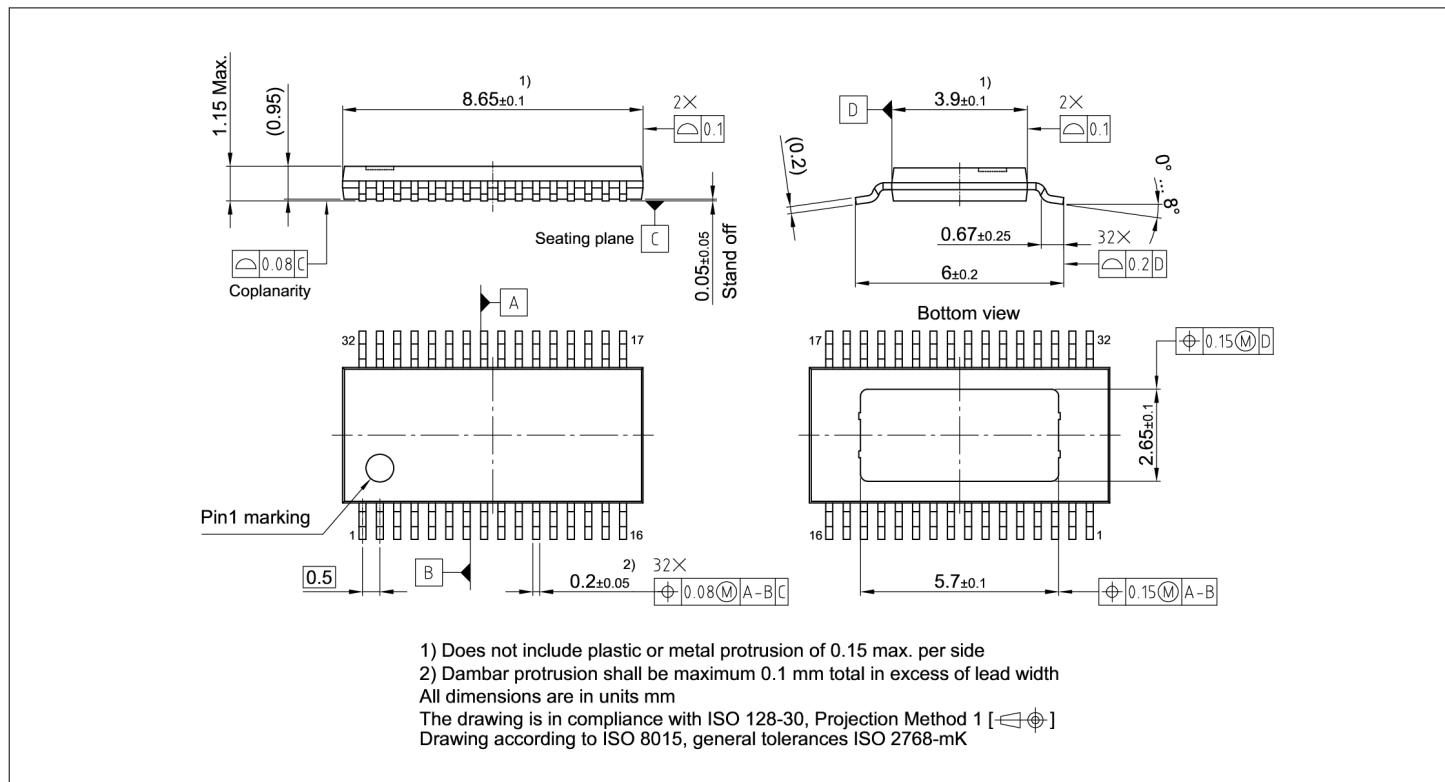


Figure 1 **Package outline PG-TSDSO-32**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e. lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision history

Document version	Date of release	Description of changes
Rev. 1.02	2025-01-22	<ul style="list-style-type: none">• Document name updated
Rev. 1.01	2024-10-03	<ul style="list-style-type: none">• Document name updated
Rev. 1.00	2024-07-24	<ul style="list-style-type: none">• Initial document release

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