

Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDA24VB17P1M3 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

ESD protection device in a small SOD-323 Surface-Mounted Device (SMD) plastic package designed to protect two automotive In-vehicle network bus lines from the damage caused by Electrostatics discharge (ESD) and other transients.

The TESDA24VB17P1M3 may be used to provide ESD protection up to $\pm 30\text{kV}$ (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 5A (8/20 μs) according to IEC61000-4-5.

FEATURES

- AEC-Q101 qualified
- ESD protect for 1 line with bidirectional
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air), $\pm 30\text{kV}$ (contact) IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- Suitable for 24V and below, operating voltage applications
- Small package saves board space
- Protect one I/O line or one power line
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

APPLICATION

- ESD protection for In-vehicle network lines in automotive environments
- CAN Bus
- General Purpose I/O
- Portable Instrumentation



PACKAGE: SOD-323	PIN CONFIGURATION	CIRCUIT DIAGRAM				
	<table border="1"> <tr> <td>PIN 1</td><td>Anode 1</td></tr> <tr> <td>PIN 2</td><td>Anode 2</td></tr> </table>	PIN 1	Anode 1	PIN 2	Anode 2	
PIN 1	Anode 1					
PIN 2	Anode 2					

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power ($tp = 8/20\mu\text{s}$)	P_{PK}	210	W
Peak pulse current ($tp = 8/20\mu\text{s}$)	I_{PP}	5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	kV
Operating junction temperature range	T_J	-55 to +150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	24	V
Reverse breakdown voltage	$I_R = 1\text{mA}$, $T_J = 25^\circ\text{C}$	V_{BR}	25.5	-	35.5	V
Reverse leakage current	$V_{RWM} = 24\text{V}$, $T_J = 25^\circ\text{C}$	I_R	-	-	50	nA
Clamping voltage ⁽¹⁾	$I_{PP} = 1\text{A}$, $tp = 8/20\mu\text{s}$	V_C	-	-	33.6	V
	$I_{PP} = 5\text{A}$, $tp = 8/20\mu\text{s}$	V_C	-	41.9	-	V
Clamping voltage ⁽²⁾	$I_{TLP} = 2\text{A}$, $tp = 100\text{ns}$	V_{CL}	-	31.9	-	V
	$I_{TLP} = 8\text{A}$, $tp = 100\text{ns}$		-	35.7	-	V
Junction capacitance	1MHz, $V_R = 0\text{V}$	C_J	-	14.9	17	pF
Dynamic resistance ⁽²⁾		R_{DYN}	-	0.63	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: $Z_0 = 50 \Omega$, $tp = 100\text{ns}$, $tr = 2\text{ns}$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 2A to 8A.

ORDERING INFORMATION		
ORDERING CODE	PACKAGE	PACKING
TESDA24VB17P1M3 RRG	SOD-323	3,000 / 7" Tape & Reel

CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

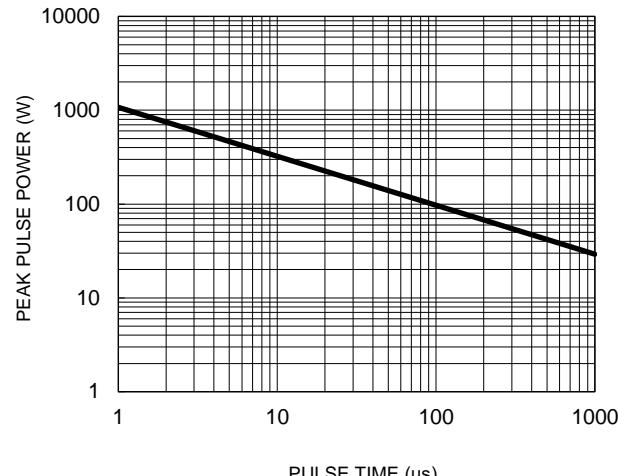
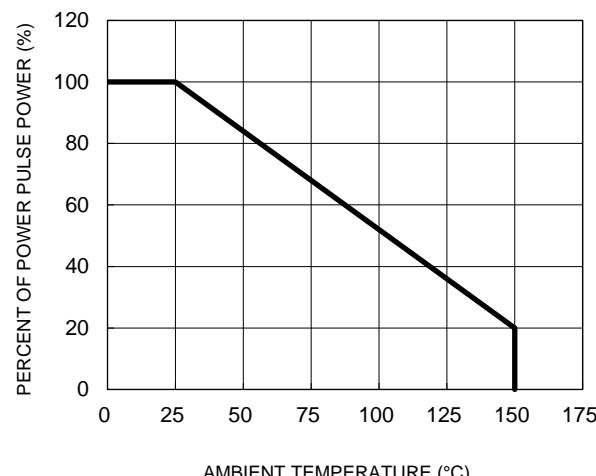


Fig.3 Clamping Voltage vs. Peak Pulse Current

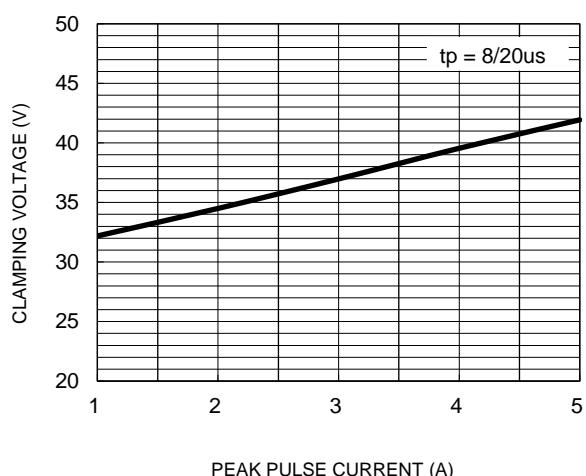


Fig.4 Capacitance vs. Reverse Voltage

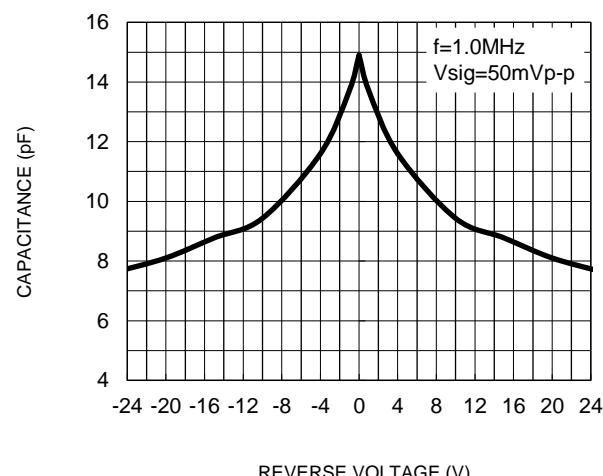
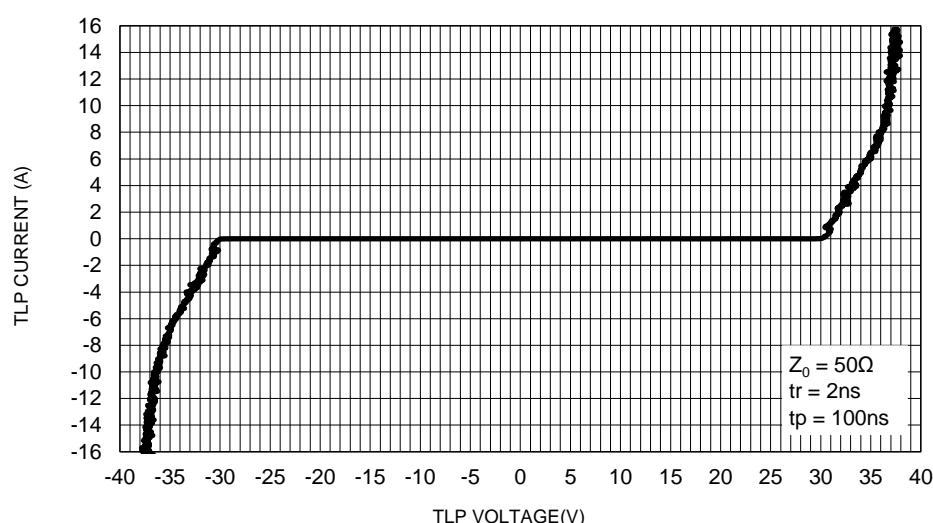


Fig.5 TLP Curve



CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.6 8/20 μs pulse waveform per IEC61000-4-5

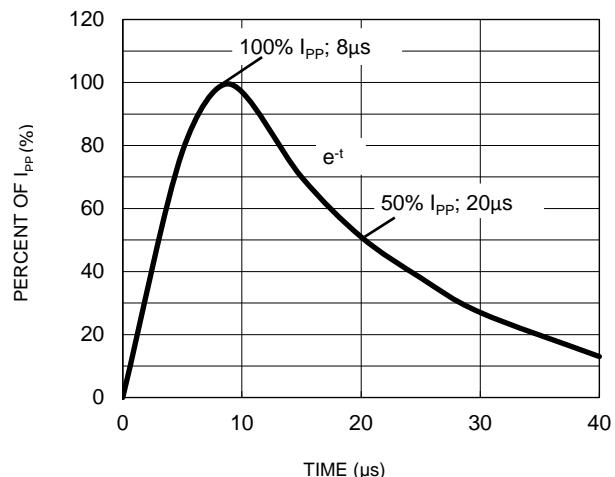
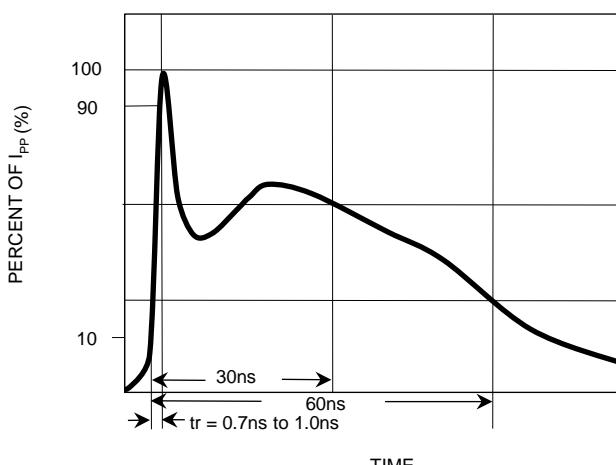


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

Device Connection

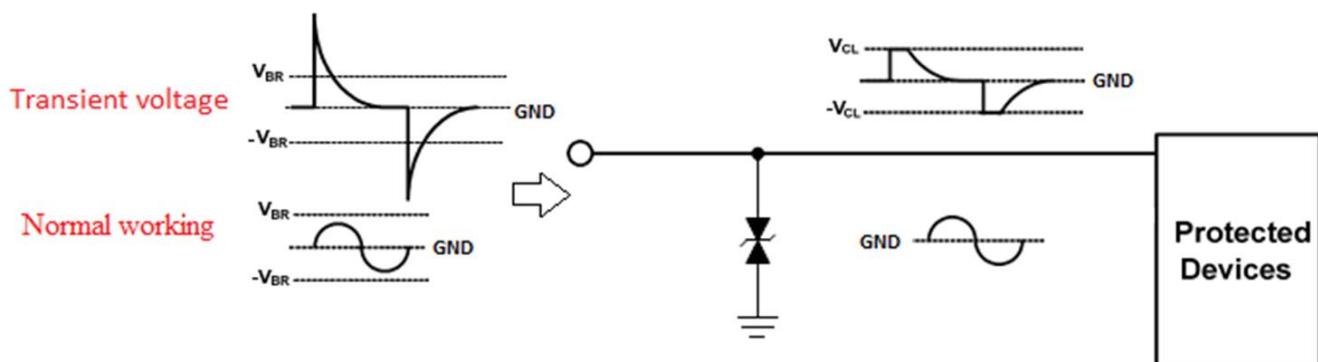
The TESDA24VB17P1M3 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.

The usage of the TESDA24VB17P1M3 is shown in Fig1. Protected line, such as data line, control line, or power line. To minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDA24VB17P1M3 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

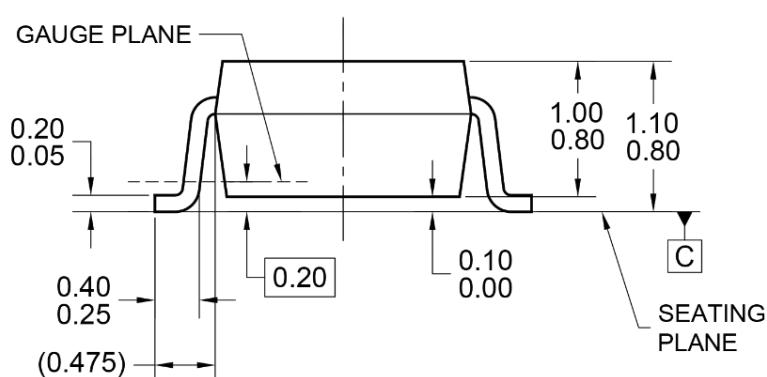
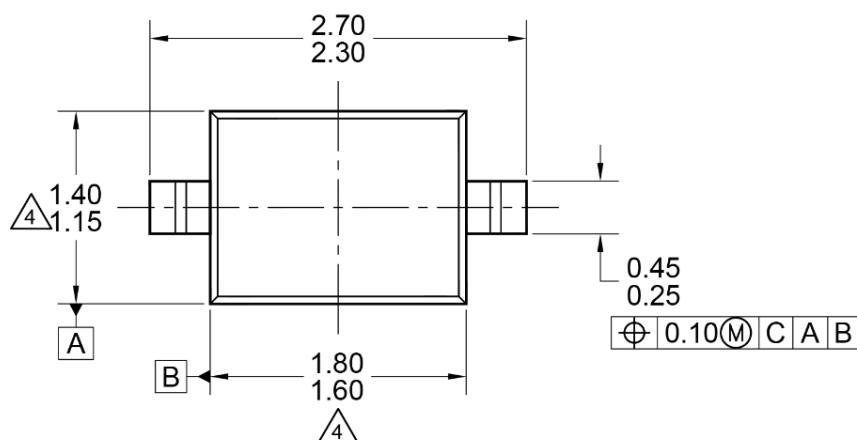
- Let the path length between the protected lines and the TESDA24VB17P1M3 minimize.
- Place the TESDA24VB17P1M3 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

Fig.1 ESD protection by TESDA24VB17P1M3



PACKAGE OUTLINE DIMENSIONS

SOD-323



MARKING DIAGRAM

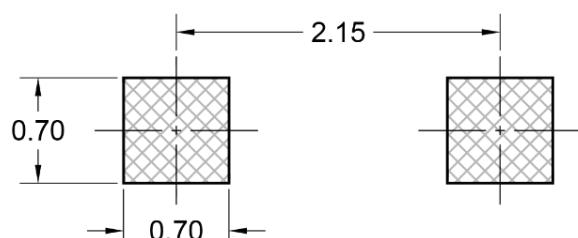
A17P = Device code
Y = Year code
W = Bi-Week code (A~Z)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: EIAJ ED-7500A, SC-76A.

4 MOLDED PLASTIC BODY LATERAL DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

5. DWG NO. REF: HQ2SD07-SOD323-113 REV A.



SUGGESTED PAD LAYOUT

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