TDA38640A Evaluation Board user guide

40 A single-phase buck regulator

About this document

Scope and purpose

This user guide describes the operation, schematic, and bill of materials (BOM) for the EVAL_TDA38640A_1.0VOUT Evaluation Board. Detailed application information for TDA38640A is available in the TDA38640A datasheet [1].

Intended audience

This document is intended as a guide for design engineers evaluating TDA38640A performance with EVAL_TDA38640A_1.0VOUT Evaluation Board.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 Introduction

The TDA38640A is a synchronous buck converter with both serial voltage identification (SVID) and PMBus communication interface, providing a compact, high-performance, and flexible solution in a small 5 mm X 6 mm Power QFN package. This Evaluation Board is to be used during the designing process for evaluating and measuring characteristic curves, and for understanding various features of the part.

The key programmable features offered by the TDA38640A are:

- Soft start
- Thermal protection
- Switching-frequency
- Enable input, output under-voltage lockout
- Over-voltage and -current protection
- High-side short detection
- Load-line, and pre-bias start-up
- All faults have configurable responses via the available XDP™ Designer GUI from Infineon
- Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous (low-side) MOSFET for optimum cost and performance and the current limit is thermally compensated.

2 Evaluation Board

EVAL_TDA38640A_1.0VOUT Evaluation Board is a synchronous buck converter that steps down 12 V_{in} to 1.0 V_{out}. It consists of an integrated point-of-load TDA38640A part. The TDA38640A is an easy-to-use, fully-integrated, and highly efficient DC-DC regulator. The onboard pulse width modulation (PWM) controller and OPTIMOS™ FETs with integrated bootstrap diode make TDA38640A a small footprint solution, providing high-efficiency power delivery. Additionally, it uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response.

This document provides description of the Evaluation Board mentioned in this document. Figure 1 shows the bench set up of this Evaluation Board using 1.0 V_{out} configuration as an example:

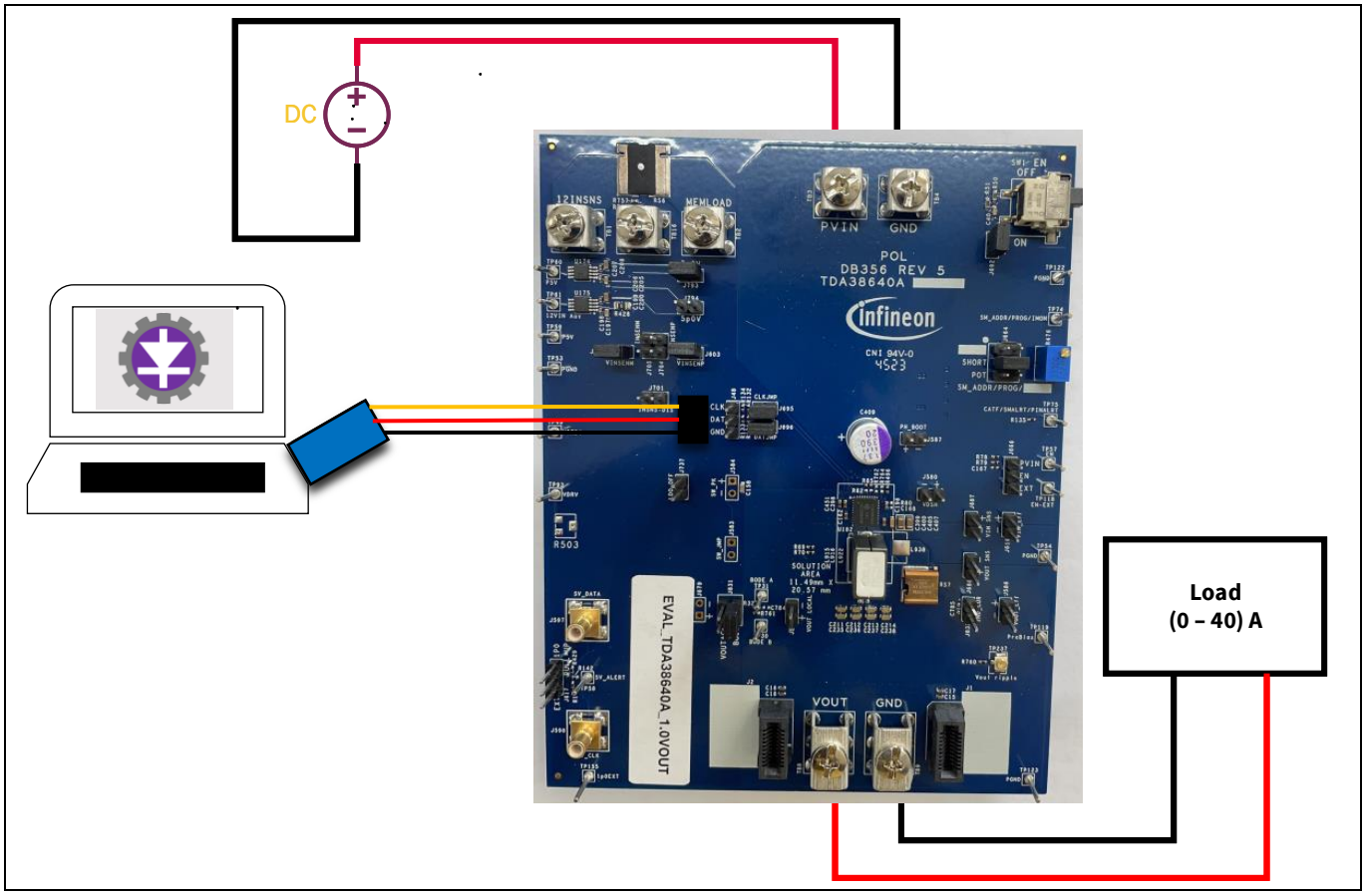

Figure 1 Bench setup block diagram

2.1 Evaluation Kit

The Evaluation Kit consists of only the Evaluation Board.

The user of this Evaluation Kit should order the USB005 dongle separately. Contact your distribution partner, account managers, or the Infineon support for more information about ordering USB005 dongles.

3 Board information

3.1 Board parameters and technical data

PV_{in} = V_{in} = +12 V

F_{sw}= 800 kHz (this is the default value, but it is configurable using the XDP™ Designer GUI)

C_{in}= 8 x 22 µF (25 V, Ceramic 0805) + 1 x 2.2 µF (25 V, Ceramic 0402) + 1x 4.7 µF (25 V, Ceramic 0603) + 1 x 390 µF (20 V, Electrolytic, optional).

Table 2 TDA38640A default output inductor and capacitor bank for each output voltage

Output voltage	Inductor	Output capacitors (C_{out})
1.0 V	100 nH	12 x 22 µF, 8 x 47µF, 2 x 470 µF (2.5 V, SP, 3 mΩ ESR)
1.1 V	150 nH	12 x 47 µF, 4 x 22 µF, 1 x 470 µF (2.5 V, SP, 3mΩ ESR)
1.8 V	470 nH	2 x 22 µF, 8 x 47 µF

3.2 Connections and operating instructions

EVAL_TDA38640A_1.0VOUT Evaluation Board require a single +12 V for the input power and can deliver up to 40 A load current. The operation modes and over-current protection (OCP) limits are programmable via XDP™ Designer GUI.

Table 3 Connections

Label		Descriptions
Input	PVIN	Connect input power (+12 V) to this pin.
	GND	Return of input power.
	VIN_Eff (J616)	Sense pins for input voltage.
	VIN_SEN (J687)	Sense pins for the input voltage.
Output	VOUT	V_{out}, connect a load (40 A max) to this pin.
	GND	Return of V_{out}
	VOUT_Eff (J586)	Sense pins for efficiency.
	VOUT_SEN (J686)	Sense pins for the output voltage.
Enable	ENABLE	Connect a scope probe to this pin to monitor the Enable signal. An external Enable signal can be applied to this pin to overdrive the on-board Enable signal by connecting a jumper on EXT-EN header J740. Alternatively, the Enable signal can be generated using PVIN using a resistor divider by connecting a jumper on PVIN-EN header J740
	GND	
BODE	A	For bode plot measurement.
	B	
SM_ADDR/PROG	I2C Slave Address Offset	Use this jumper to add an offset to the I2C Slave base address of 0x10h. By default, this is set to zero.
I2C/PMbus	J48	This is used to establish communication with the Infineon XDP™ Designer GUI, which is used to change the default configuration of the part. The dongle USB005 is used for communication.
VRRDY	TP49	This is used to indicate that the SVID communication is ready to accept the commands from the master or the VID has reached a window about the commanded VID
PROG	J664	This jumper is used to select between 16-programmed files stored in the part. By default, it is set to accept the most recent programmed config file into the part.
Vcc	J737	This jumper should be open to use internal LDO.
SVID Comm	SV_DATA & SV_CLK	These SMB connectors are used to probe and talk to the part using the SVID communication.
SVID Pull-Up	PULL-UP (J617)	The jumper decides if one wants to use the 1 V_{out} or an external 1 V for pull ups on the SVID lines

3.3 Layout

The PCB is an 8-layer board (5.25-inch x 4.1-inch) using FR4 material. The PCB thickness is 0.062 inch. TDA38640A and other major power components are mounted on the top side of the board. Table 4 details the layer stack-up order and Copper weight for each layer.

Table 4 PCB layer stack up

Layer	Layer description	Trace material
1	Top	0.5-Ounce Copper + 1.5-Ounce plating
2	Ground 1	2-Ounce Copper
3	Signal 1	2-Ounce Copper
4	Power 1	2-Ounce Copper
5	Power ground	2-Ounce Copper
6	Signal 2	2-Ounce Copper
7	Ground 2	2-Ounce Copper
8	Bottom	0.5-Ounce Copper + 1.5-Ounce plating

3.4 PCB layout

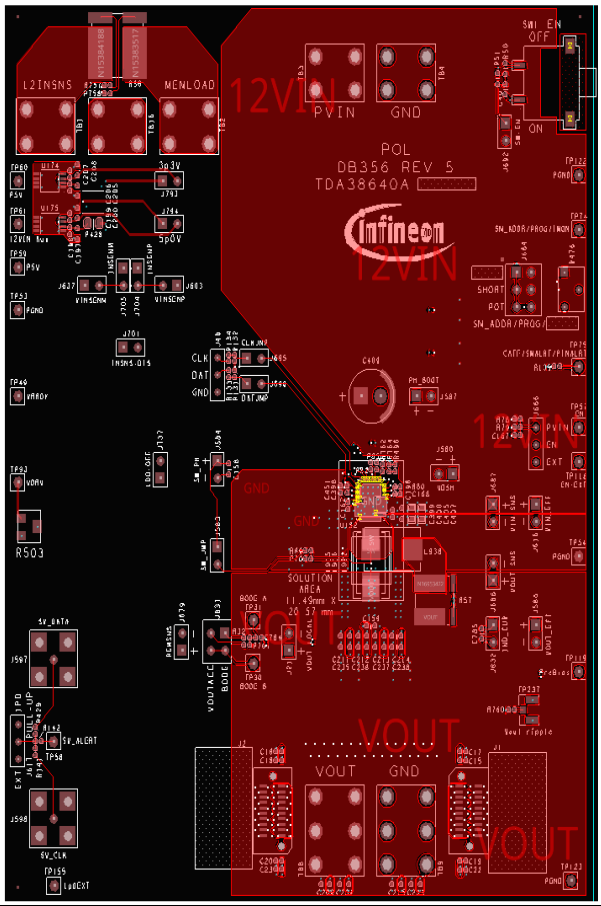

Figure 2 TDA38640A Evaluation Board top-layer

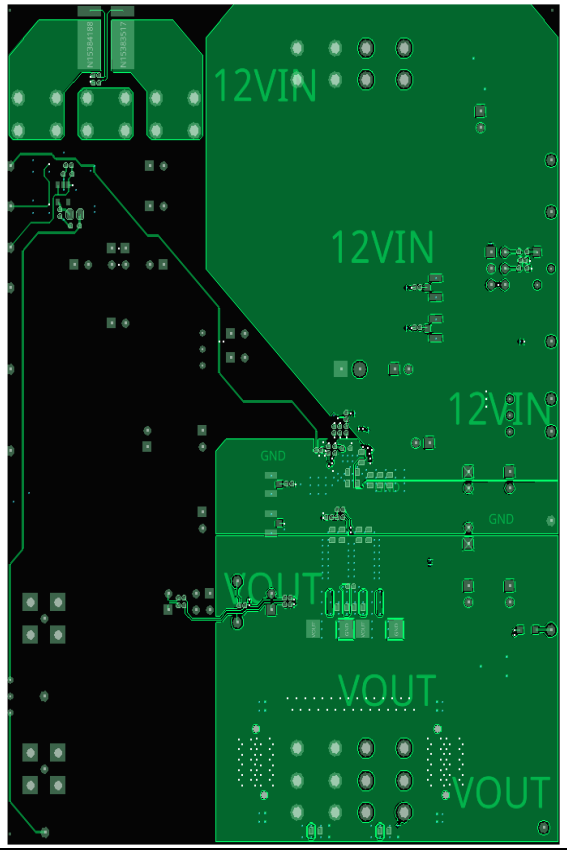

Figure 3 TDA38640A Evaluation Board bottom-layer

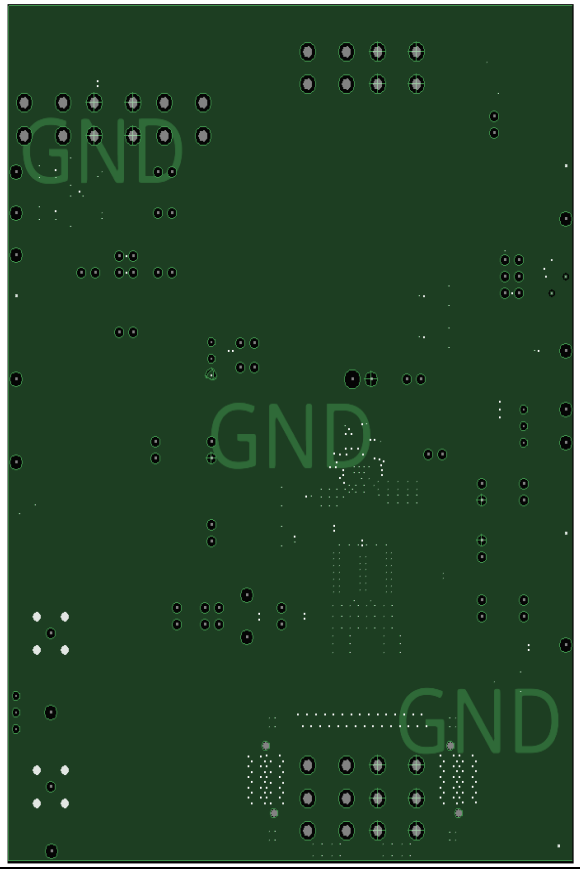

Figure 4 TDA38640A Evaluation Board mid layer 1 (ground)

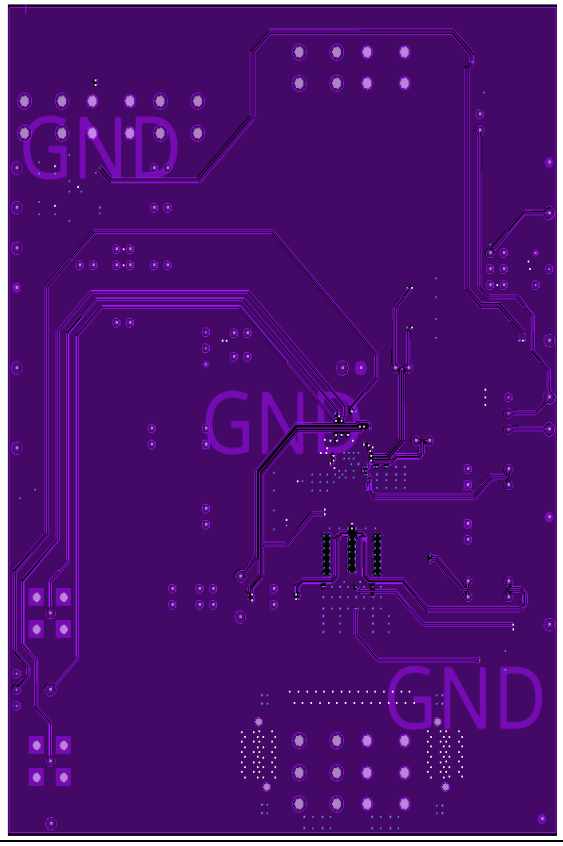

Figure 5 TDA38640A Evaluation Board mid layer 2 (signal 1)

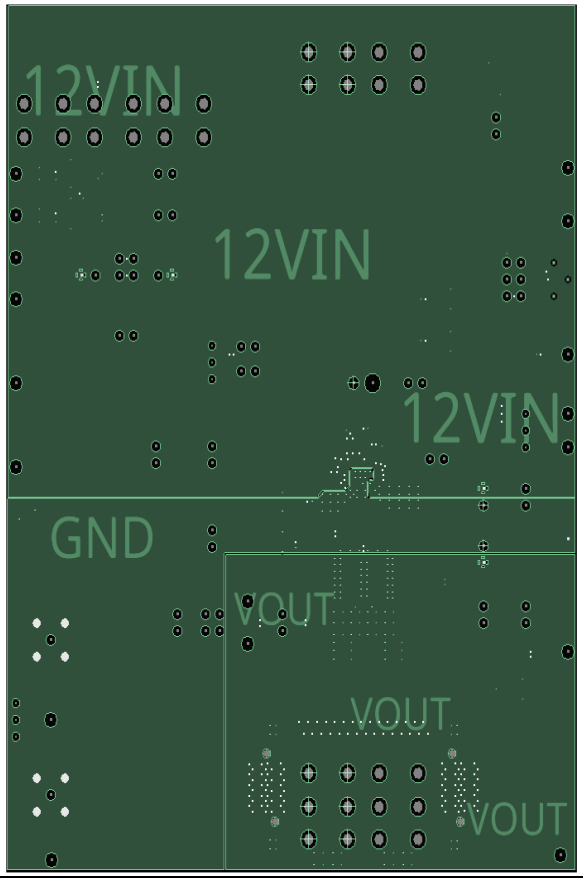

Figure 6 TDA38640A Evaluation Board mid layer 3 (power 1)

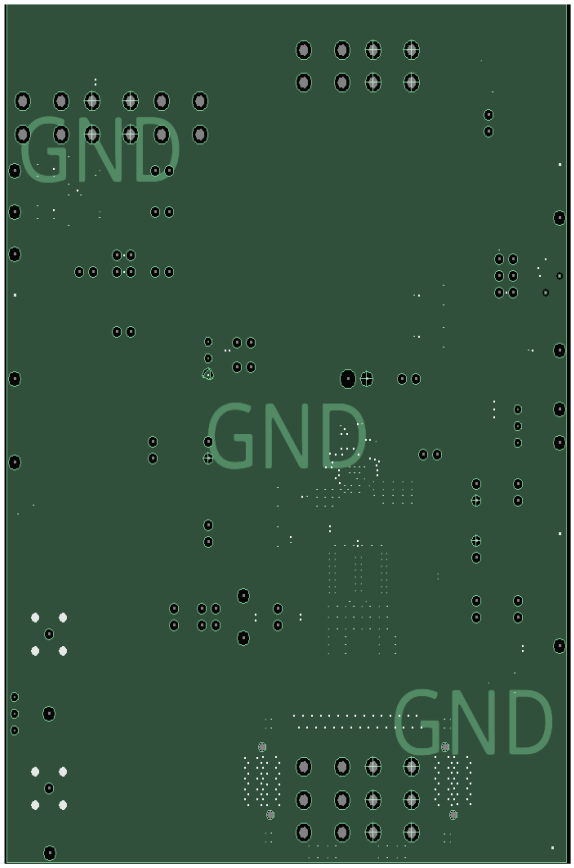

Figure 7 TDA38640A Evaluation Board mid layer 4 (power ground)

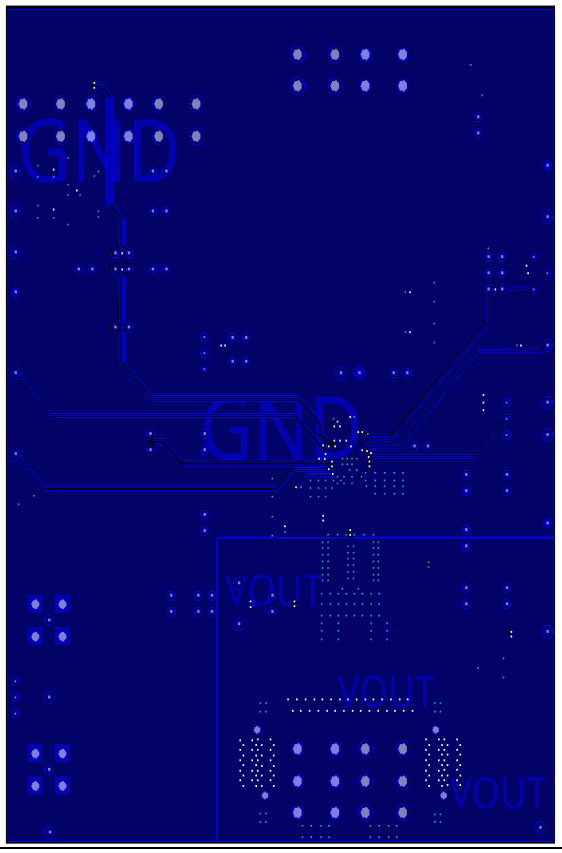

Figure 8 TDA38640A Evaluation Board mid layer 5 (signal 2)

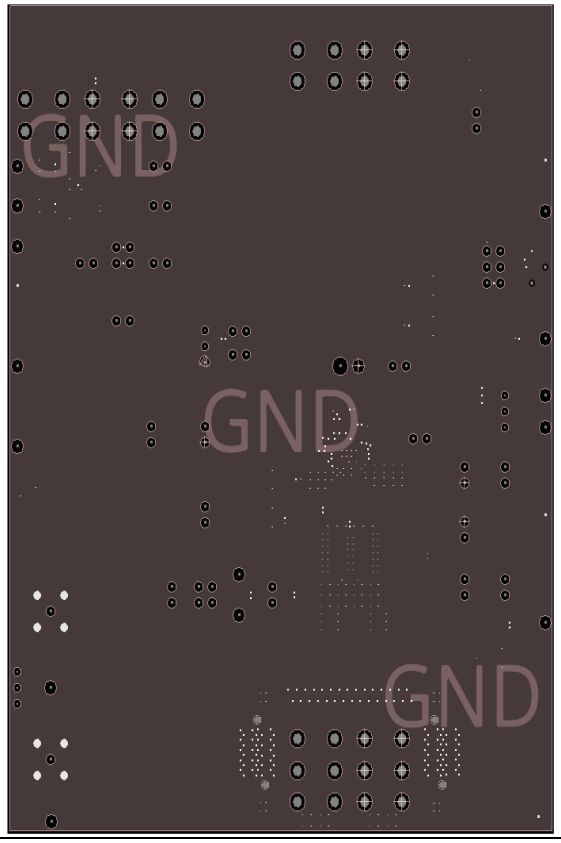

Figure 9 TDA38640A Evaluation Board mid layer 6 (ground 2)

3.5 Schematic

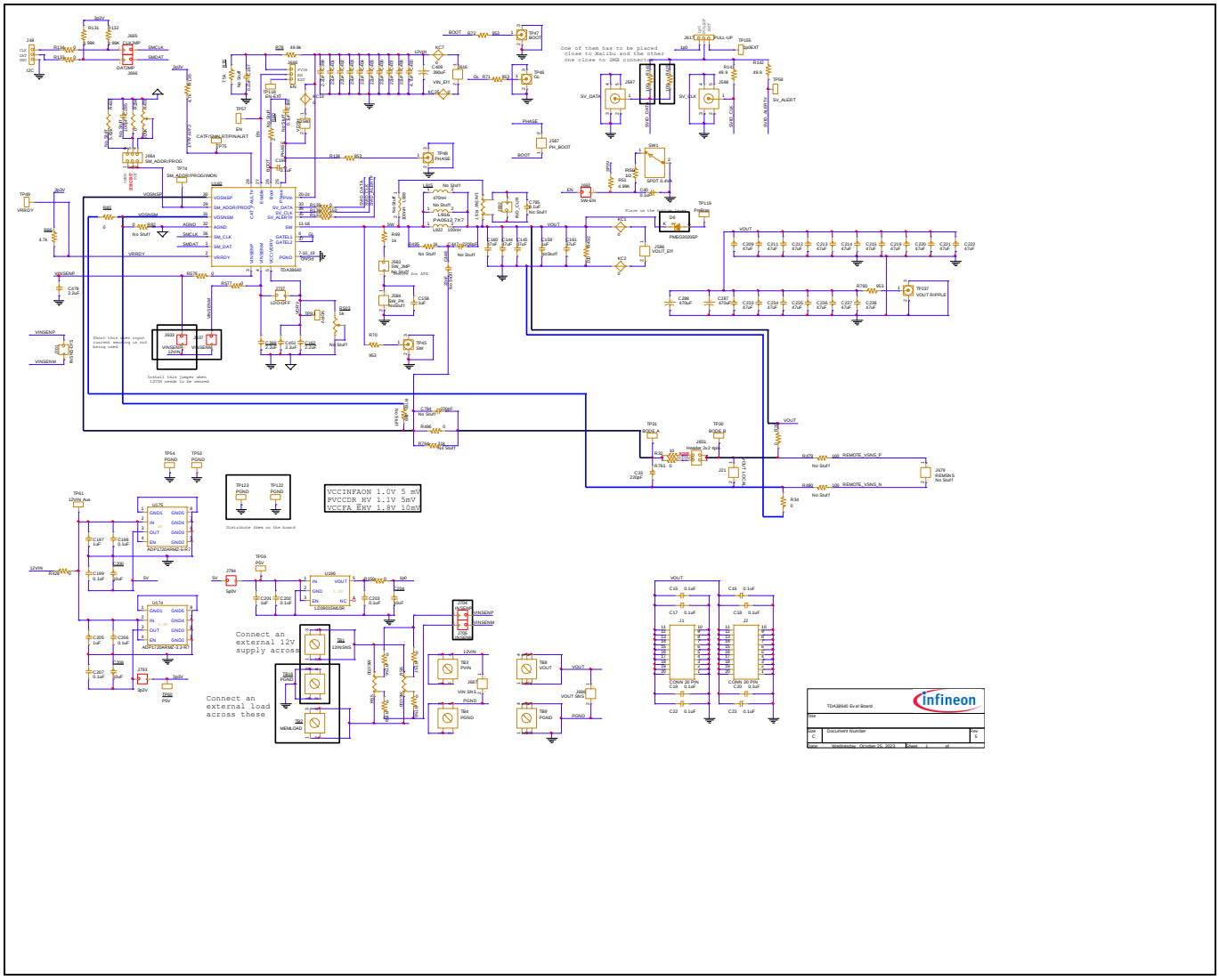

Figure 10 Schematic of EVAL_TDA38640A_1.0VOUT

3.6 Bill of materials

Table 5 Bill of materials

Item	Qty	Reference	Value	Description	Manufacturer	Part number
1	1	C196	0.1 µF	0.1 µF-0402-25 V-X7R-10%	TDK	C1005X7R1E104K
2	1	C285	No Stuff	100 pF-0402-50 V-C0G-5%	JDI	500R07N101JV4T
3	1	C159	No Stuff	1 µF-0603-25 V-X5R-10%	Samsung	CL10A105KA8NNNC
4	3	C451, C398, C162	2.2 µF	2.2 µF-0402-16 V-X6S-10%	TDK	C1005X6S1C225K050BC
5	1	C478	2.2 µF	2.2 µF-0603-25 V-X7S-10%	Murata	GRM188C71E225KE11D
6	1	C399	2.2 µF	2.2 µF-0402-25 V-X5R-10%	Murata	GRT155R61E225KE13D
7	8	C401, C402, C403, C404, C405, C406, C407, C408	22 µF	22 µF-0805-25 V-X5R-20%	Murata	GRM21BR61E226ME44L
8	1	C400	4.7 µF	4.7 µF-0603-25 V-X6S-20%	Murata	GRM188C81E475KE11
9	1	C409	390 µF	CAP, 8 mm, 20 V, TOL%	Panasonic	20SEPF390M
10	12	C209, C211 C212, C213 C214, C215 C233, C234 C235, C236 C237, C238	47 µF	47 µF-0603-6.3 V-X5R-10%	Murata	GRM188R60J476ME15D
11	1	R78	49.9k	Res,0402,1/16 W,1%	Yageo	RC0402FR-0749K9L
12	2	R576, R577	0	Res,0402,1/16 W,1%	Yageo	RC0402FR-070RL
13	1	R79	7.5k	Res,0402,1/16 W,1%	Yageo	RC0402FR-077K5L
14	1	R433	No stuff	Res,0603,1/10 W,1%	Yageo	RC0603FR-07####L
15	1	R80	No stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07####L
16	1	R86	4.7k	Res,0402,1/16 W,1%	Yageo	RC0402FR-074K7L
17	1	R494	0	Res,0603,1/10 W,1%	Yageo	RC0603FR-070RL
18	1	R32	10	Res,0402,1/16 W,1%	Yageo	RC0402FR-0710RL
19	1	R479, R480	No stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07####L
20	1	U182	TDA38640A	TDA38640A 40 A single-voltage synchronous buck regulator	Infineon	TDA38640A-0000

Item	Qty	Reference	Value	Description	Manufacturer	Part number
21	8	C144, C145 C160, C161 C219, C220 C221, C222	47 µF	47 uF-0805-4 V-X6S-20%	Murata	GRT21BC80G476ME13L
22	2	C287, C288	470 µF	SP Cap, Dcase, 2.5 V,20%	Panasonic	EEFGX0E471R
23	1	L922	100 nH	IR_Inter_Tech_L101247A_10x6p4mm	Inter-technical	L101247A-100L
24	1	R496	0	Res,0402,1/16 W,1%	Yageo	RC0402FR-070RL
25	1	R764	No Stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-0730K9L
26	1	R762	No Stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07499RL

3.7 XDP™ Designer GUI

Infineon XDP™ Designer GUI is needed to communicate with the TDA38640A part via I2C. The GUI is a part of the Infineon XDP™ Designer.

Note that Dongle driver v59.4 or higher is necessary to communicate with the TDA38640A.

Installing and configuring XDP™ Designer

1. Launch the Infineon Developer Center.
2. Locate and click on the **Manage tools** Section.
3. In the search bar of the **Manage tools** Section, search for **XDP™ Designer**.
4. Install the **XDP™ designer** from the search results.
5. Once the installation is complete, launch the XDP™ Designer.

Configure the XDP™ Designer

1. Power the Evaluation Board with +12 V V_{in} and connect to your computer with the USB005 dongle.
2. Update system or scan devices: There are two ways to establish connection with your board:

- Click the **Tuning & Debugging** button within XDP™ Designer. This should automatically update the system section with the connected device and its configuration.
- If the automatic update doesn't work, click the **Scan Devices** button.

  The device will show with the part number and I2C address, with green circles (if the connection is correct and there are no faults).

3. Use the **XDP™ Designer toolbar** to alter any system configurations or read the telemetry.

   See Figure 11 for an annotated version of the XDP™ Designer home screen shown for EVAL_TDA38640A_1.0VOUT.

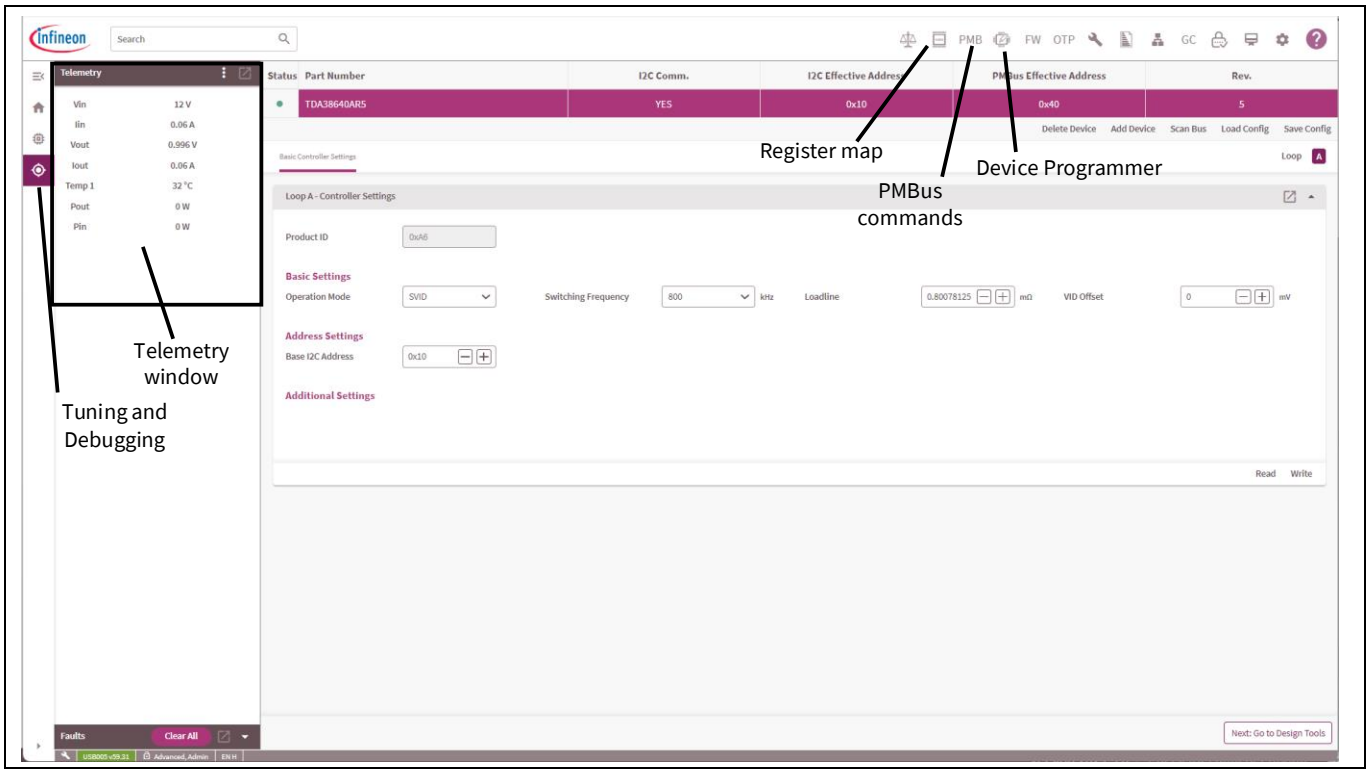

Figure 11 XDP™ Designer GUI

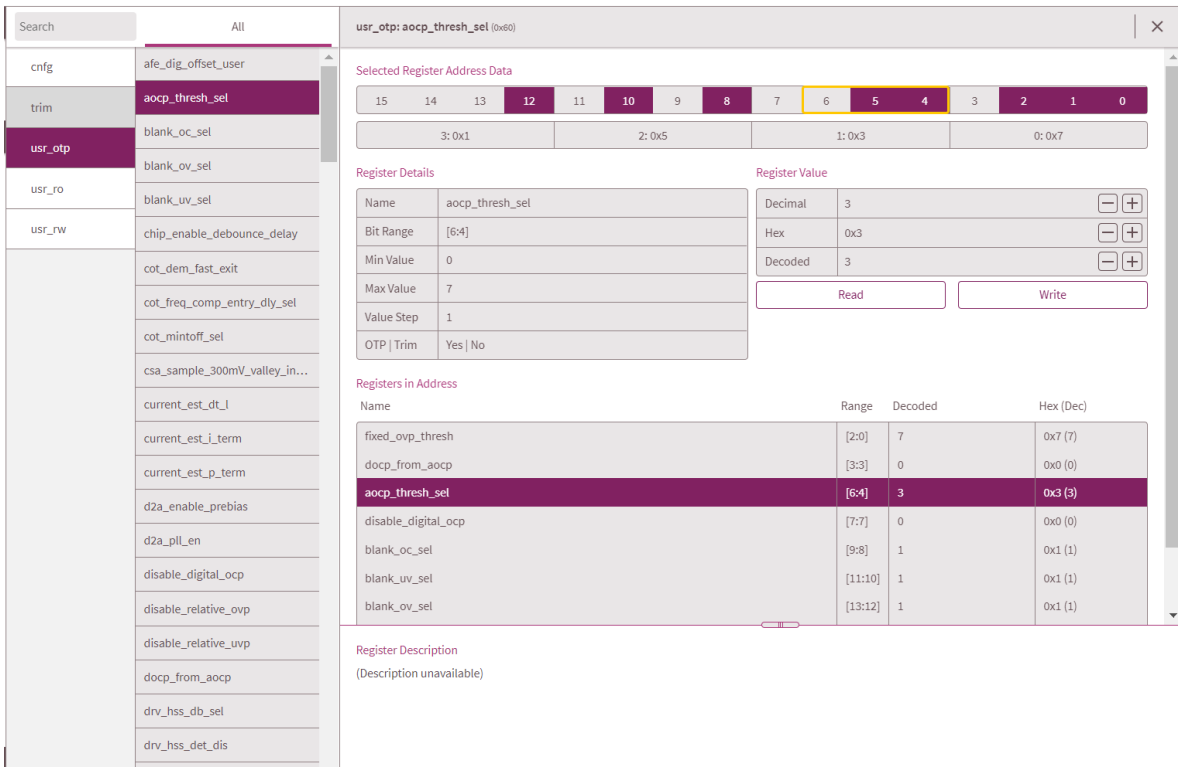

Figure 12 Register map window

4 Typical operating waveforms

Operating conditions: PV_{in} = 12.0 V, V_{out} = 1.0 V, I_{out} = 0 - 40 A, room temperature, no airflow

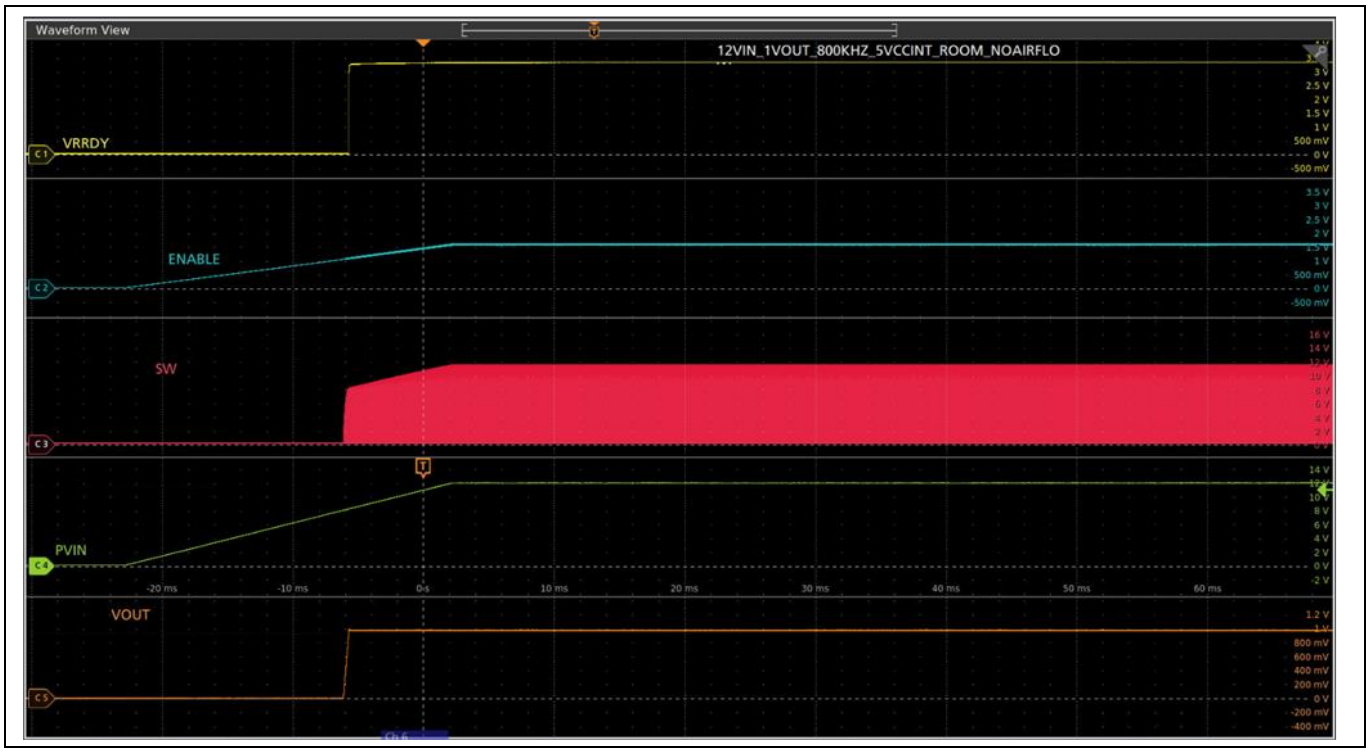

Figure 13 Start up at 0 A load (Ch_1: VRRDY, Ch_2: Enable, Ch_3: Switch node, Ch_4: PV_{in}, Ch_6: V_{out})

Figure 14 Start up at 30 A load (Ch_1: VRRDY, Ch_2: Enable, Ch_3: Switch node, Ch_4: PV_{in}, Ch_5: V_{out})

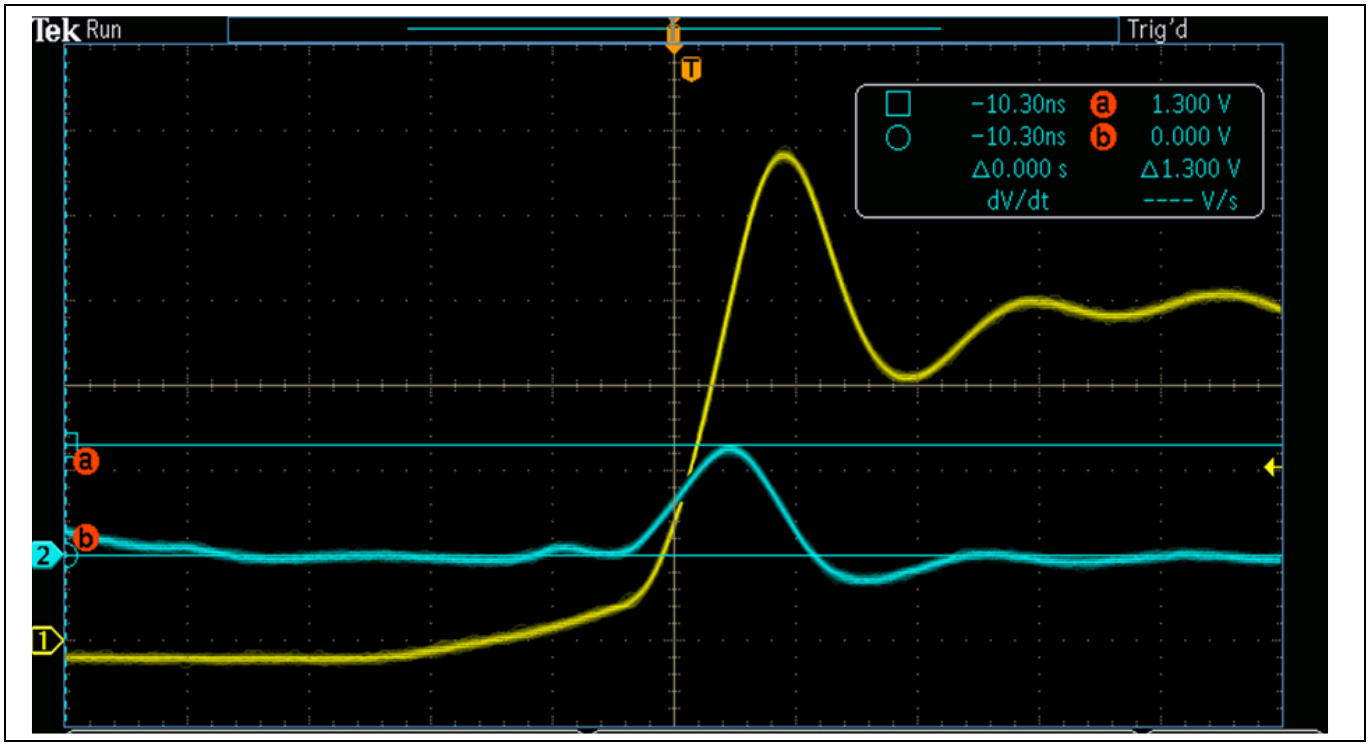

Figure 15 SW and GL, 30 A load, f_{sw} = 800 kHz

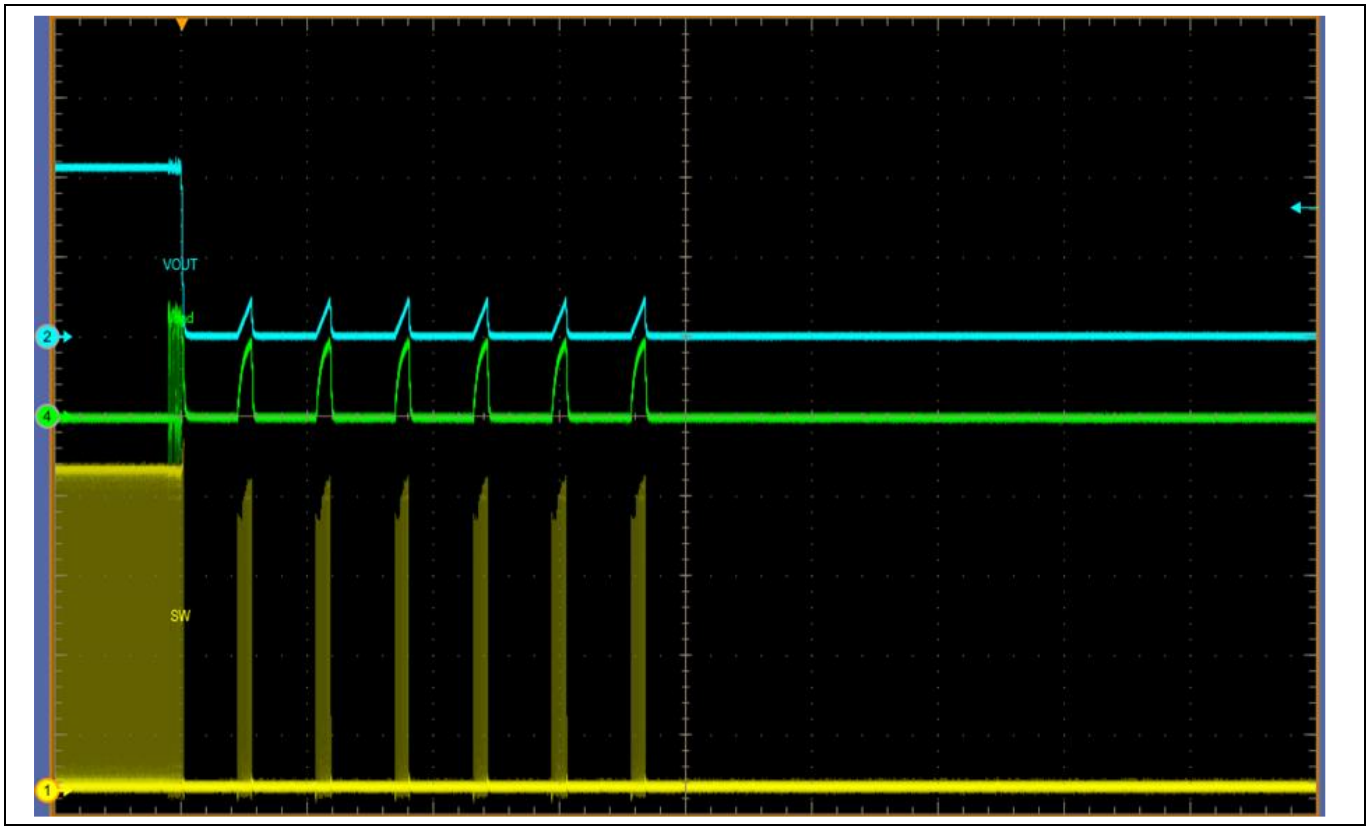

Figure 16 Short circuit and retry 6 times and shutdown (Ch_1: Switch node, Ch_2: V_{out}, Ch_3: I_{out})

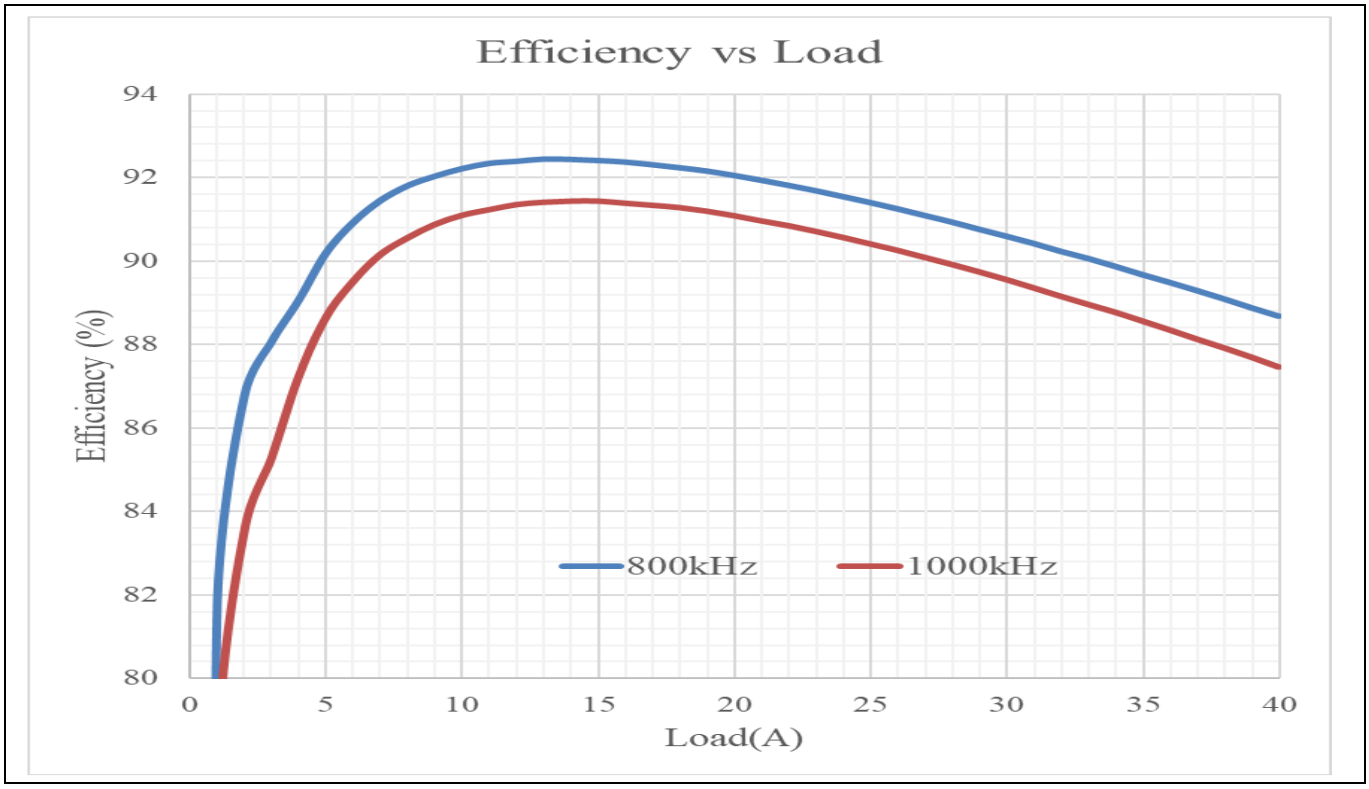

Figure 17 **TDA38640A efficiency versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 1.0 V_{out}, no air flow, 150 nH, 800 kHz/1000 kHz, T_a = 25°C)**

Figure 18 **Power loss versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 1.0 V_{out}, no air flow, 150 nH, 800 kHz/1000 kHz, T_a = 25°C)**

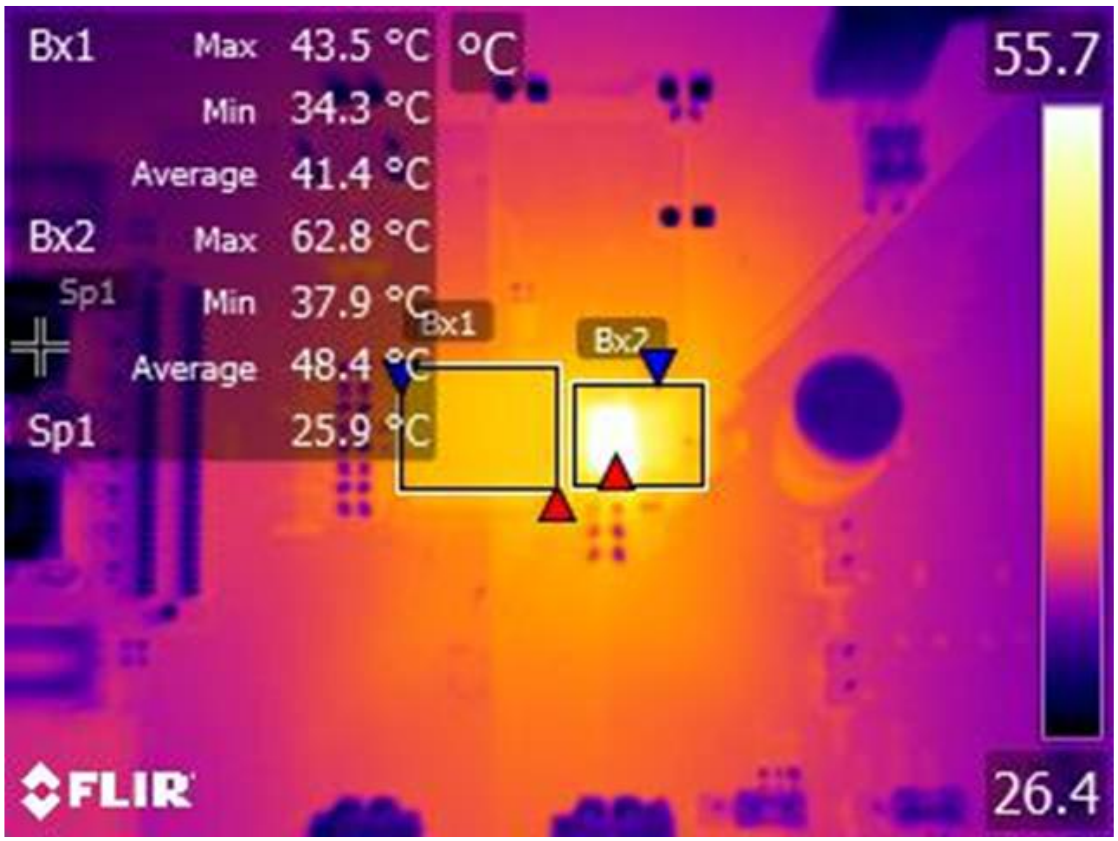

Figure 19 **Thermal image of the board at 1.0 V, 40 A load, TDA38640A = 62.8°C, L = 43°C, Amb = 25.9°C, natural convection, fsw = 800 kHz**

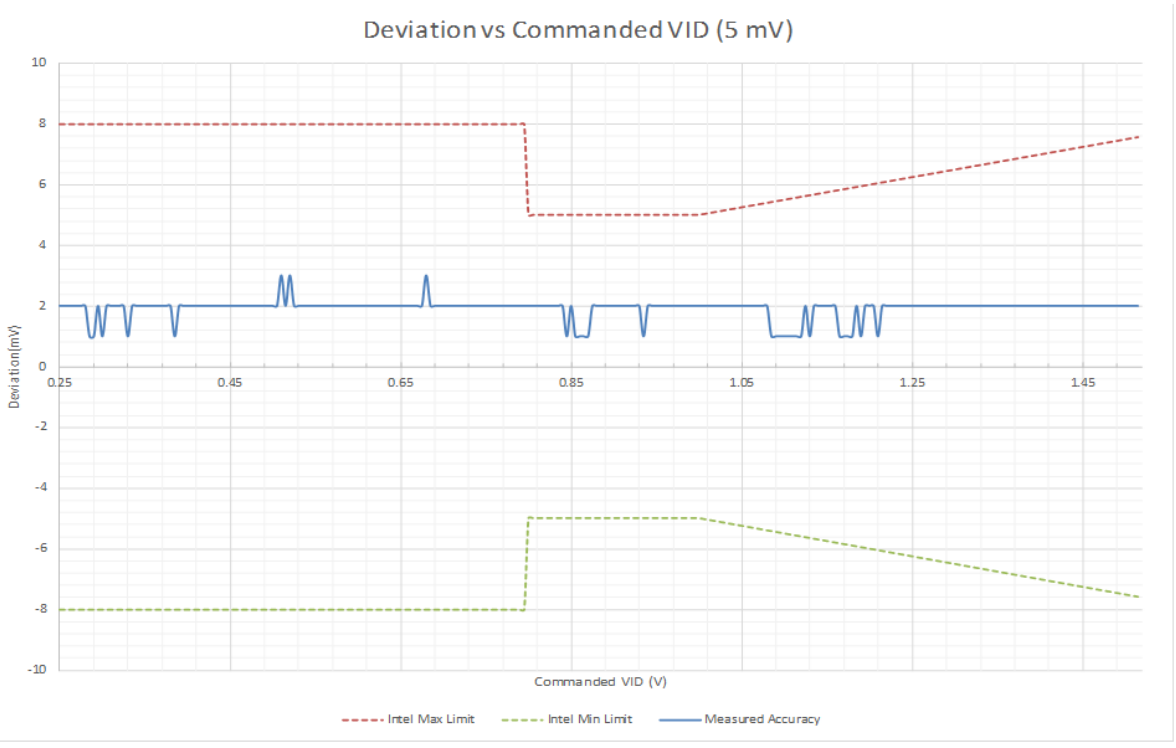

Figure 20 **TDA38640A VID regulation (12 V_{in}, 1.0 V_{out}, 5 mV step size, no air flow, 150 nH, 800 kHz, T_a = 25°C)**

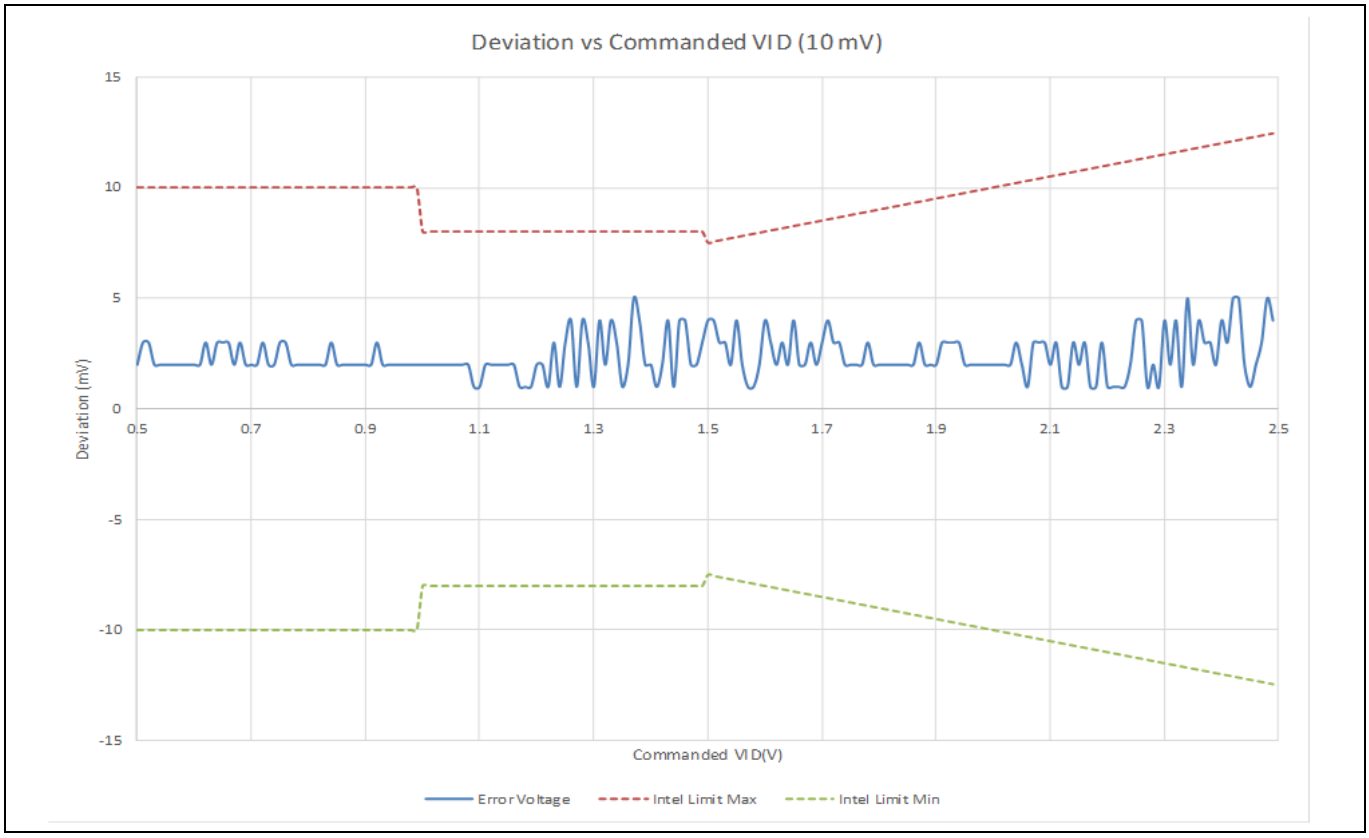

Figure 21 TDA38640A VID regulation (12 V_{in}, 1.0 V_{out}, 10 mV step size, no air flow, 150 nH, 800 kHz, T_a = 25°C)

References

[1] Infineon Technologies AG: *TDA38640A OptiMOS™ IPOL 40 A single-voltage synchronous buck regulator datasheet*.

Revision history

Document revision	Date	Description of changes
V 1.0	2024-08-20	Initial release

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