



SL871K2L Product Family

Hardware Design Guide

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1 Applicability Table

Table 1: Applicability Table

Products
SL871K2L
SL871K2L-18B
SL871K2L-18P

2 Introduction

2.1 Scope

This document introduces the Telit SL871K2L family product and presents possible and recommended hardware solutions for the development of a product based on this module. All the features and solutions described in this document apply to all variants listed in the applicability table.

This document cannot include every hardware solution or every product that can be designed. Where the suggested hardware configurations are not to be considered mandatory, the information provided should be used as a guide and starting point for the proper development of the product with the Telit module.

2.2 Audience

This document is intended for system integrators that are using the Telit SL871K2L family modules in their products.

2.3 Contact Information, Support

For technical support and general questions, e-mail:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com for Wi-Fi and Bluetooth related questions
- TS-ONEEDGE@telit.com for OneEdge related questions

Alternatively, use: <https://www.telit.com/contact-us/>

For Product information and technical documents, visit: <https://www.telit.com>

2.4 Conventions

Note: Provide advice and suggestions that may be useful when integrating the module.

Danger: This information MUST be followed, or catastrophic equipment failure or personal injury may occur.

Warning: Alerts the user on important steps about the module integration.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

2.5 Terms and Conditions

Refer to <https://www.telit.com/terms-conditions/>.

2.6 Disclaimer

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3 General Product Description

3.1 Overview

The SL871K2L is the latest evolution of the SL871 family of modules and is based on the low-power AG3352 platform from Airoha.

This new module shares the same pinout as the well-established xL871 form factor. The SL871K2L is designed to support GPS, QZSS, GLONASS, BeiDou, and Galileo. The module concurrently tracks four constellations by default, operating at the L1 frequency, including the modern BeiDou B1C signal.

Additionally, this product outputs a precise 1-pulse-per-second (1PPS) signal and includes timing-related features such as TRAIM and surveying mode for high-performance timing applications. The SL871K2L supports Assisted GNSS (A-GNSS) in both autonomous and server-based modes.

3.2 Product Variants and Frequency Bands

The SL871K2L family modules are L1-only, multi-constellations receivers, available in three variants:

- SL871K2L: 3.3 V supply voltage, low-power product.
- SL871K2L-18B: 1.8 V supply voltage, low-power product.
- SL871K2L-18P: 1.8 V supply voltage.

The table below lists the supported satellite systems, for all variants.

Table 2: Product Variants and Supported Satellite Systems

Products	Constellations
SL871K2L	GPS (L1 C/A+L1C)
SL871K2L-18B	GLONASS (L1)
SL871K2L-18P	Galileo (E1)
	BeiDou (B1I+B1C)
	QZSS (L1 C/A)
	SBAS (L1)

3.3 Target Market

The SL871K2L Product Family can ideally be applied to all positioning verticals such as:

- Telemetry
- Fleet management
- Insurance telematics / Dashcams
- Asset/personal tracking
- Sport equipment
- E-mobility



3.4 Block Diagram

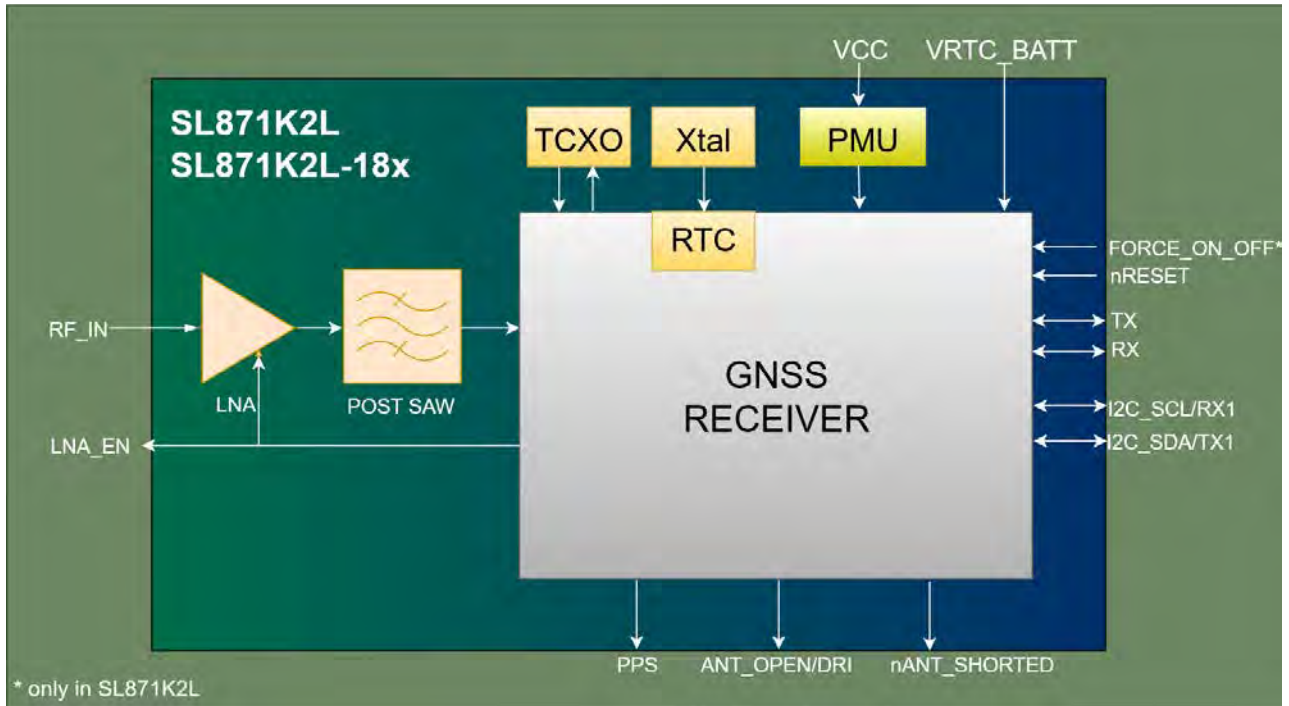


Figure 1: Block Diagram

3.5 Main Features

Table 3: Functional Features

Function	Features
GNSS	Multi-constellation Low power consumption Update rate up to 10 Hz Real Time Clock Geofence Multi-Tone AIC AGNSS Timing features (TRAIM, Satellite hold, Self Survey mode)*
Interfaces	Main UART I2C/second UART 1PPS signal LNA_EN nRESET Single Antenna pin Antenna Detection*
*: dedicated FW may be required	



3.6 Mechanical Specifications

3.6.1 Dimensions

The overall dimensions of SL871K2L product family is:

- Length: 10.1 mm
- Width: 9.7 mm
- Thickness: 2.5 mm

3.6.2 Weight

The nominal weight of the SL871K2L family product is TBD (Estimated < 1 gram).

3.7 Temperature Range

Table 4: Temperature Range

Mode	Temperature	Notes
Operating Temperature Range	-40°C / +85°C	
Storage and non-operating Temperature Range	-40°C / +85°C	

3.8 ITAR Limits

SL871K2L GNSS receivers are designed for commercial and civil use, ensuring full compliance with the speed restriction of 600 m/s imposed by the Office of Space Commerce, U.S. Department of Commerce. For more information, refer to the following link:

<https://www.space.commerce.gov/>



4 Pins Allocation

4.1 Pin-out

Table 5: Pin-out Information for SL871K2L

Pin	Signal	I/O	Function	Type	Notes
Host Interface (HIF)					
2	UART0-TX	I/O	UART0-TX	DIGITAL 3.3 V	UART0-TX default
3	UART0-RX	I/O	UART0-RX	DIGITAL 3.3 V	UART0-RX default
Digital IO					
9	nRESET	I	System Reset (active low) - Entering/exiting HW RTC	DIGITAL 3.3 V	10 k Ω internal Pull up
5	ANT_OPEN	I	Antenna detection pin: Antenna open (high true)	DIGITAL 3.3 V	Antenna detection function requires a specific FW variant
15	nANT_SHORT	I	Antenna detection pin: Antenna shorted (low true)	DIGITAL 3.3 V	Antenna detection function requires a specific FW variant
13	LNA_EN	O	External LNA control	DIGITAL 3.3 V	
4	PPS	I/O	1 st function: PPS	DIGITAL 3.3 V	1PPS time mark
16	I2C-SDA	I/O	1 st function: I2C-SDA	DIGITAL 3.3 V	
			2 nd function: UART1-TX		
17	I2C-SCL	I/O	1 st function: I2C-SCL	DIGITAL 3.3 V	
			2 nd function: UART1-RX		
18	FORCE_ON_OFF	I	Pin for entering/exiting HW RTC	DIGITAL 3.3 V	only in SL871K2L
RF Section					
11	RF_IN	I	RF signal input	ANALOG RF	
Power Supply					
8	VDD_3V3	-	Power supply	Power 3.3 V	
6	VRTC_BATT	-	Power supply	Power 3.3 V	Power supply @3.3 V always on for RTC
14	VDD_RF	-	Output Voltage for Bias-T	Power 3.3 V	
1	GND	-	Ground		
10	GND	-	Ground		
12	GND	-	Ground		
Reserved for Future Use (RFU)					
7	RFU	-	LEAVE NOT CONNECTED		

Table 6: Pin-out Information for SL871K2L-18x

Pin	Signal	I/O	Function	Type	Notes
Host Interface (HIF)					
2	UART0-TX	I/O	UART0-TX	DIGITAL 1.8 V	UART0-TX default
3	UART0-RX	I/O	UART0-RX	DIGITAL 1.8 V	UART0-RX default
Digital IO					
9	nRESET	I	System Reset (active low)	DIGITAL 1.8 V	10 k Ω internal Pull up
5	ANT_OPEN	I	Antenna detection pin: Antenna open (high true)	DIGITAL 1.8 V	Antenna detection function requires a specific FW variant
15	nANT_SHORT	I	Antenna detection pin: Antenna shorted (low true)	DIGITAL 1.8 V	Antenna detection function requires a specific FW variant
13	LNA_EN	O	External LNA control	DIGITAL 1.8 V	
4	PPS	I/O	PPS	DIGITAL 1.8 V	1 PPS time mark
16	I2C-SDA	I/O	1 st function: I2C-SDA	DIGITAL 1.8 V	
			2 nd function: UART1-TX		
17	I2C-SCL	I/O	1 st function: I2C-SCL	DIGITAL 1.8 V	
			2 nd function: UART1-RX		
RF Section					
11	RF_IN	I	RF signal input	ANALOG RF	
Power Supply					
8	VDD_1V8	-	Power supply	Power 1.8 V	
6	VRTC_BATT	-	Power supply	Power 1.8 V	Power supply @1.8 V always on for RTC
14	VDD_RF	-	Output Voltage for Bias-T	Power 1.8 V	
1	GND	-	Ground		
10	GND	-	Ground		
12	GND	-	Ground		
Reserved for Future Use (RFU)					
7	RFU	-	LEAVE NOT CONNECTED		
18	RFU	-	LEAVE NOT CONNECTED		

Warning: PIN 18 is reserved for future use in SL871K2L-18x, while it is FORCE_ON_OFF in SL871K2L

4.2 Pads Layout

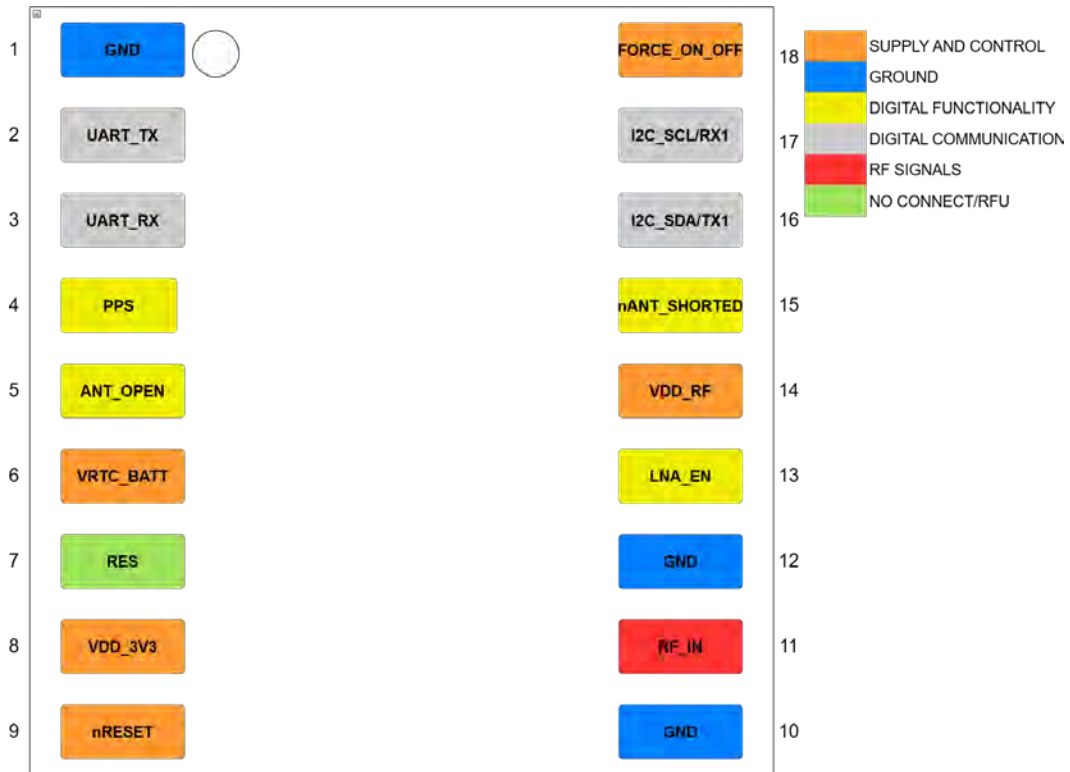


Figure 2: Pads Layout in SL871K2L – Top view



Figure 3: Pads Layout in SL871K2L-18x – Top view

5 Power Supply

5.1 Power Supply Requirements

In the SL871K2L family, the two power supply rails, VBATT_RTC (pin 6) and VDD (pin 8), are not internally connected and should be managed separately. VBATT_RTC is a continuously powered supply dedicated to the RTC section, while VDD powers the other units on the module, including the RF, analog, and digital components, according to the power-up sequence in section Power Up and Down Sequence.

The SL871K2L family includes both 1.8V and 3.3V powered modules, specifically:

- SL871K2L: 3.3V powered
- SL871K2L-18x: 1.8V powered

The following tables provide the power supply details for both products:

Table 7: Power Supply Requirements for SL871K2L

Power Supply for SL871K2L		Value
Nominal Supply Voltage	VDD	3.3V
	VBATT_RTC	3.3V
Operating Voltage Range	VDD	2.52 V -3.63 V
	VBATT_RTC	1.62 V – 3.63 V

Table 8: Power Supply Requirements for SL871K2L-18x

Power Supply for SL871K2L-18x		Value
Nominal Supply Voltage	VDD	1.8 V
	VBATT_RTC	1.8 V
Operating Voltage Range	VDD	1.75 V -1.98 V
	VBATT_RTC	1.62 V – 3.63 V

Warning: The operating voltage range must never be exceeded. The application's power supply section must be carefully designed to prevent excessive voltage drops.



5.2 Power Up and Down Sequence

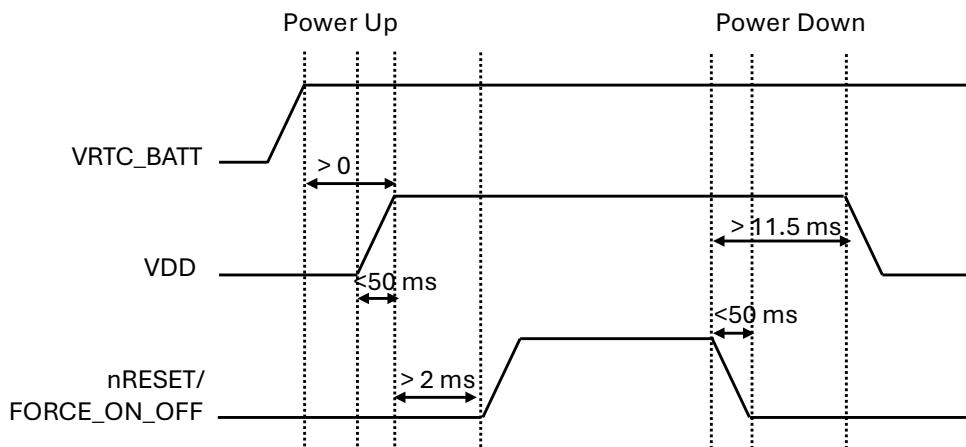


Figure 4: Power up and down sequence

5.3 Power Saving Options

The platform offers several options for power saving:

- **Fitness mode:** This mode is designed for running and walking workouts. It reduces measurement noise caused by arm movement and optimizes navigation performance in low-speed scenarios, allowing for lower power consumption.
- **ALP:** The ALP (Adaptive Low Power) mode provides two options for low power application: power-saving mode and performance mode.
 - Power-saving mode uses duty cycles to save more power, but it can have a negative effect on GNSS performance.
 - Performance mode adaptively controls number of used SV but still keeps good GNSS performance.

The ALP mode is currently only available under the “Normal” and “Fitness” navigation mode and 1 Hz update rate.

- **RTC mode:** This is the lowest power consumption operating mode, shutting down all systems. When the module enters RTC mode, commands cannot be set, and the GNSS module no longer provides position-related information. Importantly, the navigation data before entering RTC mode is saved for the next navigation. This data includes ephemeris, almanac, location, and time, which help facilitate TTFF performance. The module can be awakened by either setting the timer, pulling the nRESET pin low and releasing it, or by using the FORCE_ON_OFF (internally short-circuit to nReset only in SL871K2L for backward compatibility).

All SL871K2L series supports two ways of RTC mode: SW RTC accessed via command and HW RTC entered by removing VDD or toggling nRESET; the two modes present different power consumption values as reported in Table 10. After entering RTC with the proper command, VDD must be switched OFF, as indicated in Figure 5, to allow the minimum power consumption in RTC mode

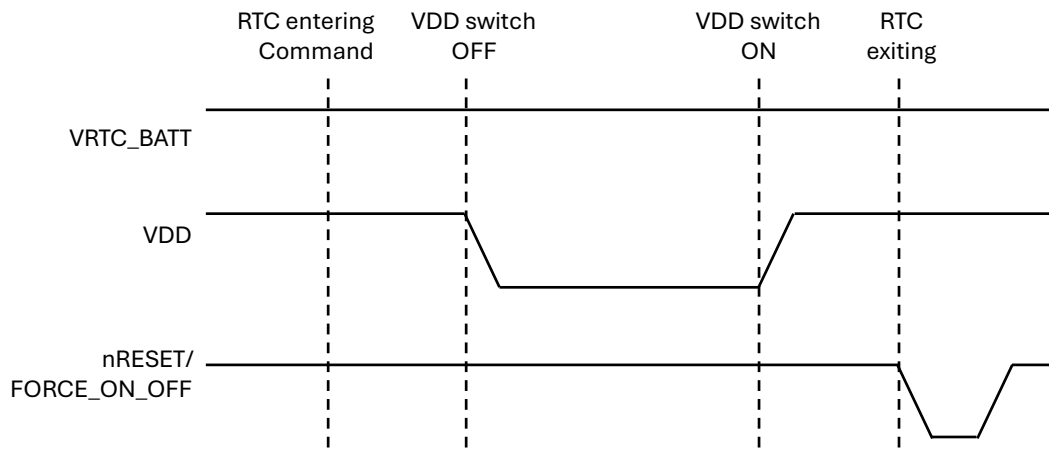


Figure 5: RTC mode entering sequence

5.4 Power Consumption

Table 9: Power Consumption in SL871K2L Product Family

Power Consumption	SL871K2L	SL871K2L-18P	SL871K2L-18B
Acquisition (avg)	44 mW	54 mW	36 mW
Tracking (avg)	45 mW	51 mW	40 mW
Navigation (avg)	44 mW	50 mW	38 mW
Peak power	76 mW	75 mW	70 mW
IDLE (avg)	7.8 mW	6 mW	6 mW

Test conditions: Room Temperature, Open Sky tests, all constellations active

Table 10: Power Saving Modes Consumption in SL871K2L Product Family

Power Saving modes	SL871K2L	SL871K2L-18P	SL871K2L-18B
Fitness	43 mW	45 mW	32 mW
ALP - power saving (Prelim.)	17 mW	17 mW	14 mW
ALP- performance (Prelim.)	37 mW	36 mW	27 mW
SW RTC*	44 μ W	23 μ W	23 μ W
HW RTC*	112 μ W	60 μ W	60 μ W

Test conditions: Room Temperature, Open Sky tests, all constellations active
 * RTC power consumption refer exclusively to the VRTC_BATT rail with VDD switched off.

5.5 Power supply Design Rules

The principal guidelines embrace three different design steps:

- Electrical design
- Thermal design
- PCB layout



5.5.1 Electrical Design Guidelines

The electrical design of the power supply strongly depends on the chosen power source. VBATT_RTC and VDD must be generated independently to allow the VDD switch-off in RTC mode which guarantees the maximum power saving for the SL871K2L.

The user can choose whether using LDOs (to reduce noise) or DC-DC (to reduce off-module power consumption) according to the specific applications needs.

All the power by-pass capacitor values must be chosen according to the vendor indication for the selected voltage regulator.

Aluminum electrolytic capacitors are not recommended at the module input due to their high ESR. When Tantalum capacitors are chosen, a minimum value of 10 μ F is recommended, in parallel with a 0.1 μ F ceramic capacitor. Ceramic capacitors can be used alone for both input and output but ensure that the voltage regulator is stable with such capacitors tied to the output.

In VDD generation, the enable PIN (CE) (both for LDO and DC-DC option) must be connected to an host microcontroller, or to VBATT_RTC to ensure the correct power up/down sequence as indicated in Figure 4 and Figure 5.

5.5.2 Thermal Design Guidelines

Pay attention to properly ground the power section to avoid overheating the module. Do not place the module near to Power amplifier or sudden heat flows to prevent clock drift.

5.5.3 PCB Layout Guidelines

As seen on the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut current peaks on the input and protect the module supply from spikes.

The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be ineffective or even degrade the performance of the power supply.

- The low ESR bypass capacitor must be placed close to the Telit SL871K2L family power input pads; in case the power supply is a switching type, it can be placed close to the switching inductor to reduce ripple.
- In case a switching power regulator is used, it is important to keep the involved current loop formed by the input capacitor, the output diode (if not embodied in the IC) and the regulator as small as possible to reduce the radiated EMI at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator, separated from the common ground plane, is recommended.

6 Digital Section

The SL871K2L product family has four main operation states:

- **OFF state:** The VBATT_RTC power level is lower than 1.1 V, and no logic is active during this state.
- **RTC state:** This is the lowest power consumption state. The module can enter SW RTC mode through a software command and in HW RTC by pulling down the nRESET pin (or FORCE_ON_OFF, only in SL871K2L).

The module can exit RTC mode via hardware by releasing the nRESET signal (or FORCE_ON_OFF, only in SL871K2L), or it can automatically exit using a timeout defined by the RTC command.

- **Active state:** This is the full power, fully operational state of the SL871K2L module. To enter this state, both VBATT_RTC and VDD must be powered on.
- **Idle state:** This is a power-saving state where location services are unavailable, but the module can still receive commands. The module can enter the Idle state through a software command.

6.1 Logic Levels

Table 11: Logic Levels Minimum and Maximum for SL871K2L

Parameter	Min	Max
Absolute Maximum Ratings – Not Functional		
Input level on any digital pin with respect to ground	-0.3 V	3.63 V
Operating Range - Interface levels (VDD=3.3 V)		
Input high level	2 V	VDD+0.3 V
Input low level	-0.3 V	0.8 V
Output high level	2.4 V	-
Output low level	-	0.4 V
Operating Range - Interface levels (VDD=2.8 V)		
Input high level	0.625*VDD	VDD+0.3 V
Input low level	-0.3 V	0.25*VDD
Output high level	0.75*VDD	-
Output low level	-	0.125*VDD

Table 12: I/O Driving Capability for SL871K2L

Parameter	MAX
Current characteristics for digital pins	
Output Current	85 μ A (with PD enabled)
Input Current	16 mA

Table 13: Logic Levels Minimum and Maximum for SL871K2L-18x

Parameter	Min	Max
Absolute Maximum Ratings – Not Functional		
Input level on any digital pin with respect to ground	-0.3 V	3.63 V
Operating Range - Interface levels (1.8V CMOS)		
Input high level	0.75*VDD	VDD+ 0.3 V
Input low level	-0.3 V	0.25*VDD
Output high level	0.85*VDD	-
Output low level	-	0.15*VDD

Table 14: I/O Driving Capability for SL871K2L-18x

Parameter	AVG
Current characteristics for digital pins	
Output Current	85 μ A (with PD enabled)
Input Current	8 mA

6.2 Communication Ports

6.2.1 Communication Interfaces to the Host MCU (HIF)

Table 15: UART0 Pins

Function	Pin on SL871K2L
HIF_UART0_TX	2
HIF_UART0_RX	3

6.2.2 Second Communication Interface

Table 16: I2C0/UART1 Pins

Function	Pin on SL871K2L
I2C0_SDA/UART1_TX1	16
I2C0_SCL/UART1_RX1	17

6.3 Digital I/O

6.3.1 LNA Enable

LNA_EN is an output signal, mapped on pin 13 and can be used to enable external LNA to achieve the better RF performance.

6.3.2 nRESET

nRESET is an input signal, mapped on pin 9. It is an active low reset signal and when pulled low send the device in HW RTC mode. Since this signal is internally pulled up (10 k Ω), connect it with an open collector/open drain circuit without pulling it high from the external. Pull low and then release it to reset the module.



6.3.3 FORCE_ON_OFF

FORCE_ON_OFF is an input signal, mapped on pin 18, ONLY on SL871K2L module. It is an active low signal and when pulled low send the device in RTC mode. Since this signal is internally pulled up (10 kΩ), connect it with an open collector/open drain circuit without pulling it high from the external.

6.3.4 1PPS

The GNSS receiver generates a one-pulse-per-second signal for synchronization. It is mapped to PIN 4 on the SL871K2L/SL871K2L-18x.

6.3.5 ANT_OPEN/DRI

This signal, mapped to PIN 5, is a high-true input. When the input is at logic 1, an open antenna line is detected. An antenna detector circuit must be connected to this pin and to PIN 15.

The Antenna detection function is available with a specific FW variant upon request.

The second function of this pin is DRI in I2C communication.

6.3.6 nANT_SHORTED

This signal, mapped to PIN 15, is a low-true input. When the input is at logic 0, a short line antenna is detected. An antenna detector circuit must be connected to this pin and to PIN 5.

The Antenna detection function is available with a specific FW variant upon request.

7 Product Performance

7.1 Horizontal Position Accuracy

Table 17: SL871K2L Product Family - Horizontal Position Accuracy

	SL871K2L	SL871K2L-18P	SL871K2L-18B
CEP50 Live	< 1.5 m	< 1.5 m	< 1.5 m
Preliminary results. All constellations active.			

7.2 Time to First Fix

Table 18: SL871K2L Product Family - Time to First Fix

Start Type	SL871K2L	SL871K2L-18P	SL871K2L-18B
Hot	1 s	1 s	1 s
Warm	25 s	25 s	25 s
Full Cold	28 s	28 s	28 s
Test conditions: Room Temperature and Nominal Voltage. All constellation active. Signal Reference Level -130 dBm			

7.3 Sensitivity

Table 19: SL871K2L Product Family - Sensitivity Values

	SL871K2L	SL871K2L-18P	SL871K2L-18B
Acquisition	-148 dBm	-148 dBm	-148 dBm
Tracking / Navigation	-166 dBm	-166 dBm	-166 dBm
Test conditions: Room Temperature and Nominal Voltage. All constellations active.			



8 RF Section

The SL871K2L family modules include a state-of-the-art receiver capable of simultaneously searching and tracking satellite signals from multiple satellite constellations. This multi-GNSS receiver uses the entire spectrum of GNSS systems available: GPS, GLONASS, Beidou, Galileo, and QZSS.

8.1 GNSS RF Signal Pin-Out

Table 20: GNSS RF Signal Pin-Out

Pin	Signal	I/O	Function	Type
11	RF_IN	I	RF signal input	Analog RF

8.2 RF Front End Design

The SL871K2L Modules Front-End characteristics make the product suitable for both passive and active antennas.

For antenna specifications, please refer to section GNSS Antenna Specification.

8.2.1 Guidelines of PCB Line for GNSS Antenna

When using the SL871K2L family modules, since there is no antenna connector on the module, the antenna must be connected to the antenna pad by means of a transmission line implemented on the PCB.

- Make sure that the antenna line impedance is 50 ohms.
- Keep the antenna line on the PCB as short as possible to reduce the loss.
- The Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- If possible, keep one layer of the PCB used only for the Ground plane.
- Surround (on both the sides, above and below) the antenna line on PCB with Ground, avoid having other signal tracks directly facing the antenna line of track.
- The ground around the antenna line on PCB must be strictly connected to the Ground Plane using vias at least once every 2mm.
- Place EM noisy devices as far as possible from antenna line.
- Keep the antenna line far away from power supply lines.
- Keep the antenna line far away from transmitting RF lines (for example Cellular, and Wi-Fi).
- If there are EM noisy devices around the PCB hosting the module, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surrounding it with Ground planes, or shielding it with a metal frame cover.



- If there are no EM noisy devices around the PCB hosting the module, use a strip-line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.

8.3 GNSS Antenna Requirements

8.3.1 GNSS Antenna Specification

Table 21: GNSS Antenna Specification

Item	Value
Frequency range	L1: 1559.0 ~ 1610.0 MHz
Gain	≤17 dB (suggested)
Impedance	50 Ω
Noise Figure of LNA	< 1.5 dB (recommended)
VSWR	≤ 3:1 (recommended)

8.3.2 GNSS Antenna – Installation Guidelines

- The antenna must be installed according to the antenna manufacturer's instructions to obtain the maximum performance from the GNSS receiver.
- The antenna location must be carefully evaluated if operating in conjunction with any other antenna or transmitter.
- The antenna must not be installed inside metal cases or near any obstacle that may degrade features such as antenna lobes and gain.

8.3.3 Powering the External LNA (Active Antenna)

The LNA of active antenna needs a power source; the VDD_RF provided by the module on pin 14 can be used for this purpose.

The electrical characteristics of the LNA_EN signal are outlined in the tables below.

Table 22: LNA_EN Signal Electrical Characteristics (SL871K2L)

Level	Min	Max
Output High Level	2.4 V	-
Output Low Level	-	0.4 V

Table 23: LNA_EN Signal Electrical Characteristics (SL871K2L-18x)

Level	Min	Max
Output High Level	0.85*VDD	-
Output Low Level	-	0.15*VDD

Customers should be aware of max bias current: in the event of an unwanted short on the antenna cable, the decoupling inductor could be damaged.



9 Mechanical Design

9.1 Drawing

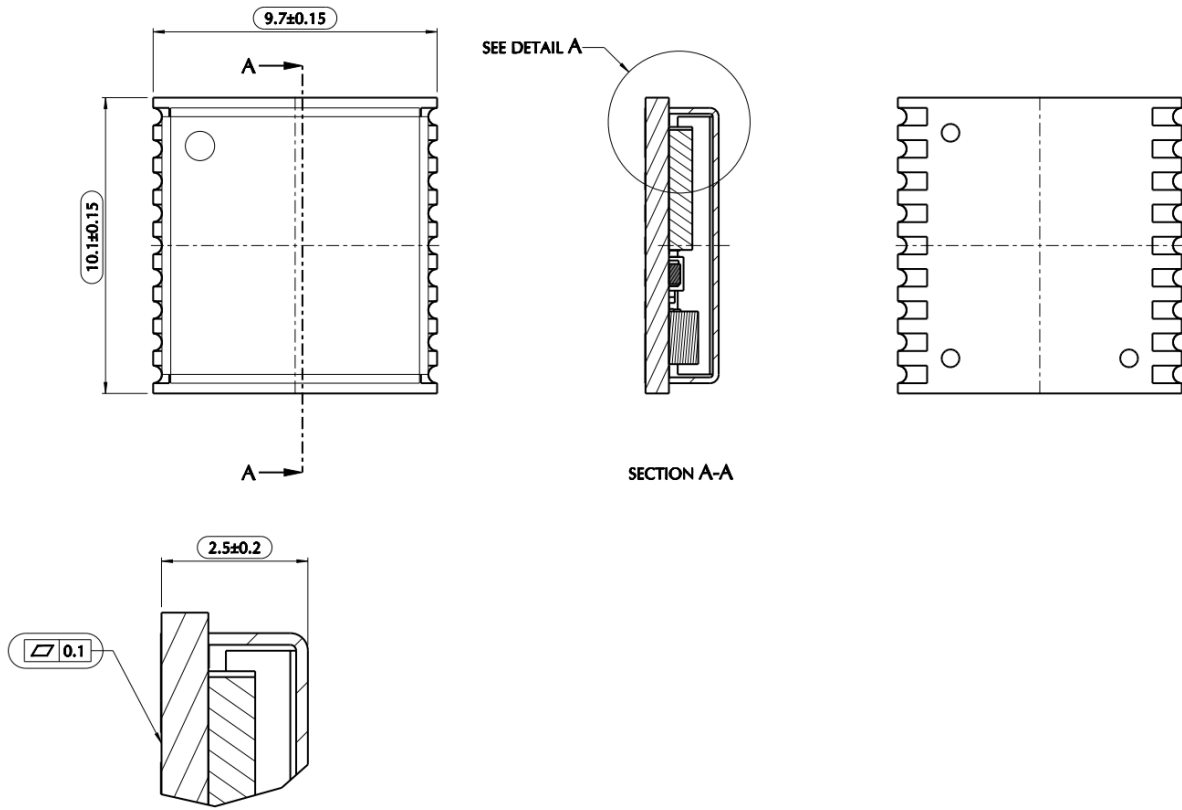


Figure 6: Mechanical drawing

10 Application PCB Design

The SL871K2L family modules are designed to be compliant with a standard lead-free SMT process.

10.1 Recommended Footprint for the Application

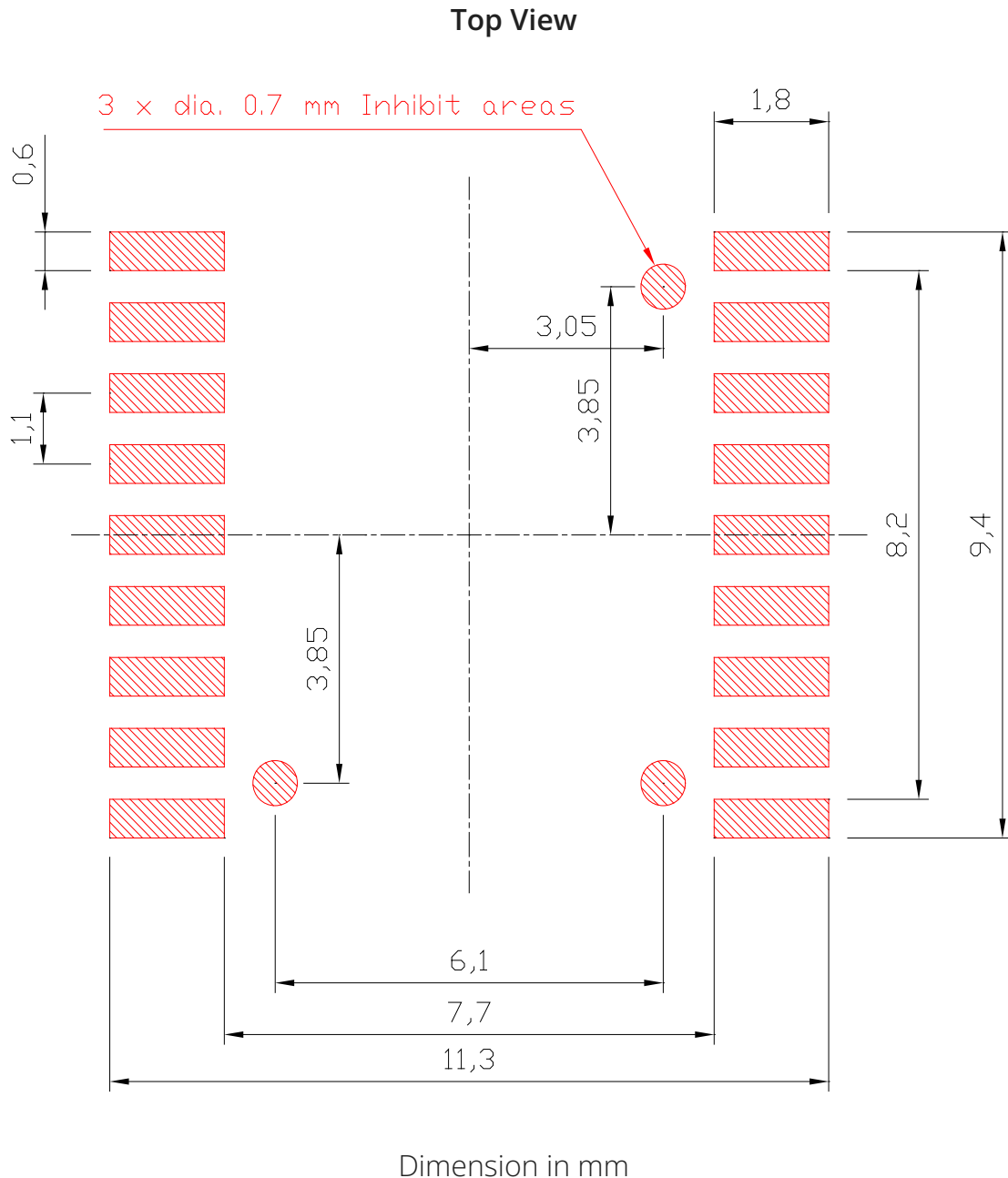


Figure 7: Recommended footprint

Note: In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths..

To make it easier to rework the SL871K2L products, it is recommended to consider a 2mm placement inhibit area around the module on the application.

As a rule, for an SMT component, avoid having any mechanical part of the application in direct contact with the module.

10.2 PCB Pad Design

In PCB design, the solder pads can be defined either as Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD). The difference between these two solder mask pad definitions is in the proximity of the solder mask to the metal pad. In SMD pads, the solder mask opening is smaller than the metal pad and overlaps the metal on all sides. The solder mask opening defines the solderable area of the pad. In NSMD pads, the solder mask opening is larger than the metal pad and does not overlap the metal. The metal edge defines the solderable area of the pad (see Figure below).

Since the metal etching process in PCB manufacturing has significantly tighter alignment and etching tolerances than the alignment registration of the solder masking process, with NSMD pads, it is possible to obtain a more accurate solder pad land pattern. Also, with SMD pads, the solder mask overlapping the metal pad introduces additional height above the metal surface which may affect solder joint adhesion and reliability. Non-solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

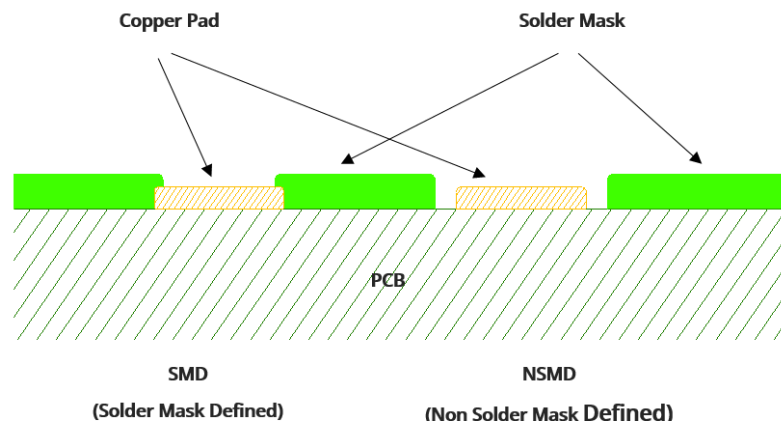


Figure 8: PCB Solder Pad Recommendations

10.3 Recommendations for PCB Pad Dimensions

It is not recommended to place via or micro-via not covered by the solder resist in an area of 0,3 mm around the pads unless it carries the same signal as the pad itself.

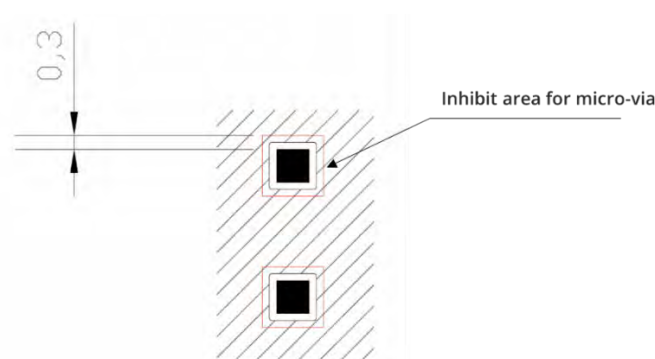


Figure 9: Pad Dimensions Recommendations

Holes in the pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Table 24: Recommendations for PCB Pad Surfaces

Finish	Layer Thickness (um)	Properties
Electroless Ni / Immersion Au	3 - 7 / 0.05 - 0.15	Good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring during the lead-free process. This issue should be discussed with the PCB supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better than compared to the lead-free solder paste.

It is not necessary to panel the application's PCB, however, in that case, it is recommended to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

10.4 Thermal Performance

FR4 is one of the most commonly used PCB materials, it is a flame-retardant composite material, composed of fibreglass-reinforced and epoxy laminate. One of the features of the FR4 is to have a very low thermal conductivity. An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias-plated through-holes (PTH) between the conductive layers. Vias are created by drilling holes and copper plating them, in the same way, a PTH or via is used for electrical interconnections between layers. A series of plated through-hole thermal vias should be located in the GND area underneath the Telit module of the PCB, to provide a thermal connection from the PCB GND to additional metal layers of the PCB.

The application PCB layout should include plated through-hole thermal vias for efficient heat dissipation from the Telit module into the PCB. One of the following thermal via types should be used:

- Open-plated through-hole vias that will provide lower PCB fabrication costs but may fill with solder.
- Plugged and capped plated through-hole vias will provide higher PCB fabrication costs but will not fill with solder.

It is recommended to use 10-mil (0.254-mm) vias arranged on a 25 mil (0.635-mm) rectilinear matrix. The reason for this choice is the combination of cost, performance and manufacturability. According to several PCB manufacturers, 10-mil holes and 25-mil spacing are reasonable and repeatable production choices.

A uniform metal plating thickness on the PCB will ensure reliable, high Telit module solder assembly yield.



10.5 Stencil

A silk-screen process will be required for the deposition of solder paste on the PCB, for the reflow of the Telit module on the PCB. The silk-screen process requires the use of a metal stencil based on an opening where the solder paste is transferred through the openings on the solder pads of the application PCB. To minimize solder voids and ensure maximum electrical and thermal connectivity of the module to the PCB, large pads, solder volume, and solder strain must be considered in the stencil design. The design and fabrication of the stencil determine the quality of the solder paste deposition onto the PCB and the resulting solder joint after reflow. The primary stencil parameters are aperture size, thickness, and fabrication method. The stencil should be made from stainless steel and the apertures layout can be the same as the recommended footprint (1:1). The recommended thickness shall be 127 μm (5 mil). A stencil thickness of 152 μm (6 mil) can be used as well.

10.6 Solder Paste

Various types and grades of solder paste can be used for surface mounting Telit modules. For lead-free applications, an Sn-Ag (SA) or Sn-Ag-Cu (SAC) solder paste can be used. Any Type 3 solder paste that is either water-soluble or not clean is acceptable.

It is recommended to use only “no clean” solder paste to avoid the cleaning of the modules after assembly.

10.7 Solder Reflow

Recommended solder reflow profile:

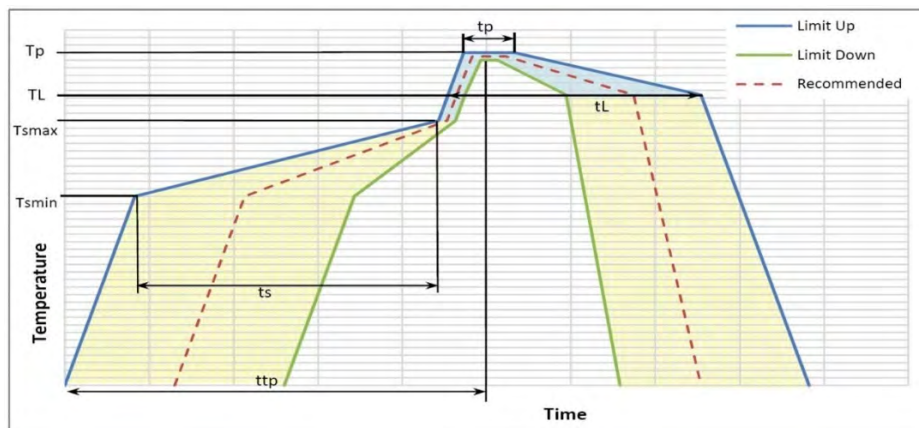


Figure 10: Recommended Solder Reflow Profile

Table 25: Profile Feature Recommendations

Profile Feature	Pb-Free Assembly Free
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat <ul style="list-style-type: none"> • Temperature Min (T_{smin}) • Temperature Max (T_{smax}) • Time (min to max) (t_s) 	150°C 200°C 60-180 seconds
T_{smax} to T_L <ul style="list-style-type: none"> • Ramp-up Rate 	3°C/second max
Time maintained above: <ul style="list-style-type: none"> • Temperature (T_L) • Time (t_L) 	217°C 60-150 seconds
Peak Temperature (T_p)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (t_p)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Note: All temperatures refer to the topside of the package, measured on the package body surface.

Warning: THE SL871K2L SERIES MODULES WITHSTAND ONE REFLOW PROCESS ONLY.

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customers must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage.

10.8 Inspection

An inspection of the solder joint between the solder pads of the Telit module and the application PCB should be performed. The best visual inspection tool for inspection of the Telit module solder joints on the PCB is a transmission X-ray, which can identify defects such as solder bridging, shorts, opens, and large voids.

Note: Small voids in large solder joints are not detrimental to the reliability of the solder joint.



11 Packaging

11.1 Reel

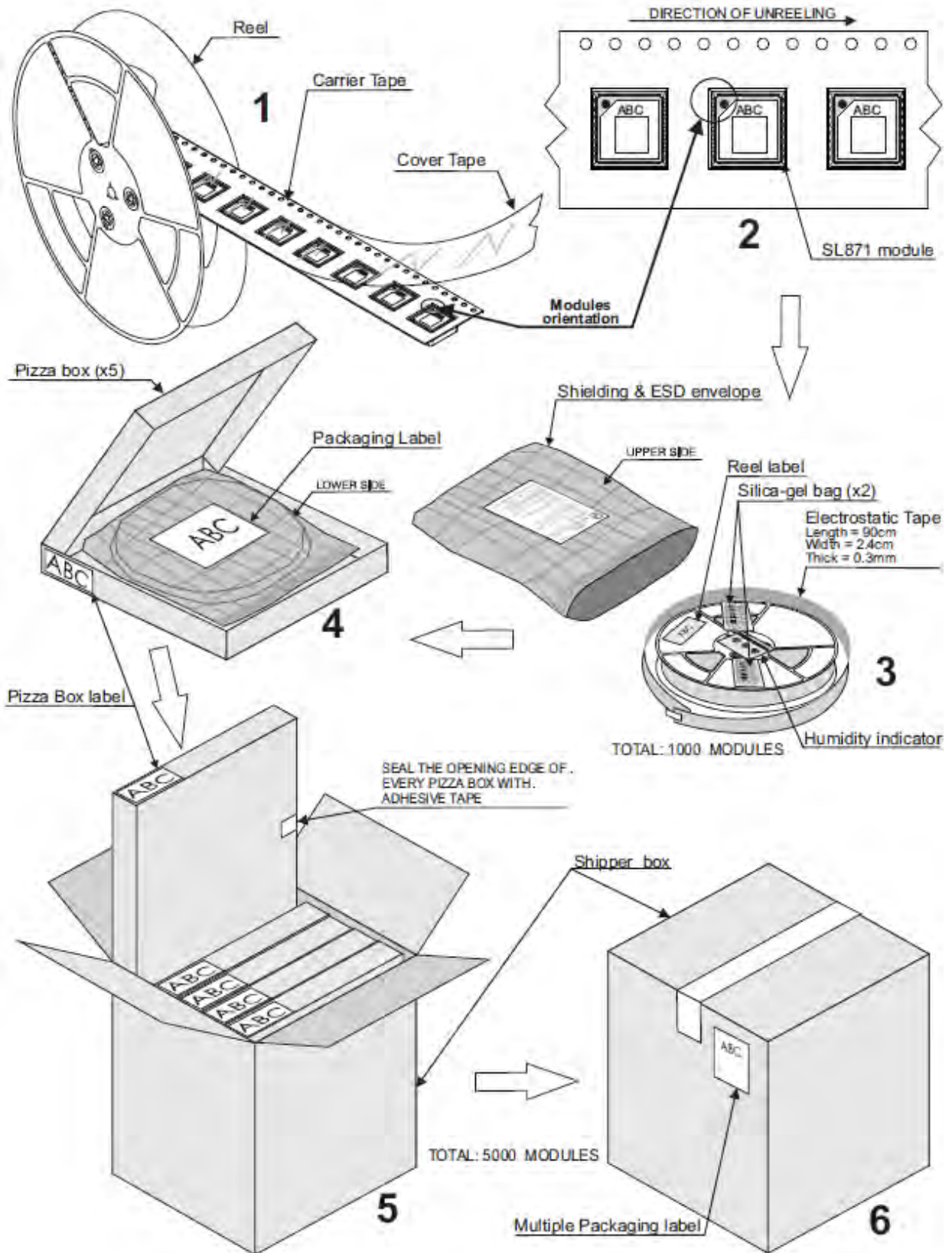


Figure 11: Reel

11.2 Mini Reel

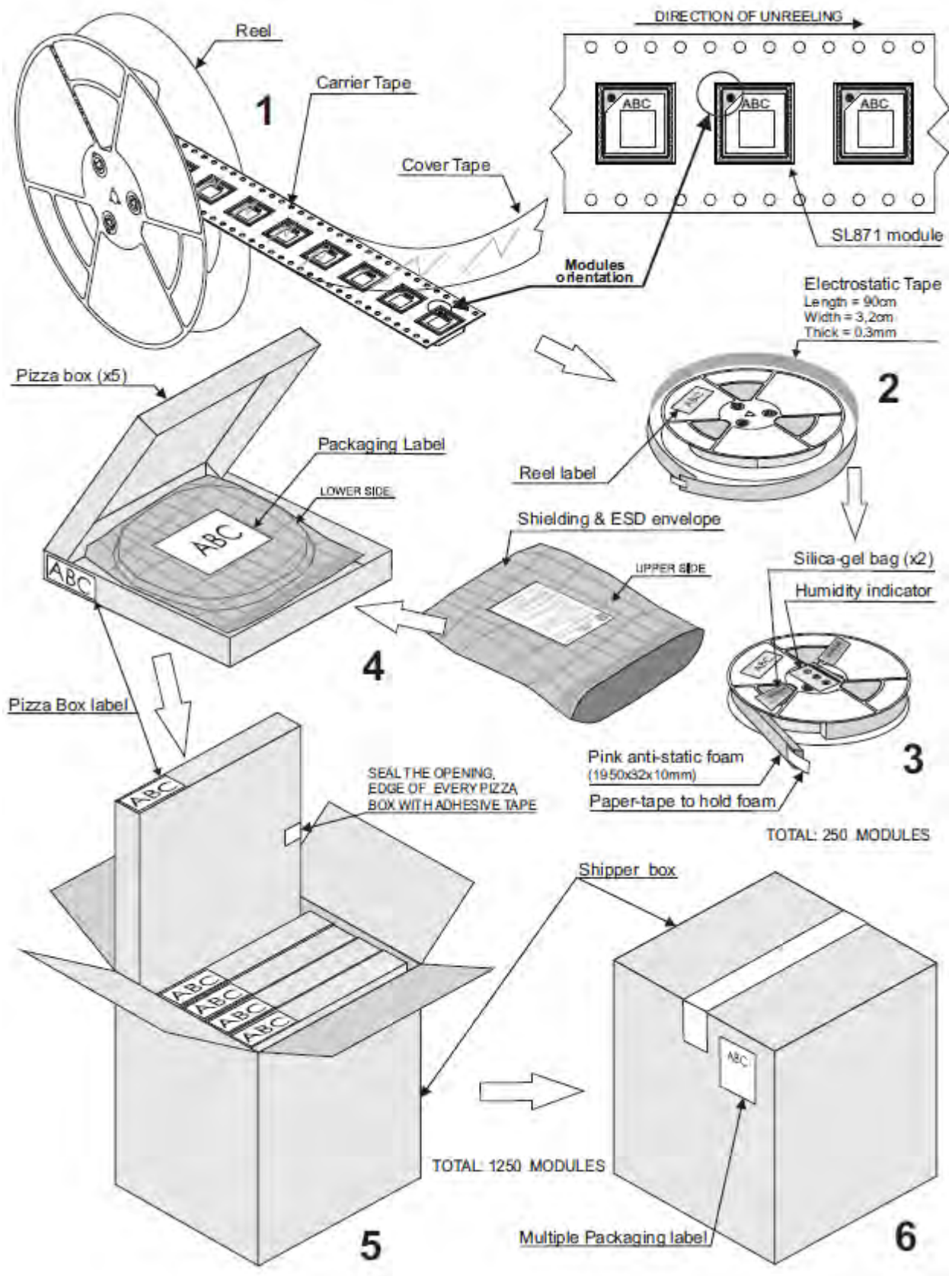


Figure 12: Mini Reel

11.3 Moisture Sensitivity

The SL871K2L modules are Moisture Sensitive Devices level 3, according to standard IPC/JEDEC J-STD-020, and takes care of all the relative requirements for using this kind of component.

Moreover, the customer has to take care of the following conditions:

- a** Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH).
- b** An environmental condition during the production: - c** The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033D paragraph 5.2" is respected
- d** Baking is required if conditions b) or c) are not respected
- e** Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

12 Conformity Assessment Issues

12.1 EU RED Declaration of Conformity

This section will be updated in a future document revision

12.2 RoHS Info

Any requests for information related to RoHS certifications can be addressed to Chemical.Certifications@telit.com.

12.3 REACH Info

Any requests for information related to REACH certifications can be addressed to Chemical.Certifications@telit.com

13 Acronyms and Abbreviations

Table 26: Acronyms and Abbreviations

Acronym	Definition
AIC	Active Interference Cancellation
CS	Chip Select
DRI	Data Ready Indicator
ESR	Equivalent Series Resistance
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPS	Global Positioning System
I/O	Input Output
LNA	Low Noise Amplifier
MISO	Master Input – Slave Output
MOSI	Master Output – Slave Input
PCB	Printed Circuit Board
1PPS	1 Pulse Per Second
QZSS	Quasi-Zenith Satellite System
RTC	Real-Time Clock
SAW	Surface Acoustic Wave
TCXO	Temperature Compensated Crystal Oscillators
UART	Universal Asynchronous Receiver Transmitter
VSWR	Voltage Standing Wave Ratio



14 Related Documents

For current documentation and downloads, refer to <https://dz.telit.com/>.

Table 27: Related Documents

S.no	Doc Code	Document Title
1	1W0302032	SL871K2L Product Family EVK User Guide
2	80832NT12188A	SL871 Family Reference Design Application Note
3	1W0302030	V12 Software User Guide
4	1W0301544	Telit GNSS Software Extensions User Guide

15 Document History

Table 28: Document History

Revision	Date	Changes
3	2025-09-08	HW RTC power consumption added (sections 5.3 and 5.4) UART0 detail (section 6.2.1)
2	2025-05-19	Logic Levels section updated (section 6.1) Sensitivity values updated (section 7.3) Power supply requirements updated (section 5.1) SL871K2 power consumption values added (section 5.4) Low power measures added (sections 5.3 and 5.4)
1	2025-04-07	Updated section 2.3 Corrected typos in sections 3.2 and 3.3 Block Diagram updated in section 3.4 RTC power up/down updated (section 5.3) Power consumption values updated (section 5.4) Power Supply Design Rules updated (section 5.5) Updated Antenna detection sections 6.3.5 and 6.3.6 Table design updated (sections 5.4, 7.1, 7.2, 7.3) Logic Levels updated (section 6.1) TTFE updated (section 7.2) Sensitivity updated (section 7.3)
0	2025-03-14	Initial release

From Mod.0818 Rev.17



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