TB3315

Getting Started with the Complimentary Waveform Generator (CWG)

Introduction

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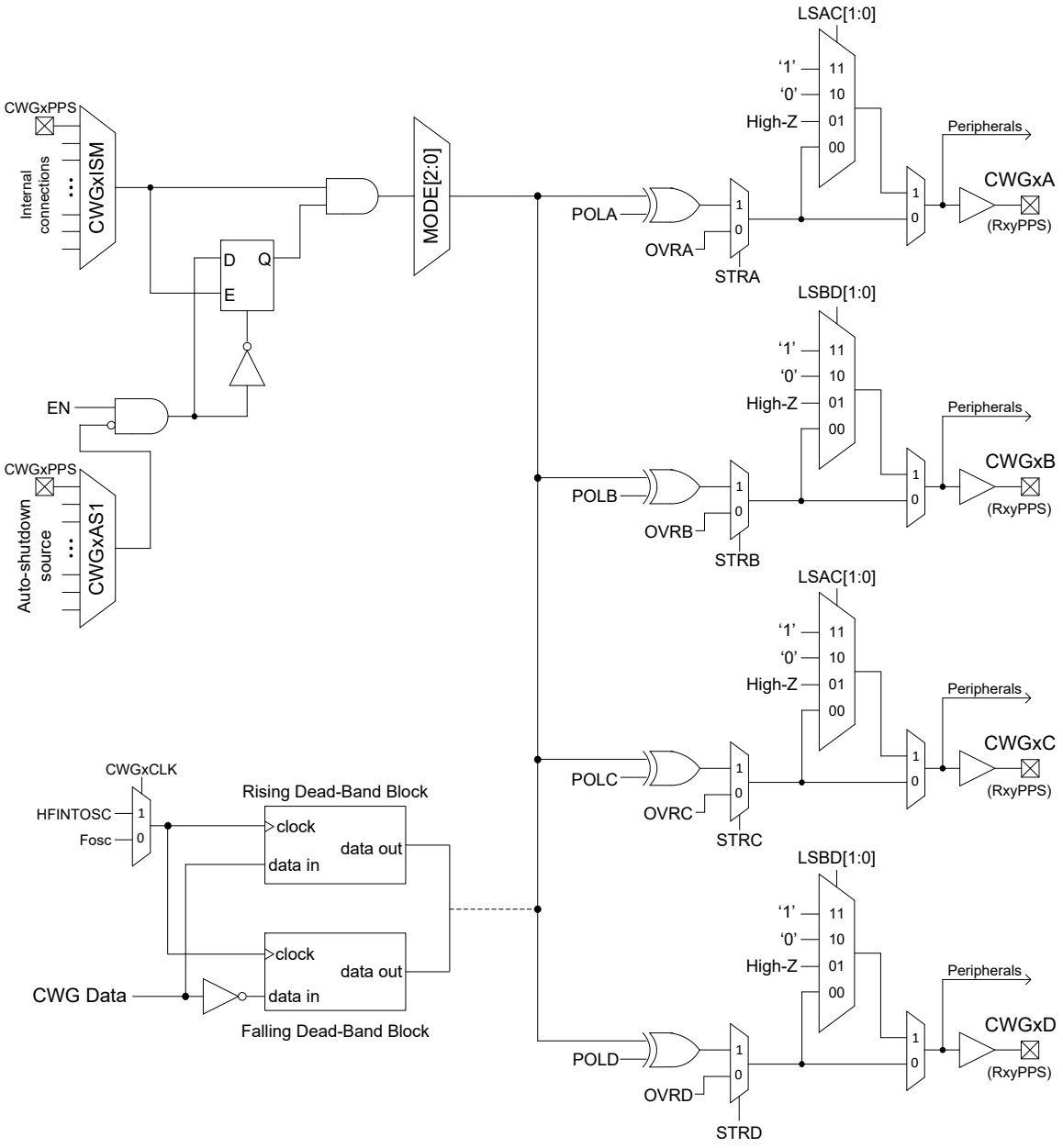
The Complementary Waveform Generator (CWG) peripheral generates Pulse-Width Modulated (PWM) waveforms that can be used in a variety of applications, such as motor control or LED lighting. The CWG can produce up to four output signals from a single selectable input source. The output signals can be used in several modes of operation, such as Half Bridge or Full Bridge modes with dead-band control, Synchronous or Asynchronous Steering modes, and Push-Pull mode. Each CWG output has its own independent polarity control, and may be routed to one of several pins through the Peripheral Pin Select (PPS) module. Selectable Auto-Shutdown sources can be used to immediately halt the CWG outputs during a fault condition, and allows the module to resume operation once the fault condition has been removed.

Figure 1 shows the simplified block diagram of the CWG module.

Figure 1. CWG Simplified Block Diagram



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1. Operating Modes

The CWG can operate in six different modes, which are selected through the CWG Mode (MODE) bits:

- Half Bridge mode
- Push-Pull mode
- Asynchronous Steering mode
- Synchronous Steering mode
- Full Bridge Forward mode
- Full Bridge Reverse mode

All modes accept a single-pulse input, and provide up to four outputs. All modes also include Auto-Shutdown control.

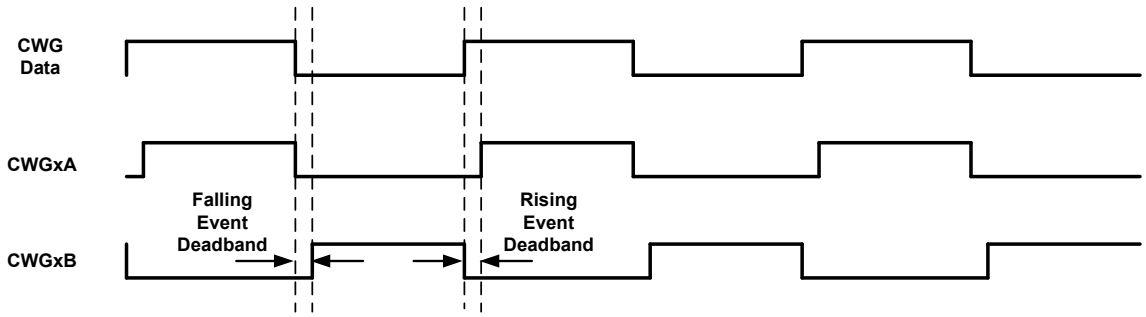
Important: Except in Full Bridge modes, mode changes must only be performed while the CWG Enable (EN) bit is clear (EN = 0).

1.1 Half Bridge Mode

In Half Bridge mode, the CWG generates two output signals which are true and inverted versions of the input signal (see Figure 1-1). A dead-band delay is inserted between the two outputs to prevent shoot-through current in power supply applications. In Half Bridge mode, outputs CWGxA and CWGxB are complimentary. The unused outputs CWGxC and CWGxD are copies of outputs CWGxA and CWGxC, respectively. The polarity of each output is controlled by the individual CWG Output Polarity (POLx) bits of the CWGxCON1 register.

Important: Steering modes are not available in Half Bridge mode.

Figure 1-1. Half Bridge Waveform



1.2 Push-Pull Mode

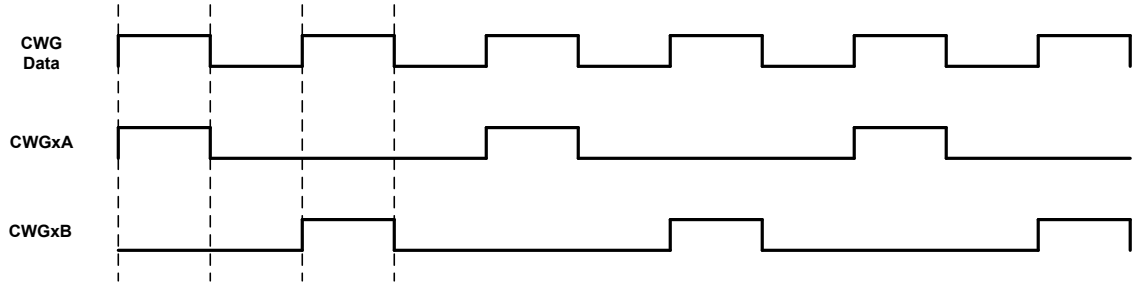
In Push-Pull mode, the CWG outputs two alternating copies of the selected input as shown in Figure 1-2 below. The alternating signals create a push-pull effect, which is required for driving many transformer-based power supply applications.

The Push-Pull sequencer is reset whenever the CWG Enable (EN) bit of the CWGxCON0 register is clear (EN = 0), or if an Auto-Shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWGxA.

The unused outputs CWGxC and CWGxD are copies of outputs CWGxA and CWGxB, respectively. The polarity of each output is controlled by the individual CWG Output Polarity (POLx) bits of the CWGxCON1 register.

Important: Steering modes are not available in Push-Pull mode.

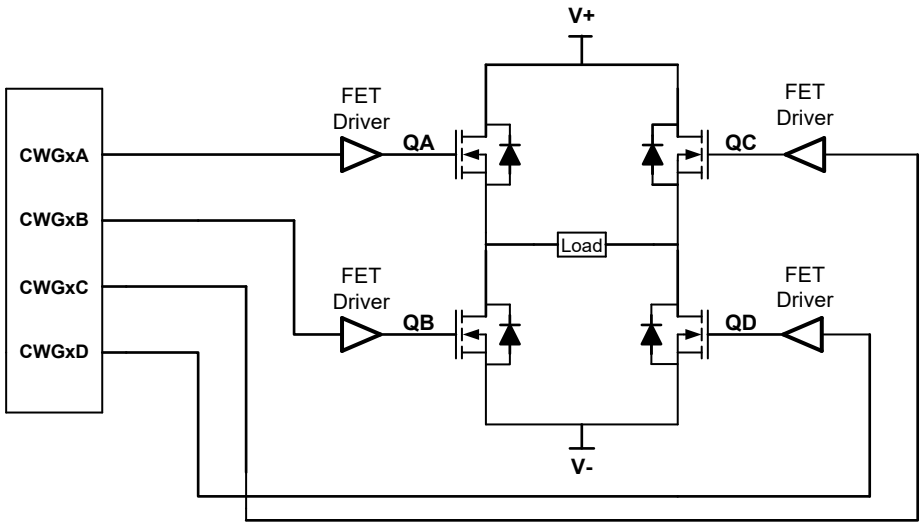
Figure 1-2. Push-Pull Mode Waveforms



1.3 Full Bridge Mode

In Forward and Reverse Full Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. The mode selection may be toggled between forward and reverse by toggling the MODE[0] bit of the CWGxCON0 register while keeping the MODE[2:1] bits static, without disabling the CWG module. When connected, as shown in Figure 1-3, the outputs are appropriate for a full bridge motor driver. Each CWG output signal has independent polarity control, so the circuit can be adapted to high-active and low-active drivers.

Figure 1-3. Example of Full Bridge Application



In Forward Full Bridge mode (MODE = `'b010`), CWGxA is driven to its Active state, CWGxB and CWGxC are driven to their Inactive states, and CWGxD is modulated by the input signal, as shown in Figure 1-4.

In Reverse Full Bridge mode (MODE = `'b011`), CWGxC is driven to its Active state, CWGxA and CWGxD are driven to their Inactive states, and CWGxB is modulated by the input signal, as shown in Figure 1-5.

In Full Bridge mode, the dead-band period is used when there is a switch from forward to reverse or vice versa. This dead-band control is described in the Dead-Band Control section, with additional details in the Rising Edge and Reverse Dead Band and Falling Edge and Forward Dead Band sections.

Important: Steering modes are not used with either of the Full Bridge modes.

Figure 1-4. Example of Full Bridge Forward Mode Output

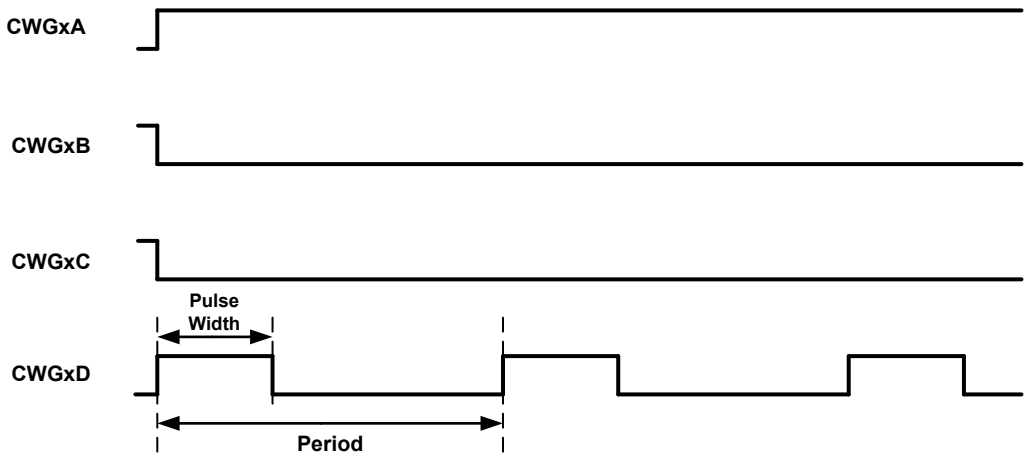
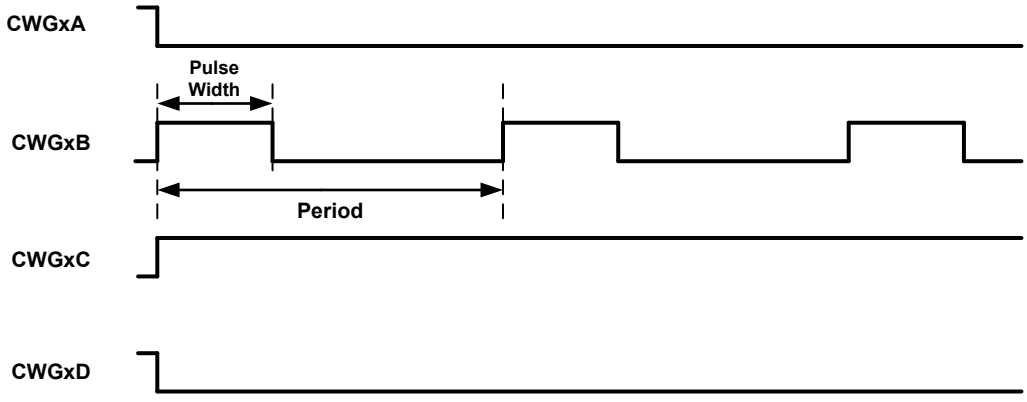


Figure 1-5. Example of Full Bridge Reverse Mode Output



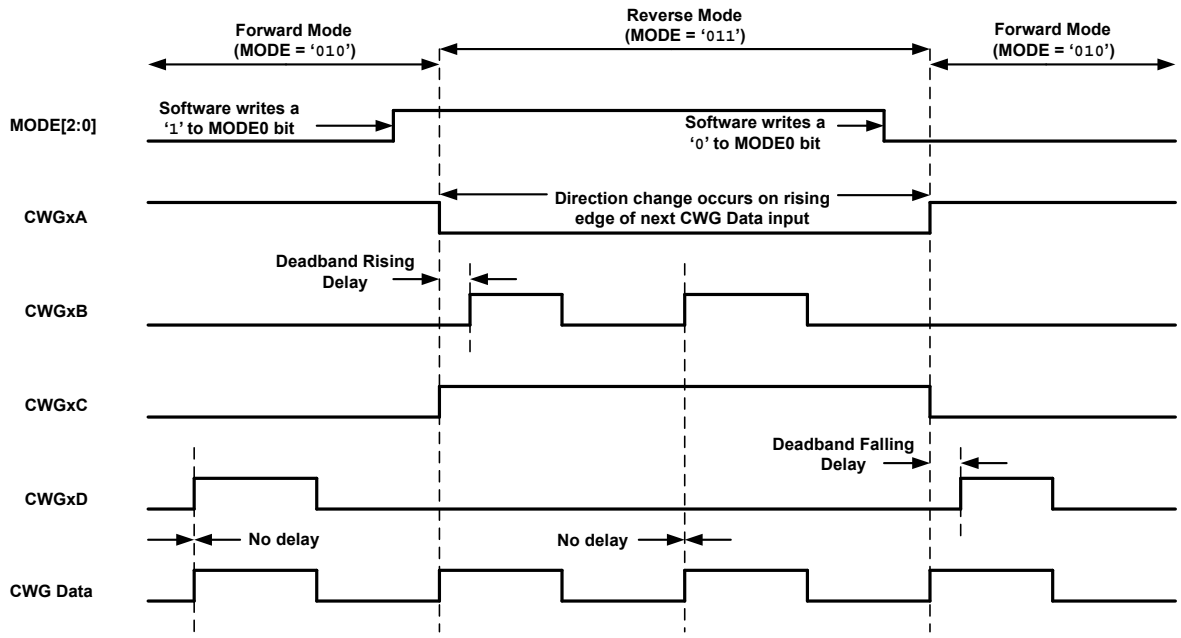
Note: A rising CWG data input creates a rising event on the modulated output.

1.3.1 Direction Change in Full Bridge Mode

In Full Bridge mode, changing the MODE[0] bit controls the forward/reverse direction. Direction changes occur on the next rising edge of the modulated input. The sequence, described as follows, is illustrated in Figure 1-6.

1. The associated active output CWGxA and the inactive output CWGxC are switched to drive in the opposite direction.
2. The previously modulated output CWGxD is switched to the Inactive state, and the previously inactive output CWGxB begins to modulate.
3. CWG modulation resumes after the direction-switch dead band has elapsed.

Figure 1-6. Example of PWM Direction Change



1.3.2 Dead-Band Delay in Full Bridge Mode

Dead-band delay is important when either of the following conditions is true:

- The direction of the CWG output changes when the duty cycle of the data input is at or near 100%.
- The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

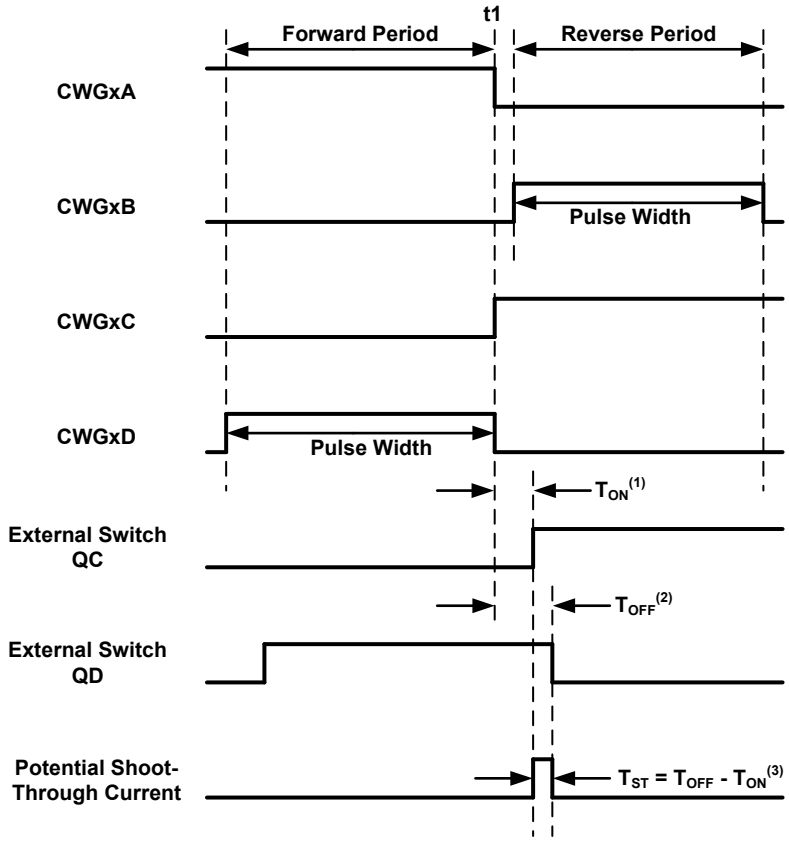
The dead-band delay is inserted only when changing directions, and only the modulated output is affected. The statically-configured outputs (CWGxA and CWGxC) are not afforded dead band, and switch essentially simultaneously.

Figure 1-7 shows an example of the CWG outputs changing directions from forward to reverse, at near 100% duty cycle. In this example, at time t1, the output of CWGxA and CWGxD becomes inactive, while the output of CWGxC becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through the power devices QC and QD (see Figure 1-3) for the duration of 'T_{ST}'. The same phenomenon will occur to power devices QA and QB for the CWG direction change from reverse to forward.

When changing the CWG direction, a high duty cycle is required for an application. Two possible solutions for eliminating the shoot-through current are:

1. Reduce the CWG duty cycle for one period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

Figure 1-7. Example of PWM Direction Change at Near 100% Duty Cycle



Notes:

1. T_{ON} is the turn-on delay of the circuit's power switch QC and its driver.
2. T_{OFF} is the turn-off delay of the circuit's power switch QD and its driver.
3. T_{ST} is the circuit's potential shoot-through current time due to both switches, QC and QD (Figure 1-3), conducting simultaneously.

1.4 Steering Modes

In both Synchronous and Asynchronous Steering modes, the CWG Data can be steered to any combination of four CWG outputs. A fixed value will be presented on all the outputs not used for the PWM output. Each output has independent polarity, steering, and shutdown options.

For example, when the Steering Enable A (STRA) bit = `0`, the corresponding pin is held at the level defined by the Steering Data A (OVRA) bit. When STRA = `1`, the pin is driven by the CWG Data signal. The Output Polarity (POLy) bits control the signal polarity only when STRy = `1`.

The CWG auto-shutdown operation also applies in Steering modes as described in the Auto-Shutdown section. An auto-shutdown event will only affect pins that have STRy = `1`.

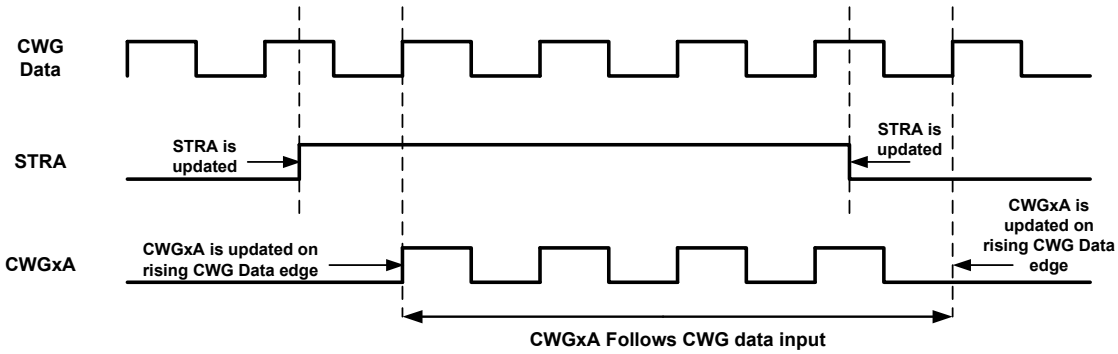
Important: Dead-band control is not used in either Steering mode.

1.4.1 Synchronous Steering Mode

In Synchronous Steering mode (MODE = `'b001`), the changes to steering selection registers take effect on the next rising edge of CWG Data (see Figure 1-8). In Synchronous Steering mode, the output will always produce a complete waveform.

Important: Only the STRx bits are synchronized with the CWG data; the OVRx bits are not synchronized.

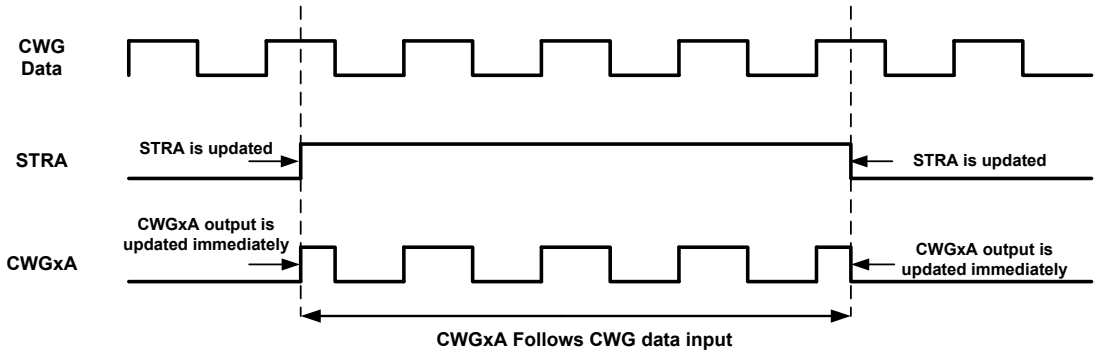
Figure 1-8. Synchronous Steering Mode Waveform



1.4.2 Asynchronous Steering Mode

In Asynchronous Steering mode (MODE = `'b000`), steering takes effect at the end of the instruction cycle that writes to STRx. In Asynchronous Steering mode, the output signal may be an incomplete waveform (see Figure 1-9). This operation may be useful when the user firmware needs to immediately remove a signal from the output pin.

Figure 1-9. Asynchronous Steering Mode Waveform



1.4.3 Start-Up Considerations

The application hardware must use the proper external pull-up and/or pull-down resistors on the CWG output pins. This is required because all I/O pins are forced to high-impedance at Reset.

The Polarity Control (POLy) bits allow the user to choose whether the output signals are active-high or active-low.

2. Input Selection

The CWG generates up to four complementary output waveforms using one of several selectable input sources. Input selections are made using the CWG Data Input Source Select (ISM) bits of the CWGxISM register. Selections include both internal signals, such as the output of a Pulse-Width Modulator (PWM) or Configurable Logic Cell (CLC), and external signals, which are routed through the CWGxINPPS pin.

Important: When using an internal peripheral as the input source, the peripheral must be configured and enabled before it can be used as an input to the CWG.

3. Clock Source

The clock source is used to drive the dead-band timing circuits. The CWG module allows the following clock sources to be selected:

- F_{OSC} (system clock)
- HFINTOSC

Important: When the HFINTOSC is selected, the HFINTOSC will be kept running during Sleep. Therefore, the CWG modes requiring dead-band can operate in Sleep, provided that the CWG data input is also active during Sleep. The clock sources are selected using the CWG Clock Source Selection (CS) bit.

4. Dead-Band Control

The dead-band control provides non-overlapping complementary outputs to prevent shoot-through current when the outputs switch. The CWG contains two 6-bit dead-band counters, the CWGx Rising Dead-Band Count (CWGxDBR) and CWGx Falling Dead-Band Count (CWGxDBF) registers. CWGxDBR is used for the rising edge of the input source control in Half Bridge mode or for reverse direction change dead band in Full Bridge mode. CWGxDBF is used for the falling edge of the input source control in Half Bridge mode or for forward direction change dead band in Full Bridge mode.

Dead band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers.

Important: Dead-band operation is employed for Half Bridge and Full Bridge modes.

4.1 Dead-Band Functionality in Half Bridge Mode

In Half Bridge mode, the dead-band counters dictate the delay between the falling edge of the normal output and the rising edge of the inverted output. This can be seen in Figure 1-1.

4.2 Dead-Band Functionality in Full Bridge Mode

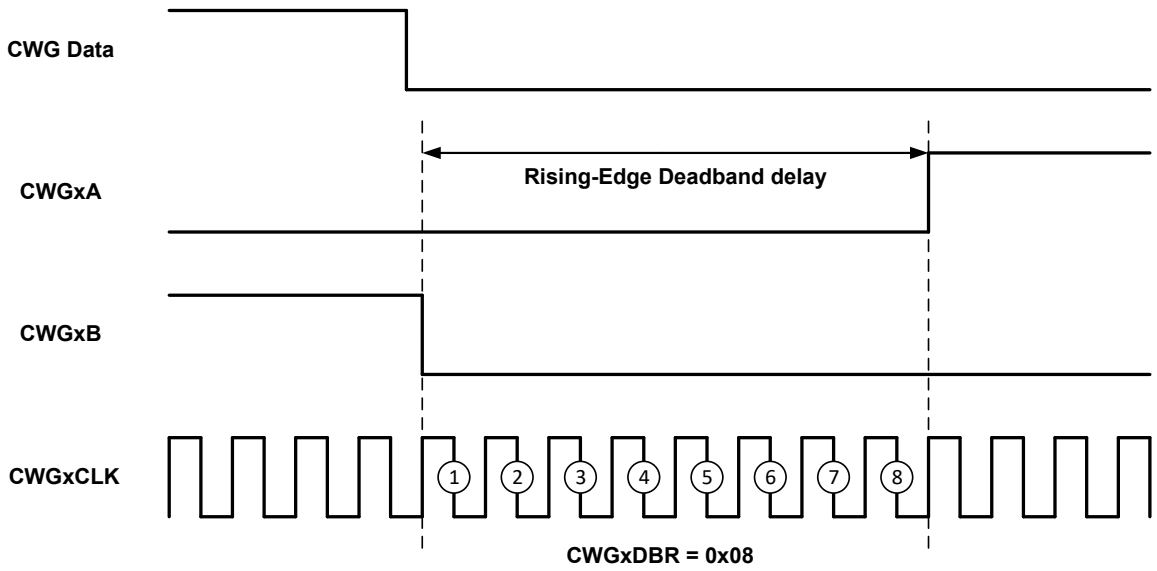
In Full Bridge mode, the dead-band counters are used when undergoing a direction change. The MODE[0] bit can be set or cleared while the CWG is running, allowing for changes from Forward to Reverse mode. The CWGxA and CWGxC signals will change immediately upon the first rising input edge following a direction change, but the modulated signals (CWGxB or CWGxD, depending on the direction of the change) will experience a delay dictated by the dead-band counters.

4.3 Rising Edge and Reverse Dead-Band

In Half Bridge mode, the rising edge dead-band delays the turn-on of the CWGxA output after the rising edge of the CWG data input. In Full Bridge mode, the reverse dead-band delay is only inserted when changing directions from Forward mode to Reverse mode, and only the modulated output, CWGxB, is affected.

The CWGxDBR register determines the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 periods of the CWG clock. Figure 4-1 illustrates different dead-band delays for rising and falling CWG Data events.

Figure 4-1. Rising Edge Dead-Band Operation, CWGxDBR = 0x08



Dead-band is always initiated on the edge of the input source signal. A count of zero indicates that no dead-band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

The CWGxDBR register value is double-buffered. When the CWG Enable (EN) bit = 0, the buffer is loaded when CWGxDBR is written. When EN = 1, the buffer will be loaded at the rising edge following the first falling edge of the CWG Data, after the CWG Load Buffers (LD) bit is set.

4.4 Falling Edge and Forward Dead-Band

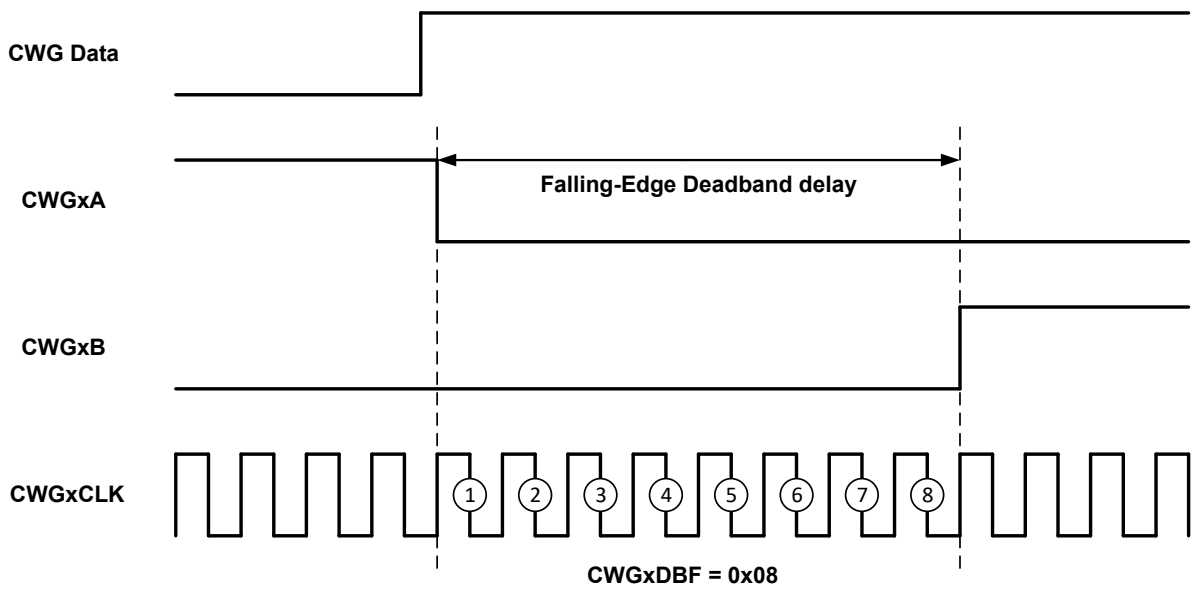
In Half Bridge mode, the falling edge dead-band delays the turn-on of the CWGxB output at the falling edge of the CWG data input. In Full Bridge mode, the forward dead-band delay is only inserted when changing directions from Reverse mode to Forward mode, and only the modulated output, CWGxD, is affected.

The CWGxDBF register determines the duration of the dead-band interval on the falling edge of the input source signal. This duration is from 0 to 64 periods of the CWG clock.

Dead-band delay is always initiated on the edge of the input source signal. A count of zero indicates that no dead-band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

Figure 4-2. Falling Edge Dead-Band Operation, CWGxDBF = 0x08



The CWGxDBF register value is double-buffered. When EN = 0, the buffer is loaded when CWGxDBF is written. When EN = 1, the buffer will be loaded at the rising edge following the first falling edge of the data input after the LD bit is set.

4.5 Dead-Band Jitter

When the rising and falling edges of the input source are asynchronous to the CWG clock, it creates jitter in the dead-band time delay. The maximum jitter is equal to one CWG clock period. Refer to the equations below for more details.

Equation 4-1. Dead-Band Delay Time Calculation

$$T_{DEAD-BAND\_MIN} = \frac{1}{F_{CWG\_CLOCK}} \bullet DBx$$

$$T_{DEAD-BAND\_MAX} = \frac{1}{F_{CWG\_CLOCK}} \bullet (DBx + 1)$$

$$T_{JITTER} = T_{DEAD-BAND\_MAX} - T_{DEAD-BAND\_MIN}$$

$$T_{JITTER} = \frac{1}{F_{CWG\_CLOCK}}$$

$$T_{DEAD-BAND\_MAX} = T_{DEAD-BAND\_MIN} + T_{JITTER}$$

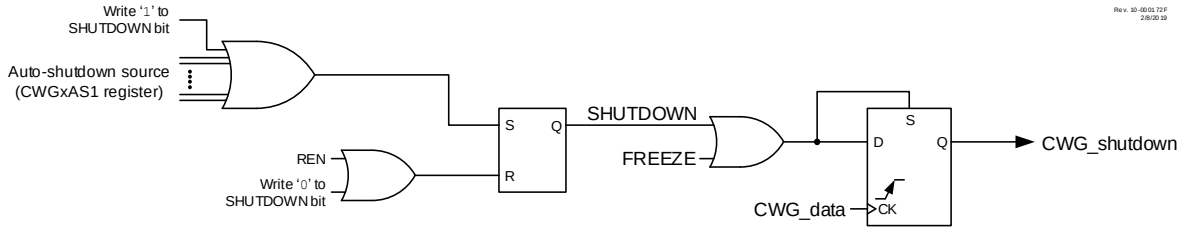
Dead-Band Delay Example Calculation

$DBx = 0x0A = 10$
$F_{CWG\_CLOCK} = 8\ MHz$
$T_{JITTER} = \frac{1}{8\ MHz} = 125\ ns$
$T_{DEAD-BAND\_MIN} = 125\ ns \bullet 10 = 1.25\ \mu s$
$T_{DEAD-BAND\_MAX} = 1.25\ \mu s + 0.125\ \ \mu s = 1.37\ \mu s$

5. Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in the following figure.

Figure 5-1. CWG Shutdown Block Diagram



5.1 Shutdown

The Shutdown state can be entered by either of the following two methods:

- Software Generated
- External Input

5.1.1 Software Generated Shutdown

Setting the CWG Auto-Shutdown Event Status (SHUTDOWN) bit will force the CWG into the Shutdown state.

When the auto-restart is disabled, the Shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event. The SHUTDOWN bit indicates when a Shutdown condition exists. The bit may be set or cleared in software or by hardware.

5.1.2 External Input Source

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition. When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the selected override levels without software delay. The override levels are selected by the CWGxB and CWGxD Auto-Shutdown State Control (LSBD) and CWGxA and CWGxC Auto-Shutdown State Control (LSAC) bits. Several input sources can be selected to cause a Shutdown condition. All input sources are active-low. The shutdown input sources are individually enabled by the CWG Auto-Shutdown Source Enable (ASyE) bits.

Important: Shutdown inputs are level sensitive, not edge sensitive. The Shutdown state cannot be cleared, except by disabling auto-shutdown, as long as the shutdown input level persists.

5.1.3 Pin Override Levels

The levels driven to the CWG outputs during an auto-shutdown event are controlled by the LSBD and LSAC bits. The LSBD bits control CWGxB/D output levels, while the LSAC bits control the CWGxA/C output levels.

5.1.4 Auto-Shutdown Interrupts

When an Auto-Shutdown event occurs, either by software or hardware setting SHUTDOWN, the CWGxIF flag bit of the PIRx register is set. If the CWGxIE bit is also set, an interrupt event will occur.

5.2 Auto-Shutdown Restart

After an Auto-Shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

In either case, the Shutdown source must be cleared before the restart can take place. That is, either the Shutdown condition must be removed, or the corresponding ASyE bit must be cleared.

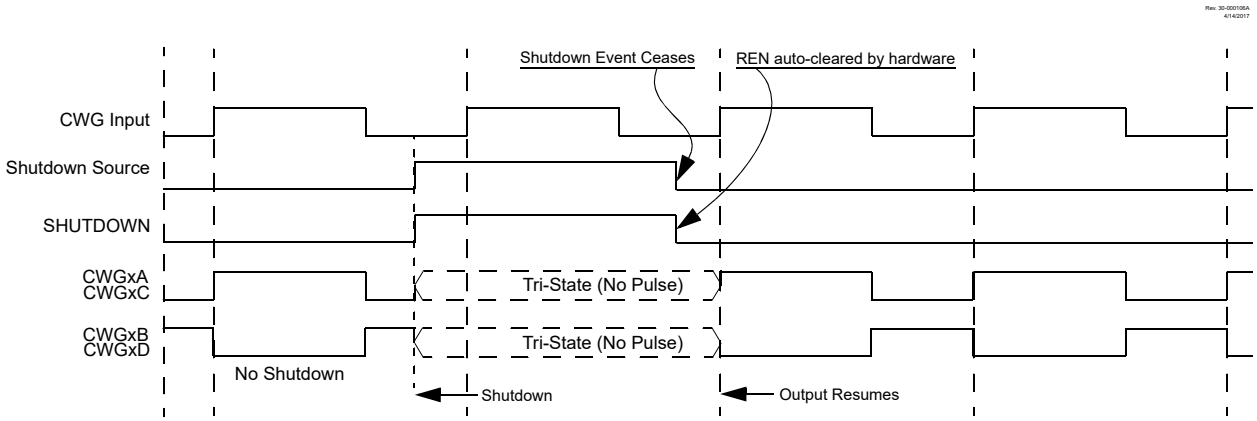
5.2.1 Auto-Restart

When the CWG Auto-Restart (REN) bit is set (REN = `1`), the CWG module will restart from the Shutdown state automatically.

Once all Auto-Shutdown conditions are removed, the hardware will automatically clear the SHUTDOWN bit. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Important: The SHUTDOWN bit cannot be cleared in software if the Auto-Shutdown condition is still present.

Figure 5-2. Shutdown Functionality, Auto-Restart Enabled (REN = `1`, LSAC = `'b01`, LSBD = `'b01`)



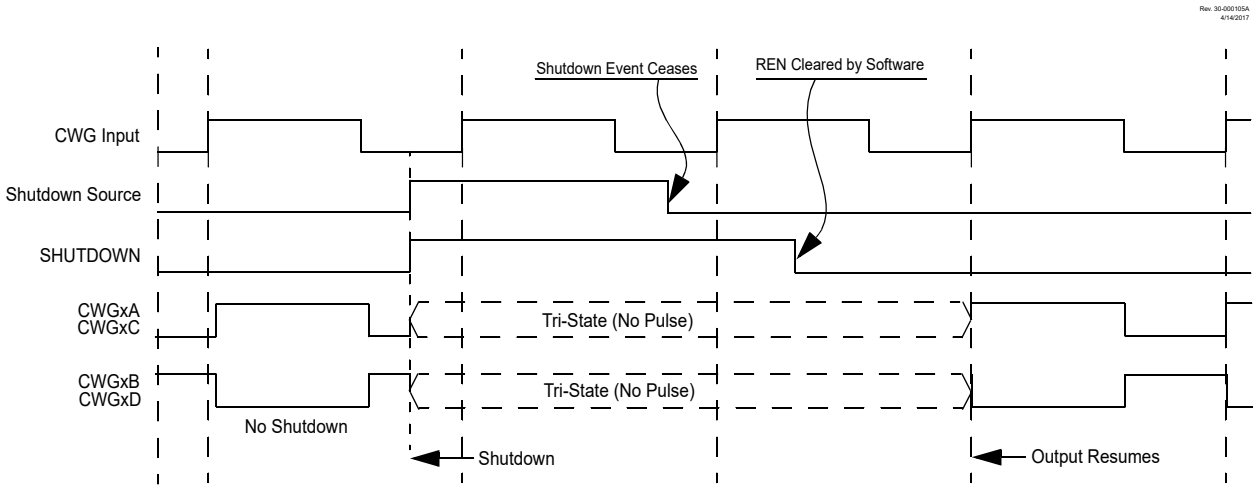
5.2.2 Software-Controlled Restart

When the REN bit is clear (REN = `0`), the CWG module must be restarted after an Auto-Shutdown event through software.

Once all Auto-Shutdown sources are removed, the software must clear the SHUTDOWN bit. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Important: The SHUTDOWN bit cannot be cleared in software if the Auto-Shutdown condition is still present.

Figure 5-3. Shutdown Functionality, Auto-Restart Disabled (REN = 0, LSAC = 'b01, LSBD = 'b01)



6. CWG Output

Each CWG output can be routed to a Peripheral Pin Select (PPS) output via the RxyPPS register. Refer to the device datasheet's **"PPS - Peripheral Pin Select Module"** chapter for more details.

6.1 Polarity Control

The polarity of each CWG output can be selected independently. Output polarity is selected with the CWG Output Polarity (POLy) bits. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. Polarity does not affect the override levels, Steering mode options, or Auto-Shutdown functionality.

7. Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, then the CPU will go Idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

Important: The system clock F_{OSC} is disabled in Sleep and thus dead-band control cannot be used.

8. Conclusion

The Complementary Waveform Generator (CWG) peripheral generates Pulse-Width Modulated (PWM) waveforms. The CWG can produce up to four output signals from a single selectable input source. The output signals can be used in several modes of operation. Each CWG output has its own independent polarity control, and may be routed to one of several pins through the Peripheral Pin Select (PPS) module. The Auto-Shutdown feature can be used to immediately halt the CWG outputs during a fault condition and allow the module to resume operation once the fault condition has been removed.

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