SuperQ™ MOSFETs The High-Voltage Discharge Switch Engineered for Superior Short-Circuit Robustness in Battery Management Systems

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Abstract

The accelerating shift to high-voltage battery platforms (72V and above) in e-mobility and power tools is placing unprecedented demands on battery management system (BMS) protection circuitry. The discharge MOSFET is the critical barrier against catastrophic failure during external short-circuit events, which can generate currents reaching thousands of amps in microseconds. Traditional MOSFET technologies often compromise between achieving low on-resistance ($R_{DS(on)}$) for high efficiency and the robust short-circuit withstand capability (SCWC) required for safety. This application note introduces iDEAL Semiconductor's SuperQ MOSFET technology, which leverages a proprietary cell structure to deliver market-leading SCWC while maintaining ultra-low $R_{DS(on)}$. Our testing demonstrates that the SuperQ device can achieve up to 1.4x the short-circuit failure current compared to leading competitors, resulting in a more reliable, lower-cost, and more efficient BMS solution.

The Market Shift to High-Voltage Battery Systems

The market for high-power battery-powered systems, especially within e-mobility (e.g., mini-EVs, scooters, drones) and professional advanced power tools, is rapidly expanding. This growth is being met with a fundamental shift to high-voltage platforms (72V, 80V, and above).

This architectural shift is driven by the physics of power delivery. Since power (P) is the product of voltage (V) and current (I), increasing the battery voltage allows the system to deliver the same or higher power output while operating at a proportional decrease in current (I = P/V).

This migration to higher voltage brings several critical advantages for system designers:

1. Reduced I2R Conduction Losses
2. Lower Thermal Stress
3. Lighter and More Compact Systems

In these high-energy applications, robust protection circuitry within the Battery Management System (BMS) is no longer a luxury - it is a mandatory safety requirement.

The Critical Role of the Discharge MOSFET in BMS Protection

A robust Battery Management System is essential for the safety and longevity of a lithium-ion battery pack, providing protection against overvoltage, undervoltage, overcurrent, and thermal runaway. At the heart of this protection system are the Charge and Discharge MOSFETs, which function as high-side or low-side switches to safely connect and disconnect the pack from its load and charger. See Figure 1 below.

While both are essential, the Discharge MOSFET plays the singular and critical role of protecting the battery pack from external short circuits (Pack+ shorted to Pack-). In a short-circuit event, the BMS must rapidly detect the fault and command the switch to turn off, thereby isolating the battery.

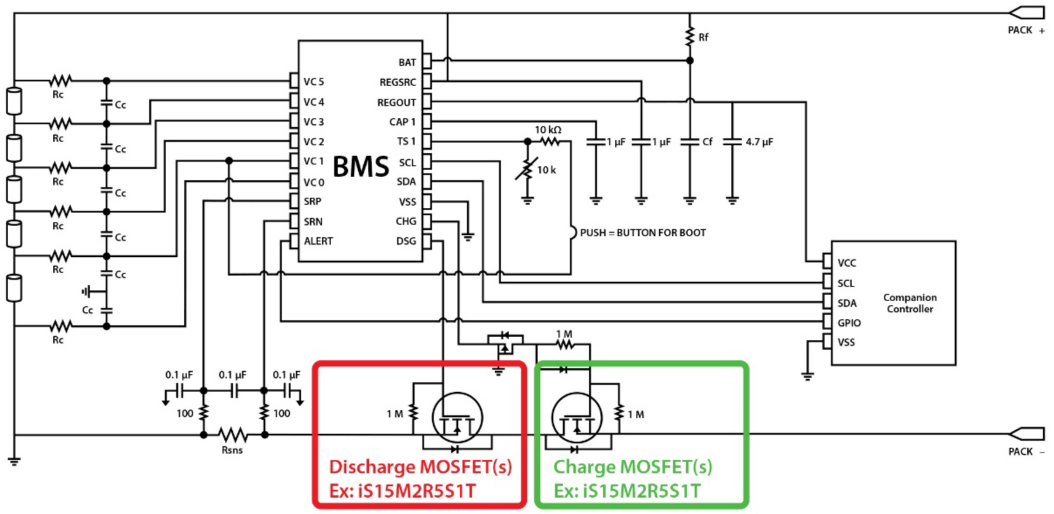

Figure 1: Example Battery Management System with Discharge and Charge MOSFETs

The Short-Circuit Challenge

The protection challenge is formidable because of two factors: current magnitude and time.

1. Current Magnitude: Short-circuit currents can rapidly escalate into thousands of amps.
2. Time: The MOSFET must turn off in the face of this massive current in tens of microseconds.

Furthermore, due to the body diode orientation of the Charge MOSFET(s), it cannot block a short circuit from Pack+ to Pack-. Therefore, the entire burden of this safety function falls exclusively on the Discharge MOSFET(s). If the Discharge MOSFET cannot withstand the surge and successfully break the circuit, the device will fail, leading to an uncontrolled current flow that can result in thermal runaway and catastrophic pack failure. This makes the Short-Circuit Withstand Capability (SCWC) the most critical reliability metric for the Discharge MOSFET.

Testing Methodology: Characterizing Short-Circuit Withstand Current

To accurately assess a MOSFET's true safety margin, iDEAL Semiconductor developed a specialized benchtop test circuit designed to characterize a device's turn-off performance under extreme, high-current, short-circuit conditions. See Figure 2 below.

The test subjects the Device Under Test (DUT) to a simulated short circuit. This is accomplished using a Half Sinewave Drain Current Source to generate the massive current pulse, while the gate is simultaneously driven by a Square Wave Gate Voltage source to initiate the turn-off sequence. The tests are performed at increasingly higher current levels until the device fails. Time is allotted between pulses to ensure the junction temperature returns to 25°C, maintaining test consistency.

A higher failure current directly translates to a more robust and reliable system, and crucially, it allows the battery pack manufacturer to potentially use fewer MOSFETs in parallel, leading to significant system-cost savings.

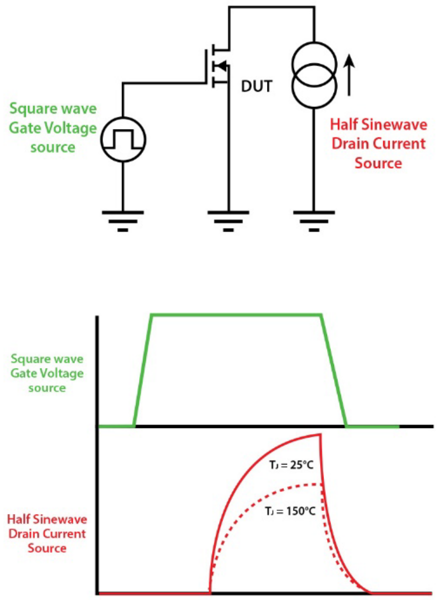

Figure 2: MOSFET testing for Short Circuit Withstand Current Capability. Example waveform (left) showing gate voltage and drain current. Circuit and illustrative waveforms (right).

SuperQ Performance: Combining Low $R_{DS(on)}$ with Superior Robustness

iDEAL Semiconductor's SuperQ™ MOSFETs were specifically designed to break the traditional trade-off between low $R_{DS(on)}$ and high SCWC. The results of the short-circuit testing demonstrate the market-leading advantage of this technology.

Quantitative Comparison (150V, 2.5mΩ TOLL Devices)

A direct, head-to-head comparison between the iDEAL iS15M2R5S1T and a leading competitor, the Infineon IPT025N15NM6, both 150V, 2.5mΩ devices in the TOLL package, yielded the following results:

Part Number 150V, 2.5mΩ TOLL	**Manufacturer**	**Short Circuit Peak Current (A)**	**SCWC Advantage**
iS15M2R5S1T	iDEAL Semi	792	1.4x Higher
IPT025N15NM6	Infineon	584	Baseline

Figure 3: Short circuit withstand current for 150V, 2.5mohm MOSFETs

The iDEAL SuperQ MOSFET demonstrated a short-circuit failure current of 792A, which is 1.4 times higher than the competitor's failure current of 584A. This level of performance puts the SuperQ device at the top of the competitive landscape for peak short-circuit current capability.

Furthermore, analysis of the key performance metrics SCWC x $R_{DS(on)}$ confirms that the SuperQ device occupies the ideal performance quadrant. Unlike other devices that must sacrifice one for the other, SuperQ delivers both ultra-low resistance (2.5 mΩ max) and the highest peak short-circuit performance, which is the definition of increased system performance and efficiency.

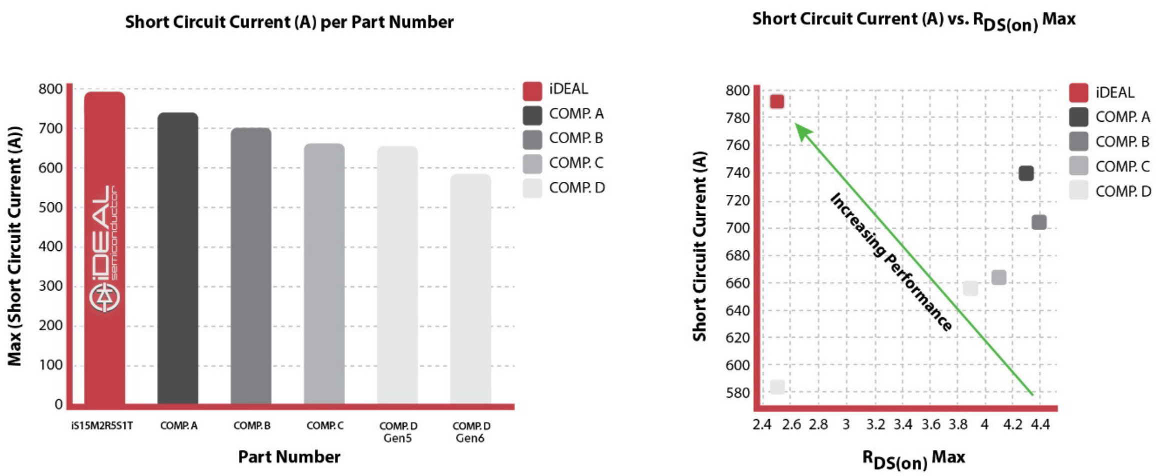

Figure 4: Peak short circuit withstand current for leading competitors (left). SCWC vs $R_{DS(on)}$ for leading competitors in TOLL package (right).

The SuperQ Technology Advantage

The superior performance of the SuperQ platform is rooted in its proprietary silicon technology. iDEAL's design approach directly addresses the limitations of previous-generation and competing technologies:

1. **Wide Mesa and Wide Metal Contact:** This unique design feature (Figure 5) enables a higher current density and current rating within the silicon. This inherent structural robustness directly translates to the industry-leading short-circuit current withstand capability and strong avalanche capability.

2. **Industry's Lowest On-Resistance:** SuperQ utilizes a fully charge-balanced structure and an asymmetrical trench design. Importantly, the power MOSFET design features a 2µm wide mesa compared to the 1.5µm (last generation) or 1µm (new generation) found in competitive MOSFETs. These narrower mesas in competing devices lead to a reduction in the conduction area, resulting in lower silicon efficiency and reduced short-circuit current ratings. The wider conduction region in the SuperQ design maximizes the power density and minimizes $R_{DS(on)}$, thus breaking the performance trade-off.

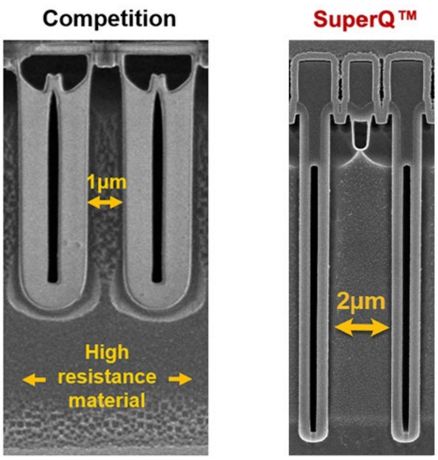

Figure 5: MOSFET unit cells showing gen-to-gen mesa width reduction (left and center) for competition vs. wide mesa design for SuperQ (right)

Value Proposition: System Cost and Reliability Savings

The superior performance of the SuperQ MOSFET translates directly into a tangible system-level value proposition for battery pack designers.

Consider a typical 80V, 10Ah battery pack:

Parameter	**Units**	**iDEAL iS15M2R5S1T**	**AOS AOTL66518**	**Infineon IPT025N15NM6**
Max $R_{DS(on)}$	mΩ	2.5	4.3	2.5
SC Current per MOSFET	A	792	740	584
# of MOSFETs in Parallel	Count	2-3	3	4-5
Solution Cost	$	$ - $$	$$	$$$

Figure 6: Comparison of leading MOSFETs for $R_{DS(on)}$ and SCWC

By leveraging SuperQ's higher SCWC, system designers can achieve:

- Up to 50% Fewer MOSFETs Required: Requiring only 2 to 3 SuperQ devices versus up to 5 of the competing devices to meet the same short-circuit current requirement.
- Up to 50% Lower Solution Cost: Reducing the component count, complexity, and board space translates directly to a lower total bill of materials (BOM).
- Up to 42% Lower $R_{DS(on)}$: Minimizing conduction losses, which extends battery life and reduces system thermal requirements.

The iDEAL SuperQ platform (including devices like the 150V iS15M2R5S1T, 200V iS20M5R5S1T, and 300V iS30M8R0S1T) offers a comprehensive portfolio spanning up to 300V to address various high-voltage battery systems from 72V up to over 144V.

Conclusion

The safety and efficiency of next-generation, high-voltage battery packs are gated by the performance of the discharge MOSFET. iDEAL Semiconductor's SuperQ MOSFET technology successfully overcomes the long-standing compromise between efficiency and safety, providing both superior short-circuit withstand capability and industry-leading low $R_{DS(on)}$. By selecting SuperQ MOSFETs, designers can reduce component count, minimize system cost, and significantly enhance the reliability of their battery management systems, ensuring a robust and safe power delivery solution in the accelerating landscape of >72V e-mobility and power tool applications.