Si86S61x/S62x/SOx : Single and Dual Channel Digital Isolators

Robust, High Speed Low Power Digital Isolators

Skyworks' new family of robust, low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. All device versions have CMOS thresholds and Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 150 Mbps are supported, and all devices achieve typical propagation delays of 10 ns. This family includes inverted output product options. Ordering options also include a choice of isolation ratings (3.75 and 6 kV_{RMS}) and product options for fail-safe operating mode to control the default output state during power loss. All products are safety certified by UL, CSA, VDE, and CQC. Products in wide-body packages support voltages of 6.0 kV_{RMS} with 1 minute withstand capability per UL 1577. These products are certified to the latest IEC 60747-17 reinforced specification and can be safely used in high power applications like inverters and motor drives.

Industrial Application

- Industrial automation systems
- Medical electronics
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for 1 minute
- CSA certification conformity
  - IEC 62368-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-17 (reinforced)
  - EN 62368-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1-2011

KEY FEATURES

- High-speed operation: DC to 150 Mbps
- No start-up initialization required
- Wide Supply Voltage: 2.25 – 5.5 V
- Up to 6000 V_{RMS} isolation
- Reinforced IEC 60747-17 rating
- High electromagnetic immunity
- Schmitt trigger + CMOS threshold inputs
- Selectable fail-safe mode: Default high or low output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 3.5 ns pulse width distortion
- Transient Immunity of 100 kV/µs (min)
- AEC-Q100 qualification
- Wide temperature range:
  - –40 to 125 °C
- RoHS-compliant packages
  - NB SOIC-8
  - SSO-8

Table of Contents

1. Ordering Guide

Table 1.1. Ordering Guide [1, 2, 3]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Non-Inverting Output						
Si86S610BC-IS	1	0	0	Low	3.75	NB SOIC-8
Si86S610BE-IS4	1	0	0	Low	6	SSO-8
Si86S610EC-IS	1	0	0	High	3.75	NB SOIC-8
Si86S610EE-IS4	1	0	0	High	6	SSO-8
Si86S620BC-IS	2	0	0	Low	3.75	NB SOIC-8
Si86S620BE-IS4	2	0	0	Low	6	SSO-8
Si86S620EC-IS	2	0	0	High	3.75	NB SOIC-8
Si86S620EE-IS4	2	0	0	High	6	SSO-8
Si86S621BC-IS	1	1	0	Low	3.75	NB SOIC-8
Si86S621BE-IS4	1	1	0	Low	6	SSO-8
Si86S621EC-IS	1	1	0	High	3.75	NB SOIC-8
Si86S621EE-IS4	1	1	0	High	6	SSO-8
Si86S622BC-IS	1	1	0	Low	3.75	NB SOIC-8
Si86S622BE-IS4	1	1	0	Low	6	SSO-8
Si86S622EC-IS	1	1	0	High	3.75	NB SOIC-8
Si86S622EE-IS4	1	1	0	High	6	SSO-8
Si86S620FC-IS	2	0	30	Low	3.75	NB SOIC-8
Si86S620FE-IS4	2	0	30	Low	6	SSO-8
Si86S620HC-IS	2	0	30	High	3.75	NB SOIC-8
Si86S620HE-IS4	2	0	30	High	6	SSO-8
Si86S621FC-IS	1	1	30	Low	3.75	NB SOIC-8
Si86S621FE-IS4	1	1	30	Low	6	SSO-8
Si86S621HC-IS	1	1	30	High	3.75	NB SOIC-8
Si86S621HE-IS4	1	1	30	High	6	SSO-8
Inverting Output						
Si86SO20BC-IS	2	0	0	Low	3.75	NB SOIC-8
Si86SO20BE-IS4	2	0	0	Low	6	SSO-8
Si86SO20EC-IS	2	0	0	High	3.75	NB SOIC-8
Si86SO20EE-IS4	2	0	0	High	6	SSO-8
Si86SO21BC-IS	1	1	0	Low	3.75	NB SOIC-8
Si86SO21BE-IS4	1	1	0	Low	6	SSO-8

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Si86SO21EC-IS	1	1	0	High	3.75	NB SOIC-8
Si86SO21EE-IS4	1	1	0	High	6	SSO-8

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.

2. Functional Description

2.1 Theory of Operation

The operation of an Si86S61x/2x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86S61x/2x channel is shown in the figure below.

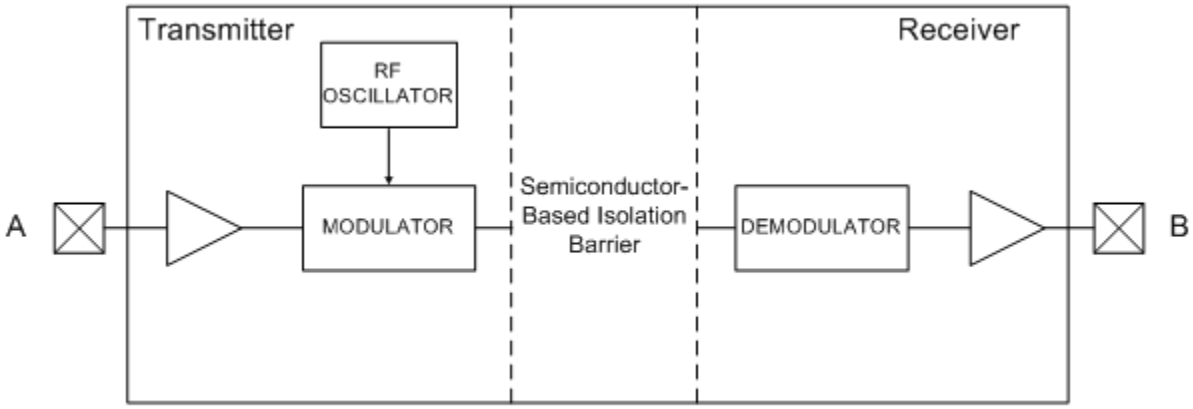

Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields. See the following figure for more details.

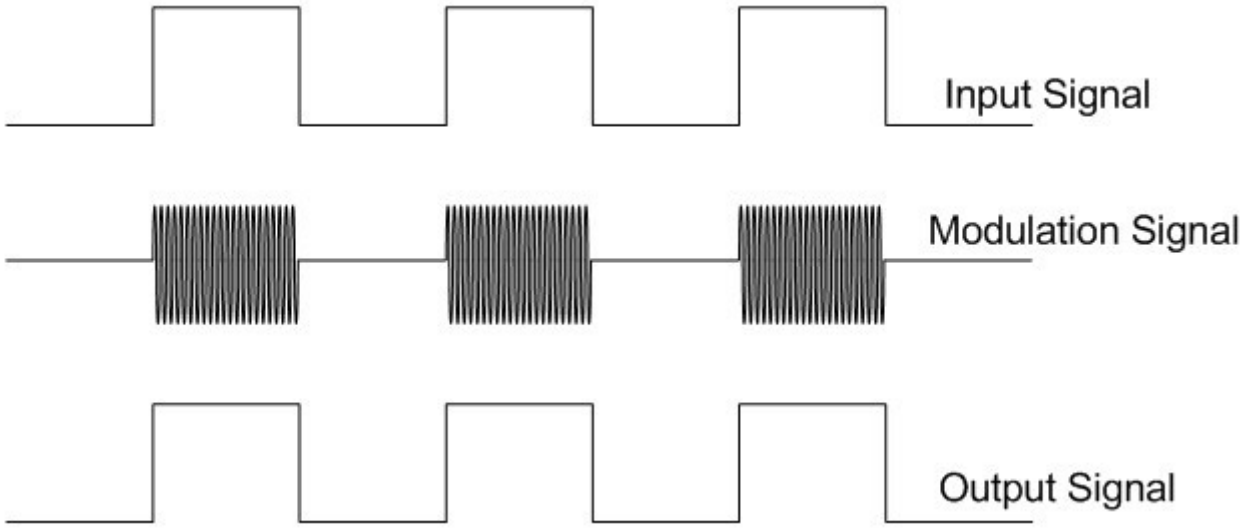

Figure 2.2. Modulation Scheme

3. Device Operation and System Overview

Device behavior during start-up, normal operation, and shutdown is shown in Figure 3.1 Device Behavior during Startup on page 7, where UVLO+ and UVLO– are the respective positive-going and negative-going thresholds. Refer to the following table to determine outputs when power supply (VDD) is not present.

Table 3.1. Si86S6x/Ox Logic Operation

V_IInput[1, 2, 3]	VDDI State[1, 4, 5]	VDDO State[1, 4, 5]	V_OOutput[1, 2, 3]	Comments
H	P	P	H/L	Normal operation
L	P	P	L/H	
X	UP	P	L[6]	Default low options
			H[6]	Default high options
X	P	UP	UD[7]	Upon transition of VDDO from unpowered to powered, V_O returns to correct state. Refer to 7 below.

Note:

1. VI and VO are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the respective input and output sides.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
4. “Powered” state (P) is defined as 2.25 V < VDD < 5.5 V.
5. “Unpowered” state (UP) is defined as VDD <2.25 V.
6. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L. For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.
7. UD =Undetermined. Refer to "Timing diagram for startup" below notes section, the start-up time from unpowered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in diagram below) but stays above RSTB level, the start-up time is 1 µs.

3.1 Device Startup, UVLO, and Reset Functionality

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs. The start-up time of the device is estimated to be 0.3 ms due to the device initialization time. During this time, the outputs will have a 100 kΩ pulldown resistor that will pull the outputs low. After stabilization, the outputs will transition to the default output state indicated by the particular product option.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, referring to the figure below, Side A unconditionally enters UVLO when VDD1 falls below VDD1(UVLO–) and exits UVLO when VDD1 rises above VDD1(UVLO+). Side B operates the same as Side A with respect to its VDD2 supply.

Along with UVLO, each side has its own self biased circuitry that can detect supply going low enough and issue a complete reset of the part. This is done to avoid loss of device configuration for the particular product option. Referring to the figure below, Side A goes into reset as soon as VDD1 goes below RSTB- (~1.7 V) and comes out of reset when VDD1 goes above RSTB+. When the supply voltage is above RSTB+ the device configuration is re-loaded. Side B operates the same as Side A with respect to its VDD2 supply.

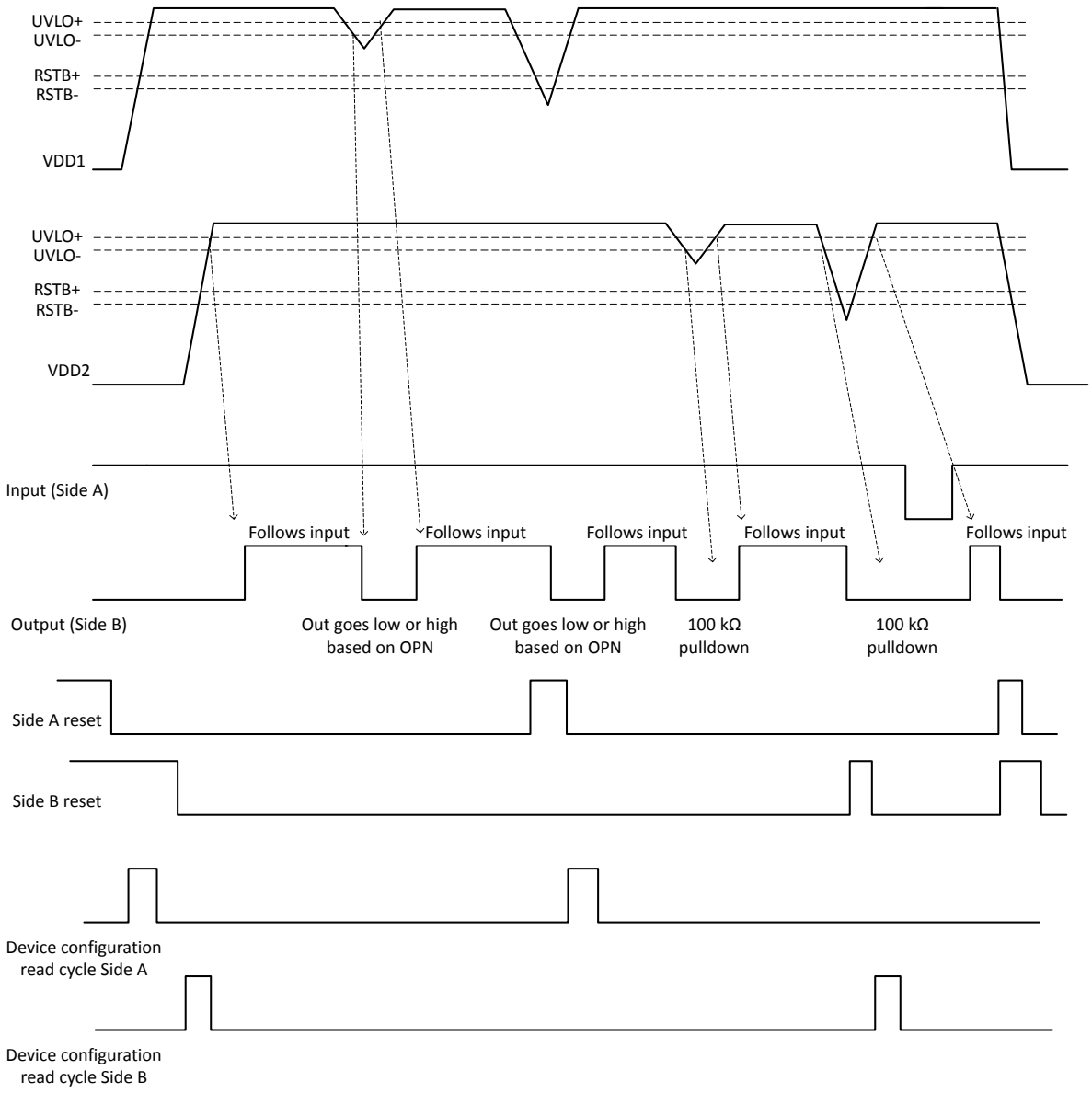

Figure 3.1. Device Behavior during Startup

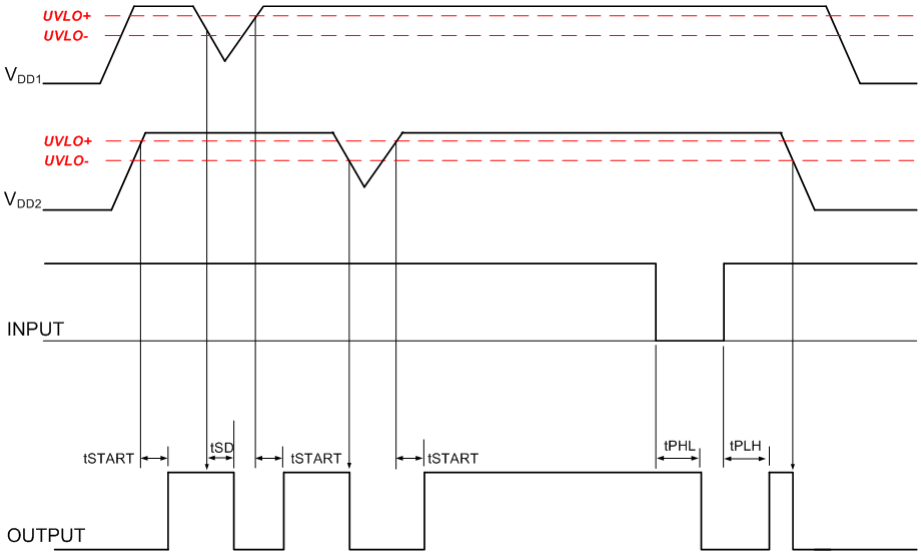

Figure 3.2. Device Behavior during Normal Operation

3.2 Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). and detail the working voltage and creepage/clearance capabilities of the Si86S61x/2x. These tables also detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 62368-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.2.1 Supply Bypass

The Si86S61x/2x family requires a 0.1 µF bypass capacitor between VDD1 and GND1 and VDD2 and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.2.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.3 Fail-Safe Operating Mode

Si86S61x/2x devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See and Section 1. Ordering Guide for more information.

3.4 Device Features and System Overview

3.4.1 Input Noise Filters with Deglitch Times of 30 ns

This product family is orderable with input deglitch filters which have delay times of 30 ns. These filters remove undesirable noise pulses (glitches) from the input signal so that the isolator only produces an output for a valid input. Any input pulse which lasts less than the deglitch time will not be passed by the filter. Any other input pulse will be passed by the filter and delayed by the filter delay time. Please see figures below.

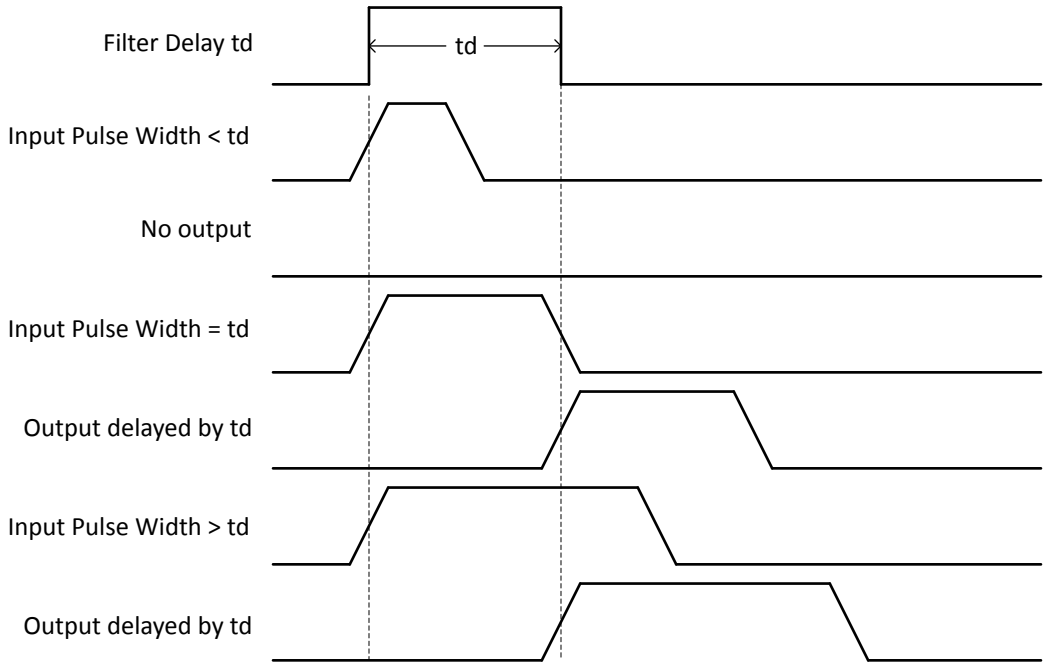

Figure 3.3. Input Noise Filter Functionality

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction Operating Temperature	T_J	—	—	150	°C
Ambient Operating Temperature[1]	T_A	–40	25	125	°C
Supply Voltage	VDD1, VDD2	2.25	—	5.5	V

Note:

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 4.2. Electrical Characteristics

T_A = –40 to 125°C; VDD1, VDD2 as specified in Recommended Operating Conditions Table above.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDD_{UV+}	VDD1, VDD2 rising	2.14	2.18	2.25	V
VDD Undervoltage Threshold	$VDD_{UV–}$	VDD1, VDD2 falling	2.01	2.05	2.10	V
VDD Undervoltage Hysteresis	VDD_{HYS}		105	131	150	mV
Input Hysteresis	V_{HYS}		0.15*VDDx	—	—	V
High Level Input Voltage	V_{IH}		0.7*VDDx	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3*VDDx	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	VDD1, VDD2–0.4	—	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	—	0.4	V
Output Impedance	Z_O		—	50	—	Ω

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Table 4.3. Electrical Characteristics

VDD1 = 5.0 V +/- 10%, VDD2 = 5.0 V +/-10%, T_A = -40 to 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.46	0.54	
IDD2		VI = 0(Bx), 1(Ex)	—	0.97	1.20	mA
IDD1		VI = 1(Bx), 0(Ex)		1.05	1.22	
IDD2		VI = 1(Bx), 0(Ex)		1.00	1.22	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	0.75	0.88	mA
IDD2				1.01	1.24	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	0.78	0.88	mA
IDD2				1.41	1.78	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	0.78	0.88	mA
IDD2				4.76	6.74	
Si86S620/O20Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.52	0.62	
IDD2		VI = 0(Bx), 1(Ex)	—	1.54	1.93	mA
IDD1		VI = 1(Bx), 0(Ex)		1.69	1.97	
IDD2		VI = 1(Bx), 0(Ex)		1.60	1.97	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	1.16	1.28	mA
IDD2				1.61	2.00	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.16	1.28	mA
IDD2				2.46	2.97	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.16	1.28	mA
IDD2				9.19	11.99	
Si86S621/O21Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.05	1.29	
IDD2		VI = 0(Bx), 1(Ex)	—	1.05	1.29	mA
IDD1		VI = 1(Bx), 0(Ex)		1.68	1.98	
IDD2		VI = 1(Bx), 0(Ex)		1.67	1.97	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	1.39	1.67	mA
IDD2				1.39	1.67	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.80	2.16	mA
IDD2				1.80	2.16	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	5.18	6.67	mA
IDD2				5.18	6.67	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S622Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.04	1.28	
IDD2		VI = 0(Bx), 1(Ex)	—	1.04	1.28	mA
IDD1		VI = 1(Bx), 0(Ex)		1.68	2.01	
IDD2		VI = 1(Bx), 0(Ex)		1.66	1.98	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	1.39	1.69	mA
IDD2				1.37	1.66	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.80	2.16	mA
IDD2				1.80	2.16	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	5.18	6.67	mA
IDD2				5.18	6.67	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps
Data Rate Si86Sx (with 30 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)			6.7	—	—	ns
Pulse Width Si86S6X (with 30 ns deglitch)			100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	7	9	14	ns
Pulse Width Distortion (no deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	2	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	0.8	2	ns
Propagation Delay (30 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	32	36	42	ns
Pulse Width Distortion (30 ns deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	2	ns
Propagation Delay Skew (30 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (30 ns deglitch)	t_{PSK}		—	1.5	4	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19.	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19.	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 7	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity Si86Sx (no deglitch) Si86Sx (with 30 ns deglitch)	CMTI	See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 20 VI = VDD or 0 V VCM = ±1500 V	100 150	— —	— —	kV/µs
Input power loss to valid default output	t_{SD}	See	—	8.0	12	ns
Start-up Time	t_{SU}		—	—	300	µs
Input Leakage Current	I_L		—	—	±8	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

Table 4.4. Electrical Characteristics

IDD1 = 3.3 V ±10%, IDD2 = 3.3 V ±10%, T_A = –40 to 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.43	0.50	
IDD2		VI = 0(Bx), 1(Ex)	—	0.94	1.17	mA
IDD1		VI = 1(Bx), 0(Ex)		1.02	1.19	
IDD2		VI = 1(Bx), 0(Ex)		0.97	1.19	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	0.72	0.84	mA
IDD2				0.75	0.88	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	0.75	0.84	mA
IDD2				1.25	1.52	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	0.75	0.84	mA
IDD2				3.45	4.78	
Si86S620/O20Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.49	0.58	
IDD2		VI = 0(Bx), 1(Ex)	—	1.51	1.89	mA
IDD1		VI = 1(Bx), 0(Ex)		1.66	1.92	
IDD2		VI = 1(Bx), 0(Ex)		1.57	1.93	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	1.07	1.24	mA
IDD2				1.11	1.28	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.17	1.24	mA
IDD2				2.16	2.61	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.17	1.24	mA
IDD2				6.59	9.13	
Si86S621/O21Bx, Ex					1.23	
IDD1		VI = 0(Bx), 1(Ex)		1.00	1.23	
IDD2		VI = 0(Bx), 1(Ex)	—	1.00	1.93	mA
IDD1		VI = 1(Bx), 0(Ex)		1.63	1.93	
IDD2		VI = 1(Bx), 0(Ex)		1.63		
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	1.34	1.61	mA
IDD2				1.34	1.61	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.63	1.95	mA
IDD2				1.63	1.95	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	3.86	5.20	mA
IDD2				3.86	5.20	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S622Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.03	1.26	
IDD2		VI = 0(Bx), 1(Ex)	—	1.03	1.26	mA
IDD1		VI = 1(Bx), 0(Ex)		1.65	1.97	
IDD2		VI = 1(Bx), 0(Ex)		1.63	1.97	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	1.35	1.62	mA
IDD2				1.35	1.62	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.63	1.95	mA
IDD2				1.63	1.95	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	3.86	5.20	mA
IDD2				3.86	5.20	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps
Data Rate Si86Sx (with 30 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)			6.7	—	—	ns
Pulse Width Si86S6X (with 30 ns deglitch)			100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	6	9	15	ns
Pulse Width Distortion (no deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	3	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	0.9	3	ns
Propagation Delay (30 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	31	36	42	ns
Pulse Width Distortion (30 ns deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	3	ns
Propagation Delay Skew (30 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (30 ns deglitch)	t_{PSK}		—	1.5	3.5	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19.	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19.	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 7	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity		See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 20				
Si86Sx (no deglitch)	CMTI	VI = VDD or 0 V	100	—	—	kV/µs
Si86Sx (with 30 ns deglitch)		VCM = ±1500 V	150	—	—	
Input power loss to valid default output	t_{SD}	See	—	8.0	12	ns
Start-up Time	t_{SU}		—	—	300	µs
Input Leakage Current	I_L		—	—	±6	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

Table 4.5. Electrical Characteristics

IDD1 = 2.5 V ±10%, IDD2 = 2.5 V ±10%, T_A = –40 to 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.41	0.49	
IDD2		VI = 0(Bx), 1(Ex)	—	0.92	1.15	mA
IDD1		VI = 1(Bx), 0(Ex)		1.00	1.17	
IDD2		VI = 1(Bx), 0(Ex)		0.95	1.17	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	0.71	0.83	mA
IDD2				0.95	1.17	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	0.72	0.83	mA
IDD2				1.14	1.42	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	0.72	0.83	mA
IDD2				2.82	3.89	
Si86S620/O20Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		0.47	0.57	
IDD2		VI = 0(Bx), 1(Ex)	—	1.49	1.88	mA
IDD1		VI = 1(Bx), 0(Ex)		1.64	1.90	
IDD2		VI = 1(Bx), 0(Ex)		1.55	1.91	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	1.06	1.22	mA
IDD2				1.54	1.92	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.09	1.22	mA
IDD2				1.99	2.42	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.09	1.22	mA
IDD2				5.37	7.37	
Si86S621/O21Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.00	1.23	
IDD2		VI = 0(Bx), 1(Ex)	—	1.00	1.22	mA
IDD1		VI = 1(Bx), 0(Ex)		1.63	1.92	
IDD2		VI = 1(Bx), 0(Ex)		1.63	1.92	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_I = 15 pF on All Outputs)	—	1.32	1.59	mA
IDD2				1.32	1.59	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_I = 15 pF on All Outputs)	—	1.54	1.84	mA
IDD2				1.54	1.84	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_I = 15 pF on All Outputs)	—	3.23	4.31	mA
IDD2				3.23	4.31	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S622Bx, Ex						
IDD1		VI = 0(Bx), 1(Ex)		1.01	1.24	
IDD2		VI = 0(Bx), 1(Ex)	—	1.01	1.24	mA
IDD1		VI = 1(Bx), 0(Ex)		1.63	1.95	
IDD2		VI = 1(Bx), 0(Ex)		1.61	1.93	
IDD1		1 Mbps Supply Current (All Inputs = 500 kHz Square Wave, C_l = 15 pF on All Outputs)	—	1.33	1.60	mA
IDD2				1.31	1.59	
IDD1		10 Mbps Supply Current (All Inputs = 5 MHz Square Wave, C_l = 15 pF on All Outputs)	—	1.54	1.82	mA
IDD2				1.54	1.82	
IDD1		100 Mbps Supply Current (All Inputs = 50 MHz Square Wave, C_l = 15 pF on All Outputs)	—	3.23	4.07	mA
IDD2				3.23	4.07	
Timing Characteristics						
Data Rate Si86Sx (no deglitch)			—	—	150	Mbps
Data Rate Si86Sx (with 30 ns deglitch)			—	—	10	Mbps
Pulse Width Si86S6x (no deglitch)			6.7	—	—	ns
Pulse Width Si86S6X (with 30 ns deglitch)			100	—	—	ns
Propagation Delay (no deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	8	11	18	ns
Pulse Width Distortion (no deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	2	ns
Propagation Delay Skew (no deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (no deglitch)	t_{PSK}		—	1.1	3	ns
Propagation Delay (30 ns deglitch)	t_{PHL}, t_{PLH}	See Figure 4.1 Propagation Delay Timing on page 19.	33	39	45	ns
Pulse Width Distortion (30 ns deglitch) |tPLH – tPHL|	PWD	See Figure 4.1 Propagation Delay Timing on page 19.	—	—	2	ns
Propagation Delay Skew (30 ns deglitch)	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew (30 ns deglitch)	t_{PSK}		—	1.7	3	ns
Output Rise Time	t_r	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19	—	2.5	—	ns
Output Fall Time	t_f	CL = 15 pF See Figure 4.1 Propagation Delay Timing on page 19	—	2.5	—	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 2.3 Eye Diagram on page 7	—	350	—	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity		See Figure 4.2 Common-Mode Transient Immunity Test Circuit on page 20				
Si86Sx (no deglitch)	CMTI	VI = VDD or 0 V	100	—	—	kV/µs
Si86Sx (with 30 ns deglitch)		VCM = ±1500 V	150	—	—	
Input power loss to valid default output	t_{SD}	See	—	8.0	12	ns
Start-up Time	t_{SU}		—	—	300	µs
Input Leakage Current	I_L		—	—	±6	µA

Note:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.
2. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to the appearance of valid data at the output. The OTP initialization time is included in the 300 µs specification.

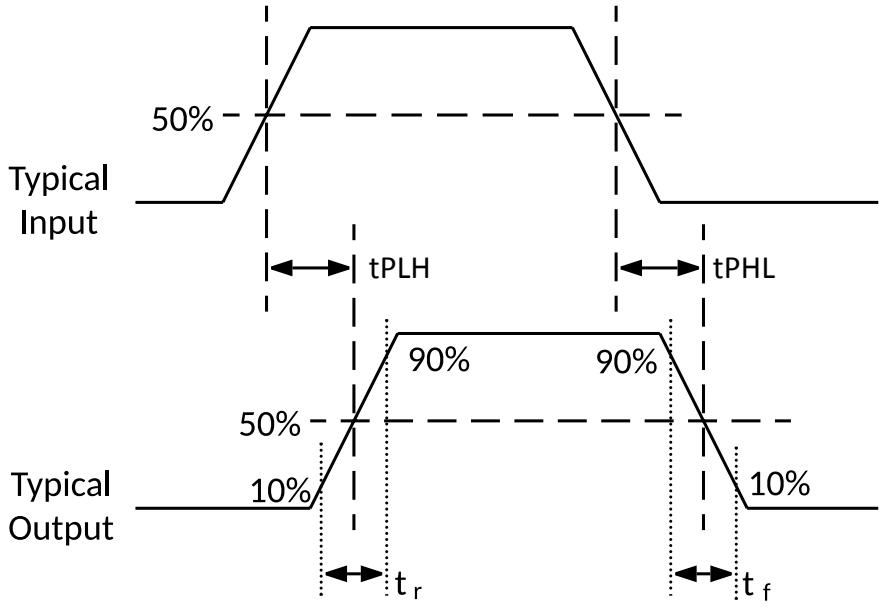

Figure 4.1. Propagation Delay Timing

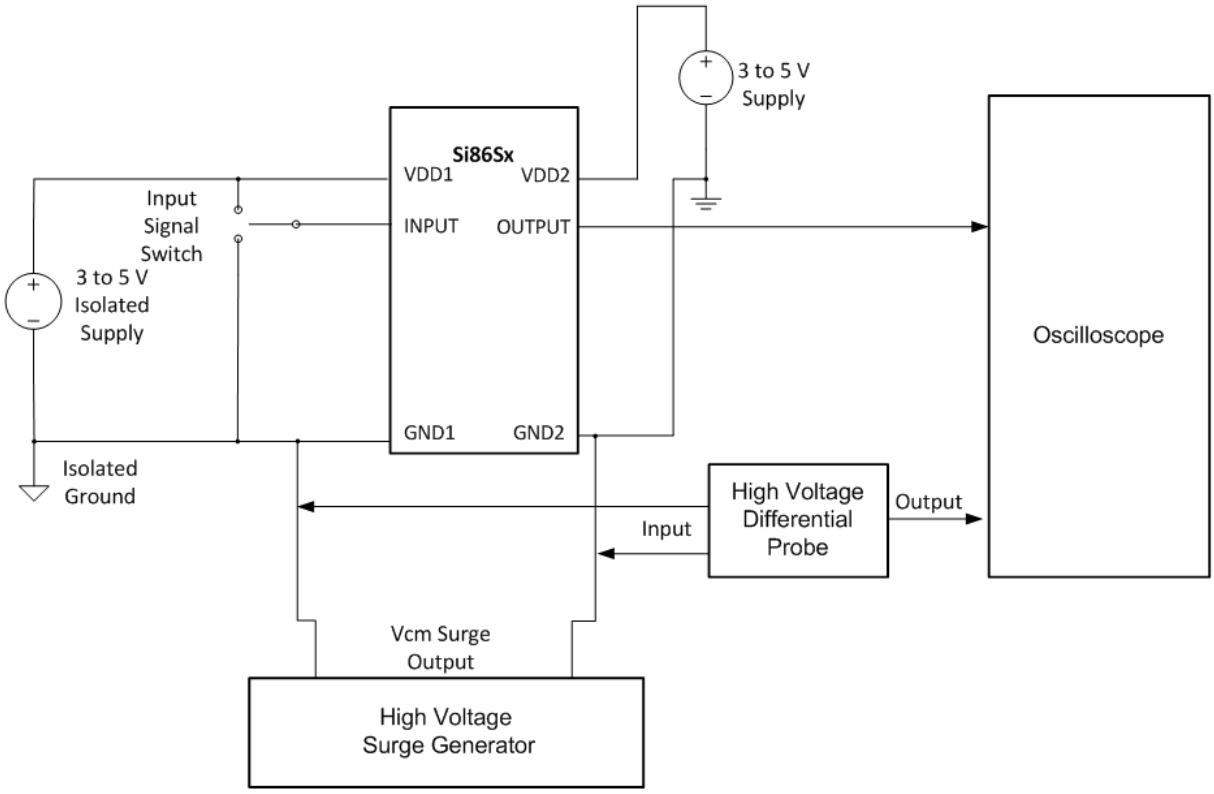

Figure 4.2. Common-Mode Transient Immunity Test Circuit

Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Electrical Characteristics tables for actual specification limits. All typical characteristics data is valid for nominal VDD and ambient temperature of 25°C.

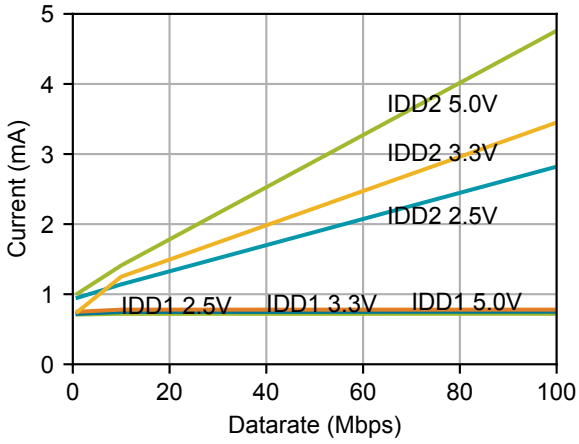

Figure 4.3. Si86S610 typical Supply Current vs. Data Rate

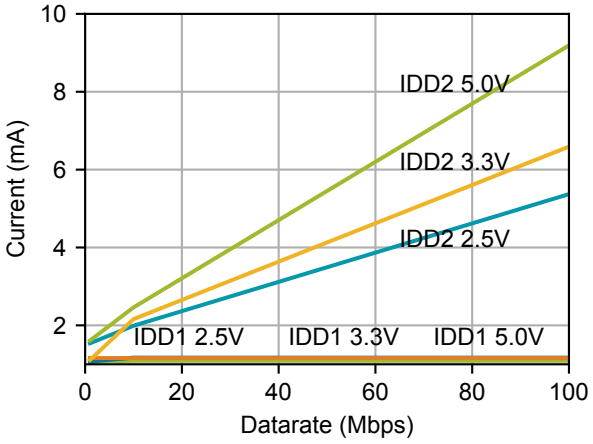

Figure 4.4. Si86S620/O20 Typical Supply Current vs. Data Rate

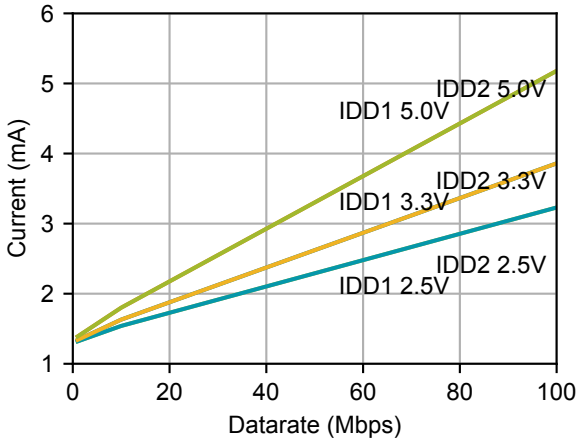

Figure 4.5. Si86S621/622/O21 Typical Supply Current vs. Data Rate

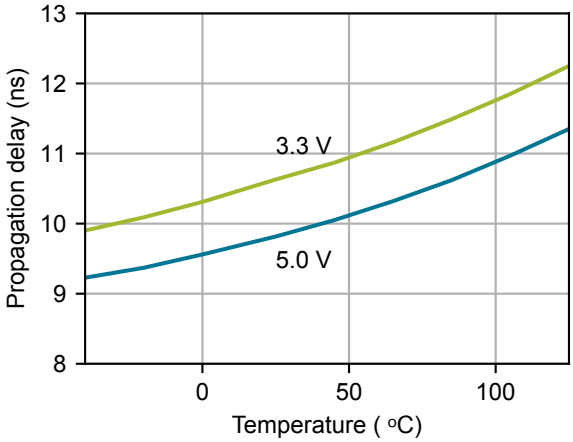

Figure 4.6. Si86Sx Propagation Delay vs. Temperature

Table 4.6. Regulatory Information[1]

CSA
The Si86S61x/2x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si86S61x/2x is certified under VDE. For more details, see File 5006301.
IEC60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si86S61x/2x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS}, V_{ISO} isolation voltage for basic protection.
CQC
The Si86S61x/2x is certified under GB4943.1-2011.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.
Note: 1. Regulatory Certifications apply to >2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 6.0 kV_{RMS} rated devices which are production tested to 7.2 kV_{RMS} for 1 sec. For more information, see Section1. Ordering Guide.

Table 4.7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			SSO-8	NB SOIC-8	
Nominal External Air Gap (Clearance)	CLR		8.0	4.9	mm
Nominal External Tracking (Creepage)	CRP		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.04	mm
Resistance (Input-Output) [1]	RIO	Test voltage = 500V	10^{12}	10^{12}	Ω
Capacitance (Input-Output) [1]	CIO	f = 1 MHz	1.0	1.0	pF
Input Capacitance [2]	CI		4.0	4.0	pF

Note:

1. To determine resistance and capacitance, the Si86Sx is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 4.8. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		SSO-8	NB SOIC-8
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV	I-III
	Rated Mains Voltages < 600 V_{RMS}	I-IV	I-II
	Rated Mains Voltages < 1000 V_{RMS}	I-III	I

Table 4.9. IEC 60747-17 Insulation Characteristics for Si86S61x/2x[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			SSO-8	NB SOIC-8	
Maximum Working Insulation Voltage	V_{IOWM}		1500	1500	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}	Method b1 (VIORM x 1.875 = VPR, 100% Production Test, tm = 1 sec, Partial Discharge < 5 pC)	2121	630	V_{peak}
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, tm = 1 sec, Partial Discharge < 5 pC)	3977	1181	V_{peak}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 60 s	8000	4000	V_{peak}
Maximum Surge Isolation Voltage	V_{IOSM}	Tested with 10400 V_{peak} and 1.2 µs/50 µs profile	8000	8000	V_{peak}
Maximum Impulse Voltage	V_{IOSM}	Tested with 8000 V_{peak} and 1.2 µs/50 µs profile	8000	8000	V_{peak}
Pollution Degree		DIN VDE 0110	2	2	
Insulation Resistance	R_S	TAMB = T_S, V_{IO} = 500 V	>10^9	>10^9	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si86S61x/2x provides a climate classification of 40/125/21.

Table 4.10. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max		Unit
			SSO-8	NB SOIC-8	
Safety Temperature	T_S		150	150	°C
Safety Input, Output, or Supply Current	I_S	Refer to θ_{JA} in Table 4.11 Thermal Characteristic on page 25,	253	221	mA
Safety Input, Output, or Total Power	P_S	V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	1392	1216	mW

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.7 (SSO-8) Thermal Derating Curve, Dependence of Safety Limiting Current on page 25.
2. The Si86Sx is tested with VDD1 = VDD2 = 5.5 V; T_J = 150ºC; CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 4.11. Thermal Characteristic

Parameter	Symbol	SSO-8	NB SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	90	103	°C/W
IC Junction-to-board Thermal Resistance	θ_{JB}	47	45	
IC Junction-to-Case Thermal Resistance	θ_{JC}	27	26	
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board	Ψ_{JB}	43	42	

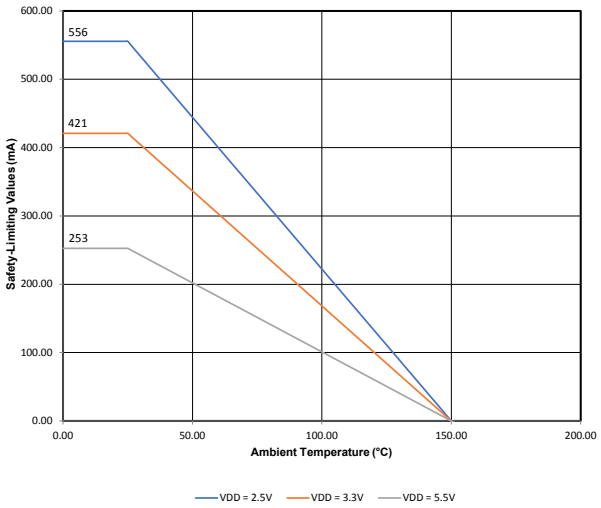

Figure 4.7. (SSO-8) Thermal Derating Curve, Dependence of Safety Limiting Current

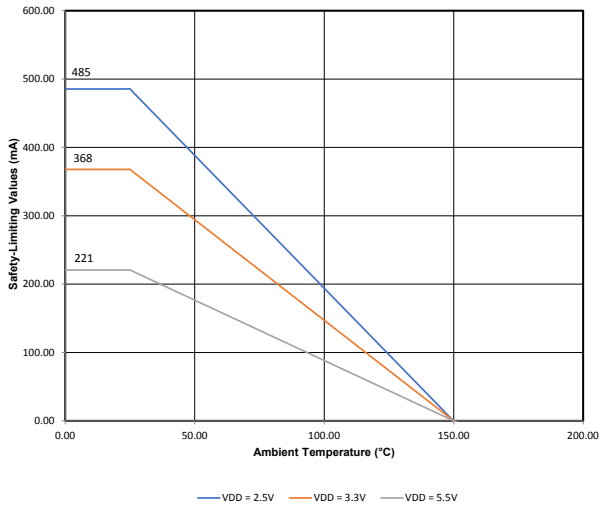

Figure 4.8. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Current

Table 4.12. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	TSTG	–65	150	°C
Operating Temperature	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	VDD1, VDD2	–0.5	7.0	V
Supply Voltage Ramp-up	VDD1, VDD2	-	1	V/µs
Input Voltage	VI	–0.5	VDD + 0.5	V
Output Voltage	VO	–0.5	VDD + 0.5	V
Output Current Drive Channel	IO	—	10	mA
ESD	HBM	—	6	kV
ESD	CDM	—	0.5	kV
ESD[2]	IEC 61000-4-2 contact discharge	—	8000	V
Lead Solder Temperature (10 s)		—	260	°C

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.
2. This test is performed across the isolation barrier with device in a two terminal configuration, with pins on each side shorted together. Tested per IEC 61000-4-2 contact discharge.

5. Pin Descriptions

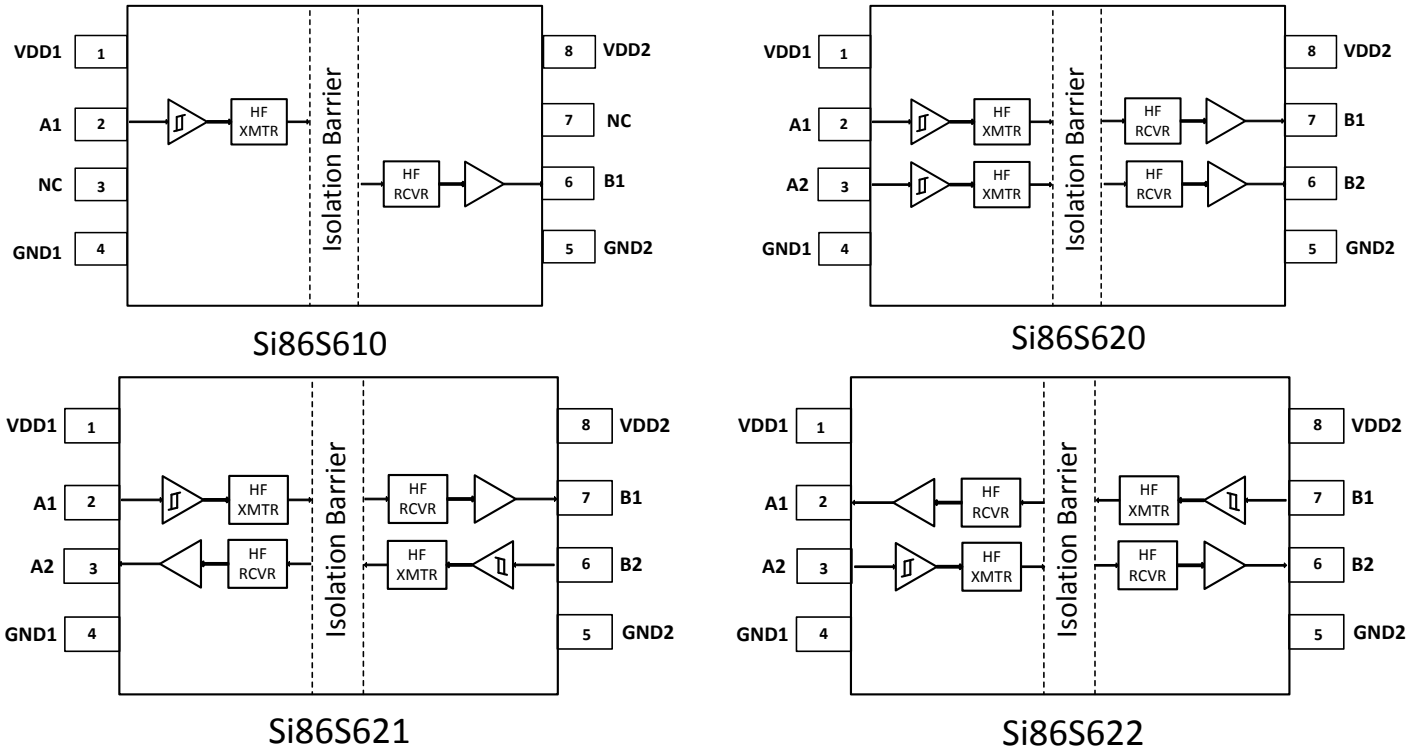

Figure 5.1. Si86S61x/2x Pinout

Table 5.1. Si86S61x/2x Pin Description

Name	Type	Description
VDD1	Supply	Side A power supply
GND1	Ground	Side A ground
A1 – A2	Digital I/O	Side A digital I/O
NC	No connect	Do not connect pin
GND2	Ground	Side B ground
B1 – B2	Digital I/O	Side B digital I/O
VDD2	Supply	Side B power supply

6. Package Outline

6.1 Package Outline (SSO-8)

The figure below illustrates the package details for the Si86S61x/2x in a SSO-8 package. The table lists the values for the dimensions shown in the illustration.

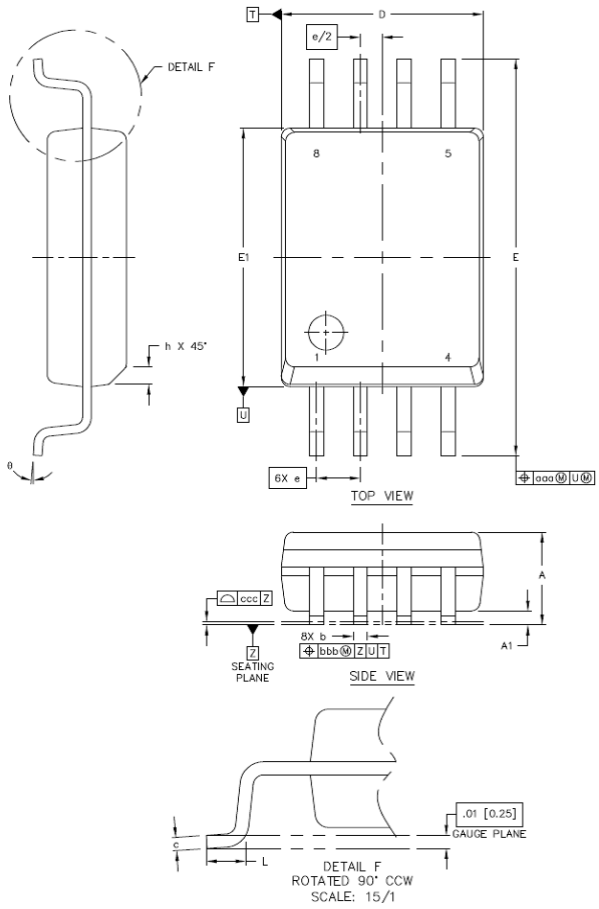

Figure 6.1. SSO-8 Package

Table 6.1. SSO-8 Package Diagram Dimensions

Dimension	MIN	MAX
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°

Dimension	MIN	MAX
aaa	--	0.25
bbb	--	0.25
ccc	--	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Package Outline (NB SOIC-8)

The figure below illustrates the package details for the Si86S61x/2x in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

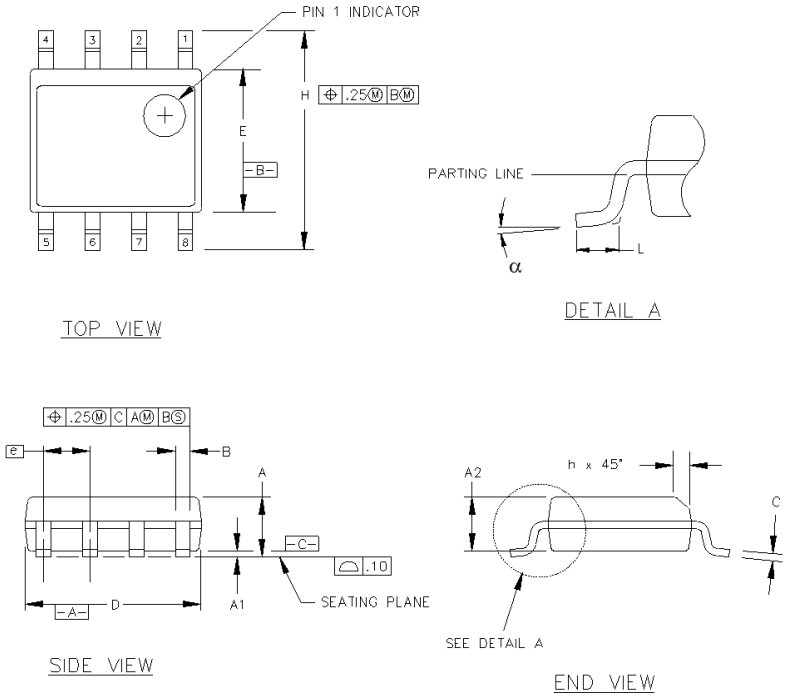

Figure 6.2. NB SOIC-8 Package

Table 6.2. NB SOIC-8 Package Diagram Dimensions

Dimension	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. This drawing conforms to JEDEC Outline MS-102.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

7. Land Pattern

7.1 Land Pattern (SSO-8)

The figure below illustrates the recommended land pattern details for the Si86S61x/2x in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

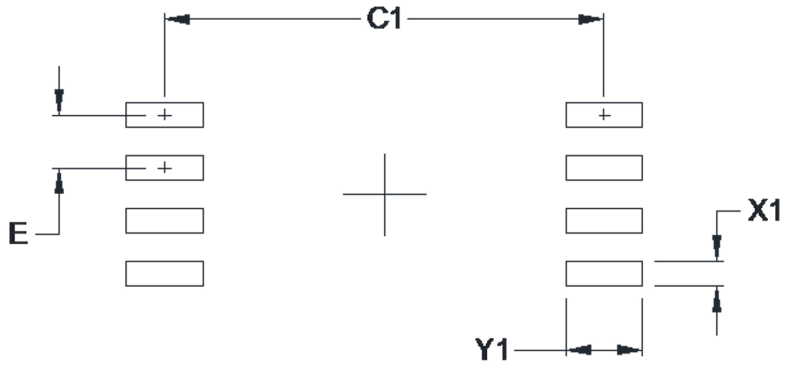

Figure 7.1. SSO-8 Land Pattern

Table 7.1. SSO-8 Land Pattern Dimensions

Symbol	mm
C1	10.60
E	1.27
X1	0.60
Y1	1.85

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 Land Pattern (NB SOIC-8)

The figure below illustrates the recommended land pattern details for the Si86S61x/2x in a 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

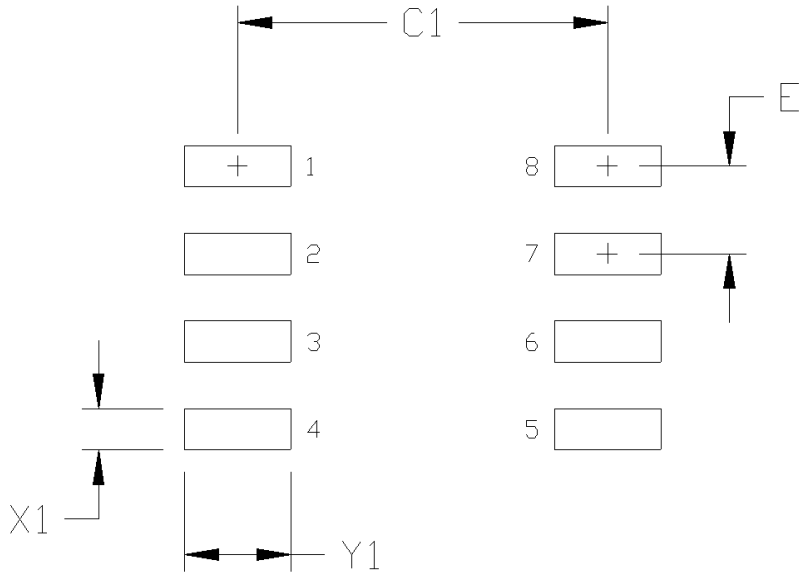

Figure 7.2. NB SOIC-8 Land Pattern

Table 7.2. NB SOIC-8 Land Pattern Dimensions

Symbol	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Marking

8.1 Top Marking: SSO-8

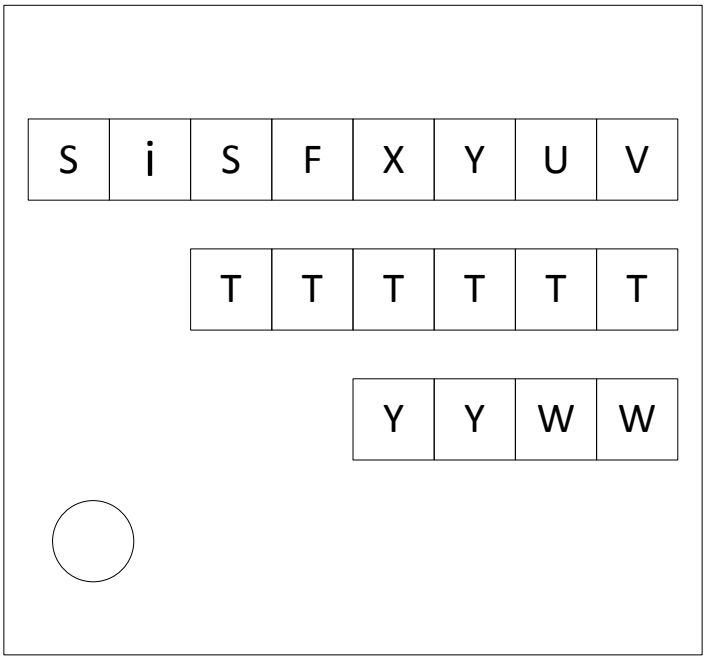

Figure 8.1. SSO-8 Top Marking

Table 8.1. SSO-8 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = product family 6 = Non-inverting outputs O = Inverting outputs X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 30 ns deglitch H = Output default high, 30 ns deglitch V = Isolation rating B = 2.5 kV_{RMS} C = 3.75 kV_{RMS} E = 6.0 kV_{RMS}
Line 2 Marking:	TTTTTT	Manufacturing code from assembly house purchase order form
Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house

8.2 Top Marking: NB SOIC-8

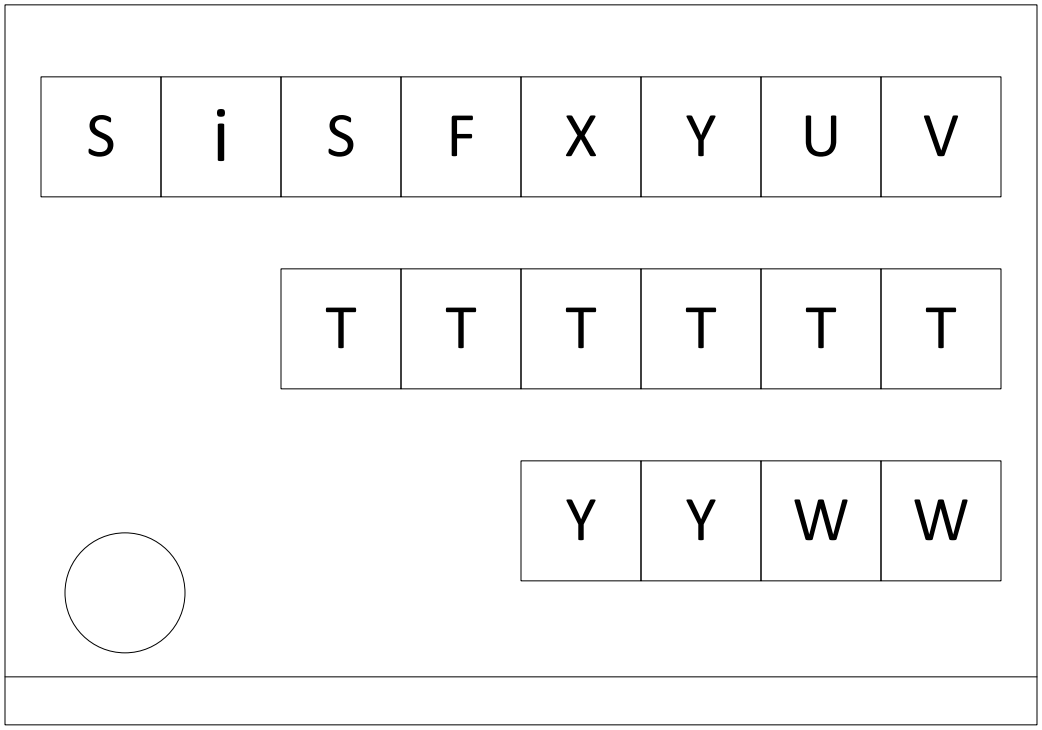

Figure 8.2. NB SOIC-8 Top Marking

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Line 1 marking:	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = product family 6 = Non-inverting outputs O = Inverting outputs X = Total # of channels Y = Total # of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 30 ns deglitch H = Output default high, 30 ns deglitch V = Isolation rating B = 2.5 kV_{RMS} C = 3.75 kV_{RMS} E = 6.0 kV_{RMS}
Line 2 Marking:	TTTTTT	Manufacturing code from assembly house purchase order form
Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house

9. Revision History

Revision 0.1

June 2020

- Initial release.

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