2 or 4 Outputs, Ultra-Low Additive Jitter, 1.2V to 1.8V LVCMOS Clock Buffers

SY75712/14

General Description

The SY75712 and SY75714 are the industry's leading low-power LVCMOS clock buffers with ultra-low additive jitter and extended temperature range. SY75712 and SY75714 are two- and four-output (respectively) 1.2V to 1.8V LVCMOS clock buffers with synchronous global output enable control input.

SY75712 and SY75714 are pin-to-pin compatible with TI LMK1C1102 and LMK1C1104, respectively. The TI parts are rated for 1.8V to 3.3V supply voltage, while the SY75712 and SY75714 devices are rated for 1.2V to 1.8V supply voltage, targeting lower-voltage system architectures.

Each SY75712/14 device is available in a 2 mm × 2 mm TDFN package. Both parts have an extended temperature range of –40°C to +105°C, allowing these parts to be used in harsh environments.

Features

- One-to-Two (SY75712) and One-to-Four (SY75714) 1.2V to 1.8V LVCMOS Clock Buffers
- Ultra-Low Additive Jitter 16.9 fs (typical) in 12 kHz to 20 MHz Band for 156.25MHz Input Clock
- Supports Frequencies from 0 Hz up to 250 MHz
- Output-to-Output Skew Less than 50 ps (maximum)
- Transparent for Spread Spectrum
- Glitch Free (Synchronous) Output Enable
- Extended Temperature Range: –40°C to +105°C
- 2 mm x 2 mm TDFN Package

Applications

- Clock Distribution
- Green Servers
- Battery Powered Applications

Functional Block Diagrams

Figure 1. SY75712 Functional Block Diagram

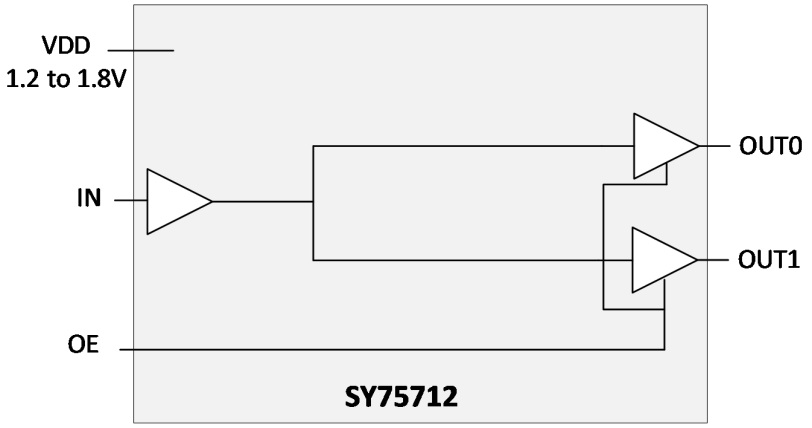


Figure 2. SY75714 Functional Block Diagram

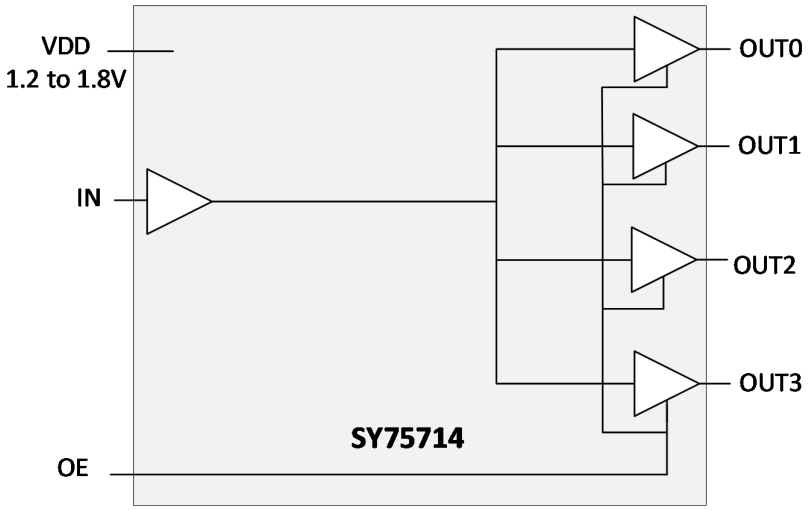
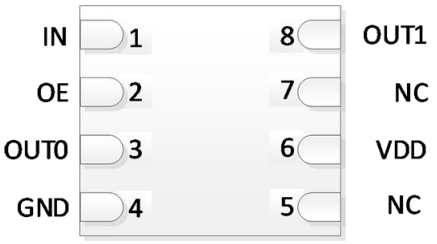


Table of Contents

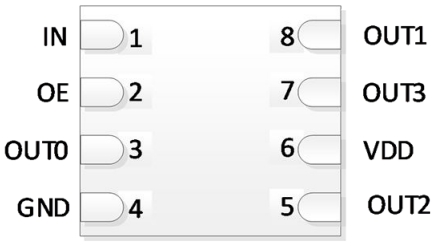
1. Pin Configuration

1.1. Package Types

SY75712
8-Lead TDFN
(Top View)



SY75714
8-Lead TDFN
(Top View)



1.2. Pin Descriptions

Table 1-1. SY75712 Pin Descriptions

Pin #	Pin Name	Type	Functional Description
Input Reference			
1	IN	I	**LVCMOS Input Reference.** Input frequency range >0 Hz to 250 MHz. Input has a fail-safe circuit to prevent oscillation if the input is not driven. >0 Hz because OE is synchronous and requires three to five clock cycles to enable/disable the output. The device can transfer a DC level, but it needs three to five cycles for output to be enabled/disabled. This pin is pulled down internally with 100 kΩ to 300 kΩ resistor.
Output Clocks			
3 8	OUT0 OUT1	O	**Ultra-Low Additive Jitter LVCMOS Outputs.** Output frequency range >0 Hz to 250 MHz. These outputs have an embedded series resistance of 50Ω (at 1.2V VDD) >0 Hz because OE is synchronous and requires three to five clock cycles to enable/disable the output. The device can transfer a DC level, but it needs three to five cycles for output to be enabled/disabled.
Control Input			
2	OE	I	**Output Enable (Synchronous).** When low, the outputs are low; when high, the outputs are enabled. This pin is pulled down internally with 100 kΩ to 300 kΩ resistors.
Power and Ground			
6	VDD	P	**Positive Supply Voltage.** Connect to supply of 1.2V to 1.8V.
4	GND	P	**Ground.** Connect to ground.
No Connect			
5, 7	NC	N/A	**No connect.** Leave open or connect to ground.

Table 1-2. SY75714 Pin Descriptions

Pin #	Pin Name	Type	Functional Description
Input Reference			
1	IN	I	**LVCMOS Input Reference.** Input frequency range >0 Hz to 250 MHz. Input has a fail-safe circuit to prevent oscillation if the input is not driven. >0 Hz because OE is synchronous and requires three to five clock cycles to enable/disable the output. The device can transfer a DC level, but it needs three to five cycles for output to be enabled/disabled. This pin is pulled down internally with 100 kΩ to 300 kΩ resistor.
Output Clocks			
3 8 5 7	OUT0 OUT1 OUT2 OUT3	O	**Ultra-Low Additive Jitter LVCMOS Outputs.** Output frequency range >0 Hz to 250 MHz. These outputs have an embedded series resistance of 50Ω (at 1.2V VDD). >0 Hz because OE is synchronous and requires three to five clock cycles to enable/disable the output. The device can transfer a DC level, but it needs three to five cycles for output to be enabled/disabled.
Control Input			
2	OE	I	**Output Enable (Synchronous).** When low, the outputs are low; when high, the outputs are enabled. This pin is pulled down internally with 100 kΩ to 300 kΩ resistors.
Power and Ground			
6	VDD	P	**Positive Supply Voltage.** Connect to supply of 1.2V to 1.8V.
4	GND	P	**Ground.** Connect to ground.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Supply Voltage (V_{DD})	–0.5V to +2.3V
Input Voltage (V_{IN})	–0.5V to V_{DD} + 0.5V
Input ESD Protection (HBM)	2 kV
Input ESD Protection (CDM)	1 kV

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet.

2.2. Operating Ratings

1.2V Operating Voltage (V_{DD})	+1.08V to +1.32V
1.5V Operating Voltage (V_{DD})	+1.35V to +1.65V
1.8V Operating Voltage (V_{DD})	+1.62V to +1.98V

Note: The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

2.3. Electrical Parameters and Values

Table 2-1. SY75712 Current Consumption

V_{DD} = 1.8V ±10%, V_{DD} = 1.5V ±10%, V_{DD} = 1.2V ±10%, T_A = –40°C to +105°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
V_{DD} Supply Current	$I_{DD\_1.8V}$	—	6.5	7.5	mA	Note 1
	$I_{DD\_1.5V}$	—	5.3	6.1		
	$I_{DD\_1.2V}$	—	4.1	4.7		

Note:

1. Tested with 25 MHz clock with outputs driving 4” long trace with 50Ω characteristic impedance, terminated with 2 pF capacitors to ground.

Table 2-2. SY75714 Current Consumption

V_{DD} = 1.8V ±10%, V_{DD} = 1.5V ±10%, V_{DD} = 1.2V ±10%, T_A = –40°C to +105°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
V_{DD} Supply Current	$I_{DD\_1.8V}$	—	9.8	11.3	mA	Note 1
	$I_{DD\_1.5V}$	—	8.0	9.2		
	$I_{DD\_1.2V}$	—	6.3	7.3		

Note:

1. Tested with 25 MHz clock with outputs driving 4” long trace with 50Ω characteristic impedance, terminated with 2 pF capacitors to ground.

Table 2-3. Input Electrical Characteristics

V_{DD} = 1.8V ±10%, V_{DD} = 1.5V ±10%, V_{DD} = 1.2V ±10%, T_A = –40°C to +105°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input High Voltage	V_{IH}	0.7 × V_{DD}	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.3 × V_{DD}	V	—
Input Leakage Current	I_{IL_IN}	–5	—	50	µA	V_{IN} = V_{INMAX}, V_{IN} = GND
Input Capacitance	C_{IN}	—	—	5	pF	—
Input Leakage Current for OExb Inputs (includes current due to pull-down resistors)	I_{IL_OE}	–5	—	50	µA	V_{IN} = V_{DD}, V_{IN} = GND
Maximum Input Voltage	V_{INMAX}	—	—	V_{DD} + 0.4	V	—
Minimum Input Voltage	V_{INMIN}	–0.3	—	—	V	—
Input Frequency	f_{IN}	0	—	250	MHz	—
Input Pulse Width	t_{PW}	2	—	—	ns	—
Input Rise/Fall Time (20% to 80%)	t_r/t_f	—	0.6	10	ns	—

Table 2-4. Output Electrical Characteristics

V_{DD} = 1.8V ±10%, V_{DD} = 1.5V ±10%, V_{DD} = 1.2V ±10%, T_A = –40°C to +105°C, see Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Rise Time (20% to 80%)	t_r	—	350	580	ps	Note 1
Output Edge Fall Time (80% to 20%)	t_f	—	350	580	ps	Note 1
Output High Voltage	V_{OH}	0.8 × V_{DD}	—	—	V	I_{OUT} = 3 mA
Output Low Voltage	V_{OL}	—	—	0.2 × V_{DD}	V	I_{OUT} = –3 mA
Output Duty Cycle (when input has 50% duty cycle)	DC	45	50	55	%	f_{OUT} = 156.25 MHz
Output Frequency	f_{MAX}	0	—	250	MHz	—
Output-to-Output Skew	t_{OOSK}	—	38	50	ps	—
Device-to-Device Skew	t_{DDSK}	—	—	550	ps	—
Input-to-Output Delay	$t_{IOD\_CMOS\_IN}$	1.1	1.5	2.1	ns	—
Output Enable Time	t_{EN}	3	—	5	Clock cycles	—
Output Disable Time	t_{DIS}	3	—	5	Clock cycles	—
Output Impedance	O_{IMP}	40	50	60	Ω	Note 2

Notes:

1. Bench tested with 100 MHz clock with outputs driving 4” long trace with 50Ω characteristic impedance, terminated with 2 pF capacitors to ground.
2. 50Ω output impedance is with 1.2V V_{DD}. When output is powered with 1.8V V_{DD}, the output impedance will be slightly lower (approximately 40Ω).

Table 2-5. SY75712/14 Jitter and Phase Noise

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{DD} = 1.8V ±10%, T_A = –40°C to +105°C, see Note 1						
Additive RMS Jitter in 1 MHz to 5 MHz Band	$t_{j\_1M\_5M}$	—	15.3	26.5	fs_{RMS}	25 MHz clock
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	16.0	25.2	fs_{RMS}	100 MHz clock
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	15.8	24.7	fs_{RMS}	156.25 MHz clock
Additive RMS Jitter in 12 kHz to 5 MHz Band	$t_{j\_12k\_5M}$	—	19.7	34.4	fs_{RMS}	25 MHz clock
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	16.9	26.3	fs_{RMS}	100 MHz clock
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	16.9	26.1	fs_{RMS}	156.25 MHz clock
Noise Floor	N_F	—	–175.2	—	dBc/Hz	25 MHz clock
		—	–172.8	—	dBc/Hz	100 MHz clock
		—	–169.7	—	dBc/Hz	156.25 MHz clock
V_{DD} = 1.2V ±10%, T_A = –40°C to +105°C, see Note 1						
Additive RMS Jitter in 1 MHz to 5 MHz Band	$t_{j\_1M\_5M}$	—	35.1	56.8	fs_{RMS}	25 MHz clock
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	33.7	53.9	fs_{RMS}	100 MHz clock
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	32.0	48.7	fs_{RMS}	156.25 MHz clock
Additive RMS Jitter in 12 kHz to 5 MHz Band	$t_{j\_12k\_5M}$	—	42.2	66.7	fs_{RMS}	25 MHz clock
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	36.3	57.1	fs_{RMS}	100 MHz clock
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	35.9	53.5	fs_{RMS}	156.25 MHz clock
Noise Floor	N_F	—	–171.9	—	dBc/Hz	25 MHz clock
		—	–168.8	—	dBc/Hz	100 MHz clock
		—	–165.2	—	dBc/Hz	156.25 MHz clock

Note:

1. Tested with input fed with low jitter clock from R&S SMA100B function generator and with outputs driving R&S FSWP8 Phase Noise Analyzer via SMA cable.

2.4. Temperature Specifications

Table 2-6. 8-Lead TDFN Package Thermal Properties

Parameter	Symbol	Value	Units	Condition
Junction to Ambient Thermal Resistance	Θ_{JA}	122.9	°C/W	Still air
		115.1	°C/W	1 m/s airflow
		111.1	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	Θ_{JB}	65.8	°C/W	—
Junction to Case Thermal Resistance	Θ_{JC}	129.2	°C/W	—
Thermal Characterization, Junction to Top of Package	Ψ_{JT}	10.5	°C/W	Still air

3. Functional Description

The SY75712 and SY75714 are two- or four-output, ultra-low additive jitter, 1.2V to 1.8V LVCMOS fanout clock buffers with synchronous Output Enable (OE) control signal. The devices can operate at an extended temperature range from –40°C to +105°C.

The outputs have built-in 50Ω series resistance which makes them suitable for driving standard transmission lines (50Ω characteristic impedance) without any external components.

The following phase noise plots captured with an R&S FSWP8 Phase Noise Analyzer show typical phase noise performance. Figure 3-1 shows the phase noise of input clock generated with R&S SMA100B signal generator and Figure 3-2 shows the SY75712/14 output phase noise.

Figure 3-1. Clock Phase Noise of the 100 MHz Input Clock Generated with R&S SMA 100B

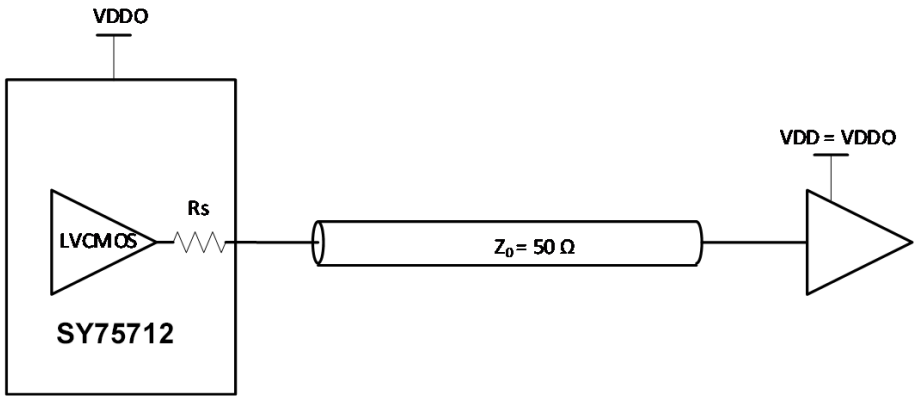
Figure 3-2. Phase Noise of SY75712/SY75714 Output Clock

The plot in Figure 3-2 shows that the device has a very low noise floor of –171.7 dBc/Hz, which results in ultra-low additive jitter in the 12 kHz to 20 MHz band of only 15 fs.

3.1. Clock Output

The LVCMOS output has built-in 50Ω series termination, which reduces BOM cost and area on the PCB. Figure 3-3 shows how to terminate the LVCMOS output.

Figure 3-3. Terminating Device Output

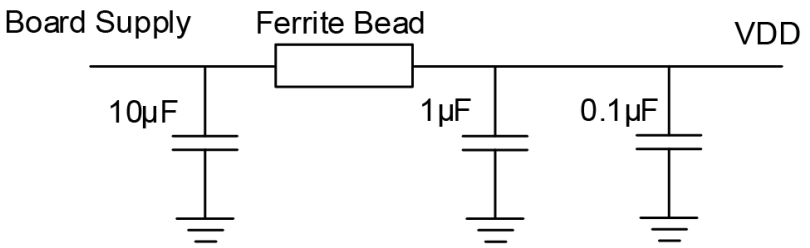


3.2. Power Supply Filtering

The power pin (VDD) should be decoupled with a 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R ceramic capacitors with a 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pin. To reduce the power noise from adjacent digital components on board, the power supply pin could be further insulated with a low resistance ferrite bead with two capacitors. The

ferrite bead will also insulate adjacent components from the noise generated by the device. Figure 3-4 shows the recommended decoupling for each power pin.

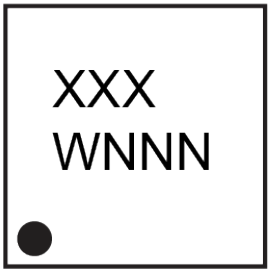
Figure 3-4. Power Supply Filtering



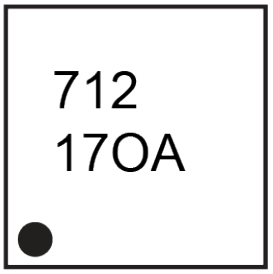
4. Packaging Information

4.1. Package Marking Information

8-Lead TDFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

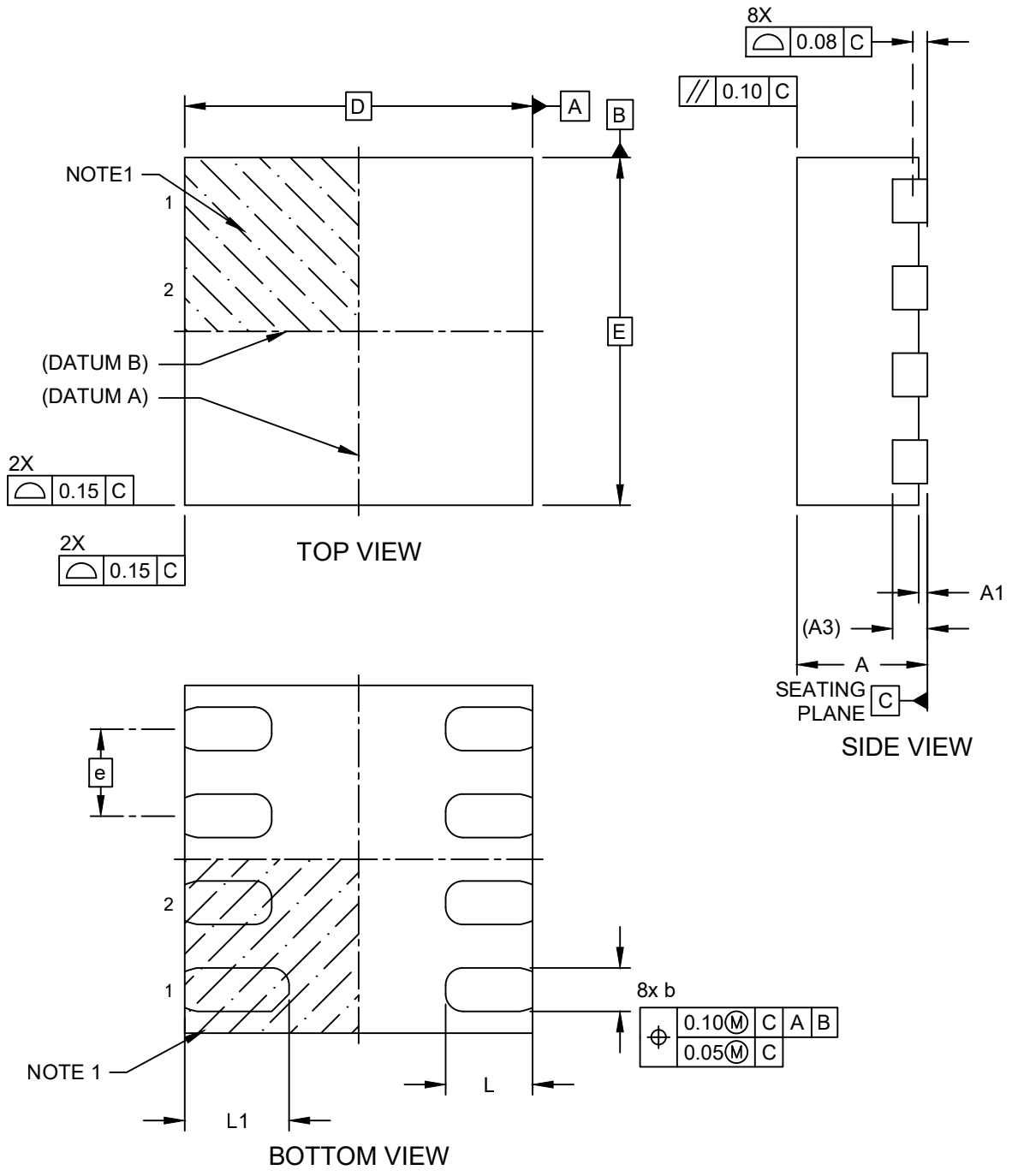
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

4.2. Package Outline Drawing

8-Lead Thin Dual Flatpack No-Lead (8HW) 2x2x0.8mm Body [TDFN] With Chip On Lead

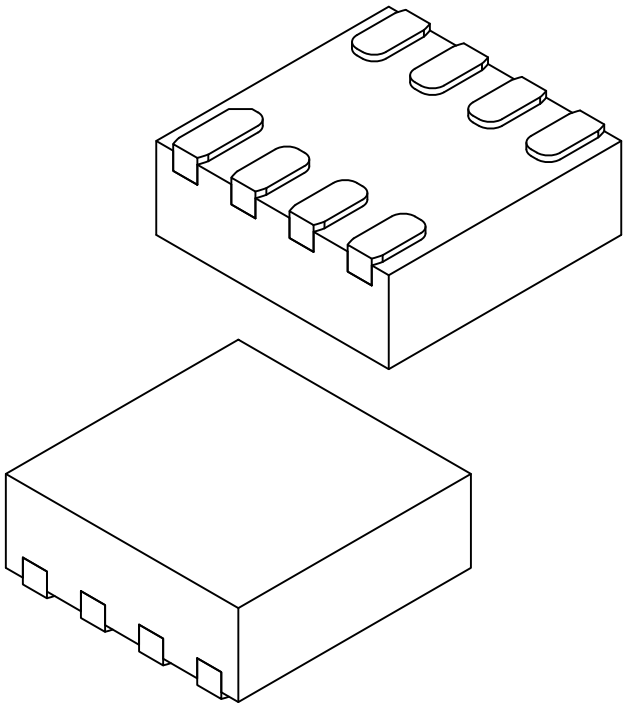
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00662 Rev D Sheet 1 of 2

8-Lead Thin Dual Flatpack No-Lead (8HW) 2x2x0.8mm Body [TDFN] With Chip On Lead

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	-	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.40	0.50	0.60
Pin 1 Terminal Length	L1	0.50	0.60	0.70

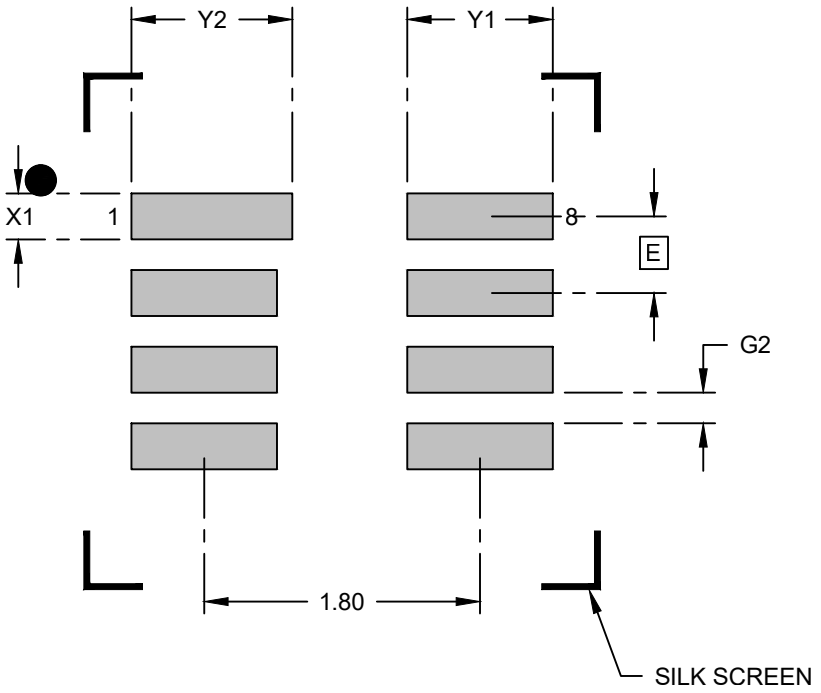
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00662 Rev D Sheet 2 of 2

8-Lead Thin Dual Flatpack No-Lead (8HW) 2x2x0.8mm Body [TDFN] With Chip On Lead

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		1.80	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X7)	Y1			0.95
Pin 1 Contact Pad Length (X1)	Y2			1.05
Contact Pad to Contact Pad (X6)	G2	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
2. For best soldering results, please refer to the current industry standard IPC-7093.

Microchip Technology Drawing C04-02662 Rev D

5. Revision History

Table 5-1. Data Sheet Revision History

Revision	Date	Description
A	09/2025	Internal preliminary release of the SY75712/14 data sheet as DS20007045A.
B	06/2026	Initial public release of the SY75712/14 data sheet as DS20007045B.

6. Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	XXX	-XX
Part Number	Package Option	Media Type

Device:	SY75712: Two Output, Ultra-Low Additive Jitter, 1.2V to 1.8V LVCMOS Clock Buffer SY75714: Four Output, Ultra-Low Additive Jitter, 1.2V to 1.8V LVCMOS Clock Buffer	
Package Option:	TWL	= 8-Lead 2 mm × 2 mm TDFN
Media Type:	TR	= 3000 Pieces Tape and Reel

Examples:

- SY75712TWL-TR: Two-Output, Ultra-Low Additive Jitter, 1.2V to 1.8V LVCMOS Clock Buffer, 8-Lead 2 mm × 2 mm TDFN Package, 3000 Pieces Tape and Reel
- SY75714TWL-TR: Four-Output, Ultra-Low Additive Jitter, 1.2V to 1.8V LVCMOS Clock Buffer, 8-Lead 2 mm × 2 mm TDFN Package, 3000 Pieces Tape and Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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