

Table of Contents	
1	Title Page
2	PCA9422, PMIC
3	PCA9422, I2C INTERFACE
4	PCA9422, DNP/JUMPER TABLES

Revisions			
Rev	Description	Date	Approved
X1	Initial Design based on PCA9420UK-EVM board	04/27/2022	J. Romero
X2	Several parts updated	05/24/2022	J. Romero
A	Final release	09/23/2022	J. Romero
AX1	Several parts updated	02/24/2023	J. Romero
B	Final release	03/07/2023	J. Romero
BX1	-C14 changed to DNP. -J5, J8, R8, R42 & U6 pin 1 and pin 5 updated connections. L1, L5, L6 & L7 footprint updated . -J10, J11, J21, J23, J30-J39, J43-J44, J50, TP15, TP26 & TP27 removed. -D3-D5, R11, SJ1-SJ26 & U9 added. -J10 changed from 3 pin HDR to 2pin HDR. -J28 jumper default changed from 1-2 to 2-3. -R9 value changed from 68 to 91 ohms.	09/25/2023	J. Romero
C	Final release	10/10/2023	J. Romero
CX1	- R15, R16 removed - C100-C102 added - SJ27-SJ29 added - SJ16.1 connection update - SJ17.1 connection update - J8 changed from open to closed 1-2 - J1-J4 part number changed	07/22/2024	J. Romero
D	J1-J4 & U7 updated part number Final release	08/12/2024	J. Romero
D1	J14 default setting changed	10/09/2024	J. Romero
DX2	J3 connections updated	12/17/2024	J. Romero
E	Final release	01/02/2025	J. Romero
EX1	- Added TP6, J29 & J30. - J8, J40, J41, J42, J46 & J47 changed default jumper position. - VPU signal split into VPU_AO & VPU_IO	03/06/2025	J. Romero
F	- Removed SJ27, U9, D3, D4 & D5. Replaced APN of C7, C8, C84, C88, C93, C95 & C97. - Rearrange signals of J6, Pins swapped of J45. Changed silk property of: TP26. - Renamed some nets: LX1, LX2, LX3, LX4A & LX4B. - Changed silk property of: J8, J29, J30, J46 & J47. Connection swapped of: J14, J28 & J29. Final release.	05/14/2025	J. Romero
F1	Changed U7 to 315-80122	06/25/2025	J. Romero
F2	Updated L5, L6 & L7.	10/13/2025	J. Romero

PCA9422-EVB
PCA9422 (PMIC) Evaluation Board



Advanced Analog
6501 William Cannon Drive West
Austin, TX 78725-6598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

© NXP SEMICONDUCTORS

Designer: **Juan Carlos Becerra**

Drawn by: **Diego Garay**

Approved: **Juan Romero**

Classification: **Company Internal/Proprietary**

Drawing Title: **PCA9422-EVB**

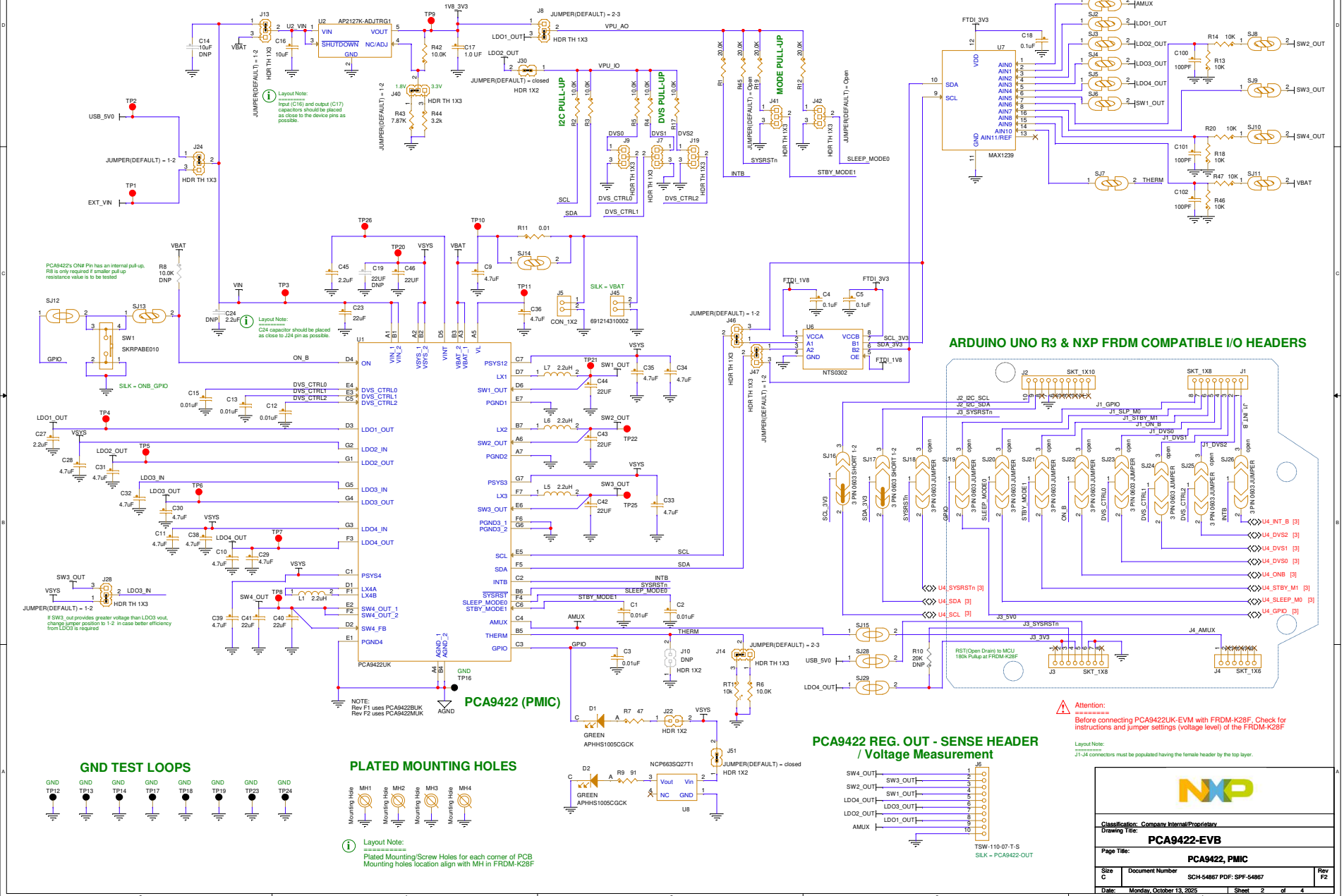
Page Title: **Title Page**

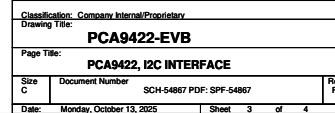
Size: **C** Document Number: **SCH-54867 PDF: SPF-54867** Rev: **F2**

Date: **Monday, October 13, 2025** Sheet: **1** of **4**

PCA9422 (PMIC) EVALUATION CIRCUIT INTERFACE

LDO
3.3V or 1.8V / 150mA (Max-Derated)





REF DES	JUMPER(DEFAULT)	PAGE NAME
J13,J24,J28,J40,J46,J47	1-2	02 PMIC
J8,J14	2-3	02 PMIC
J7,J9,J19,J41,J42	Open	02 PMIC
J30,J51	closed	02 PMIC
J22	open	02 PMIC
J29	2-3	03 I2C INTERFACE

REF DES	ASSY. OPT	PAGE NAME
C14,C19,C24,J10,R8,R10	DNP	02 PMIC

REF DES	SHORT(DEFAULT)	PAGE NAME
SJ16,SJ17	1-2	02 PMIC
SJ1,SJ2,SJ3,SJ4,SJ5,SJ6,SJ7, SJ8,SJ9,SJ10,SJ11,SJ13,SJ14	closed	02 PMIC
SJ12,SJ15,SJ18,SJ19,SJ20, SJ21,SJ22,SJ23,SJ24,SJ25, SJ26,SJ28,SJ29	open	02 PMIC

- + Kit will include additional jumpers (shunts) for open headers for further applications
- + All SJs parts are solder blob jumpers



Classification: Company Internal/Proprietary			
Drawing Title: PCA9422-EVB			
Page Title: DNP/JUMPER/SHORT TABLES			
Size C	Document Number SCH-54867 PDF: SPF-54867	Rev F2	
Date: Monday, October 13, 2025	Sheet 4 of 4		