RT Voice Solution - Voice Control Board

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REVISION HISTORY

REVISION	DESCRIPTION OF CHANGE	DATE	Author	Reviewer
C2	Voice Control Board Production release. Changed TFA9894N2RDL2 into TFA9894DUK to reflect the official product name. J4 and J26 connectors populated by default.	01-October-19	Jerome BRILLANT	Vincent FILLATRE

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **Voice Control Board**

Page Title: **Cover Page**

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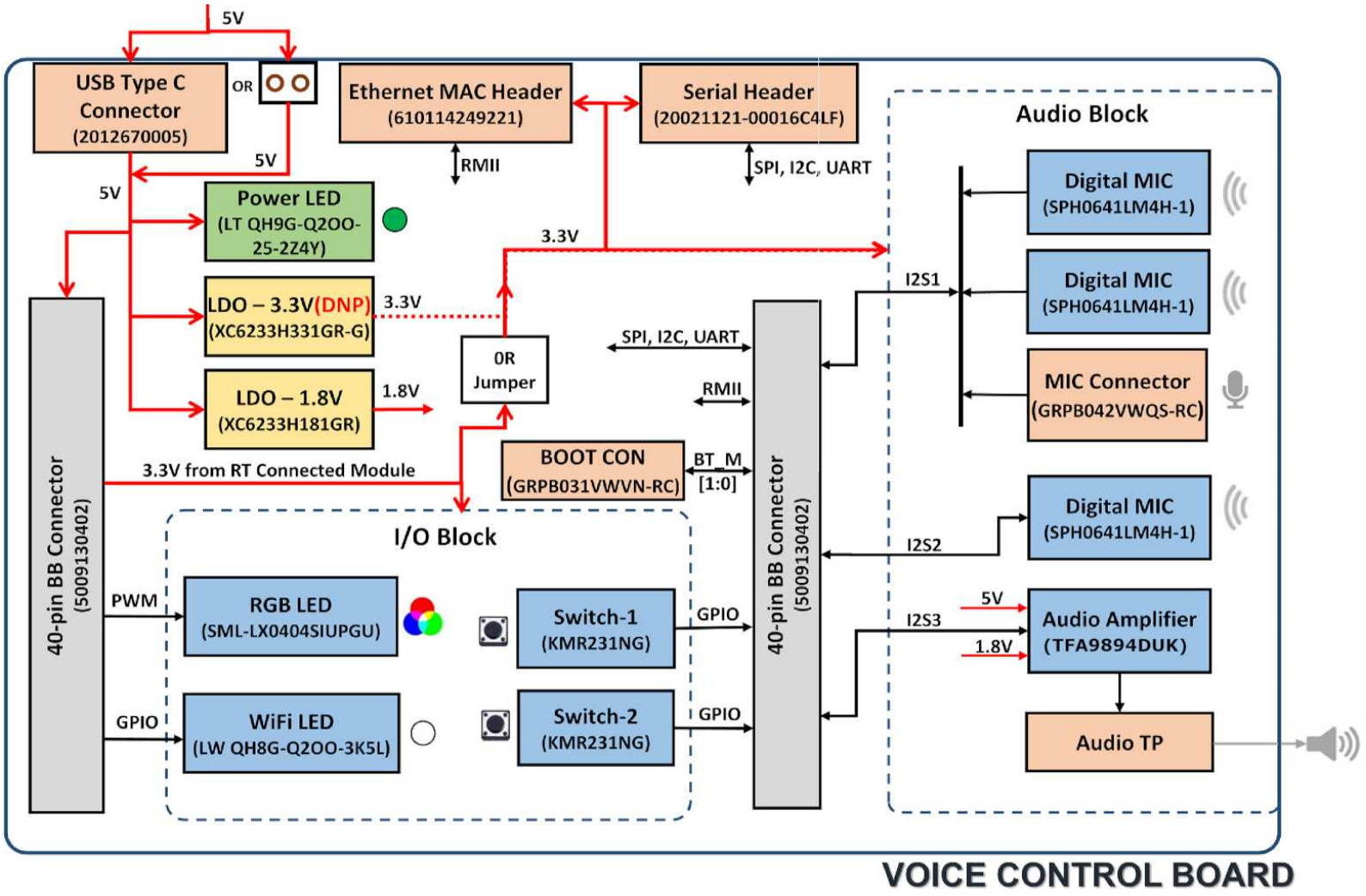
System Block Diagram



ICAP Classification: CP: ___ IUO: X PUBL: ___

Drawing Title: Voice Control Board

Page Title: System Block Diagram

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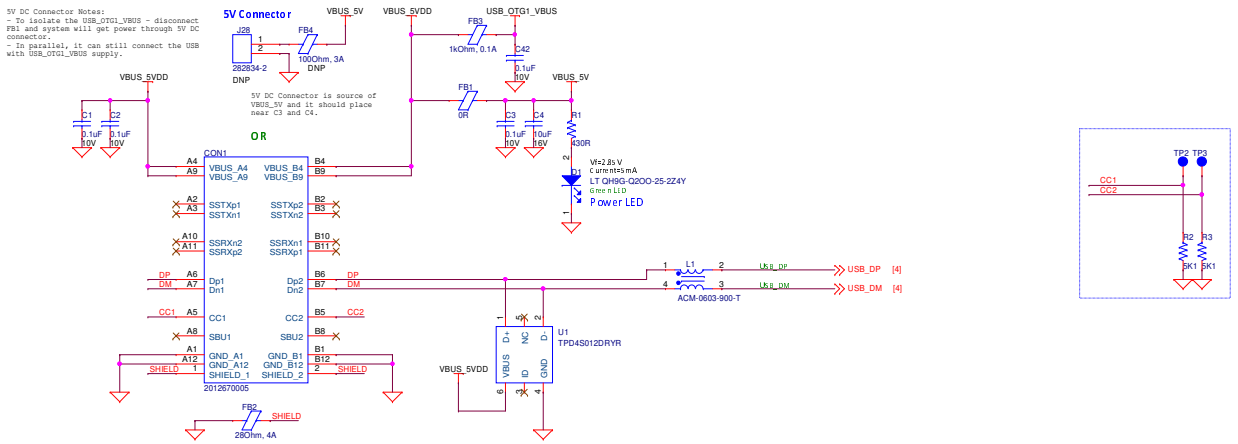
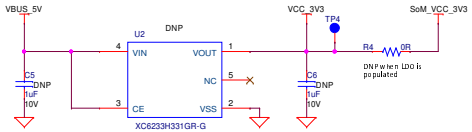
Power Supply Section

USB Type C Connector



5 to 3.3V LDO section

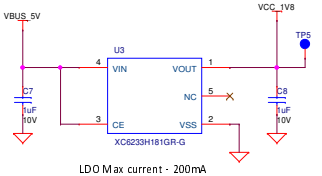
Do not Populate this section



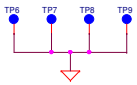
Optional

LDO Max current - 200mA

5V to 1.8V LDO section



LDO Max current - 200mA



Ground Testpoints

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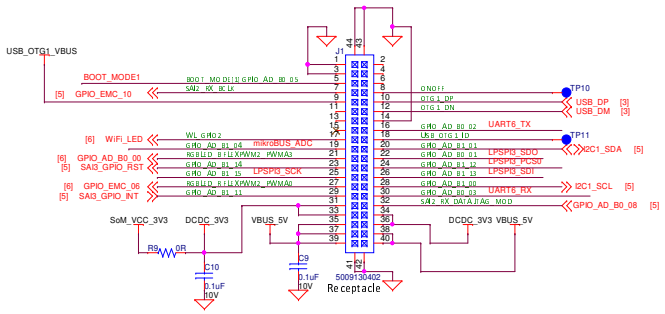
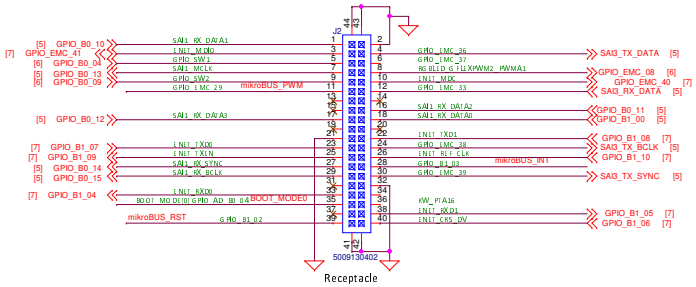
Board to Board Receptacles

B2B Connector#1



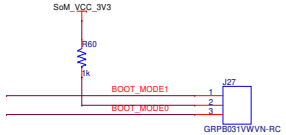
B2B Connector#2



Board Stacking Height - 1.8mm

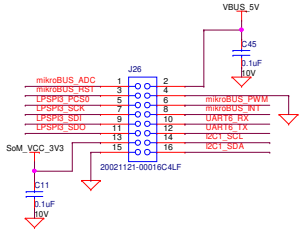
Board to Board Mating Height - 2.3mm

Boot Mode selection Header



Use only during Development phase

Serial Port Header



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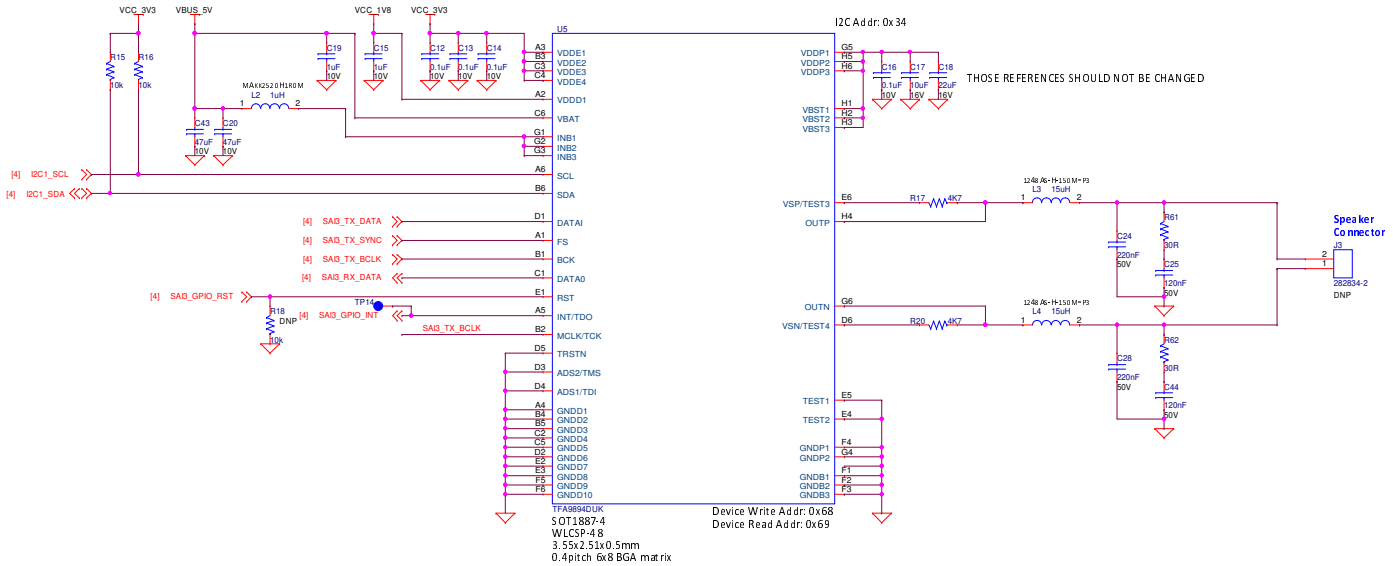
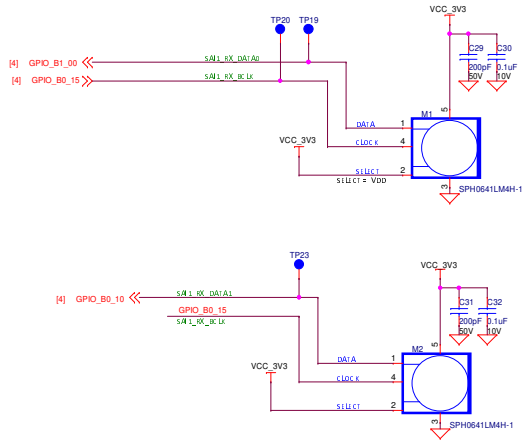
Audio Interface Section

Audio Amplifier

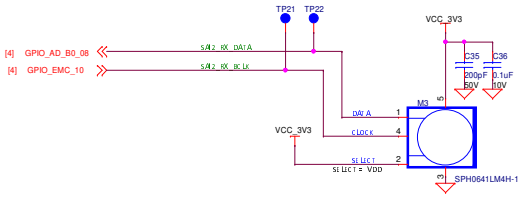


PDM MICROPHONE Interface

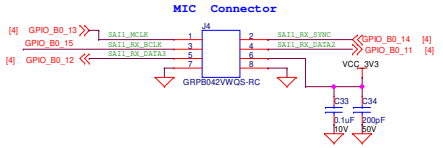
SAI1 RX SLAVE



SAI2 RX SLAVE



SAI1 Header



Notes :

1. Decoupling Capacitors mounted as close as possible are required for optimum SNR.
2. RF filter capacitors in the range of 20-200 pF may be needed depending upon the RF environment.
3. If both decoupling capacitors and RF filter capacitors are used, the RF filter capacitors should be close to the microphone.

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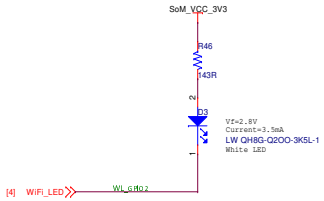
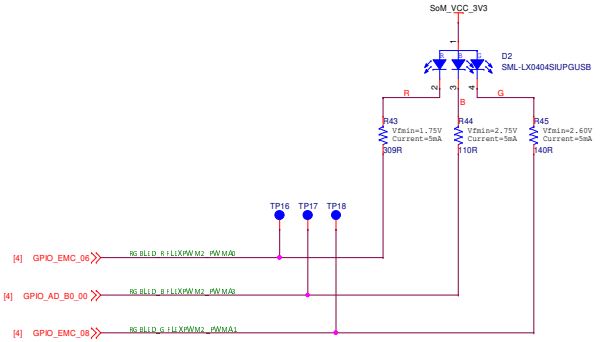
Input & Output Interface

User LED Interface

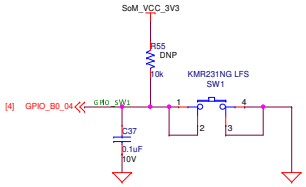
1DX Wi-Fi+BLE Status LED

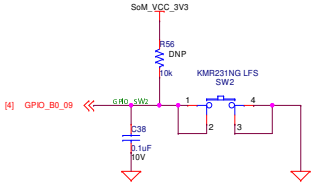


RGB LED Interface



Switch interface





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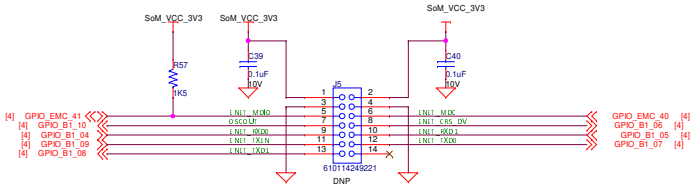
Ethernet Interface

Ethernet Header



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Miscellaneous

DMY1

LAY-SOL0002-C

Voice Control Board PCB

DMY2

CONN JUMPER SHORTING 1.27MM GOLD

2-Pin Shunt jumper_1.27MM pitch

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: **Voice Control Board**

Page Title: **Miscellaneous**

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MIMXRT106LDVL6A - Connected Module

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REVISION HISTORY

REVISION	DESCRIPTION OF CHANGE	DATE	Author	Reviewer
C3	SLN-LOCAL-IOT production release. Remove A71 section (not used in this project)	02-October-19	Jerome BRILLANT	Vincent FILLATRE

ICAP Classification: CP: IUO: PUBL

Drawing Title: i.MXRT Connected Module

Page Title: Cover Page

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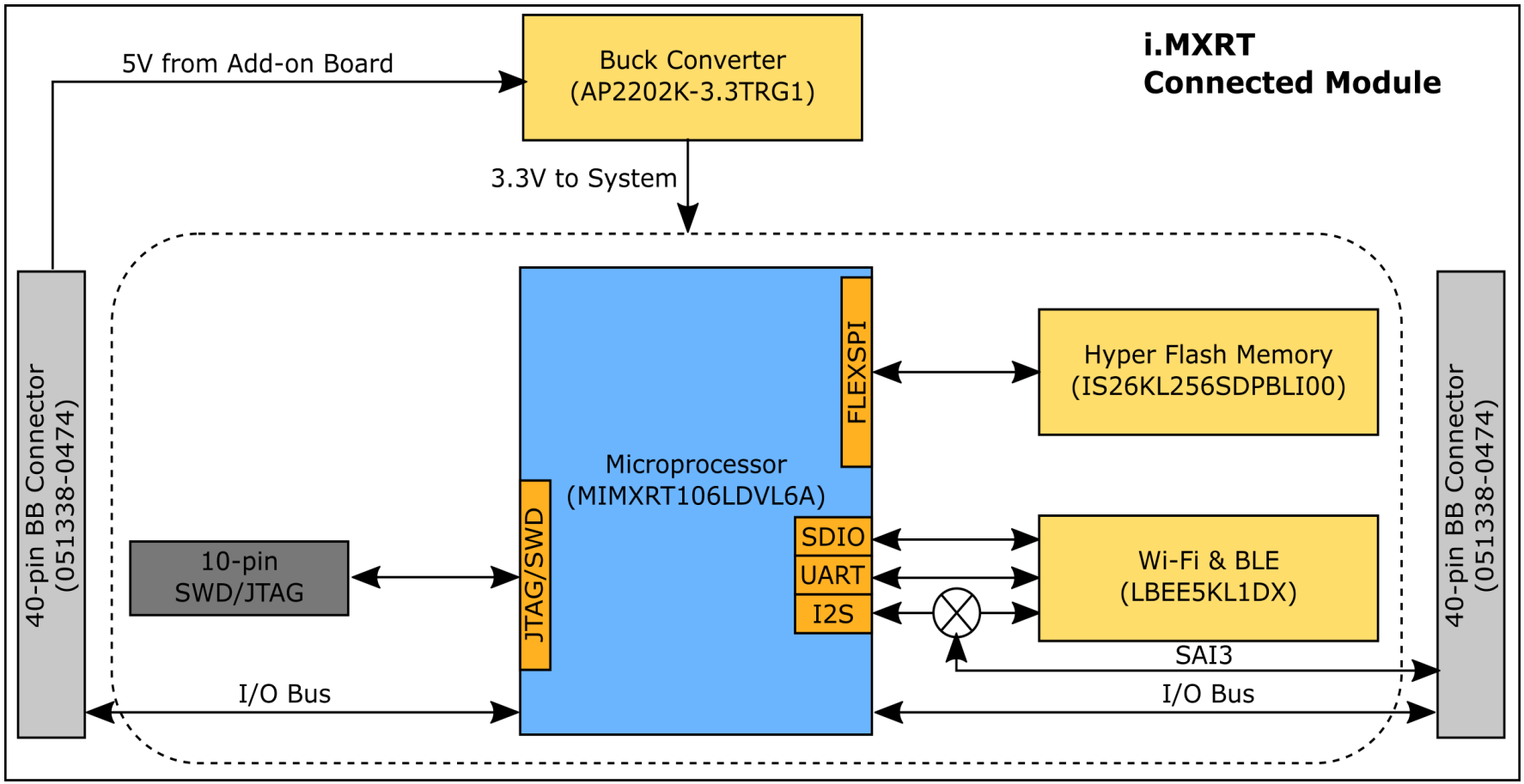
Block Diagram



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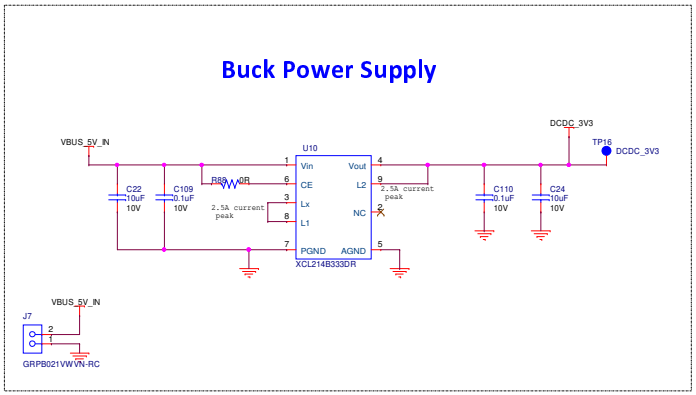
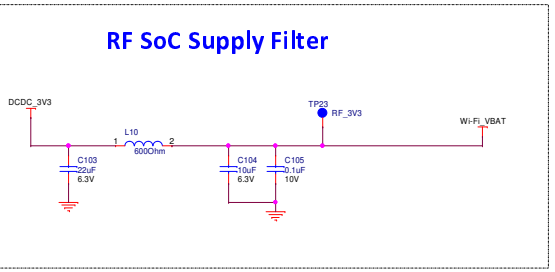
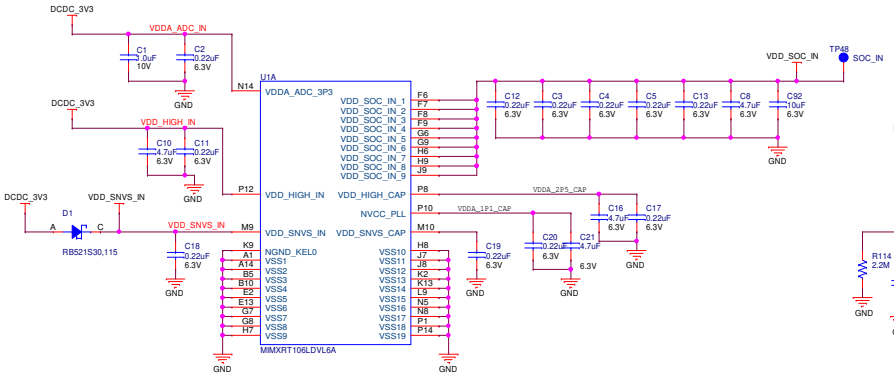
iMXRT Connected Module Power Section

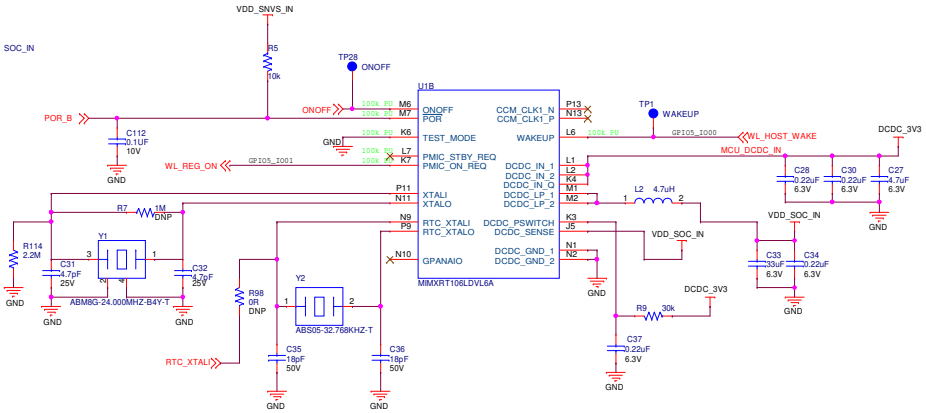
Buck Power Supply



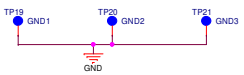
RF SoC Supply Filter







Ground Test Points



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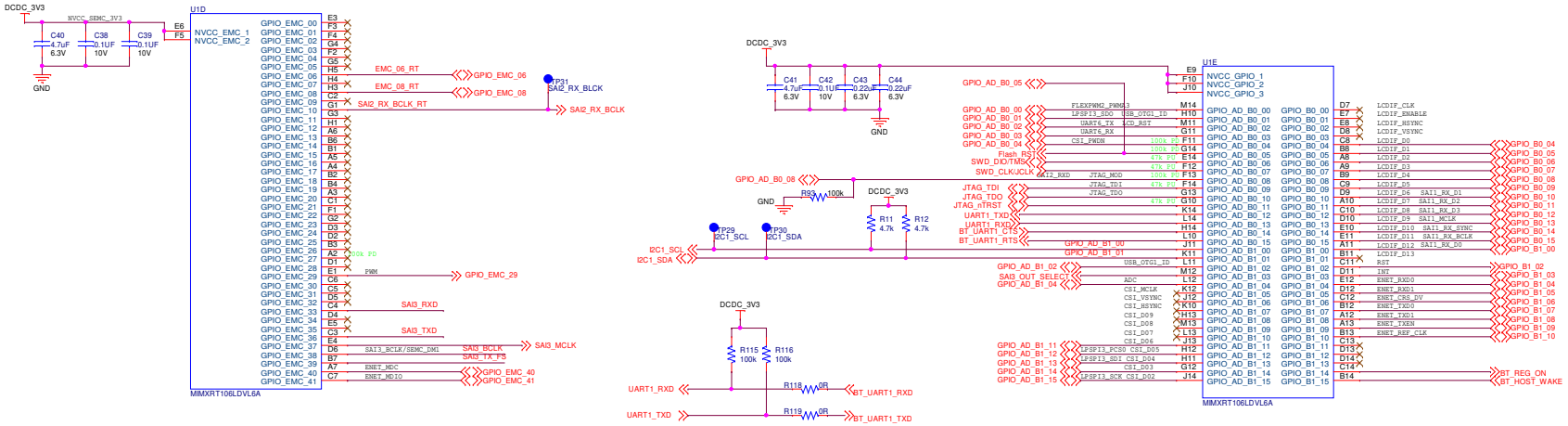
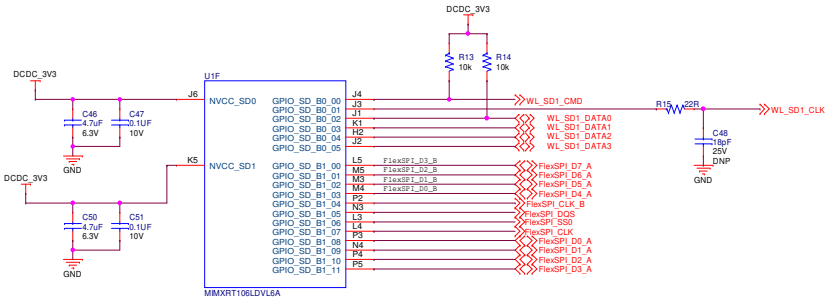
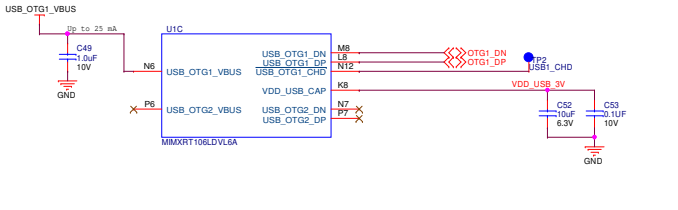
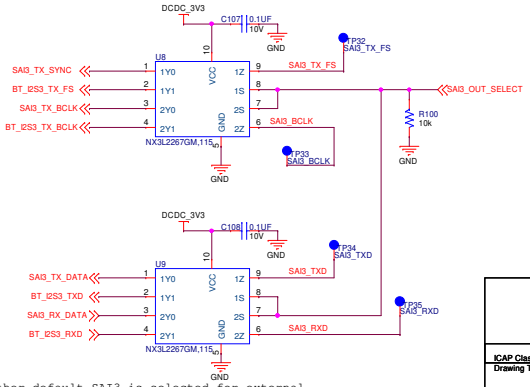
i.MXRT Section









Note: Further default SAI3 is selected for external
Audio interface on ADD-on-Board.
- Need to Toggle SAI3_OUT_SELECT signal "High" to use SAI3 for onboard BT

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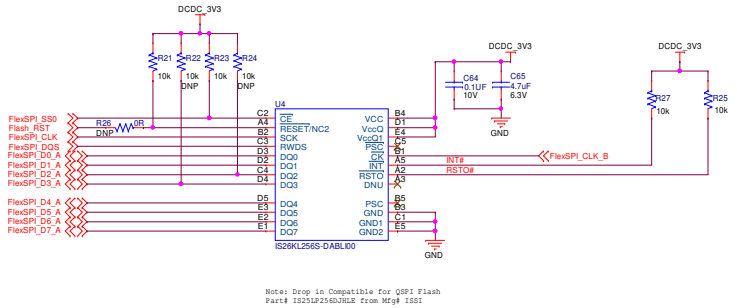
Memory Section

HyperFlash or QSPI Flash Memory



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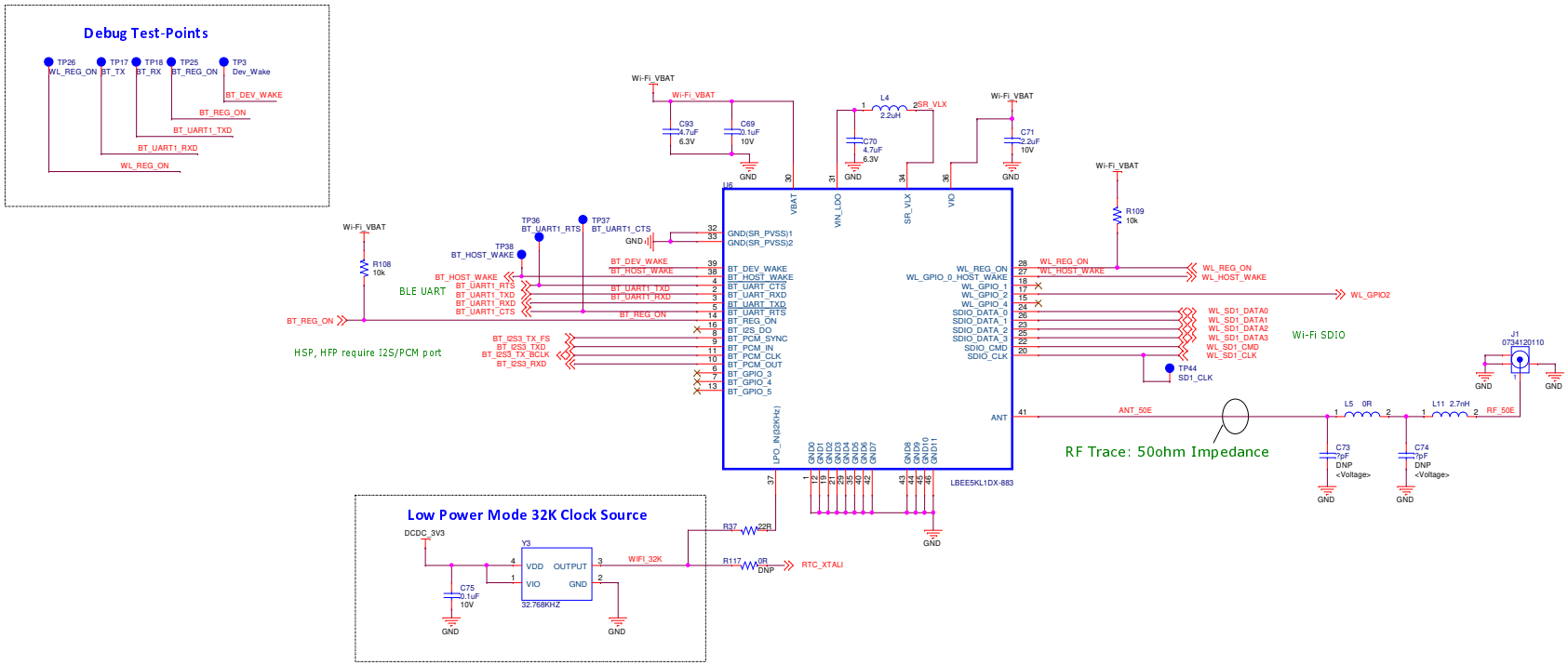
Wi-FI & BT/BLE Module Section



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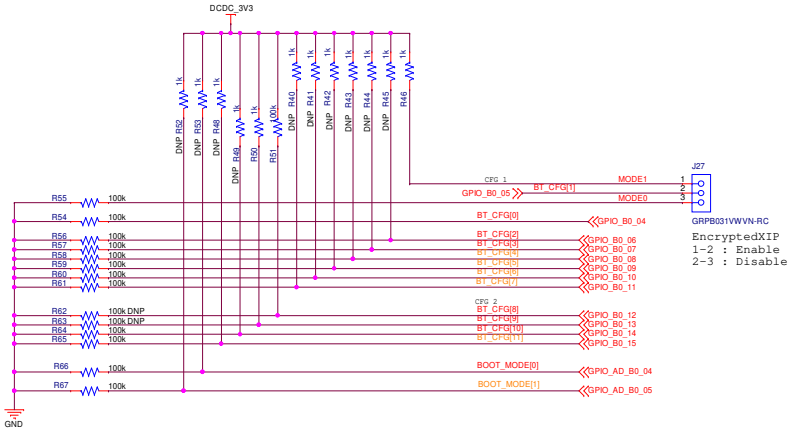
Boot Configuration & Debug Interface

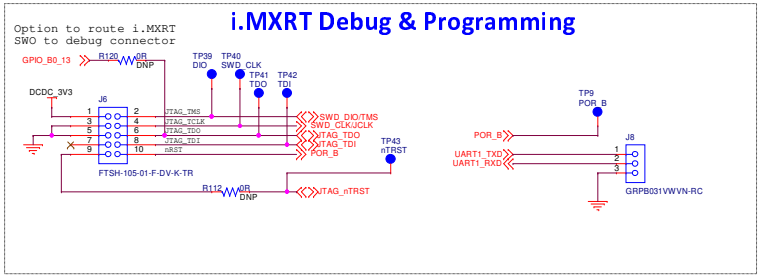
Boot Configuration



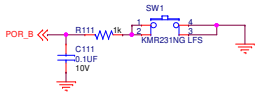
Boot Mode selection Header

EncryptedXIP
1-2 : Enable
2-3 : Disable

i.MXRT Debug & Programming



i.MXRT Reset Button



FUSE MAP

	0	0	1	1	0	0	0	0	0	0	0	0
TYPE	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI1 - Serial NOR	Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1- Enabled	Reserved
SD	Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot

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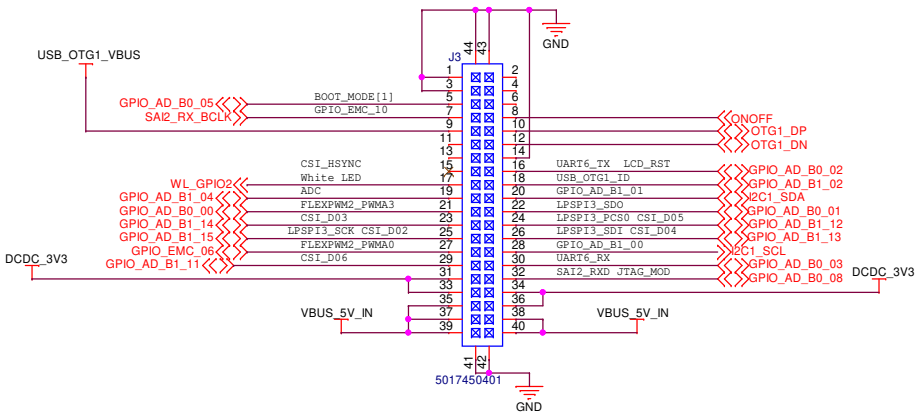
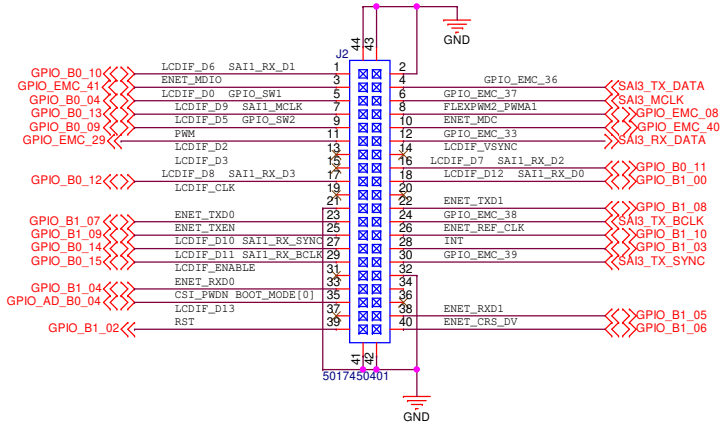
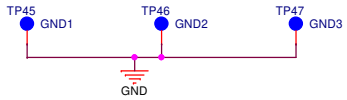
B2B Connector





Ground Test Points



DMY1 i.MXRT Connected Module PCB Rev C
LAY-SOL0001-C

DMY2 NPB02SVAN-RC
CONN JUMPER SHORTING 1.27MM GOLD

DMY3 1461530100
2.4/5G DUAL BAND ANTENNA 100MM

ICAP Classification: CP: IUO: PUBI:

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