REVISION	DESCRIPTION	DATE	APPROVED

Revision History:

REV	DATE	Description:
A	09-MAR-2022	Initial Release
	11-APR-2022	Modifications from first Design Review
	20-APR-2022	Modifications from second Design Review
	24-JUN-2022	Made GPIO changes, moved hi-speed signals away from Port 0. Many moves as a result
	01-AUG-2022	Changed the QFN164 from a 9.0 x 9.0 paddle size to 8.5 x 8.5. Allows room for vias
	23-AUG-2022	Added 2nd camera connector, SEUART header + res, isolated VDD_MIPI_1V8
A2	28-NOV-2022	Removed RF Module components from design.
	05-DEC-2022	New GPIO mapping, based on design team performance of OSPI ports
	30-DEC-2022	Changed Alif E7 from QFN164 ro BGA194. Added GNSS and RESET pins
	04-JAN-2023	Minor changes from design review. Renumerated reference designators
	24-JAN-2023	Put back SD Flash 3.3V and level translators
	31-JAN-2023	It was "discovered" that OSPI1 cannot support HyperRAM, only OSPI0 can. Moving HyperRAM to OSPI0 and Flash to OSPI1
		Changed GNSS RF path to 0201 components. Removed Bypass (R99 and R100)
	15-FEB-2023	Replaced Y3 with a 38.4MHz TCXO + caps
A3	13-APR-2023	Removed OVP LED. Changed OVP components. Power LED dimmed.
		3 Off-page naming errors (3 wires). C_EN_MIPI_PWR, I2C_CL_SDA, and I2C_CL_SCL
		D12 backwards (part different from Alif library)
B	18-APR-2023	From Rev A3, added PCB Fab and Mounting Hardware for BOM
C	15-JUN-2023	Fixed swapped MIPI_CSI_C pair with MIPI_CSI_0 pair on BGA194
	07-SEP-2023	Changed C28 (VREG_AON) to 1.0uF
	12-SEP-2023	Changed OSPI Flash and HyperRAM to 64MB devices
		Swapped USB_DEV_ID resistor divider for 1.8V signaling
C1	04-OCT-2023	Removed J1, R67, Added label
D	04-NOV-2023	VREG_AON RC, added VCC_PLL_0V8, changed SDMMC voltage translator,
		Add regulatory icons, removed unnedded power decoupling components
		Removed GPS components, changed TCXO to crystal
	07-DEC-2023	Added shunt to isolate VDD_USB_3V3, DNI caps to MIPI CSI pairs
	25-JAN-2024	Design Review: Remove MIPI caps, GND TEST_MODE, change TP49 & TP50 to header pins
D1	18-APR-2024	Change VREG_AON series resistor R33 to 1K.
		Added note on VREG_DIG_1V8 for 1.8V oprtation
		Bypass VBATT circuit, connect to VDD_MAIN.
		Remove D12, Q9, Q10, BT1 and J7. Rework wire across D12
		Click I2C missing connection. Rework wire from V_CON_IO to V_CLICK

Required 2.54mm Shunts:
J5 VDD_3V3 Current Measurement

J6 VDD_1V8 Current Measurement

J7 Battery Current Measurement

J31 VDD_3V3 USB Current Measurement

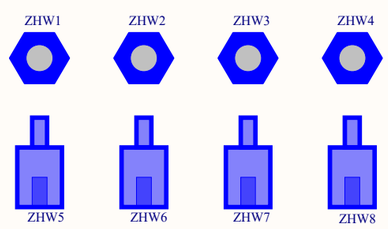
J8-1 J8-2 FLEXIO = 1.8V * default
J8-2 J8-3 FLEXIO = 3.3V

J9-1 J9-2 SD Flash Power = 3.3V * default
J9-2 J9-3 SD Flash Power = 1.8V for "LV" Cards

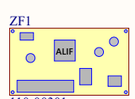
J13-1 J13-2 Click Board Power = 1.8V * default
J13-3 J13-4 Click Board Power = 3.3V
J13-5 J13-6 Click Board Power = 5.0V

J19-1 J19-2 Camera Analog V = 2.8V
J19-2 J19-3 Camera Analog V = 2.6V * default

Optional 2.54mm Shunts:
J26-1 J26-3 and J24-2 J24-4 UART2
J26-3 J26-5 and J24-4 J24-6 UART4 * default



Nylon Mounting Hardware (H1 - H4)



APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00301	
ASSY DWG: 120-00301	
FAB DWG: 210-00301	
PCB DWG: 110-00301-D	

PROJECT 00301

ALIF SEMICONDUCTOR

Alif Semiconductor
7901 Stoneridge Drive
Suite 300
Pleasanton, CA 94588 USA

TITLE

ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none | FILE NAME 1-RevisionHistory.SchDoc | SHEET 1 OF 12

DWG NO. 220-00301 | REVISION D 1

REVISION	DESCRIPTION	DATE	APPROVED

USB Host only gets power from DC Jack

ESD Protection

OVER VOLTAGE PROTECT (SCR)

Device	R(raw)	R(gnd)
NCP690	out	out
NCP691	out	in
NCP692	in	out

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00301	
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FAB DWG: 210-00301	
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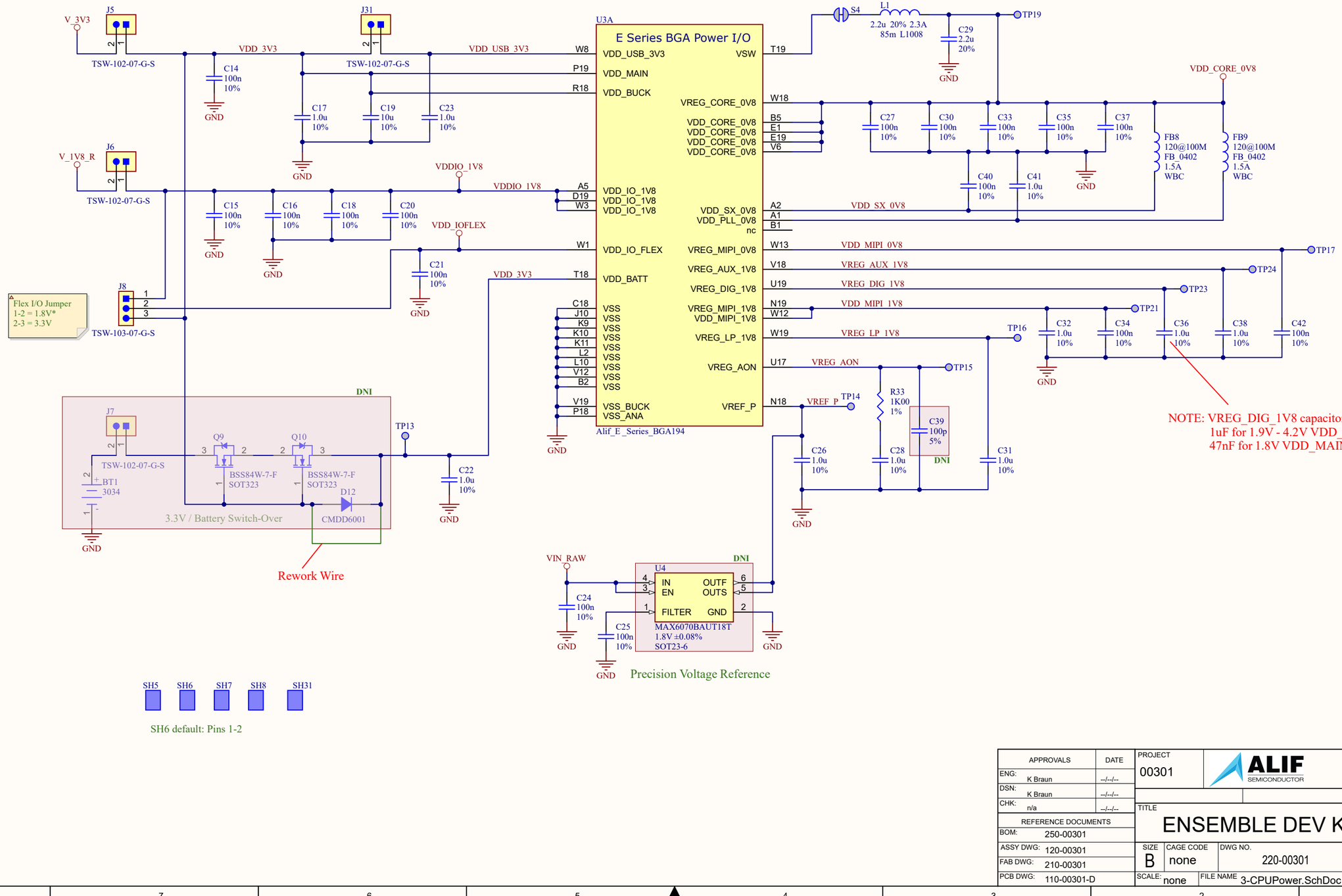
SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none | FILE NAME 2-PowerInput.SchDoc | SHEET 2 OF 12

DWG NO. 220-00301 REV D SHT 2

REVISION	DESCRIPTION	DATE	APPROVED

CPU Power Supplies



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REFERENCE DOCUMENTS	
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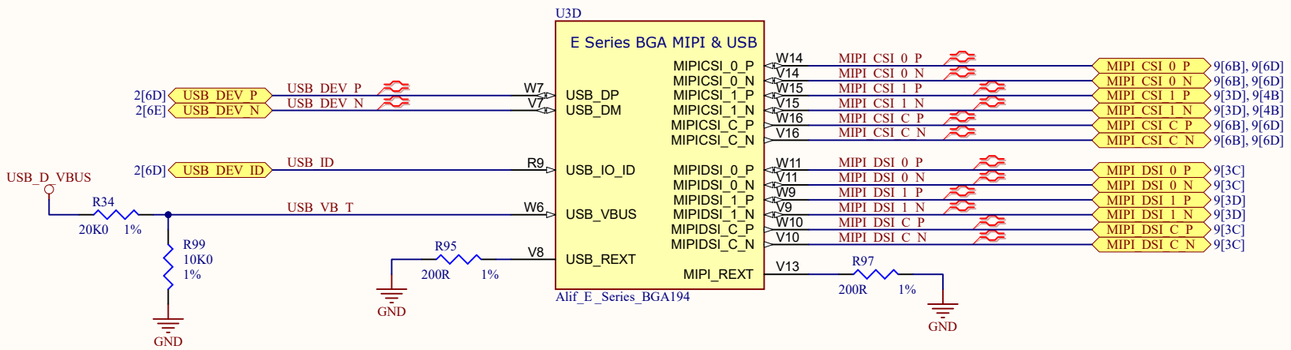
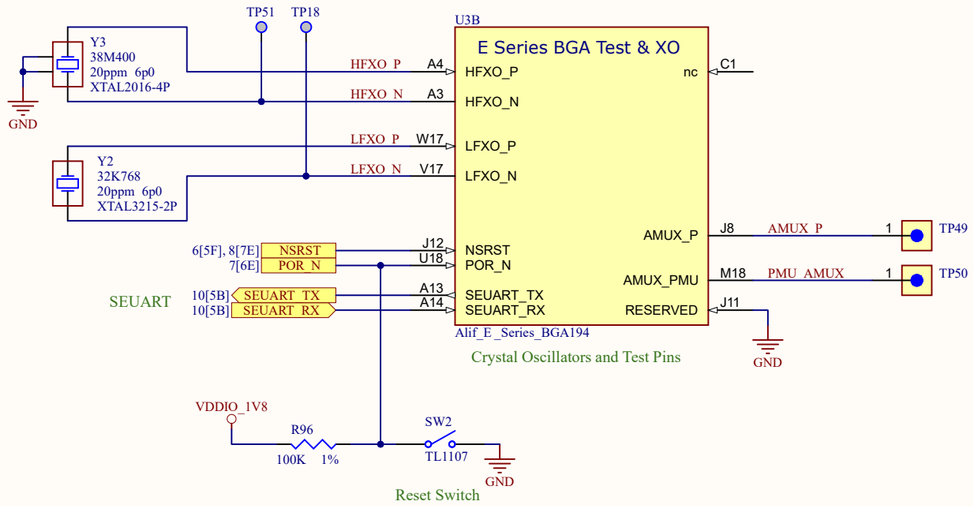
DWG. NO. 220-00301 REV/SH D 3

REVISION	DESCRIPTION	DATE	APPROVED



USB, MIPI CSI and DSI Interfaces



Crystal Oscillators and Test Pins

Reset Switch

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

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PCB DWG:	110-00301-D

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DWG. NO. 220-00301
REV/SHT D 4

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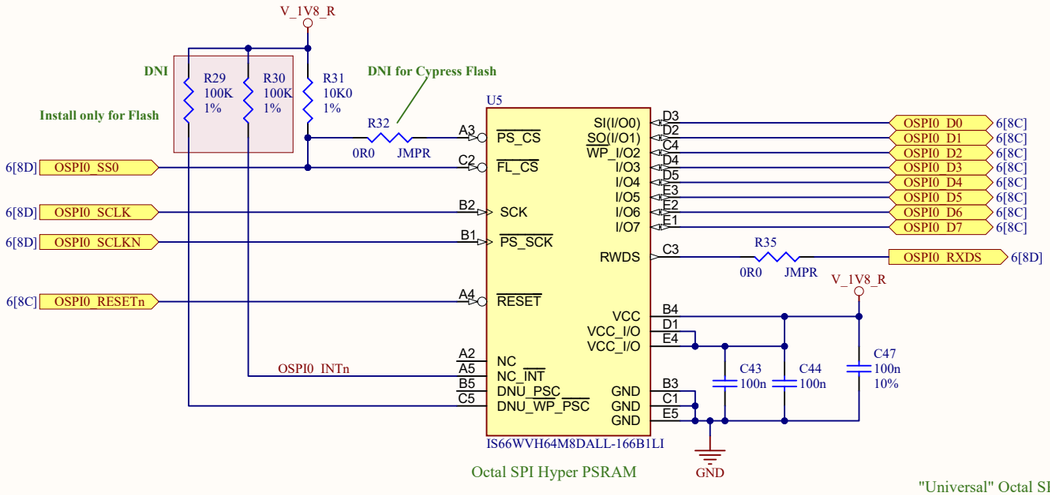
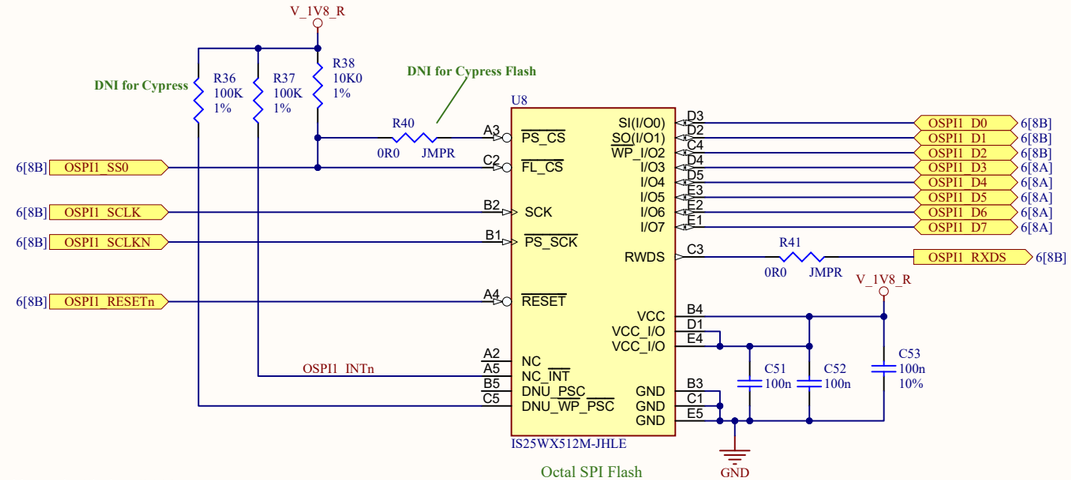
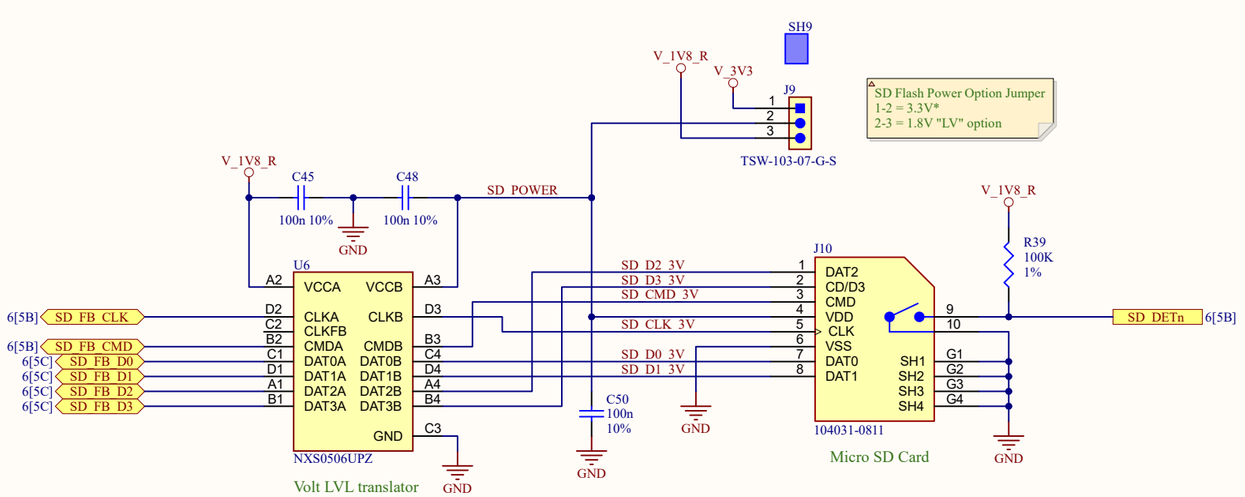




"Universal" Octal SPI Devices. Either chip can be Flash or RAM



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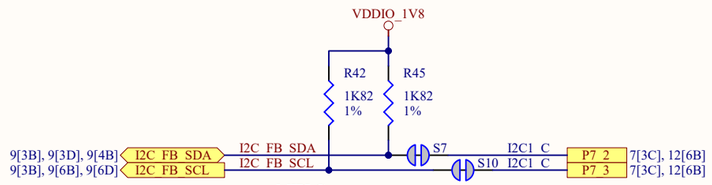
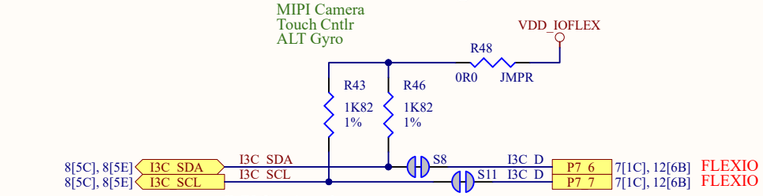
B	none	220-00301	D

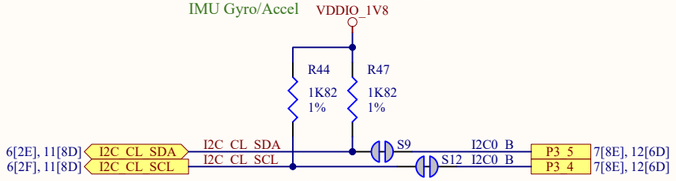
SCALE: none | FILE NAME 5-Memory.SchDoc | SHEET 5 OF 12

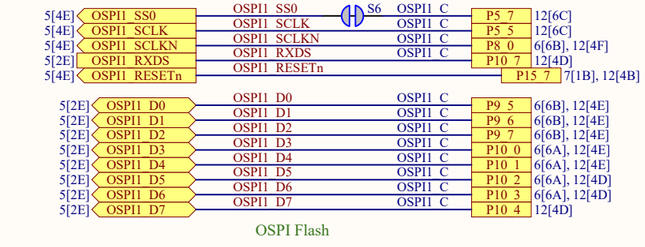
DWG NO 220-00301 REV D SHT 5

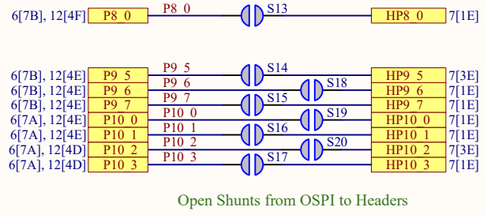
REVISION	DESCRIPTION	DATE	APPROVED

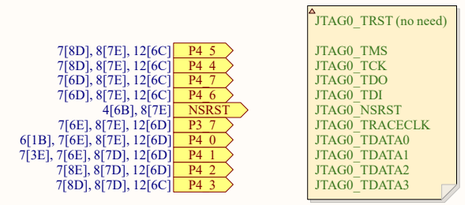


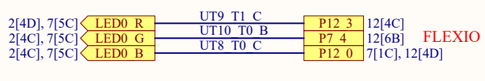


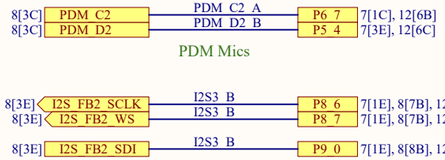


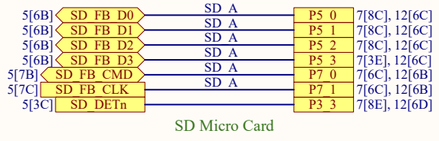


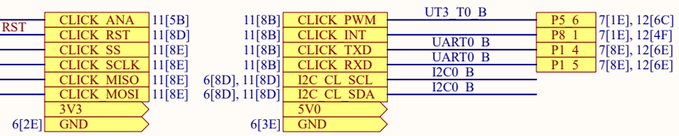


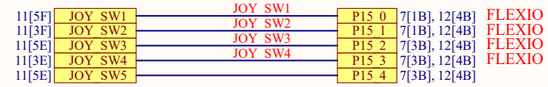


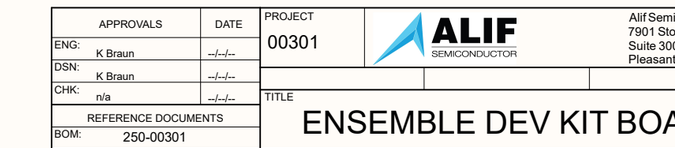


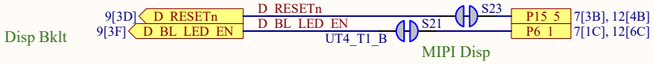


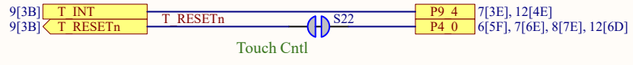












APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00301
ASSY DWG:	120-00301
FAB DWG:	210-00301
PCB DWG:	110-00301-D

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SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

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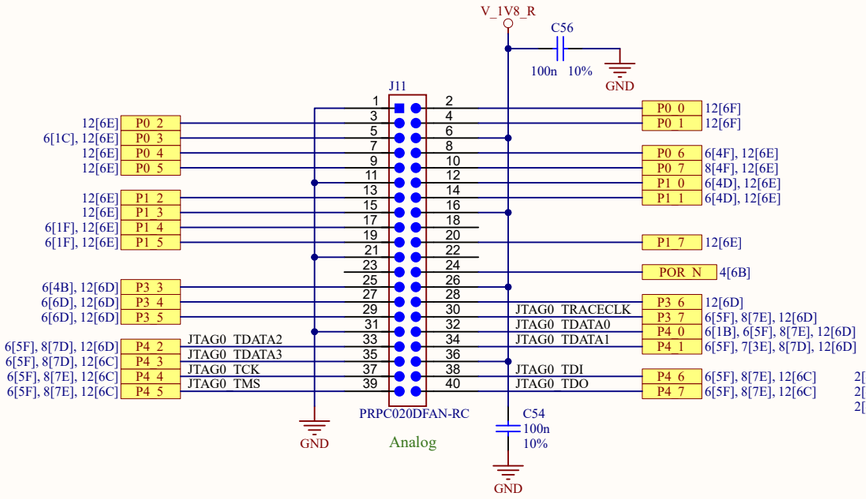
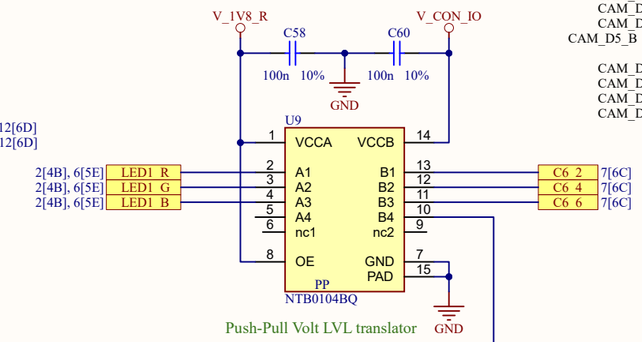
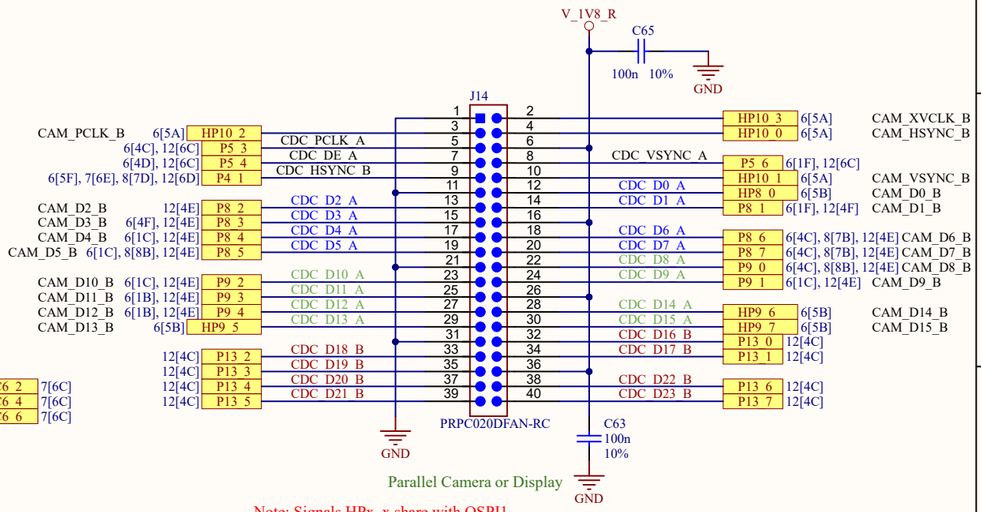
220-00301 DWG. NO. | D REV | 6 SHT

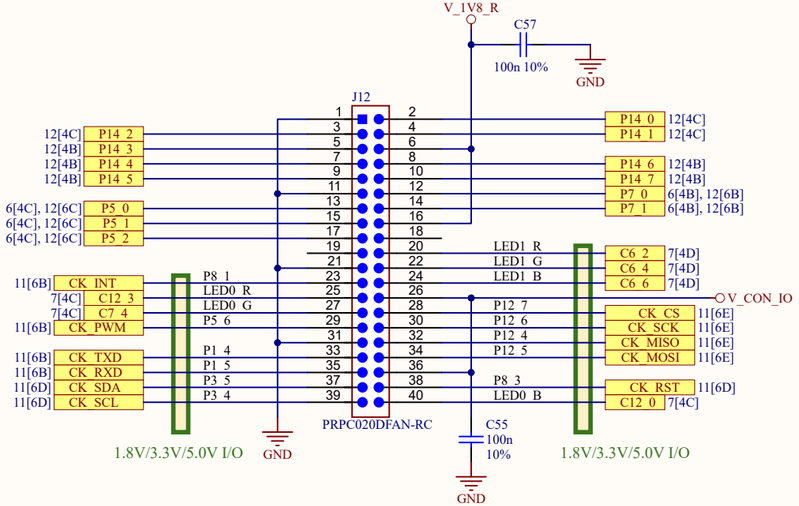
REVISION	DESCRIPTION	DATE	APPROVED

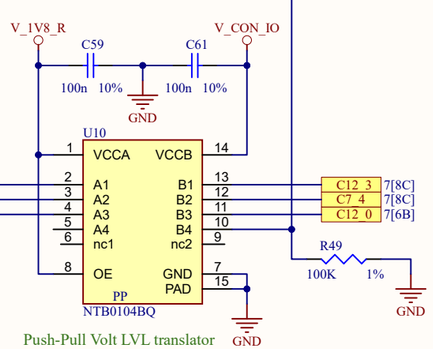


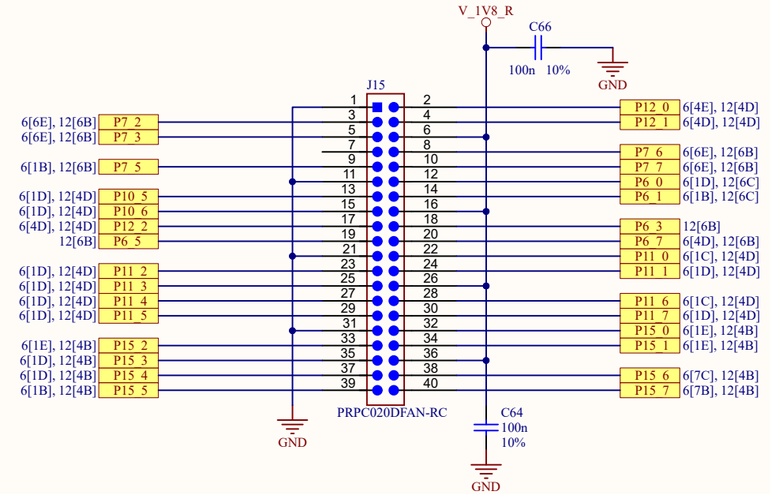


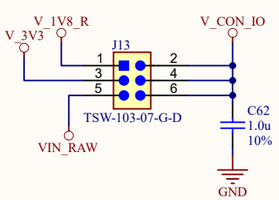


Note: Signals HPx_x share with OSPI1
Shunts need to be soldered before signal(s) is/are available









SH13 J11 1-2 Jumper

Connector I/O Voltage
1-2 = 1.8V
3-4 = 3.3V
5-6 = 5.0V

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00301
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FAB DWG:	210-00301
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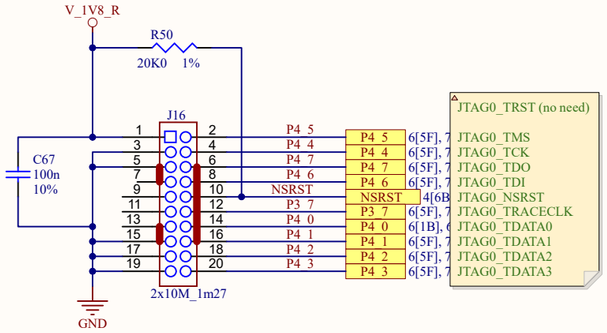
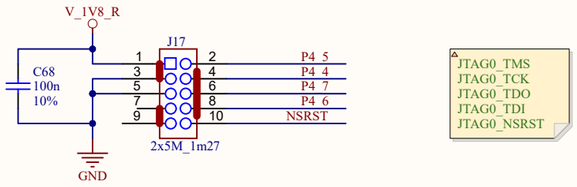
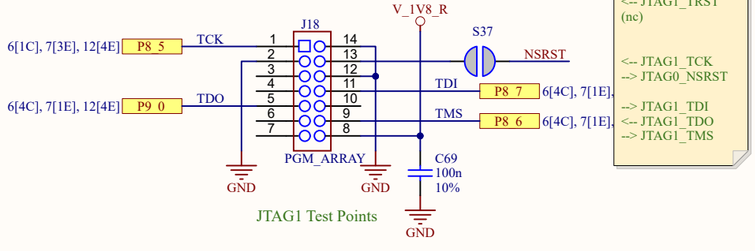
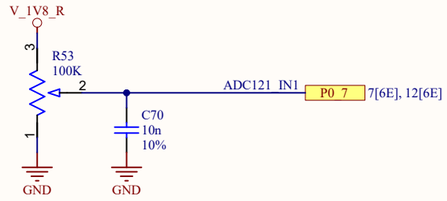


JTAG Debug Connectors

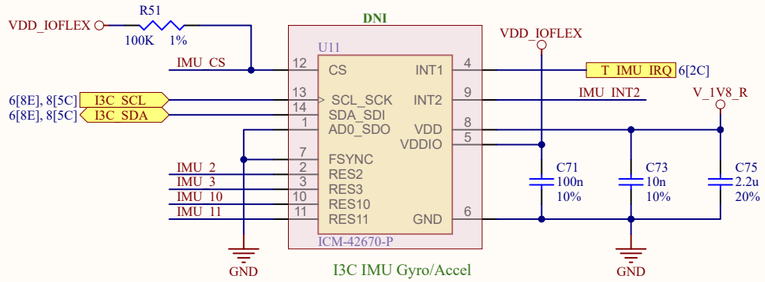




JTAG1 Test Points

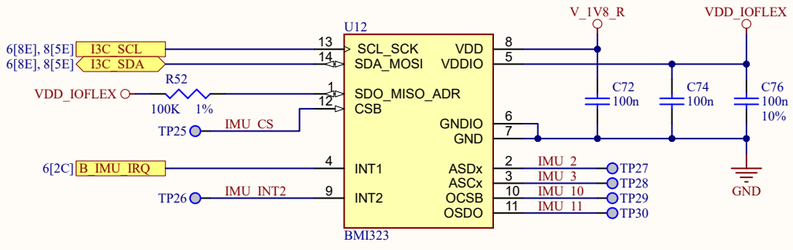


Analog Variable Resistor



I3C IMU Gyro/Accel

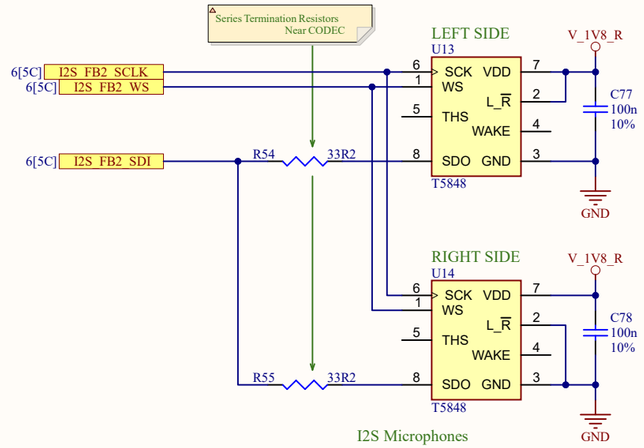
I2C Address:
AD0
0 7-bit = 0x68, 8-bit = 0xD0*
1 7-bit = 0x69, 8-bit = 0xD2



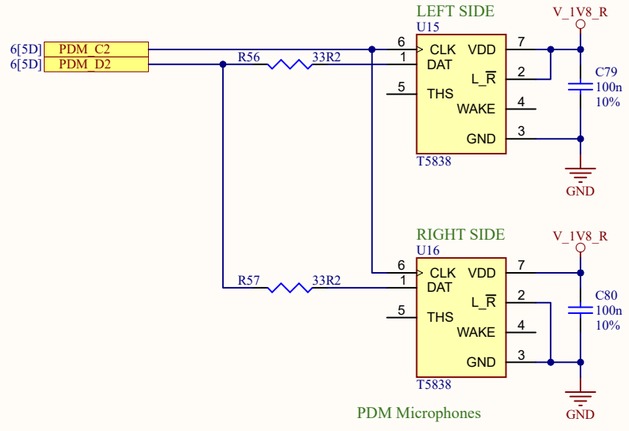
I2C Address:
SDO_MISO_ADR
0 7-bit = 0x68, 8-bit = 0xD0
1 7-bit = 0x69, 8-bit = 0xD2*

Table 29: Mapping of the secondary interface pins

Pin#	Name	I/O Type	Description	Connect to (secondary IF)		
				in SPI4W	in SPI3W	in I2C
2	ASDx	Digital I/O	Secondary Magnetometer interface	MOSI	SISO	SDA
3	ASCx	Digital I/O	Secondary Magnetometer interface	SCK	SCK	SCL
10	OCSB	Digital in	Secondary OIS interface	CSB	CSB	DNC
11	OSDO	Digital out	Secondary OIS interface	MISO	DNC	DNC



I2S Microphones



PDM Microphones

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--
REFERENCE DOCUMENTS	
BOM: 250-00301	
ASSY DWG: 120-00301	
FAB DWG: 210-00301	
PCB DWG: 110-00301-D	

PROJECT 00301

ALIF SEMICONDUCTOR

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7901 Stoneridge Drive
Suite 300
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TITLE

ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none FILE NAME 8-SensorsAndJTAG.SchDoc SHEET 8 OF 12

DWG NO 220-00301 REV D 8

REVISION	DESCRIPTION	DATE	APPROVED

Off by Default

6[2B] C_EN_MIPI_PWR — C_EN_MIPI_PWR

VIN_RAW — C81 1.0u 10% — U17 NCV8164ASNADJT1G (VIN, GND, EN, OUT, ADJ) — TP32 — V_1V2 — C83 10u 10% — GND

1.2V LDO

VIN_RAW — C82 1.0u 10% — U18 NCV8164ASNADJT1G (VIN, GND, EN, OUT, ADJ) — TP31 — V_2V6V8 — C84 10u 10% — R60 23K7 1% — R59 150K 1% — R61 20K0 1% — R58 100K 1% — SH19 — J19 TSW-103-07-G-S

2.6V / 2.8V LDO

J18 2-3 Jumper

2.6V / 2.8V LDO Power:
1-2 = 2.8V
2-3 = 2.6V *

MIPI Camera Power Supplies

MIPI Camera Datasheet: ARX3A0/D (page 21)

www.onsemi.com

TIMING SPECIFICATIONS
Power−Up Sequence
The recommended power−up sequence for ARX3A0 is showed in Figure 21. the available power supplies must have the separation specified below.
1. Set XSHUTDOWN LOW.
2. Power up VDD_IO (1.8 V only)
3. After 1−500 ms, power up VDD, VDD_ANA, VDD_PLL VDD_PHY (1.2 V) and VAA, VAA_PIX (2.7 V) (any order).
4. Apply EXTCLK (can be applied anytime).
5. After 1−500 ms, set XSHUTDOWN.
6. HOST configuration through I2C (PLL, output, etc).
7. Set stream = 1 (R0x301A[2]).
8. PLL internally enables and locks.
9. ARX3A0 enters streaming mode.

V_2V6V8: C85 2.2u 20%, C86 2.2u 20%, C87 2.2u 20%, C88 10u 10%

V_1V2: C89 2.2u 20%, C90 10u 10%

V_1V8_R: C91 2.2u 20%, C92 10u 10%

VIN_RAW: C93 2.2u 20%, C94 100n 10%

6[3B] D_BL_LED_EN

L2 22u 20% 700mA 350m 4x4x2mm — D13 40V 1A SOD123 — C100 2.2u 20% — BL_LED_A

U19 CAT4139TD-GT3 (VIN, SW, SHDN, GND, FB) — R65 100K 1% — R70 1K00 1% — R71 7R50 1% — J24 TSW-103-07-G-S — BL_LED_K

Display LED Backlight

V_1V8_R: C95 10u 10%; V_3V3: C96 100n 10%, C97 100n 10%, C99 10u 10%

J20 BM20B(0.8)-34DS-0.4V(51)

6[2C], 9[6B] C_FLASH — CAM_VSYNC_A
6[8E], 9[3B], 9[6B] I2C_FB_SCL

CAM_HSYNC_A — C_TRIGGER 6[2B], 9[4B]; C_RESETn 6[2C], 9[4B]; I2C_FB_SDA 6[8E], 9[3B], 9[4B]

R62 10K0 1%

4[4E], 9[6B] MIPI_CSI_C_N / MIPI_CSI_C_P — TP34 TP36

4[4E], 9[6B] MIPI_CSI_0_N / MIPI_CSI_0_P — TP33 TP35

MIPI_CSI_1_N 4[4E], 9[4B]; MIPI_CSI_1_P 4[4E], 9[4B] — TP37 TP38

C_XVCLK 6[2C], 9[4B]

MCAM_I2C — R63 10K0 1% — V_1V8_R

R64 0R0 JMPR — DNI

"Selfie" MIPI Camera

MIPI Camera I2C Address Option:
Pin 34:
1.8V: 7-bit = 0x37, 8-bit = 0x6E
GND: 7-bit = 0x36, 8-bit = 0x6C

J22 FH52-20S-0.5SH (MT1, MT2)

BL_LED_K — BL_LED_A

6[3B] D_RESETn — R69 10K0 1%

4[4E] MIPI_DSI_1_P / MIPI_DSI_1_N

4[4E] MIPI_DSI_C_P / 4[4D] MIPI_DSI_C_N

4[4E] MIPI_DSI_0_P / 4[4E] MIPI_DSI_0_N — TP39 TP40 TP41 TP42 TP43 TP44

MIPI Display

With Bottom Entyr FPC's
- Pin order is reversed from LCD

J21 BM20B(0.8)-34DS-0.4V(51)

6[2C], 9[6D] C_FLASH — 6[8E], 9[3B], 9[6D] I2C_FB_SCL

C_TRIGGER 6[2B], 9[3D]; C_RESETn 6[2C], 9[3D]; I2C_FB_SDA 6[8E], 9[3B], 9[3D]

4[4E], 9[6D] MIPI_CSI_C_N / MIPI_CSI_C_P

4[4E], 9[6D] MIPI_CSI_0_N / MIPI_CSI_0_P

MIPI_CSI_1_N 4[4E], 9[3D]; MIPI_CSI_1_P 4[4E], 9[3D]

C_XVCLK 6[2C], 9[3C]

MCAM_I2C

"Standard" MIPI Camera

V_1V8_R — R68 10K0 1% — C98 2.2u 20% — V_3V3

6[8E], 9[6B], 9[6D] I2C_FB_SCL
6[8E], 9[3D], 9[4B] I2C_FB_SDA

T_INT_3V3

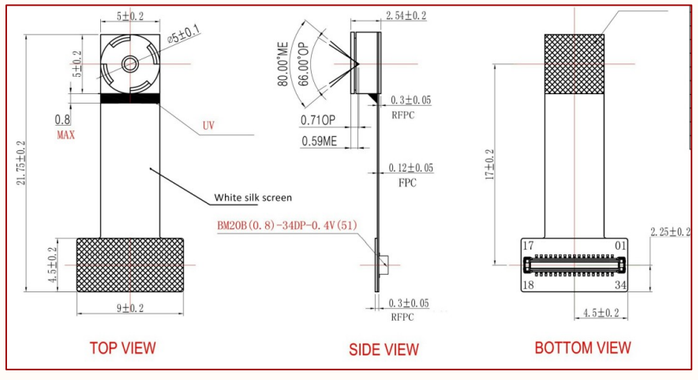
6[3B] T_RESETn

6[3B] T_INT — R66 4K75 1% — R67 4K75 1% — DNI

J23 FH52-8S-0.5SH (MT1, MT2)

Touch Control

Touch Controller I2C Address:
INT at power-up:
1 7-bit = 0x14, 8-bit = 0x28
0 7-bit = 0x5D, 8-bit = 0xBA



APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00301
ASSY DWG:	120-00301
FAB DWG:	210-00301
PCB DWG:	110-00301-D

PROJECT 00301

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7901 Stoneridge Drive
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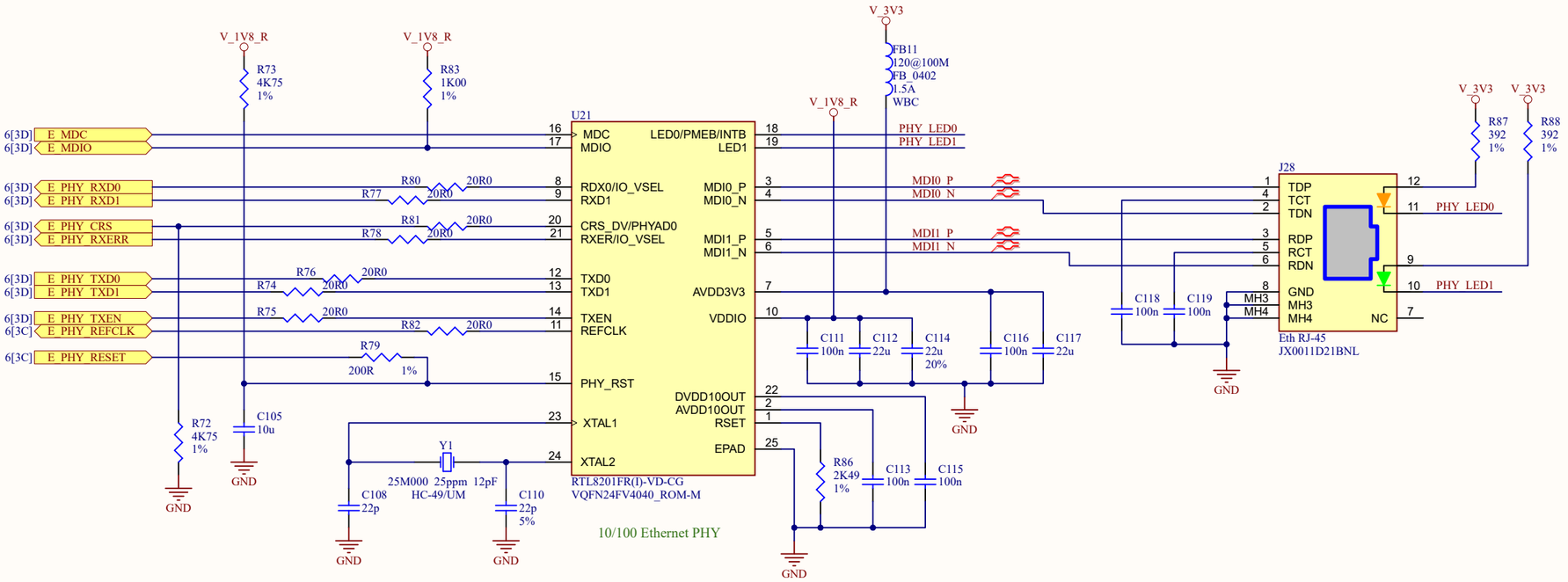
Pleasanton, CA 94588 USA

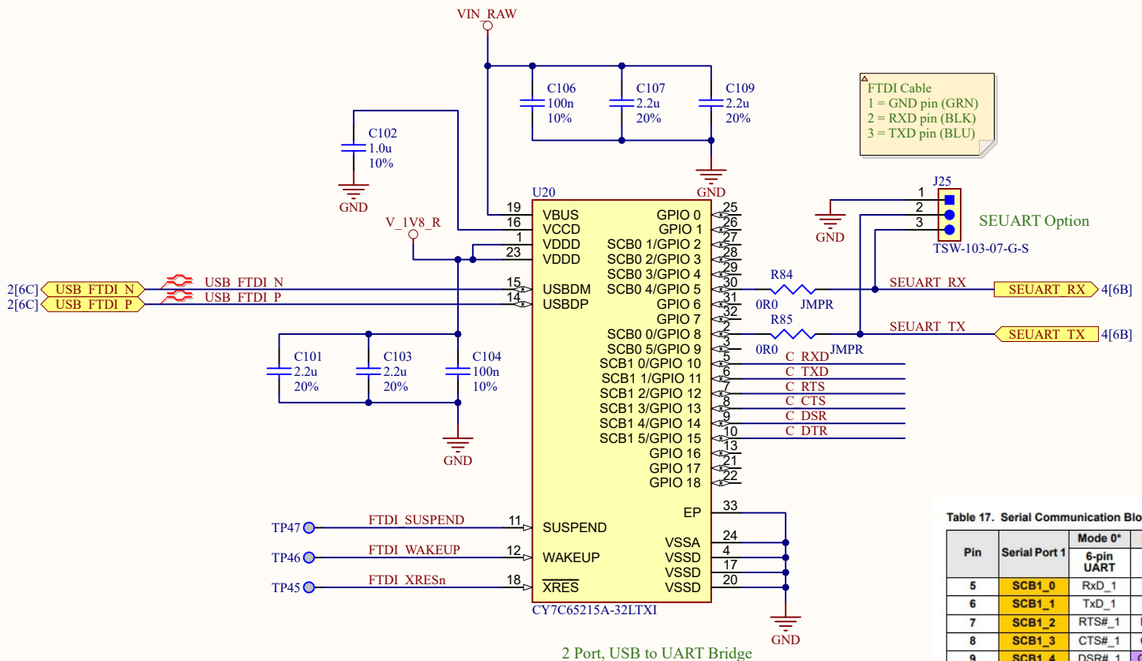
TITLE: ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none FILE NAME 9-MIPI.SchDoc SHEET 9 OF 12

REVISION	DESCRIPTION	DATE	APPROVED





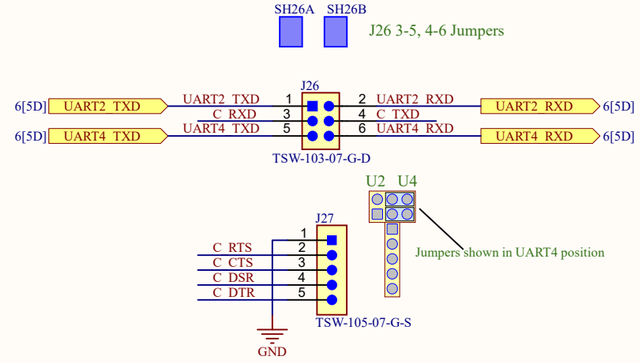


Table 17. Serial Communication Block (SCB1) Configuration

Pin	Serial Port 1	Mode 0*	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
		6-pin UART	4-pin UART	2-pin UART	SPI Master	SPI Slave	I^2C Master	I^2C Slave	JTAG Master
5	SCB1_0	RxD_1	RxD_1	RxD_1	MISO_IN_1	MISO_OUT_1	SCL_OUT_1	SCL_IN_1	TDO
6	SCB1_1	TxD_1	TxD_1	TxD_1	MOSI_OUT_1	MOSI_IN_1	SDA_1	SDA_1	TDI
7	SCB1_2	RTS#_1	RTS#_1	GPIO_12	SSEL_OUT_1	SSEL_IN_1	GPIO_12	GPIO_12	TMS
8	SCB1_3	CTS#_1	CTS#_1	GPIO_13	SCLK_OUT_1	SCLK_IN_1	GPIO_13	GPIO_13	TCK
9	SCB1_4	DSR#_1	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	GPIO_14	TRST#
10	SCB1_5	DTR#_1	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15	GPIO_15

*Note: Device configured in Mode 0 as default. Other modes can be configured via Cypress-supplied configuration utility.

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM: 250-00301
ASSY DWG: 120-00301
FAB DWG: 210-00301
PCB DWG: 110-00301-D

PROJECT 00301

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7901 Stoneridge Drive
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TITLE

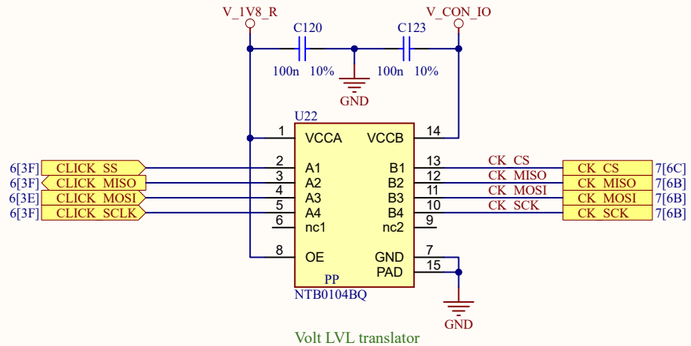
ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

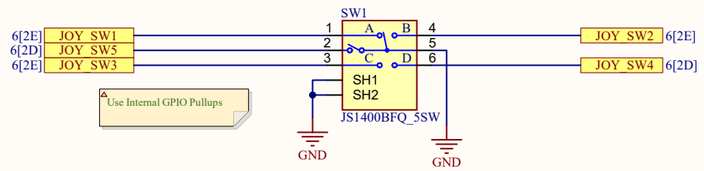
SCALE: none | FILE NAME 10-Eth_FTDI.SchDoc | SHEET 10 OF 12

DWG NO. 220-00301 REVISION D 10

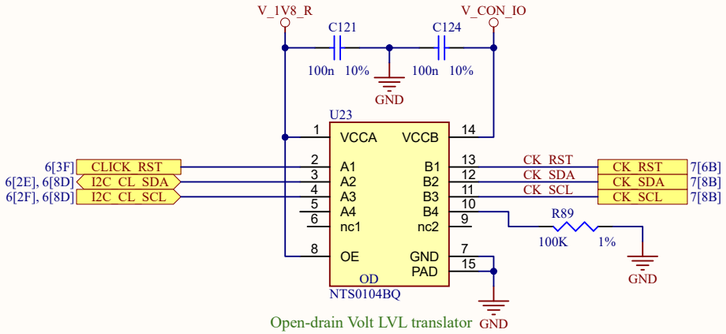
REVISION	DESCRIPTION	DATE	APPROVED



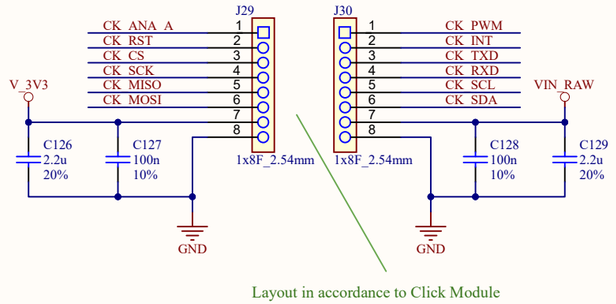
Volt LVL translator



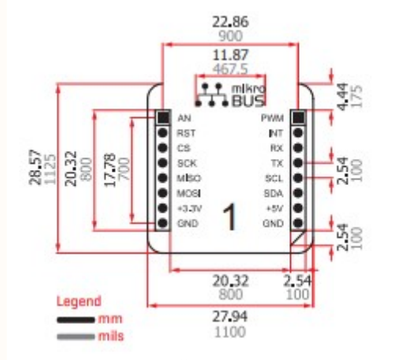
Navigation Buttons



Open-drain Volt LVL translator



Layout in accordance to Click Module



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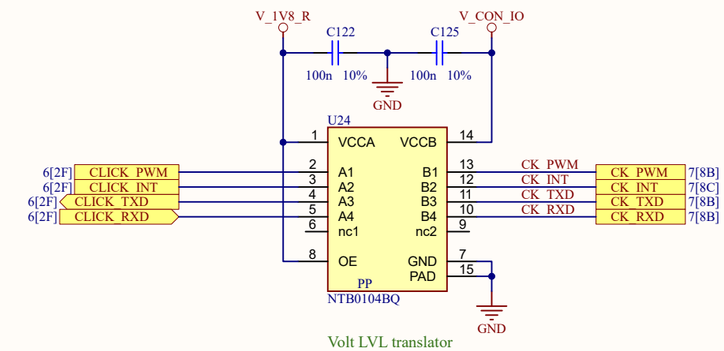
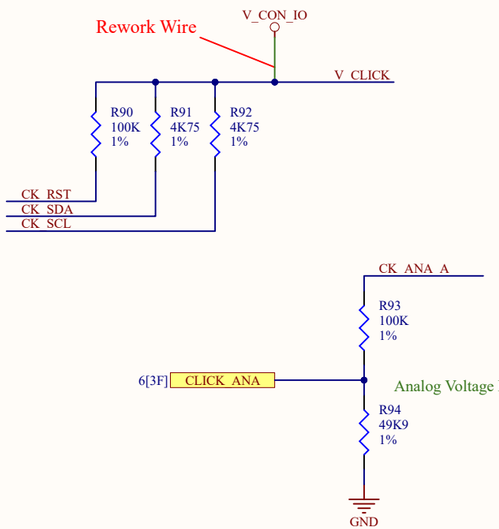


Volt LVL translator



Analog Voltage Divider from 3.3V / 5V

APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00301
ASSY DWG:	120-00301
FAB DWG:	210-00301
PCB DWG:	110-00301-D

PROJECT 00301

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7901 Stoneridge Drive
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Pleasanton, CA 94588 USA

TITLE

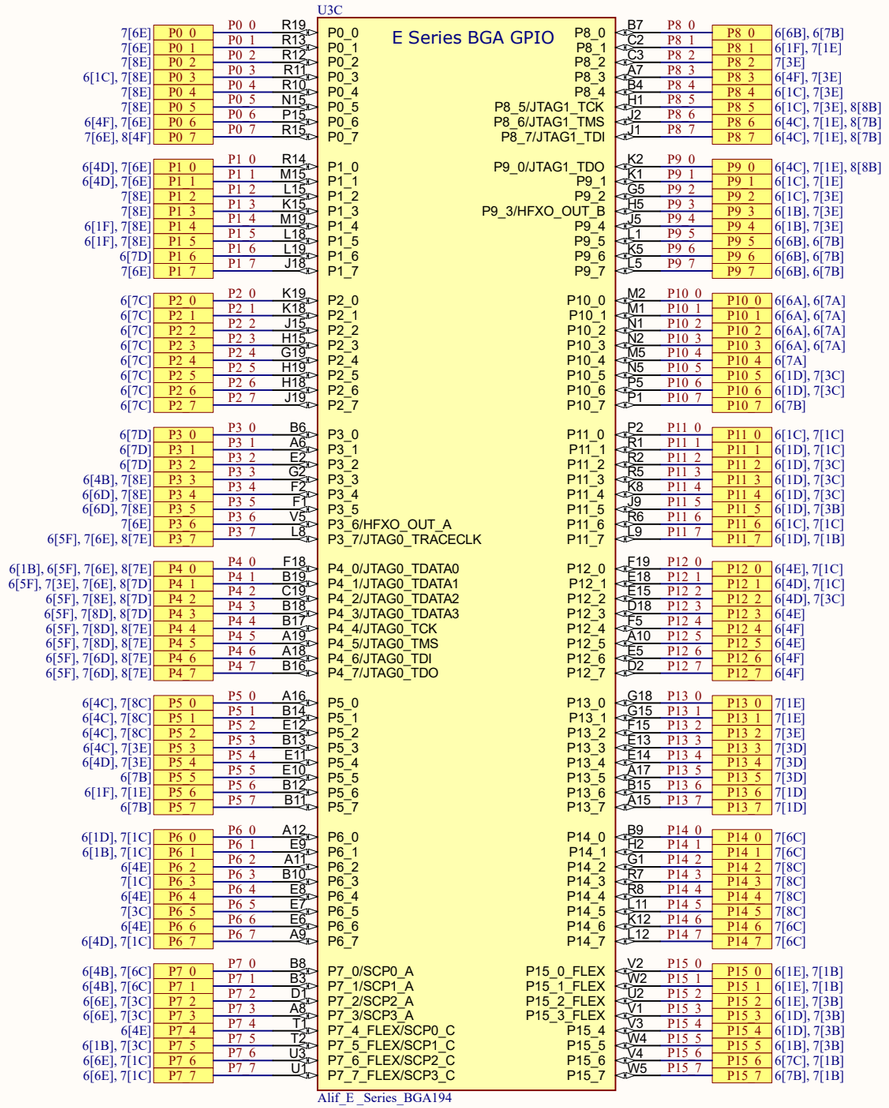
ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none | FILE NAME 11-Click.SchDoc | SHEET 11 OF 12

DWG NO. 220-00301 REV D 11

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: K Braun	--/--/--
DSN: K Braun	--/--/--
CHK: n/a	--/--/--

REFERENCE DOCUMENTS

BOM:	250-00301
ASSY DWG:	120-00301
FAB DWG:	210-00301
PCB DWG:	110-00301-D

PROJECT 00301

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TITLE

ENSEMBLE DEV KIT BOARD

SIZE	CAGE CODE	DWG NO.	REV
B	none	220-00301	D

SCALE: none FILE NAME 12-CPU_GPIO.SchDoc SHEET 12 OF 12

DWG NO 220-00301 REV/SHT D 12