AN4962

SAM9X75 Hardware Design Considerations

Scope

This document is intended to facilitate the bring-up of any hardware design featuring a SAM9X75 MPU by providing a short checklist intended for the hardware designer.

Abbreviations

- SDRAM – Synchronous Dynamic Random-Access Memory
- DDR – Double Data Rate
- PCB – Printed Circuit Board

References

Type	Name	Literature No.	Available
Data sheet	SAM9X7 Series	DS60001813	www.microchip.com
Data sheet	MCP16501	DS20006388	ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/MCP16501-Data-Sheet-DS20006388.pdf
Data sheet	MCP16502	DS20006275	ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/MCP16502-Data-Sheet-DS20006275.pdf

1. Design Checklists

1.1 Schematic Checklist

- Is the MPU supplied with the correct voltage levels?
- Does the power management IC provide enough current for the system?
- Are the correct power supply power-up and power-down sequences implemented?
- Are the decoupling capacitors adequate?
- Is the MPU configured correctly?
- Is the DDR controller configured correctly?

1.2 Layout Checklist

- Does the board feature an uninterrupted GND plane?
- Is a proper layer stack-up defined?
- Are the decoupling capacitors placed as close as possible to the IC pins?
- Are high-speed signal lengths matched and routed over continuous planes (USB, SDCARD, DDR, etc.)?

2. Schematic Checklist Description and Examples

This section describes each item in the schematic checklist and provides implementation examples.

2.1 Provide Adequate Voltage and Sufficient Current

2.1.1 Requirements

Refer to the table “Recommended Operating Conditions on Power Supply Inputs”, in the Electrical Characteristics chapter of the SAM9X7 Series data sheet, for the power supplies needed to power the MPU.

The MPU requires only a few voltage supplies which can be split into three main categories:

- Core: VDDCORE (1.15V/1.2V depending on the working frequency)
- Memories: VDDNF (1.8V/3.3V), VDDQSPI (1.8V/3.3V), VDDIOM (1.35V/1.5V/1.8V depending on the SDRAM)
- Peripherals: VDDANA (3.3V), VDDIOP[0,2] (1.8V/3.3V), VDDIN33 (3.3V), VDDBU (1.6V-3.6V)

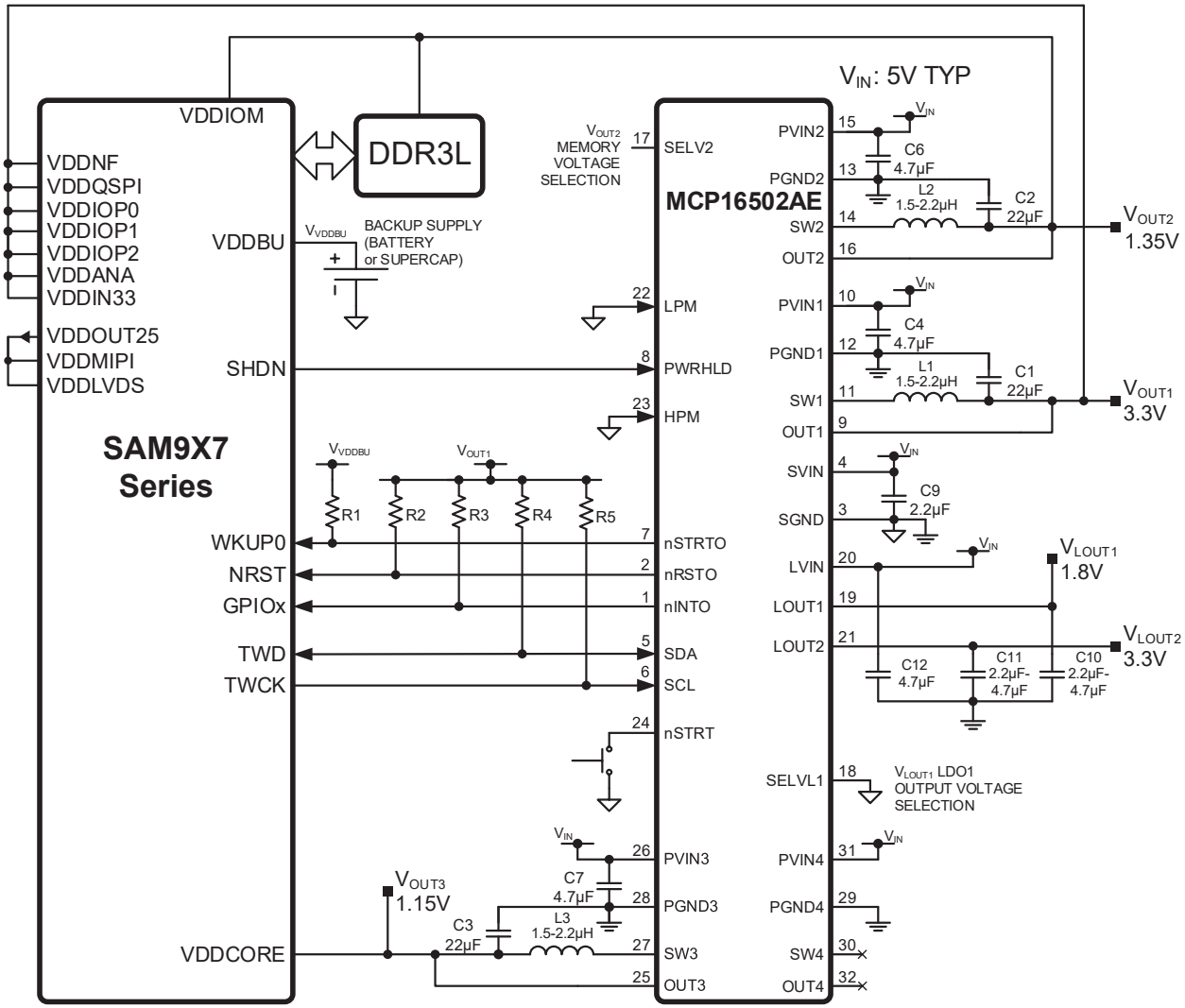
The same power supply can be used to power several MPU power rails. For example, the same 3.3V supply can be used to power VDDANA, VDDIOP0, VDDIOP1 and VDDBU.

VDDMIPI and VDDLVDS are supplied by the internal LDO of the MPU, which outputs 2.5V on the VDDOUT25 pin.

2.1.2 Recommended Power Implementations

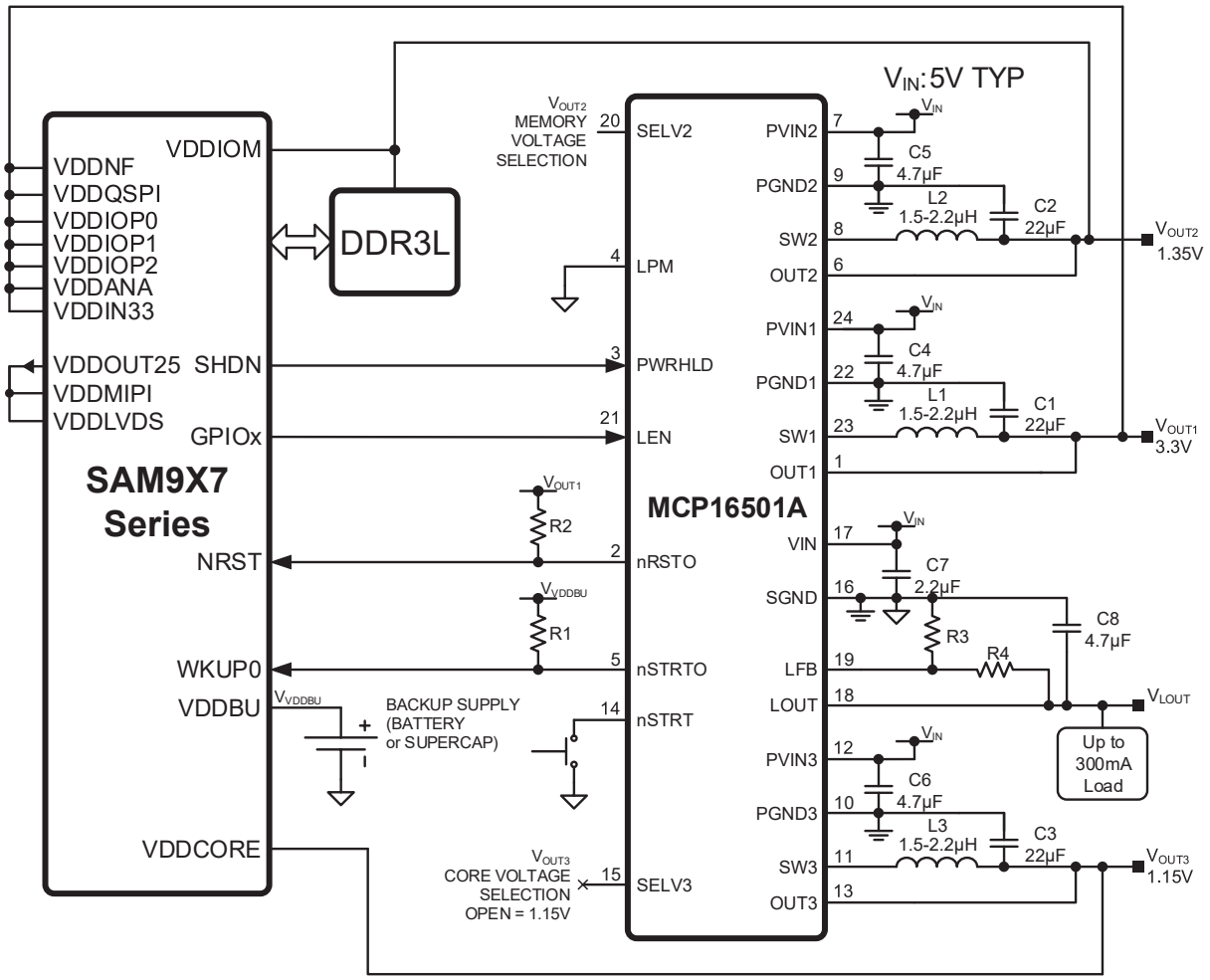
MCP16502 and MCP16501 are multi-channel Power Management Integrated Circuits (PMICs) recommended for the SAM9X7.

Figure 2-1. MCP16502 Simplified Application Block Diagram



MCP16502 features four 1A DC-DC buck regulators and two 0.3A auxiliary LDO regulators, and provides a comprehensive interface to the MPU, which includes an interrupt flag and a 1-MHz I²C interface. The two LDO regulator outputs LOUT1 and LOUT2 are auxiliary power rails available for the application. LOUT1 output is on by default at power-up and its default voltage is set to 1.8V, 2.5V or 3.3V depending on the SELV1 pin connection. Buck4 and LOUT2, off by default at power-up, can be started by software through the I²C control bus to the necessary voltage.

Figure 2-2. MCP16501 Simplified Application Block Diagram



MCP16501 is a 4-channel PMIC designed for PCB area constrained applications. In a 4x4mm QFN24 package, it features three 1A DC-DC buck regulators and one 0.3A auxiliary LDO regulator, and provides a simple, leakage-free interface with SAM9X7. The 3.3V, 1.35V/1.5V/1.8V and 1.15V supply rails are fed from DC-DC converters for maximum efficiency. The LDO regulator output LOUT is controlled with the LEN input and its output voltage is set with a resistive divider.

For further details, refer to the MCP16501 and MCP16502 documentation. See References.

2.2 Ensure Correct Power-Up and Power-Down Sequences

2.2.1 Requirements

In the section “Recommended Power Supply Sequencing”, in the Electrical Characteristics chapter of the SAM9X7 Series data sheet, refer to the figures “Recommended Power Sequence at Power-Up” and “Recommended Power Sequence at Power-Down” for the applicable power supply sequencing.

The Power-Up Timing Requirements table shows the following:

- VDDBU must be established within 0.2 ms after VDDIN33 is established.
- VDDIN33 must be stable for at least 0.1 ms before the periphery group (VDDIOM, VDDLVDS, VDDQSPI, VDDNF, VDDIOPx) gets established.

- VDDCORE must be established after the periphery group.
- The NRST line must be kept low for at least 8 ms after all other power supplies have become stable.

The Power-Down Timing Requirements table shows the following:

- The NRST line must be pulled low before the power supplies are powered off and there is no specific order and no specific timing required among the channels.

2.2.2 Implementation Example

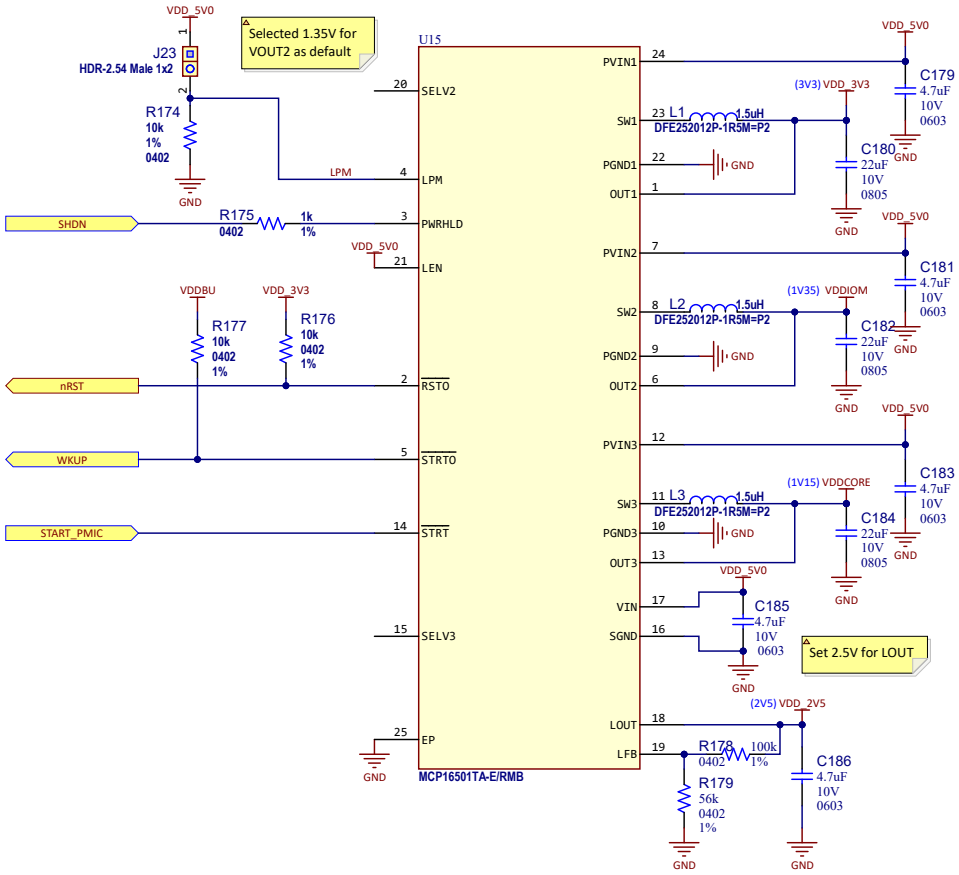
The low cost and space saving option to power the SAM9X75 is the MCP16501 PMIC. The current implementation introduces an MCP16501TA-E/RMB schematic configured to supply all necessary power rails(1) in the recommended sequence:

1. 3.3V to the periphery group (default V_{OUT1} output)
2. 1.15V to the MPU core (by leaving pin SELV3 floating in Hi-Z)
3. 1.35V to the VDDIOM rail (by leaving pin SELV2 floating in Hi-Z)

Note:

1. Except for VDDBU, which can be connected to a non-removable power source such as a 3V lithium battery or directly to 3.3V.

Figure 2-3. Power Management Integrated Circuit



2.3 Ensure that the Power Supply Pins have Adequate Decoupling Capacitors

2.3.1 Requirements

As described in the Electrical Characteristics chapter of the SAM9X7 Series data sheet, low impedance decoupling of the device power supply inputs must be provided. A 10 nF to 220 nF ceramic X7R (or X5R) capacitor placed very close to each power supply input is a minimum requirement.

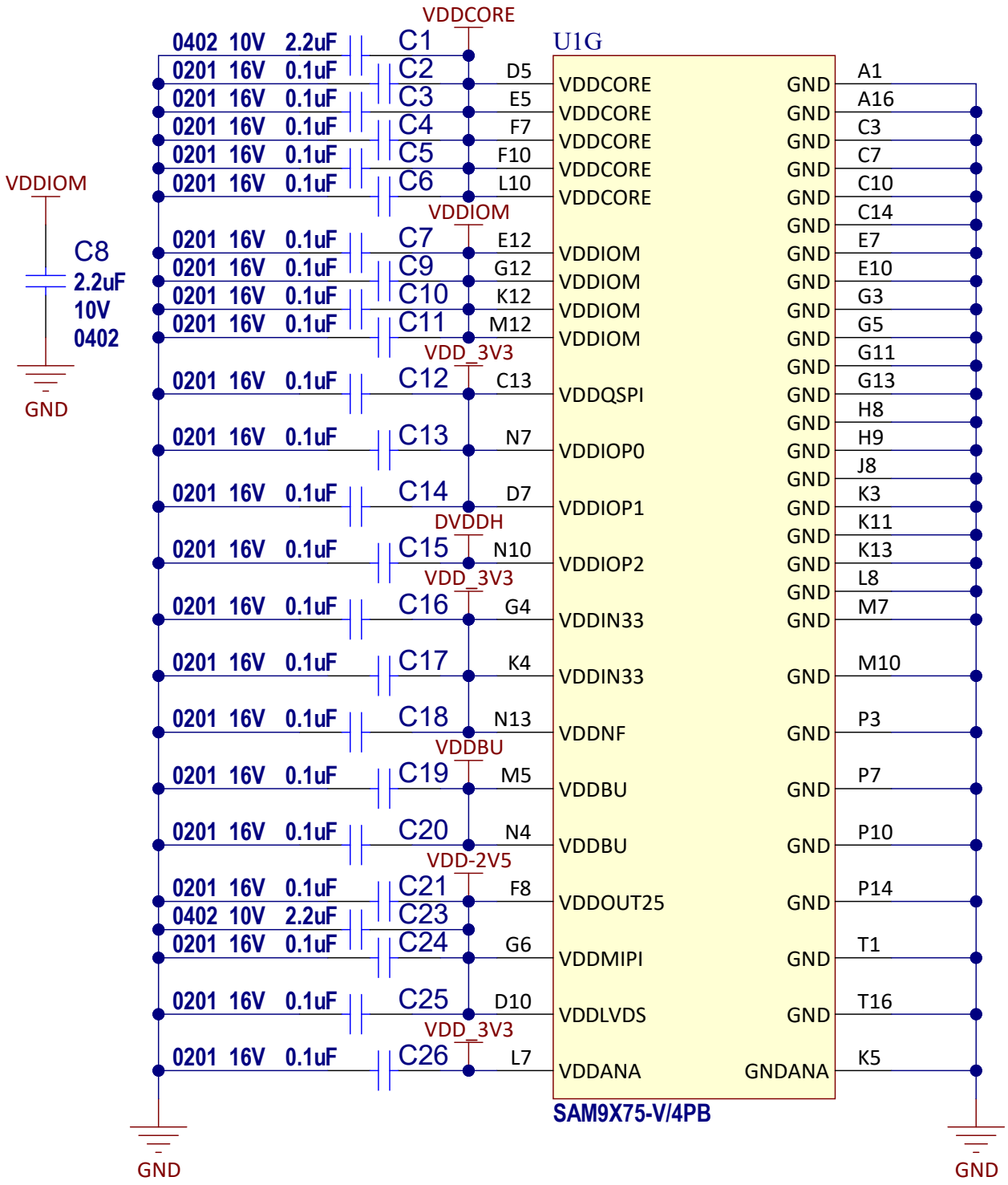
In the example below, 100 nF 0201, X5R rated at 16V multilayer ceramic capacitors were used with good results. Using small footprint capacitors enabled an optimal placement on the bottom of the PCB, very close to vias connected to the power pins of the MPU.

Additionally, the internal LDO that generates VDDOUT25 requires two extra capacitors. As stated in table “VDDOUT25 Voltage Regulator Characteristics” in the SAM9X7 Series data sheet Electrical Characteristics chapter:

- A 2.2 µF (min) capacitor should be connected at its input (at VDDIN33).
- A 1 to 2.7 µF (typ) capacitor should be connected at its output (at VDDOUT25).
- The output capacitor should have a low ESR, between 0.01 and 0.3 ohm.

2.3.2 Implementation Example

Figure 2-4. Processor Power Supplies



In addition to the 100 nF capacitors, 2.2 µF to 10 µF low ESR ceramic capacitors rated at 10V should be implemented on each power rail to serve as bulk/storage elements.

2.4 Check MPU Configuration

2.4.1 Requirements

- A 5.62 kΩ resistor is connected to the RTUNE pin for USB external tuning and a 1% tolerance voltage divider is placed on USB VBUS to transform the 5V into the PIO voltage for VBUS detection.
  → Refer to section “Typical Connection” in the USB High Speed Device Port (UDPHS) and USB Host High Speed Port (UHPHS) chapters of the SAM9X7 Series data sheet.
- The TST pin is grounded.
- The ADVREFN pin is connected to the PCB ground plane.
- If the design does not need JTAG boundary scan, tie the JTAGSEL pin to GND or leave it floating.
- A 32.768 kHz crystal is placed between XIN32 and XOUT32.
  → Refer to section “32.768 kHz Crystal Oscillator” in the Electrical Characteristics chapter of the SAM9X7 Series data sheet.
- A high-frequency clock source is provided either through a crystal placed between XIN and XOUT or through an external clock generator.
- If the clock generator option is chosen, it is recommended to ground XOUT to improve stability.
  → Refer to section “Main Crystal Oscillator” in the Electrical Characteristics chapter of the SAM9X7 Series data sheet.
- Clock sources should be chosen with great care.
  → Refer to section “Crystal Oscillator Design Considerations” in the Electrical Characteristics chapter of the SAM9X7 Series data sheet.

2.4.2 Implementation Example

Figure 2-5. Processor Configuration

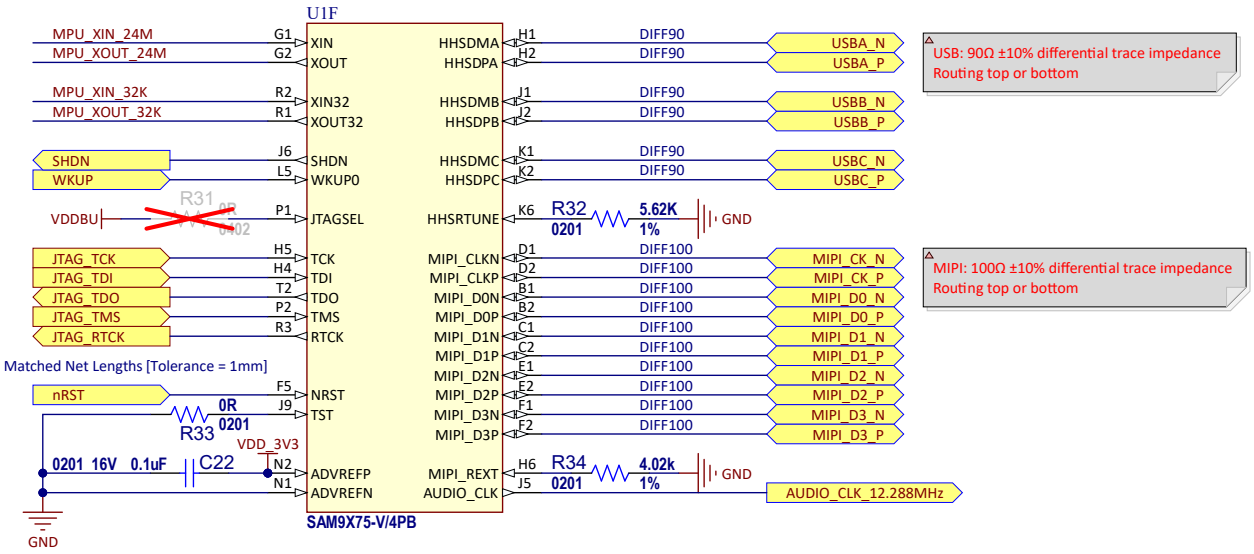
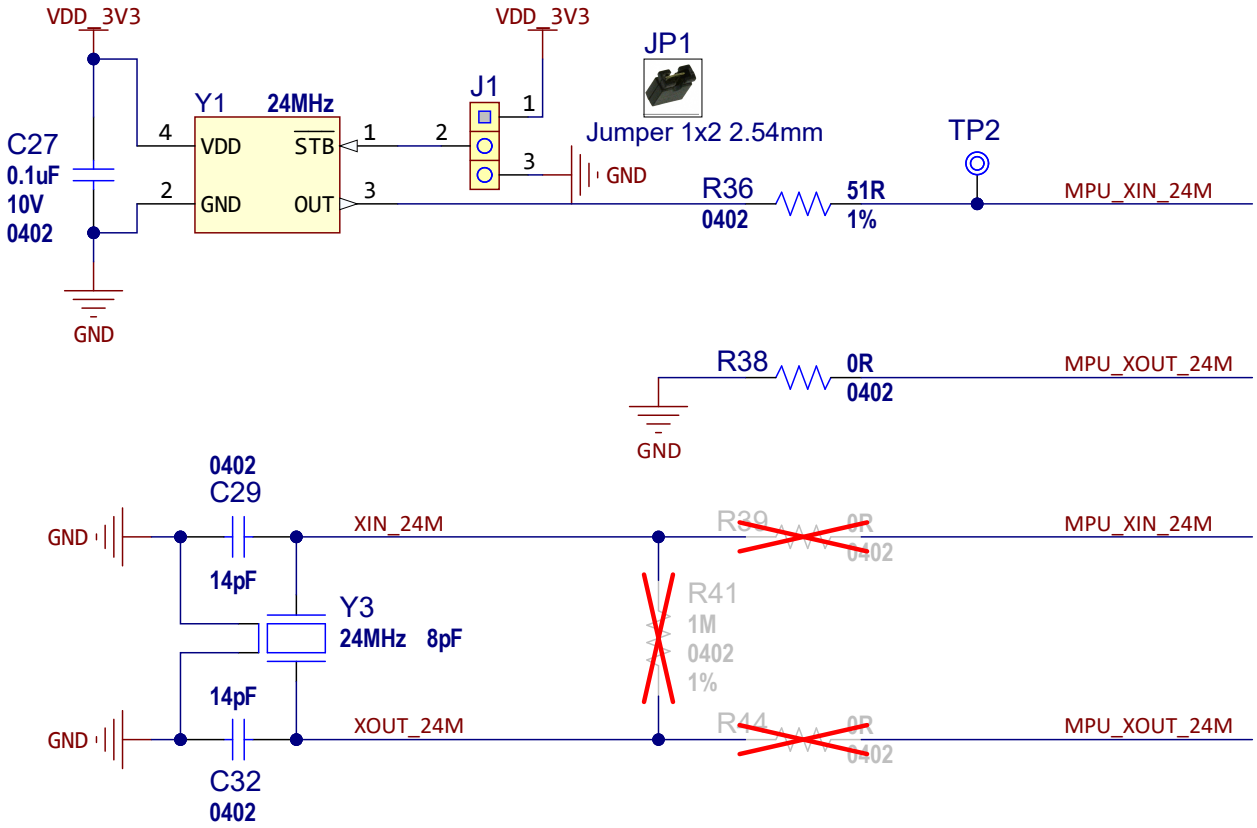


Figure 2-6. Main Oscillator Implementation



Two implementations are possible.

One uses an oscillator, which requires using the Bypass mode of the main crystal oscillator. Prior to bypassing the main crystal oscillator, the XOUT pin must be grounded (using R38, in the above figure), and the external clock frequency provided on the XIN pin must be stable and within the values specified under “Main Crystal Oscillator”, in the section “Electrical Characteristics” of the data sheet.

The other implementation is done with a crystal oscillator, which is more straightforward: one crystal and two capacitors must be grounded.

To select the capacitors, use the following formula:

$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_{PARA} - C_{PCB} / 2)$.

where C_{PCB} is the single-ended (ground-referenced) parasitic capacitance of the PCB on the XIN and XOUT tracks.

As an example, if the crystal is specified for an 8 pF load, with C_{PCB} = 1 pF (on XIN and on XOUT):

$C_{LEXT} = 2 \times (8 - 1 - 0.5) = 13$ pF

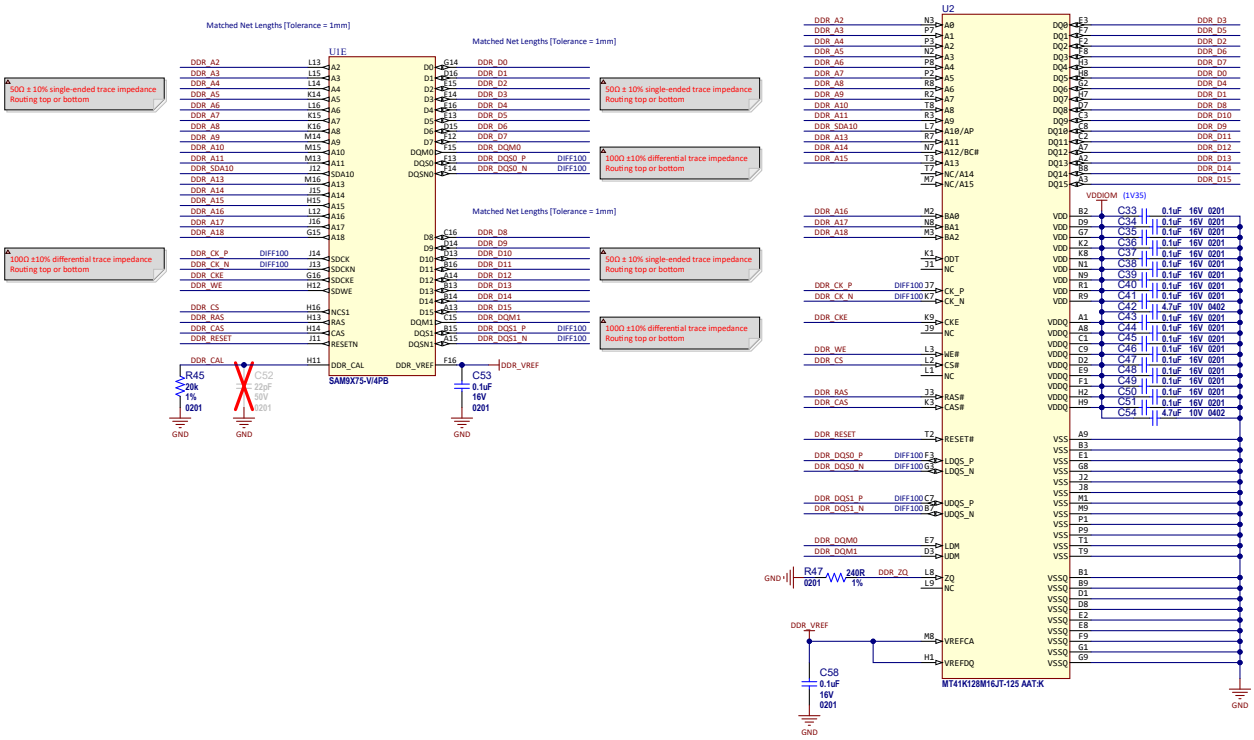
2.5 Check the DDR Controller Configuration

2.5.1 Requirements

- Connect the external memory chosen as required in table “DDR I/O Calibration and DDR Voltage Reference” in the Electrical Characteristics chapter of the SAM9X7 Series data sheet.
- The DDR_CAL pin must be connected to ground via a 20 kΩ high precision calibration resistor, both for DDR2 and DDR3L SDRAM devices.
- Connect the DDR_VREF pin to a filtered high precision voltage divider which outputs VDDIOM/2.

2.5.2 Implementation Example for DDR3L

Figure 2-7. DDR Controller Configuration



In the above figure, the data bits connected to the DDR3L memory appear to be scrambled. This is called “bit swapping” and was done on purpose to ease up the layout routing. Refer to 4.1. Bit and Byte Swapping.

Make sure to define the Clock and DQS signals as differentials with a 100-ohm differential characteristic impedance, in order to export the information to the PCB and route them coupled as required.

3. Layout Checklist Description and Examples

This section describes each item in the layout checklist and provides implementation examples.

The implementation examples are based on a 4-layer adaptation of the SAM9X75-DDR3-EB Early Adopter board (EA14J50A).

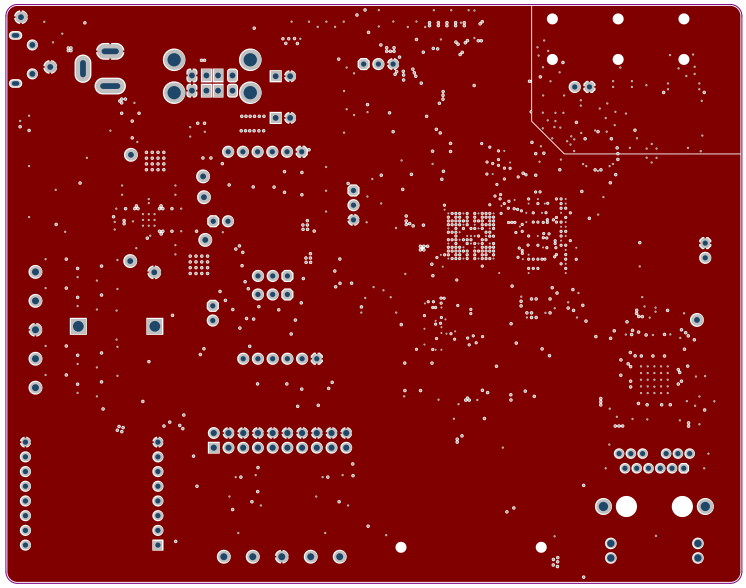
3.1 Check that the Board has an Uninterrupted GND Plane

3.1.1 Requirements

As described in the SAM9X7 Series data sheet Electrical Characteristics chapter, a PCB with a low impedance ground plane must be provided. A single unbroken ground plane is a minimum requirement.

3.1.2 Implementation Example

Figure 3-1. Correct GND Plane



The above figure shows a solid GND plane on layer 2 of the four-layer PCB. This solid ground plane's purpose is to serve as a low impedance return path for the power planes and also as a reference plane and return path for high speed signals. All these factors reduce the board EMI generation.

The only exception to this rule can be seen in the upper right corner of the board where a small plane serves as AGND (analog ground) plane for an audio application. Its existence is application-dependent and only serves as model of how an acceptable split plane looks like. This is acceptable because there are no other signals routed over that area that could capture undesired external ElectroMagnetic Interference (EMI).

3.2 Define a Layer Stack-up so that Line Impedances are Matched to Driver Impedances

3.2.1 Requirements

Match the PCB line impedances to their corresponding driver impedances to reduce line reflections:

- Single-ended lines should have a 50 Ω +/-10% single-ended impedance.
- USB lines should have a 90 Ω +/-15% differential impedance.

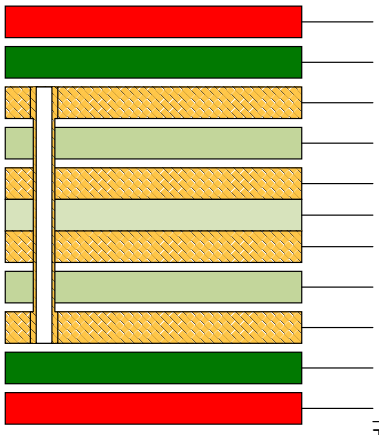
- MIPI, LVDS, DDR CLOCK and STROBE signals should have a 100 Ω +/-10% differential impedance.

3.2.2 Implementation Example

The SAM9X75 was especially engineered to be placed on a four-layer PCB.

To achieve the best performance, we recommend using the following layer stack-up and line width and clearances.

Figure 3-2. Four-Layer Stack-up



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.020mm	Solder Resist	Solder Mask	GTS
Copper	L1 - Top Layer	0.035mm		Signal	GTL
Prepreg		0.085mm		Dielectric	
Copper	L2 - GND	0.035mm		Signal	G1
Core		1.200mm	FR-4	Dielectric	
Copper	L3 - PWR	0.035mm		Signal	G2
Prepreg		0.085mm		Dielectric	
Copper	L4 - Bottom Layer	0.035mm		Signal	GBL
Surface Material	Bottom Solder	0.020mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.560 mm ± 10%

PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L4	L3	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L4	L3	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L4	L3	125	

This stack-up was chosen because it can provide all the required impedances by using minimum 100 µm-wide traces.

The minimum trace width is 100 µm (~4 mil) which is relatively standard nowadays for PCB manufacturers. This also ensures that the routing does not take much space on the board.

3.2.3 Extra Tips

Important: Make sure that your PCB manufacturer can manufacture that specific stack-up.

The PCB manufacturer may not have the required materials in stock, and have to order it specifically, which can increase the overall production cost.

Also, the manufacturer can recommend a different layer stack-up that they can produce cheaper with the materials in stock.

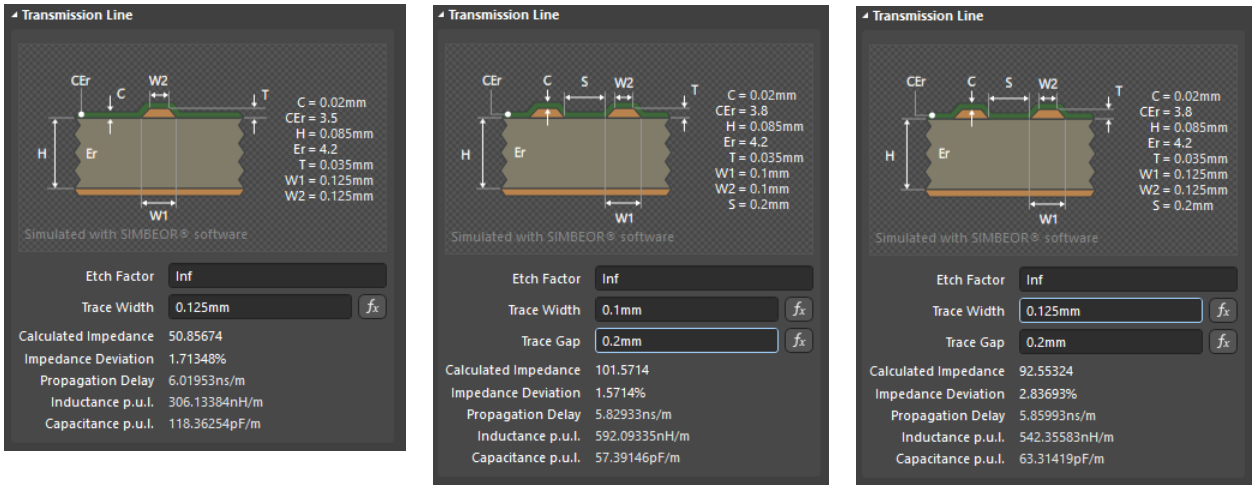
In such cases, you can easily adapt your layout to the proposed stack-up by changing the width of the traces so the required impedances are preserved. With the help of an impedance calculator tool, make sure that the recommendations previously given can still be respected (for example, check that enlarging the traces will satisfy the impedance while not infringing the minimal spacing).

Designing proper transmission lines is easier nowadays with the help of impedance calculators available on the market.

The following example shows the Altium Designer impedance calculator.

Here, after defining the PCB stack-up, you can either use the software to compute the ideal trace width that will yield a specific impedance, or input the trace width so that the tool calculates the resulting impedance.

Figure 3-3. Impedance Calculation



The board used as example in this application note was designed so that the final thickness of the board should be 1.6 mm. In designs that do not have this constraint, we recommend reducing the thickness of the inner core from 1.2 mm to as low as possible. This does not impact the previously calculated trace impedances, but it allows the creation of a better plane capacitor created by the close-neighboring power layer and GND layer. This plane capacitor will then be very efficient to filter high-frequency noise, as it should have a very low ESR.

3.3 Place Decoupling Capacitors as Close as Possible to IC Pins

3.3.1 Requirements

As described in the SAM9X7 Series data sheet Electrical Characteristics chapter, low impedance decoupling of the device power rail inputs must be provided. A 10 nF to 220 nF ceramic X7R (or X5R) capacitor placed very close to each power supply rail is a minimum requirement.

3.3.2 Implementation Example

In the following figure, capacitors are the green rectangles.

Figure 3-4. SAM9X75 Capacitor Placement

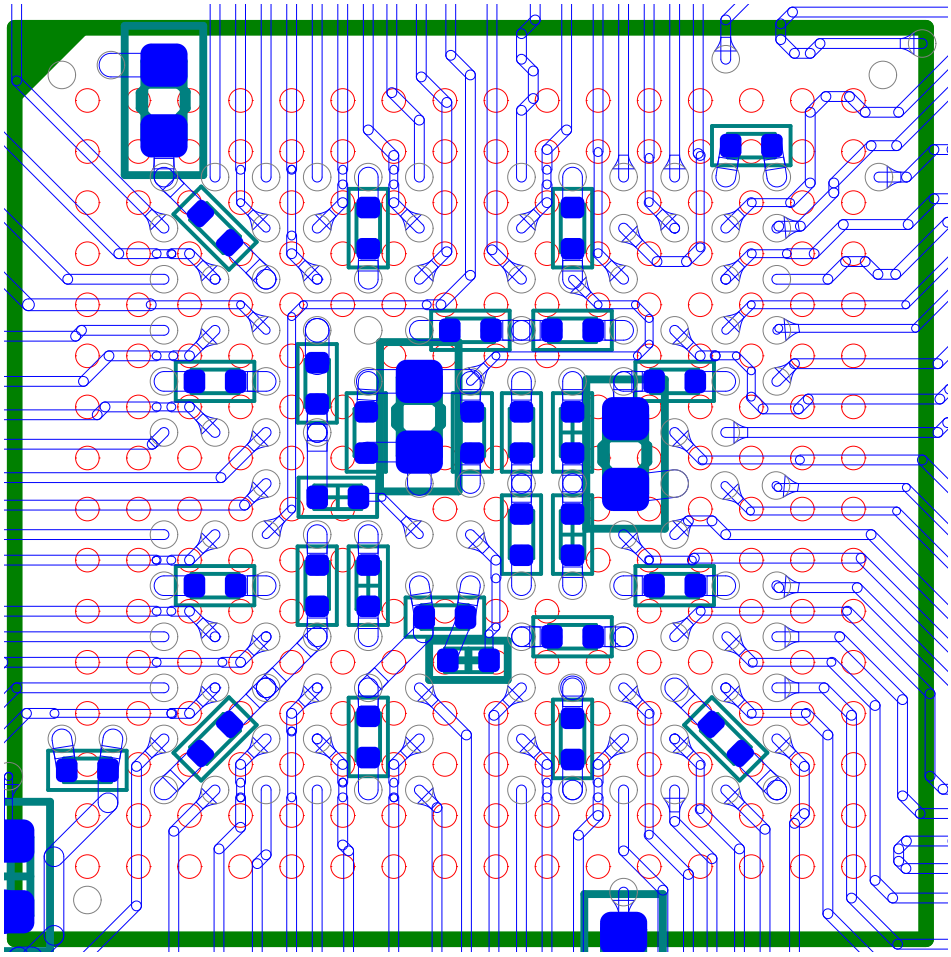
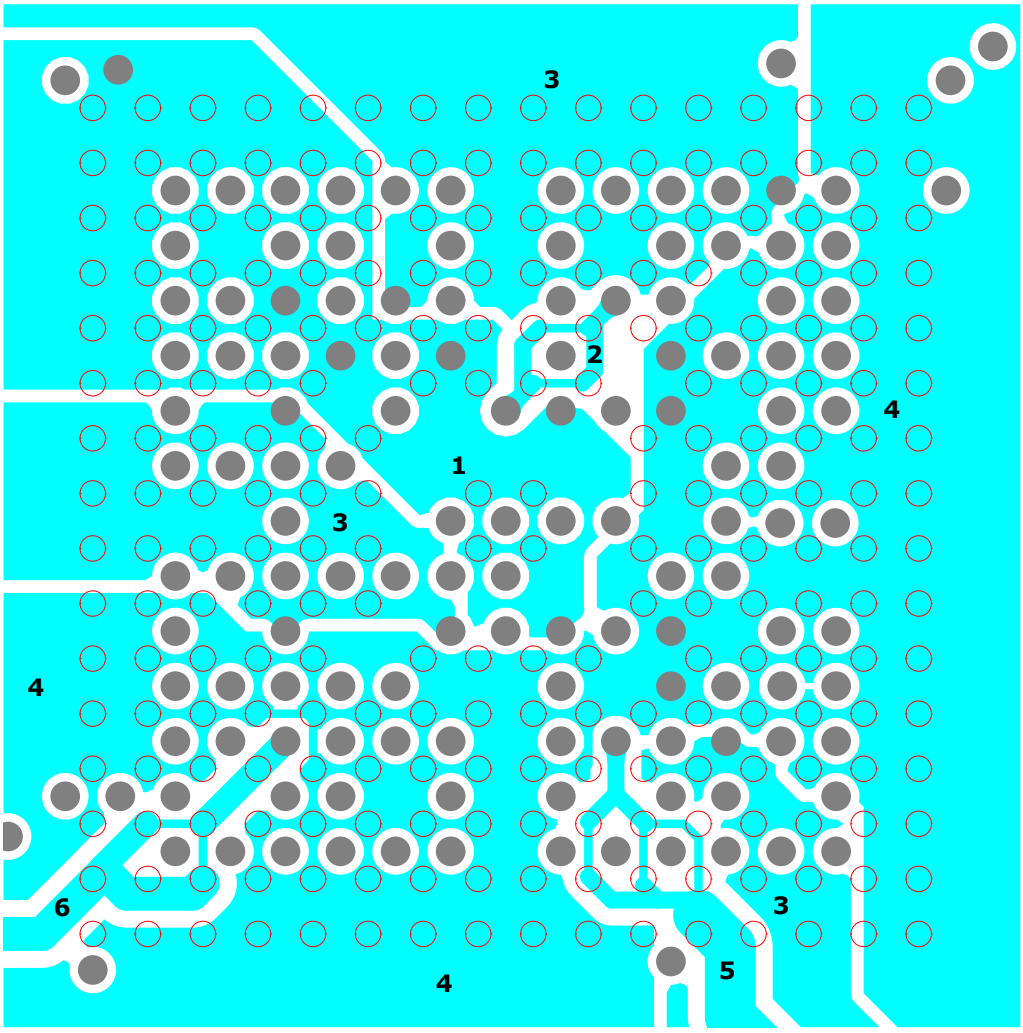


Figure 3-5. SAM9X75 Power Planes



The SAM9X75 had some of its balls strategically depopulated in order to fit 0201 decoupling capacitors on the bottom layer, right next to the power balls, under the BGA array.

Whenever possible, the power is supplied through solid copper polygons placed on the inner layer (power layer). These polygons are formed in such a way that the signals on the bottom layer have their return path through them. However, some of the power rails can be connected with traces if the current drawn is low and they do not serve as reference rails for high speed signals. Such power rails are VDDBU and VDD-2V5.

The power rails depicted in the image above are:

1. VDDCORE
2. VDDMIPI, VDDLVDS (the power rail generator is VDDOUT25)
3. VDDIN33, VDDQSPI, VDDANA, VDDIOP0, VDDIOP1
4. VDDIOM
5. VDDIOP2
6. VDDBU

3.4 High Speed Signals Routing

3.4.1 Requirements

High speed signals must be length-matched and impedance-matched, and routed over an uninterrupted reference plane (power or ground). If the reference plane is a power plane, the best option is to use the power plane that powers the rail of the signals.

3.4.2 Implementation Example for DDR3

Note that the following design, which aims at minimizing the area covered by the SDRAM interface implementation and at keeping the layer stack to a minimum of 4 layers, does not fully comply with the recommendations set forth in 4.2. Good Practices and must be considered as experimental.

Figure 3-6. DDR3 Routing on Top Layer

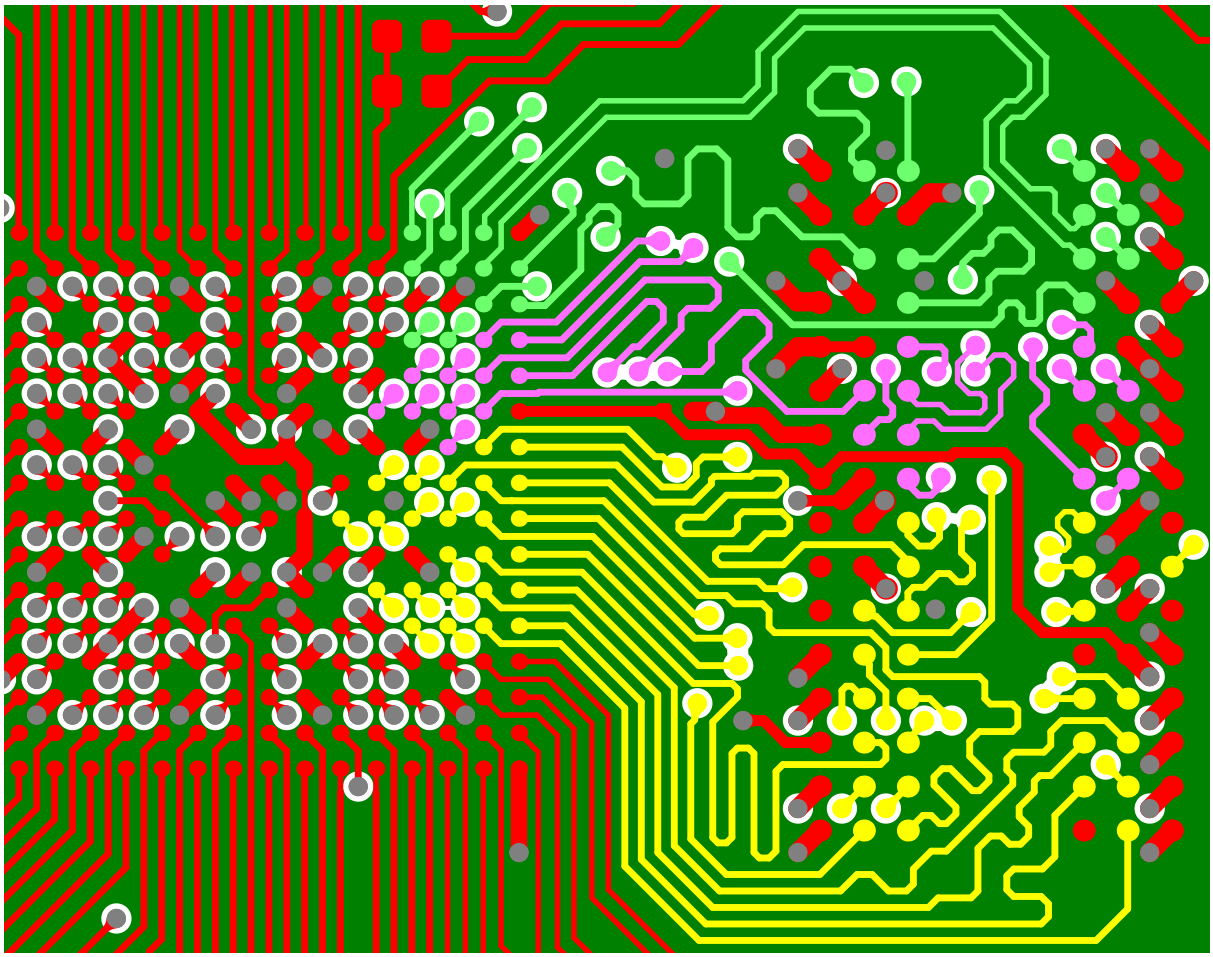
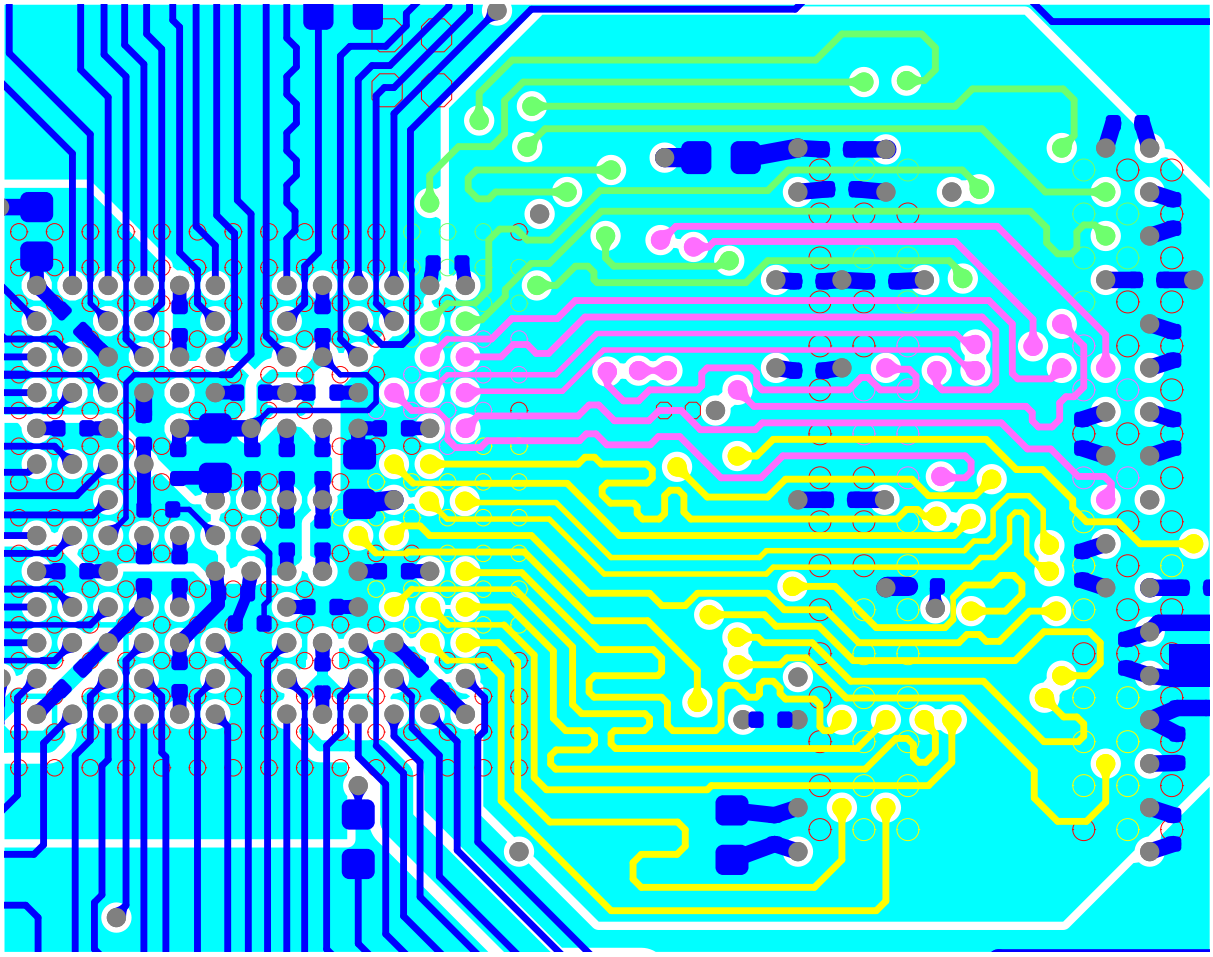


Figure 3-7. DDR3 Routing on Bottom Layer



In the board used as example for this application note, the SDRAM signals routed on the bottom layer use the VDDIOM power plane as reference.

On both the top and the bottom layers, signals are impedance-matched and length-matched. Differential signals are routed accordingly, with a differential impedance of 100 ohms (50 ohms for single-ended signals).

Special care was taken when designing the SAM9X75 stand-alone MPU package ball-out to ease an optimal routing path for the SDRAM memory.

The same rules must be applied to all other high speed interfaces, like MII/RMII/RGMII, QSPI, SDMMC, MIPI, LVDS and USB.

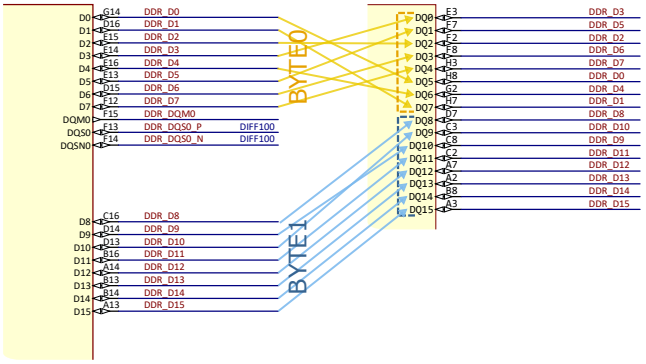
4. Appendix

4.1 Bit and Byte Swapping

DDR3 and DDR2 memories support **bit swapping**, a technique the designer can use to interchange data lines with one another, provided that they correspond to the same byte lane (for example, any bits inside the D[0..7] lane). This is very useful when trying to optimize a DDR layout routing.

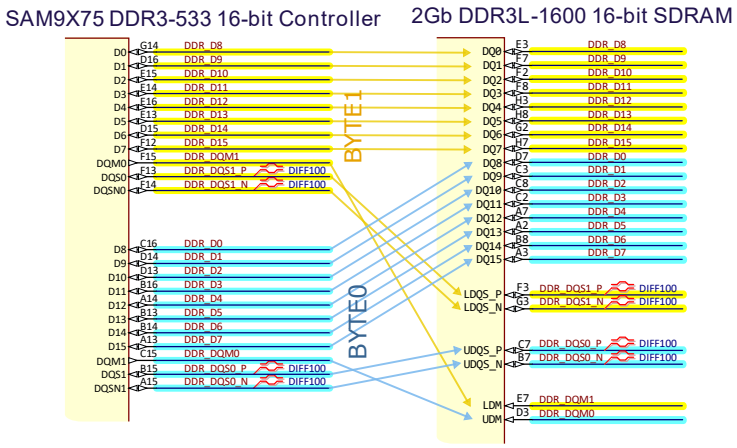
The following figure shows an example of the bit swapping technique implemented in the board used as example in this application note.

Figure 4-1. DDR3 Bit Swapping



Byte swapping is another technique that can be used on DDR3 and DDR2 memories. It allows the designer to swap the data lanes with one another, also for the purpose of optimizing the layout. Remember to also swap the DQMx and DQSx signals corresponding to the swapped byte lanes, as illustrated below.

Figure 4-2. DDR3 Byte Swapping



4.2 Good Practices

The following is a list of suggestions for designing with high speed signals:

- Use controlled impedance PCB traces that match the specified single-ended (50Ω) and differential (90Ω/100Ω) impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing required to achieve the specified differential impedance.

- Maintain maximum possible separation between the differential pairs, any high speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- Route CMOS/TTL and differential signals on different layers, which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 135° turns or an arc instead of a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high speed clock and periodic signal traces that run parallel to high speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Use a minimum of 20 mils spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all high speed traces over continuous planes (VCC or GND), avoiding cross splits or openings in those planes.
- For microstrip or stripline transmission lines, keep the spacing between adjacent signal paths at least twice the line width.
- Keep all traces at least five line widths away from the edge of the board.
- Follow the return path of each signal and keep the width of the return path under each signal path at least as wide, and preferably at least three times as wide, as the signal trace.
- To reduce EMI, avoid routing switching signals across copper splits or openings in ground planes. Routing around them is preferable even if it results in longer paths.
- Minimize the loop inductance between the power and ground paths.
- Allocate power and ground planes on adjacent layers with as thin a dielectric as possible to create plane capacitance.
- Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
- Supply voltages must be composed of planes only, not traces (except for very low current voltage rails such as VDDBU). Short connections (≈ 8 mils) are commonly used to attach vias to planes. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance (20 mils trace width).

5. Revision History

5.1 Rev. A - 03/2023

First issue.

Table of Contents

Microchip Information

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