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AC ADAPTER SPECIFICATIONS

DC Voltage Output: 12VDC
Current Output: ~ 5A (depending on application)
Polarity: 
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

		Automotive Product Group 6501 William Cannon Drive West Austin, TX 78735-8099	
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Approved: Ankur Kala	Size C	Document Number SCH-50784 PDF: SPF-50784	Rev A
Date: Friday, July 09, 2021		Sheet 1 of 22	

Revision History		
Revision	Date	Description
X2	9 May, 2021	Draft Schematic
A	9 July, 2021	1. Change R143 from 22ohm to 0ohm based on PISI result 2. Remove R825 based on PISI result 3. Add R1278, R1279 to prevent PF53 damage in case no silicon in the socket 4. Change VR5510 BUCK1, BUCK2 feedback, PSYNC and VCOREMON option headers to 0ohm resistors so there will be no chance to users to damage VR5510 with wrong config 5. Move VDD_IO_GMAC0/1, VDD_IO_SDHC and eMMC Chip 1.8V supply from LDO2/BUCK1 to LDO1



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REVISION HISTORY

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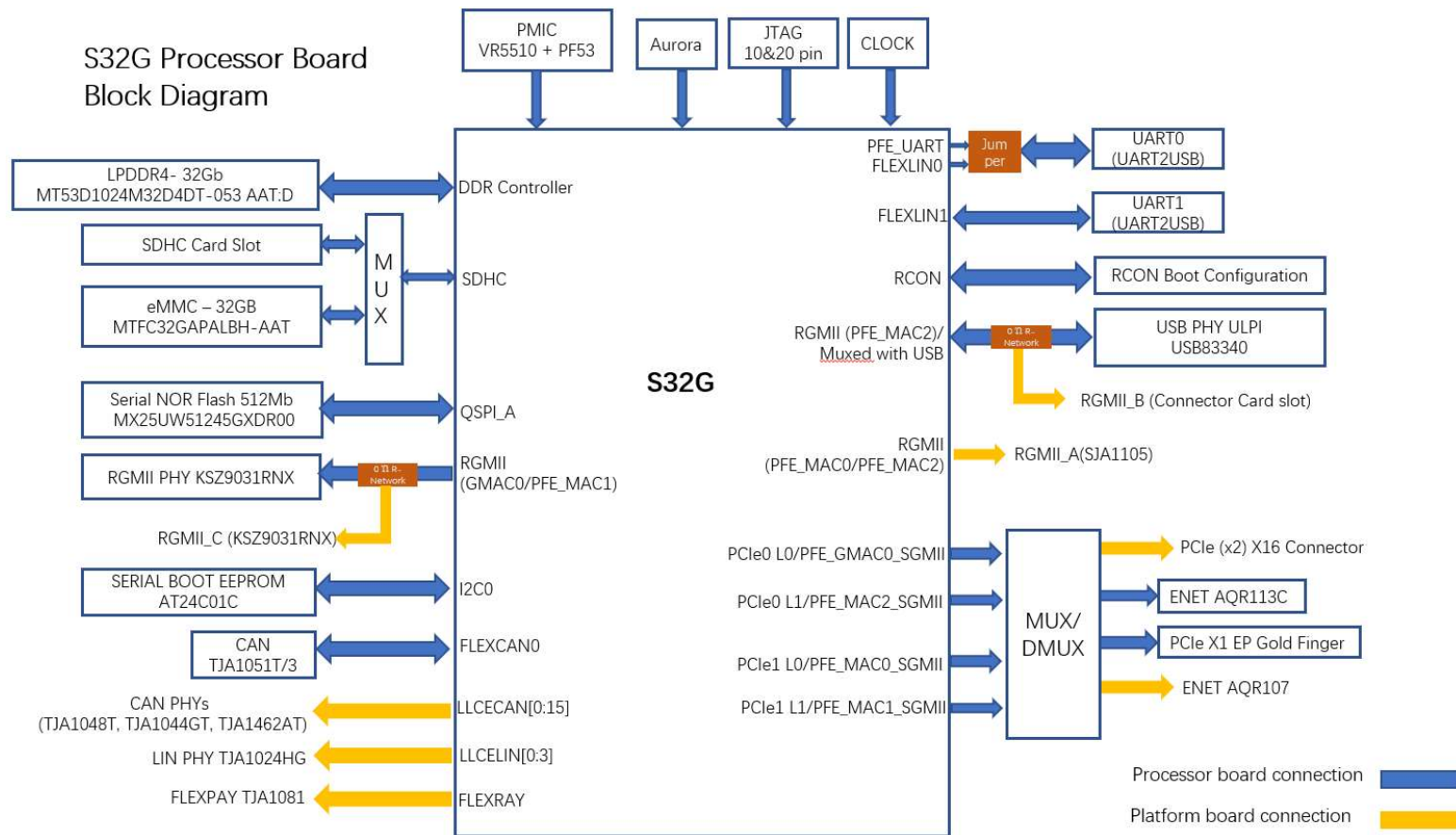
Document Number SCH-50784 PDF: SPF-50784

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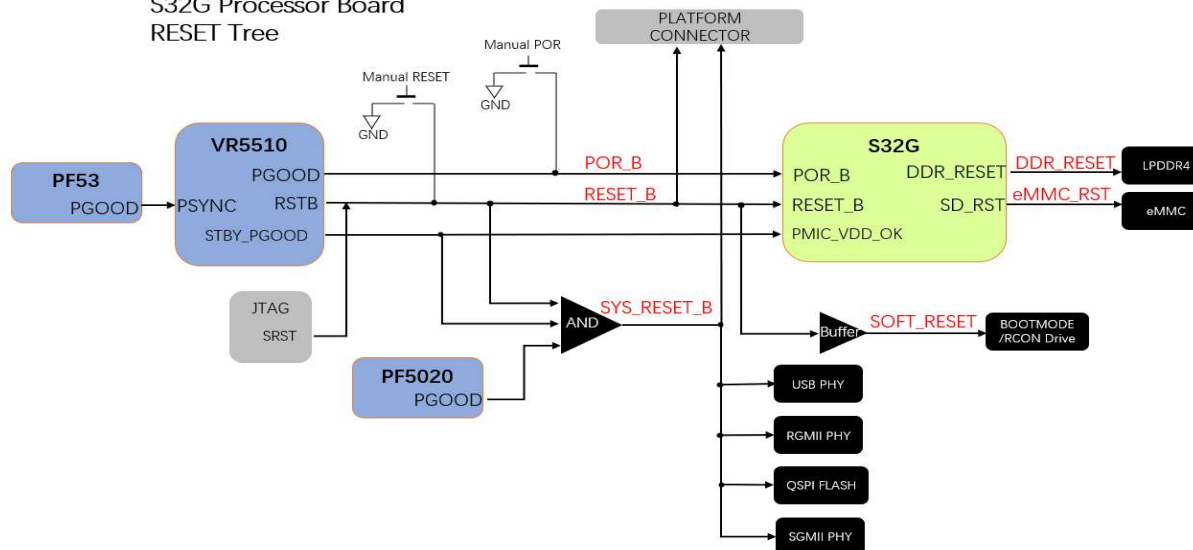
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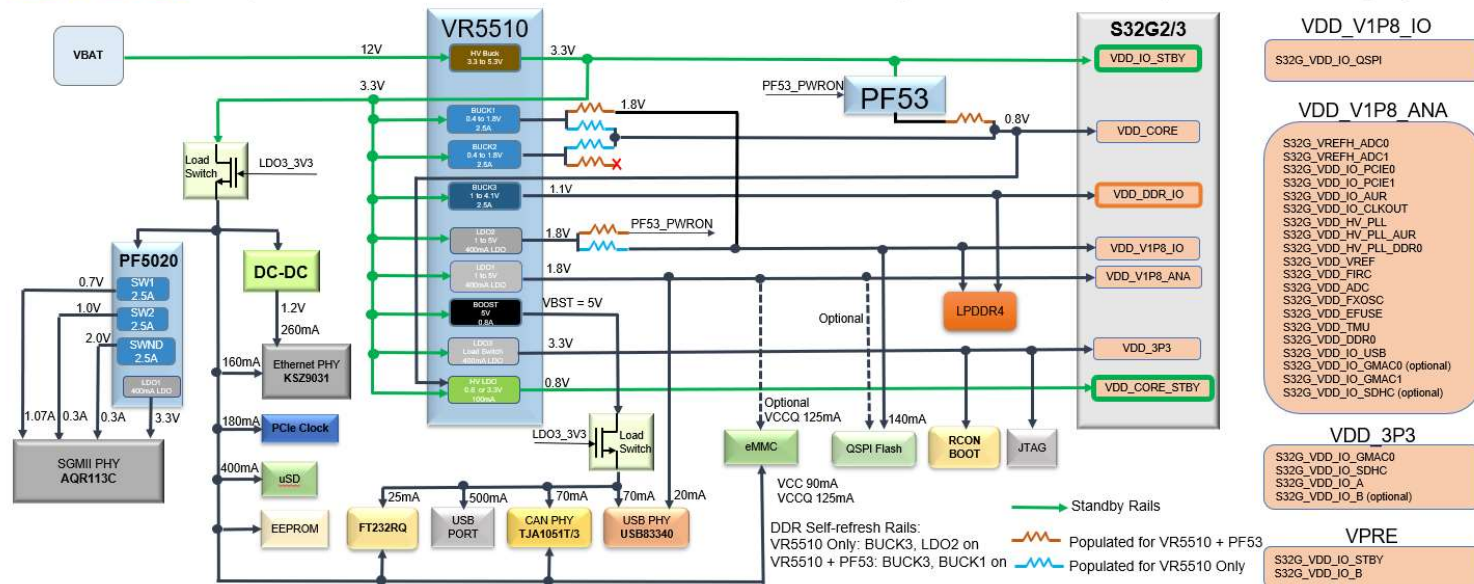
S32G Processor Board Block Diagram



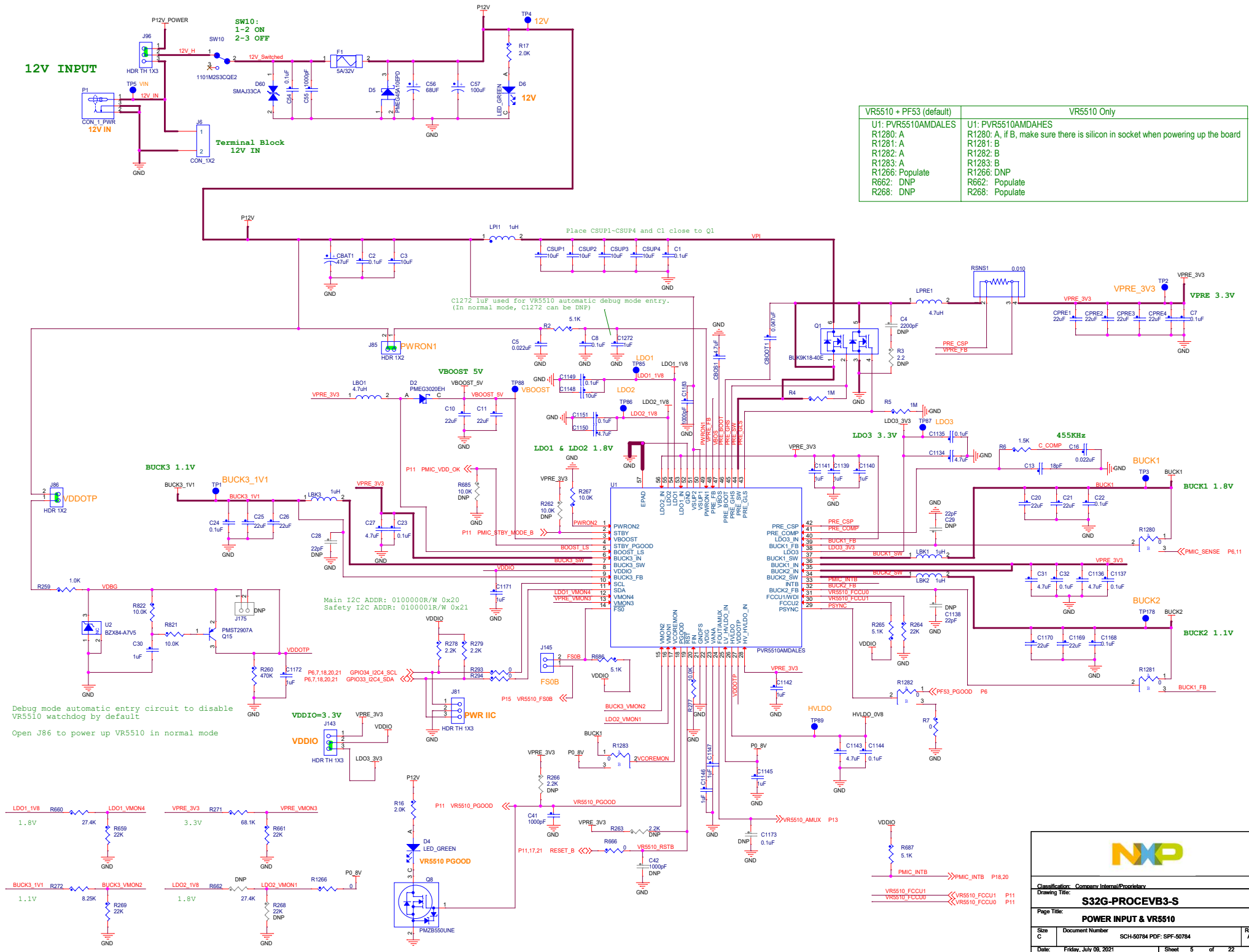
S32G Processor Board RESET Tree



S32G EVB3 - System Power Tree with VR5510 + PF53 (S32G2/G3 Compatible Design)



12V INPUT



VR5510 + PF53 (default)	VR5510 Only
U1: PVR5510A0MA0ALES	U1: PVR5510A0MA0ALES
R1280: A	R1280: A, if B, make sure there is silicon in socket when powering up the board
R1281: A	R1281: B
R1282: A	R1282: B
R1283: A	R1283: B
R1266: Populate	R1266: DNP
R662: DNP	R662: Populate
R268: DNP	R268: Populate

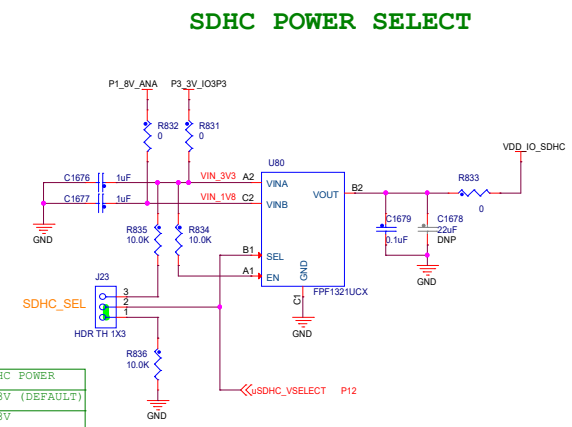
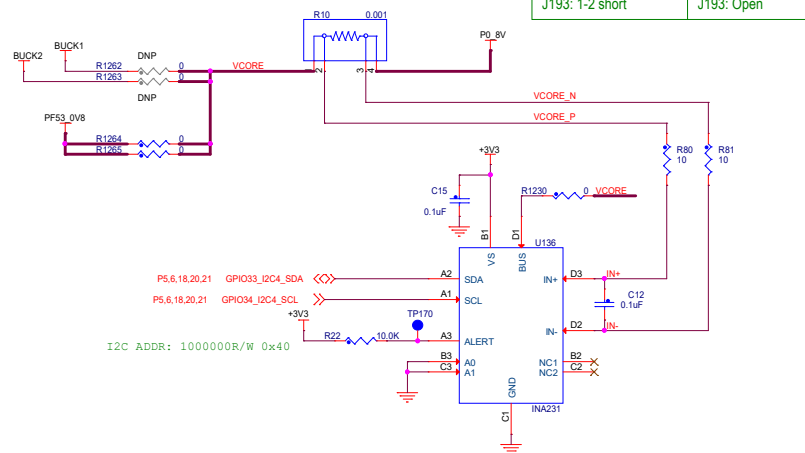
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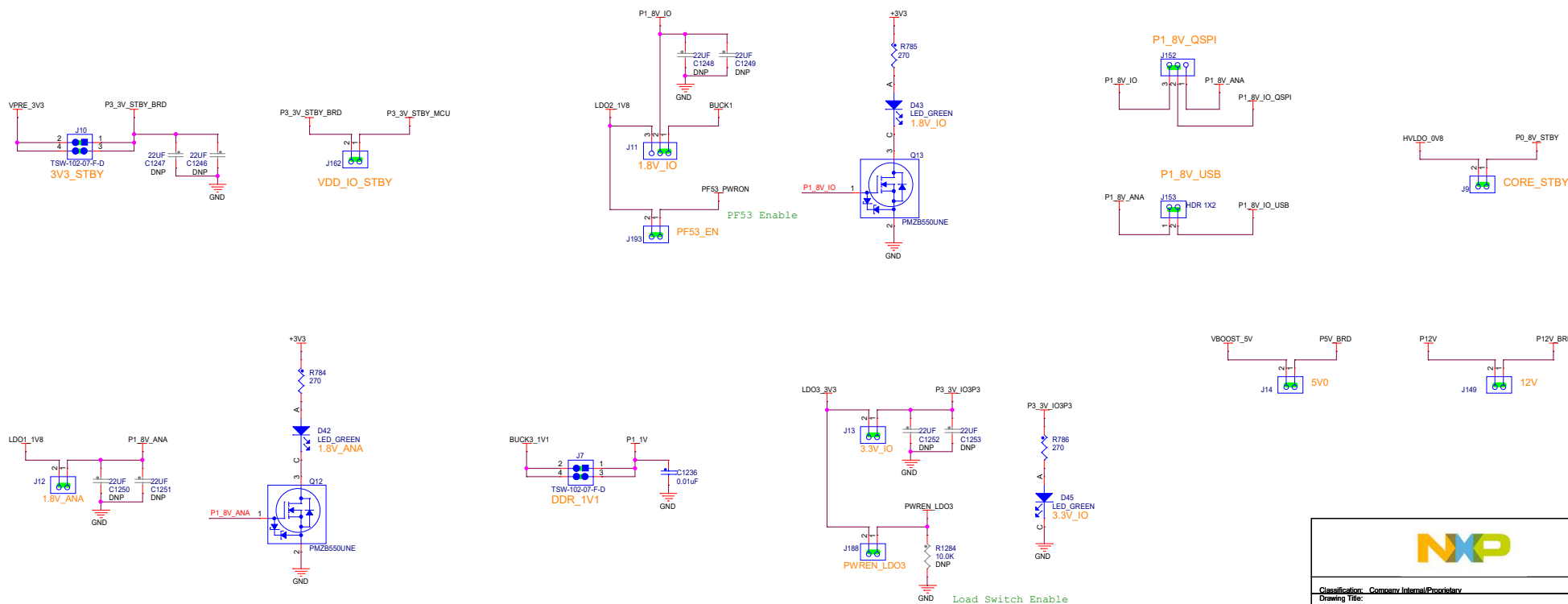
Page Title: **POWER INPUT & VR5510**

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VR5510 + PF53 (default)	VR5510 Only
R1262: DNP	R1262: Populate
R1263: DNP	R1263: Populate
R1264: Populate	R1264: DNP
R1265: Populate	R1265: DNP
J11: 1-2 short	J11: 2-3 short
J193: 1-2 short	J193: Open



J23	SDHC POWER
SHORT 1-2	3.3V (DEFAULT)
SHORT 2-3	1.8V



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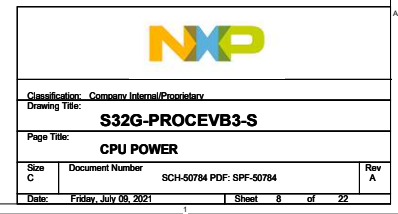
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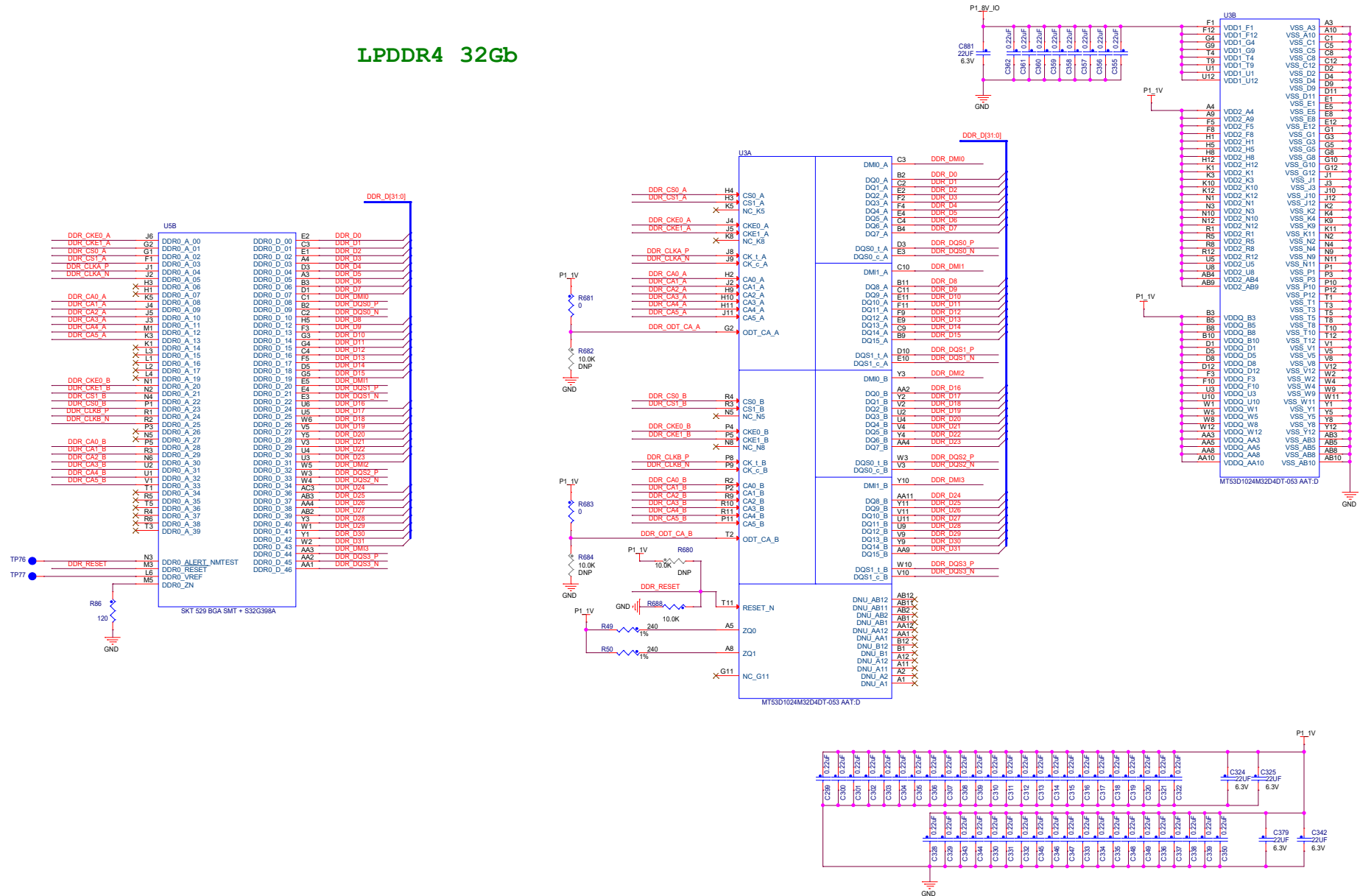
Page Title: POWER JUMPERS

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LPDDR4 32Gb



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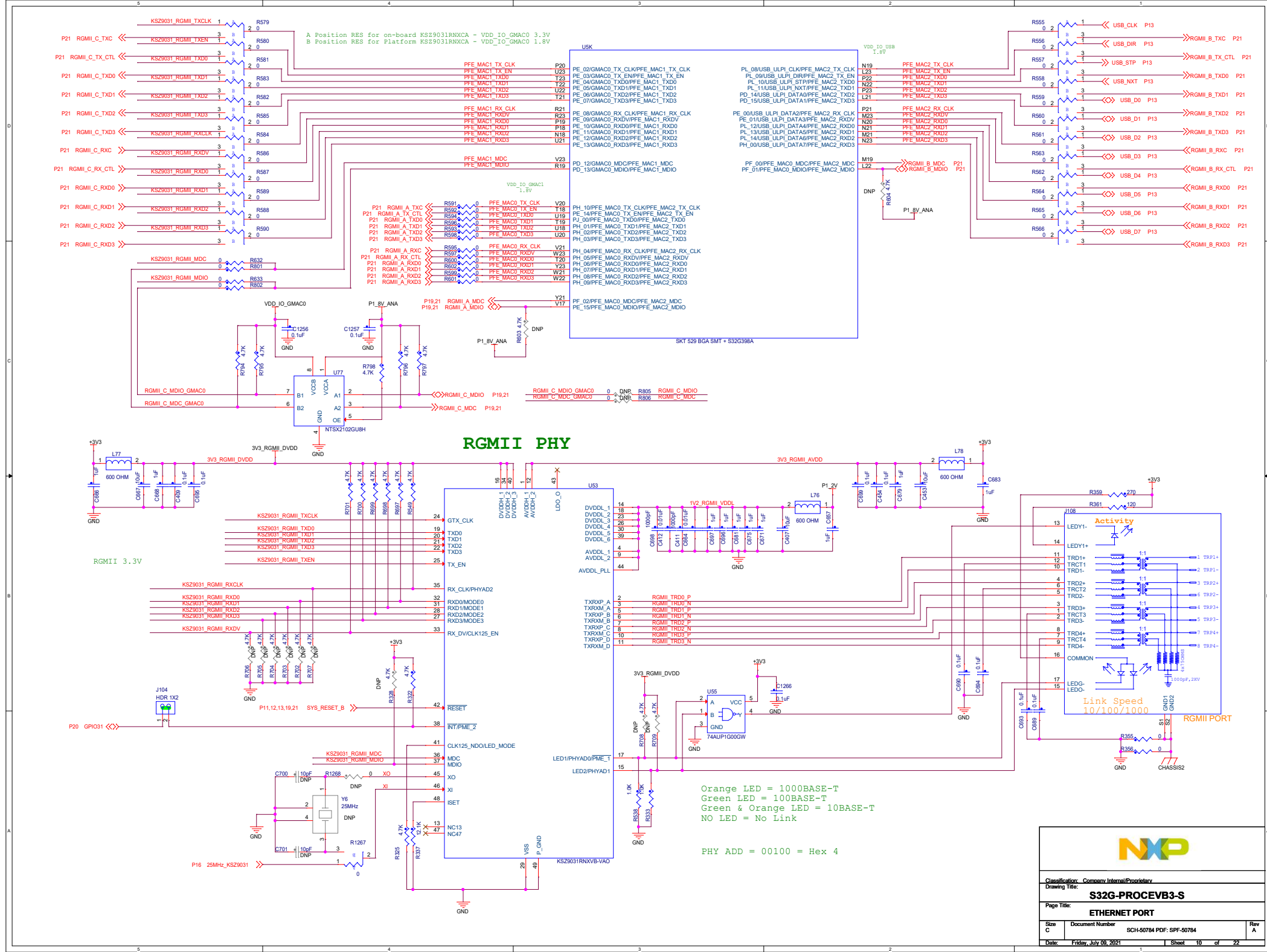
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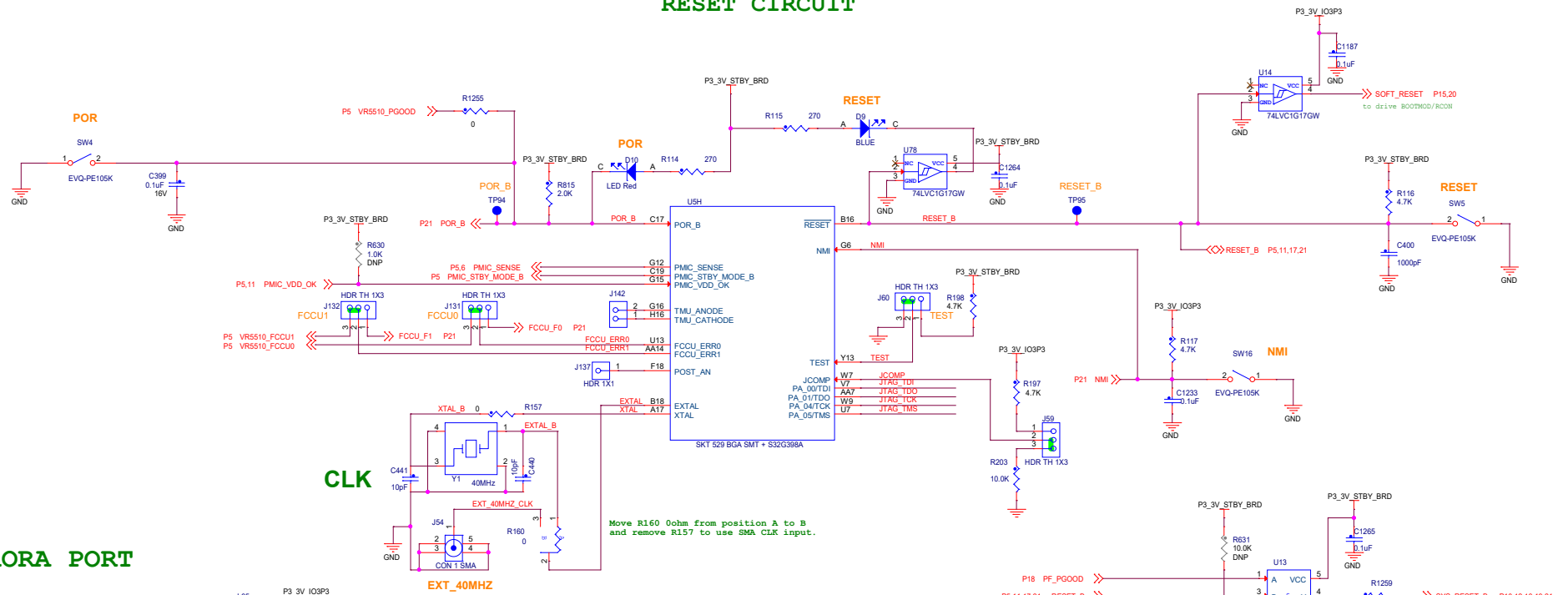
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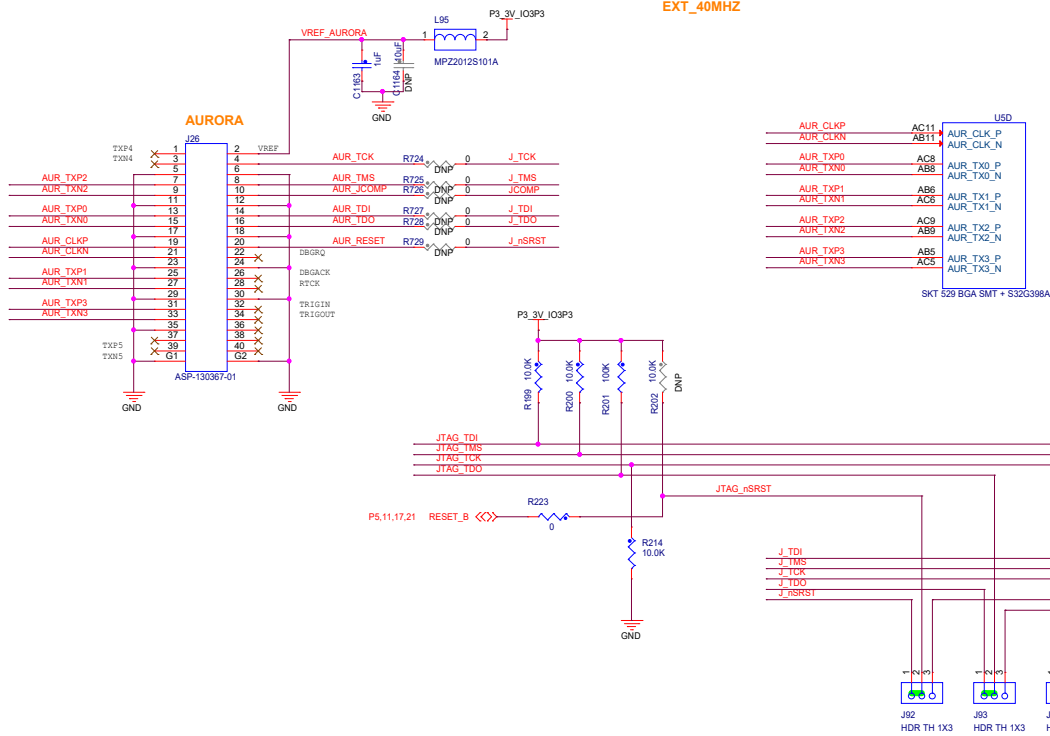
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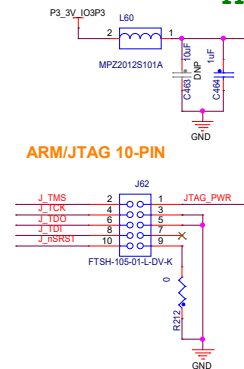
RESET CIRCUIT



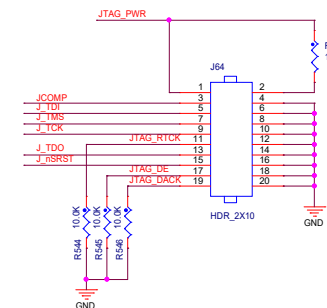
AURORA PORT



ARM JTAG



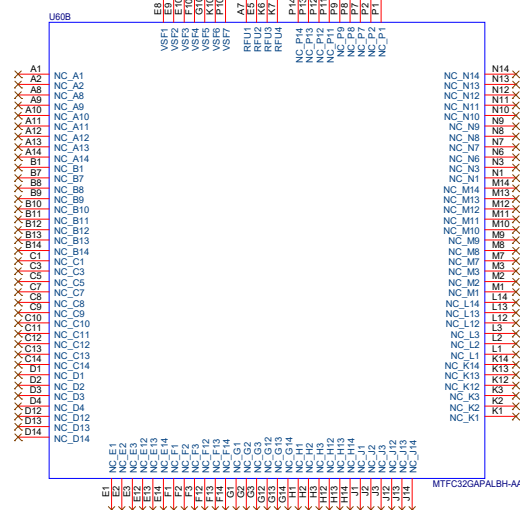
ARM/JTAG 20-PIN



SWD Signals from Platform

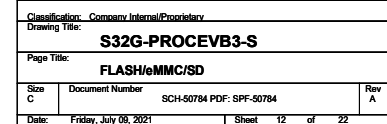
[illegible]

The schematic diagram illustrates the internal circuitry of the MAX4886ETG+ module and its connections to a host system. The module is powered by a 3.3V regulator (U18) which is connected to a 3.3V input. The regulator's output is connected to the module's VDD1 pin. The module also includes a 600 Ohm resistor (R1273) and several capacitors (C417, C418, C419, C420, C421, C422, C423, C424). The module is connected to a host system via a ribbon cable, with signals for eMMC data and address, SD data and address, and various control signals like COM1+, COM2+, COM3+, COM4+, and SEL. The module also has a TP83 test point and a R1273 resistor.

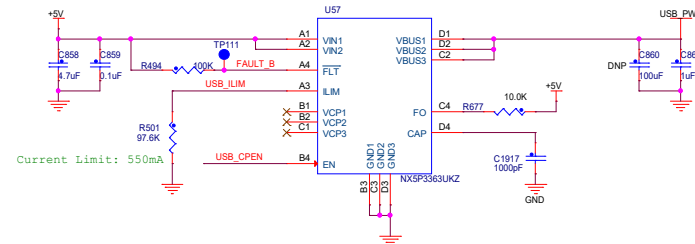
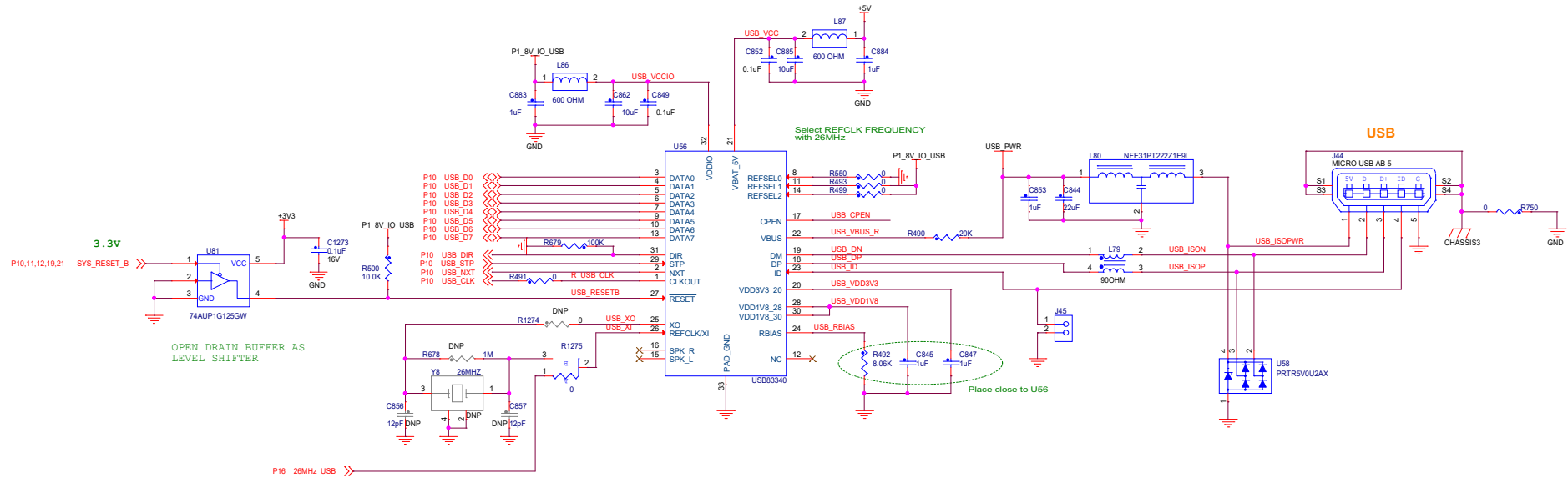


SD_eMMC_SEL

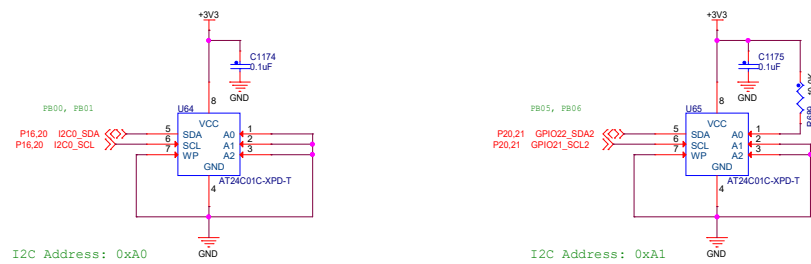
J50	INTERFACE
SHORT 1-2	SD (DEFAULT)
SHORT 2-3	eMMC



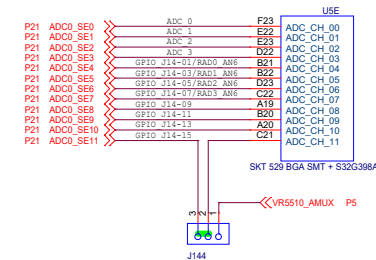
ULPI USB



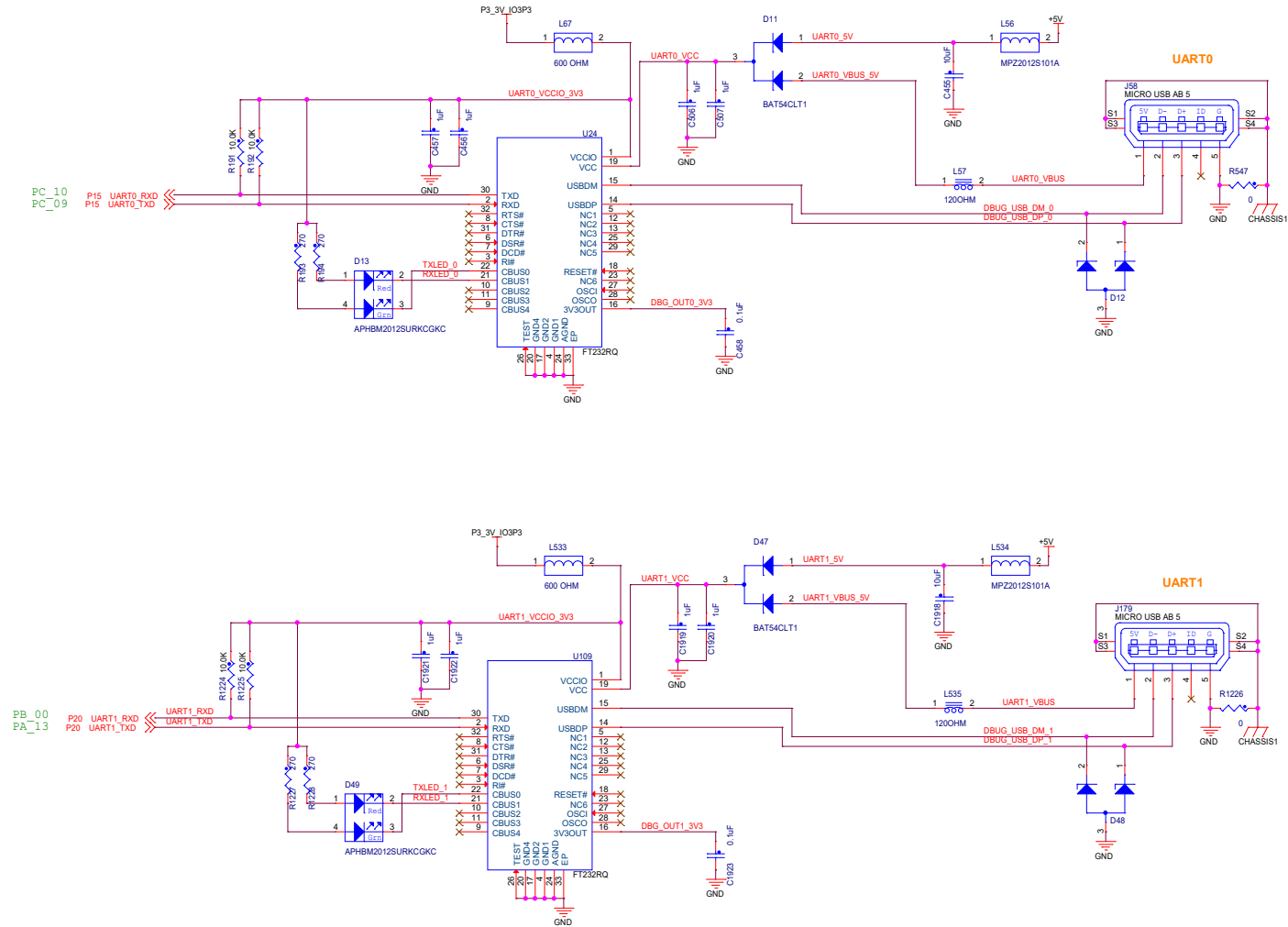
SERIAL BOOT EEPROM



ADC Connection



UART TO USB CONVERSION



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UART

Size

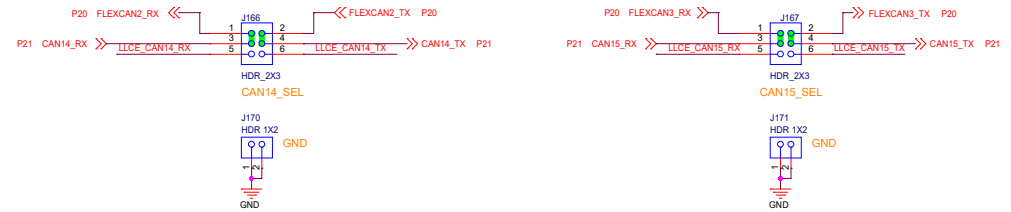
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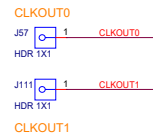
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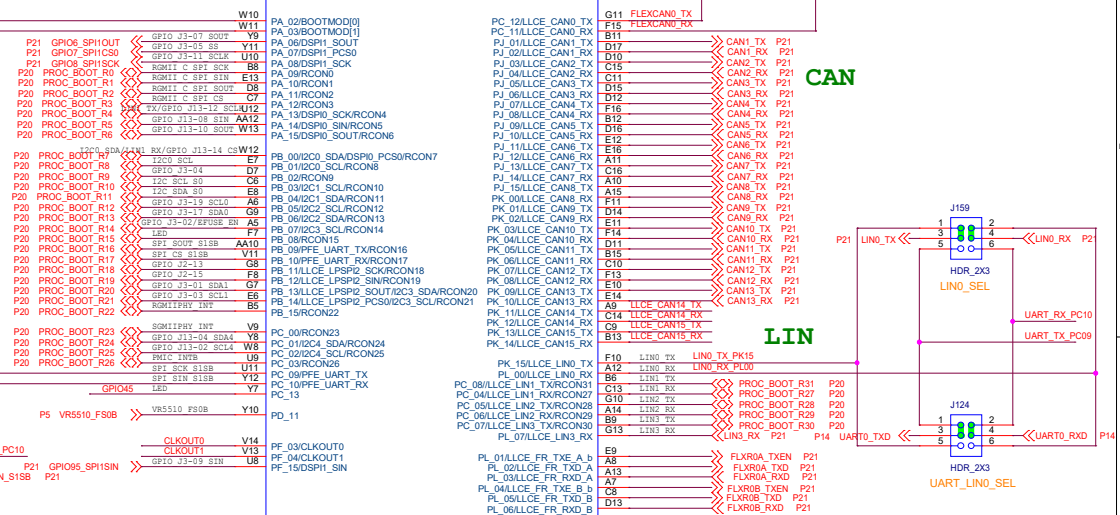


Boot Mode Select

SW15[1:2]	BOOTMOD0
OFF OFF	0 (default)
ON OFF	1
OFF ON	RESET (RESERVED)
ON ON	INVERTED RESET (RESERVED)



SW14[1:2]	BOOTMOD0
OFF OFF	0
ON OFF	1 (default)
OFF ON	RESET (RESERVED)
ON ON	INVERTED RESET (RESERVED)



FlexRAY



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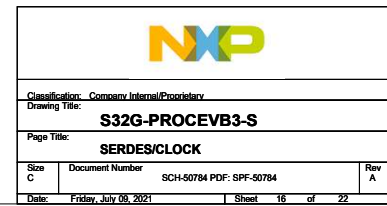
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[illegible]

The diagram illustrates the SERDES I/O architecture for the S32G. It is divided into two main sections: SERDES 0 CLK and SERDES 1 CLK.

SERDES 0 CLK: This section shows a clock signal path. A clock signal (CLK GEN) with outputs OUT5 and OUT1 is connected to a 100MHz clock source. The signal path includes a DNP (Do Not Populate) component (R1269/R1270) and a DNP component (R1271/R1272). The signal is then connected to the PCIE0_CK_P/N and SERDES_0_CLKP/N pins. The SERDES_0_CLKP/N pin is connected to the PLATFORM CONNECTOR, which is then connected to the PCIe x16 CONNECTOR.

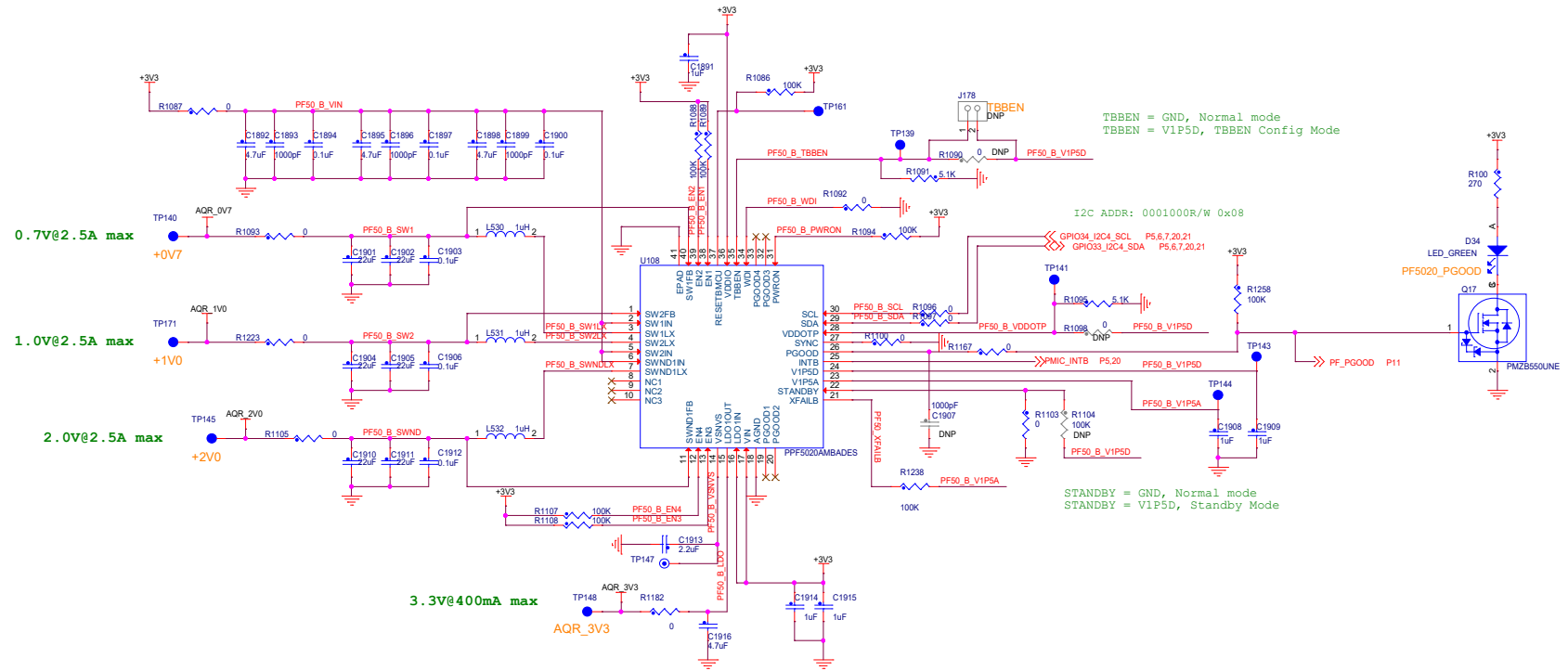
SERDES 1 CLK: This section shows a clock signal path. A clock signal (CLK GEN) with outputs OUT4 and OUT0 is connected to a 100/125MHz clock source. The signal path includes a DNP component (R716/R717) and a DNP component (R718/R719). The signal is then connected to the PCIE1_CK_P/N and PCIE_EP_P/N pins. The PCIE_EP_P/N pin is connected to the PCIe X1 (EP) GOLD FINGER.



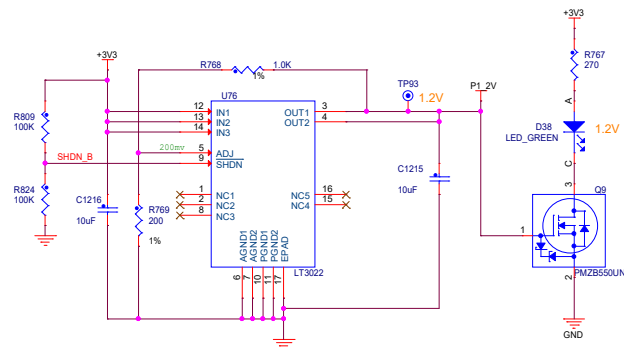
P: Platform Board
D: Processor Board

[illegible]

AQR113C Power Supply



RGMII PHY KSZ9031 1.2V Supply



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AQR113C POWER SUPPLY

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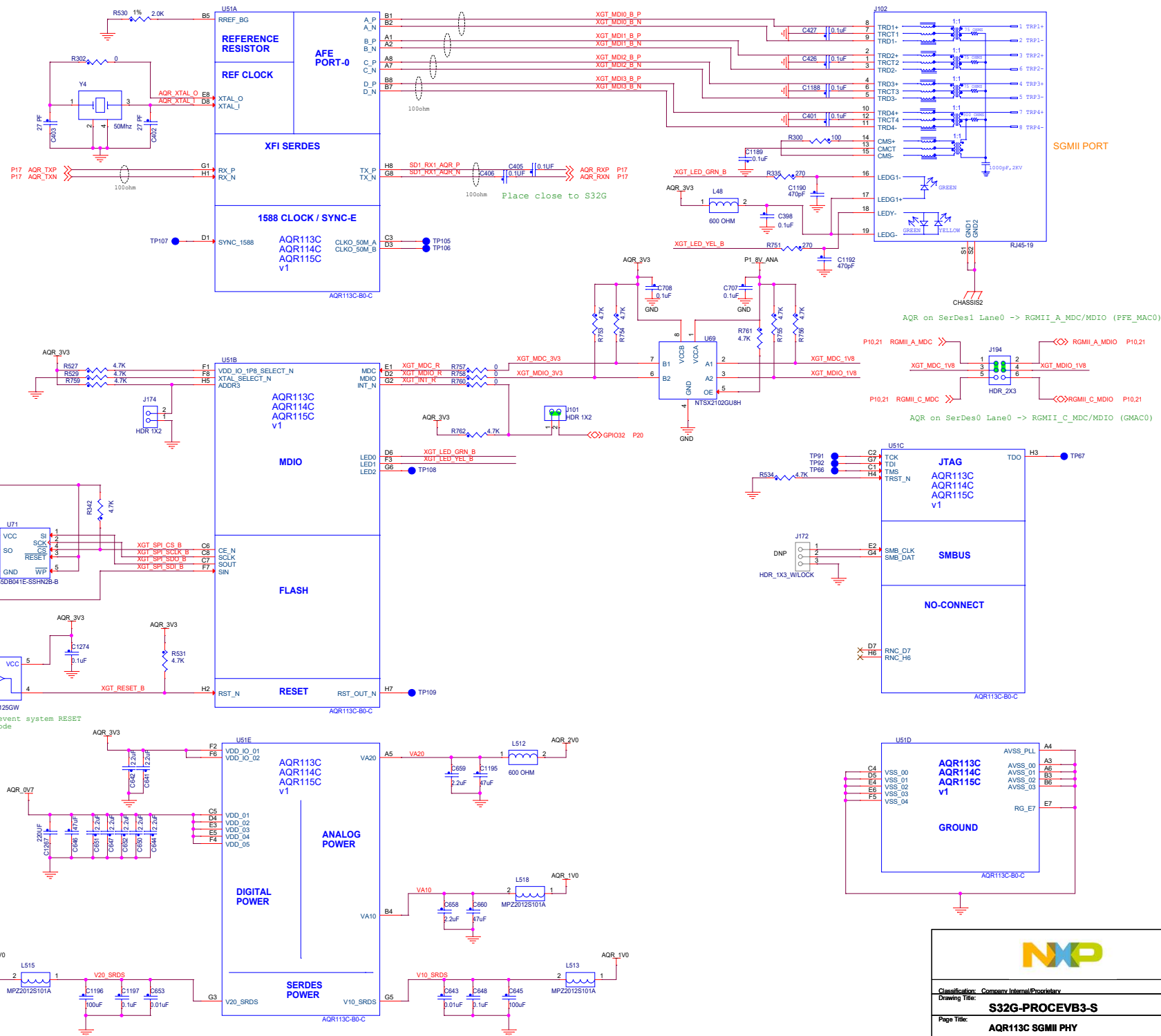
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SGMII Port



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Drawing Title: **S32G-PROCEVB3-S**

Page Title: **AQR113C SGMII PHY**

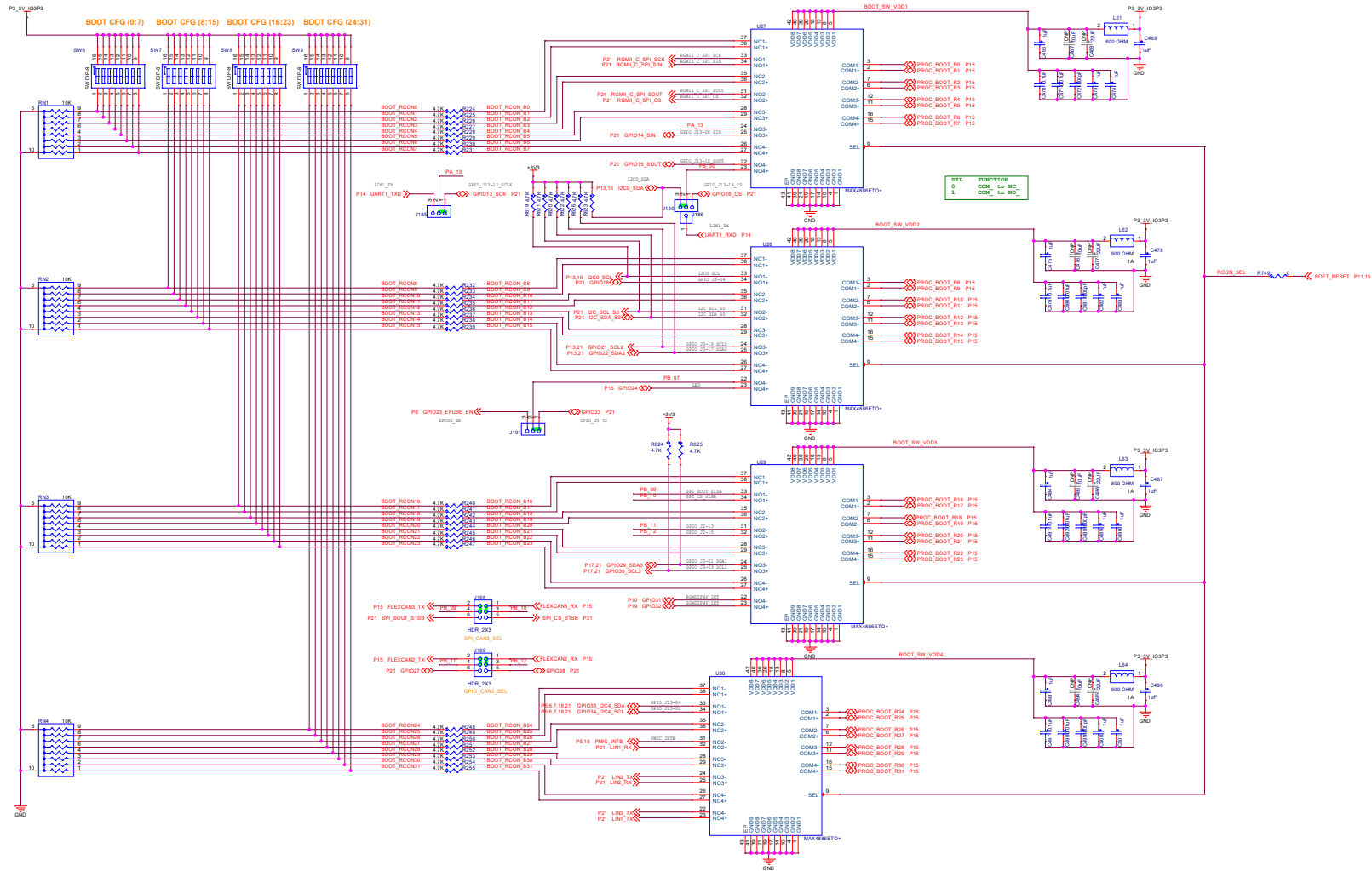
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SW6-SW9 Default Setting

	1	2	3	4	5	6	7	8
SW6	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
SW7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SW8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SW9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

RCON Boot Selection



Default Jumper setting

REF DES	JUMPER(DEFAULT)	PAGE NAME
J86,J96,J85	1-2	05 POWER INPUT & VR5510
J143	2-3	05 POWER INPUT & VR5510
R1283,R1282,R1280,R1281	A	05 POWER INPUT & VR5510
J189,J141,J187	1-2	06 PF53 & LOAD SWITCH
R939,R940,R1192	A	06 PF53 & LOAD SWITCH
J7,J10	1-2, 3-4	07 POWER JUMPERS
J23,J153,J12,J14,J188,J162,J13,J9,J193,J11,J149	1-2	07 POWER JUMPERS
J152	2-3	07 POWER JUMPERS
J98	1-2, 3-4	08 CPU POWER
J161	1-2	08 CPU POWER
J129,J150	2-3	08 CPU POWER
J104	1-2	10 ETHERNET PORT
R1267,R557,R566,R590,R564,R560,R563,R559,R580,R556,R581,R579,R587,R565,R561,R585,R562,R584,R588,R589,R558,R582,R583,R586,R555	A	10 ETHERNET PORT
J154,J94,J95,J92,J93	1-2	11 RESET/CLOCK/JTAG/AURORA
J131,J132,J60,J59	2-3	11 RESET/CLOCK/JTAG/AURORA
R160	A	11 RESET/CLOCK/JTAG/AURORA
J50	1-2	12 FLASH/eMMC/SD
J110	2-3	12 FLASH/eMMC/SD
J144	2-3	13 USB/ADC/EEPROM
R1275	A	13 USB/ADC/EEPROM
J173	1-2	15 CAN/LIN/FLXR
J155,J167,J166,J159,J124	1-3, 2-4	15 CAN/LIN/FLXR
J158	3-5, 4-6	15 CAN/LIN/FLXR
J192	1-2	16 SERDES/CLOCK
J101	1-2	19 AQR113C SGMII PHY
J194	1-3, 2-4	19 AQR113C SGMII PHY
J191,J185	1-2	20 BOOT SELECT
J168,J169	1-3, 2-4	20 BOOT SELECT
J130	2-3	20 BOOT SELECT
J195	1-3, 2-4	21 INTERCONNECTOR
R1256	A	21 INTERCONNECTOR

Default Switch setting

REF DES	SWITCH(DEFAULT)	PAGE NAME
SW10	2-3 OFF	05 POWER INPUT & VR5510
SW15	1-OFF, 2-OFF	15 CAN/LIN/FLXR
SW14	1-ON, 2-OFF	15 CAN/LIN/FLXR
SW17	1: OFF 2: ON	17 SERDES SWITCH
SW9,SW8,SW7	1-OFF,2-OFF,3-OFF,4-OFF,5-OFF,6-OFF,7-OFF,8-OFF	20 BOOT SELECT
SW6	1-OFF,2-OFF,3-OFF,4-OFF,5-OFF,6-OFF,7-ON,8-OFF	20 BOOT SELECT



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DEFAULT JUMPER SETTING

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