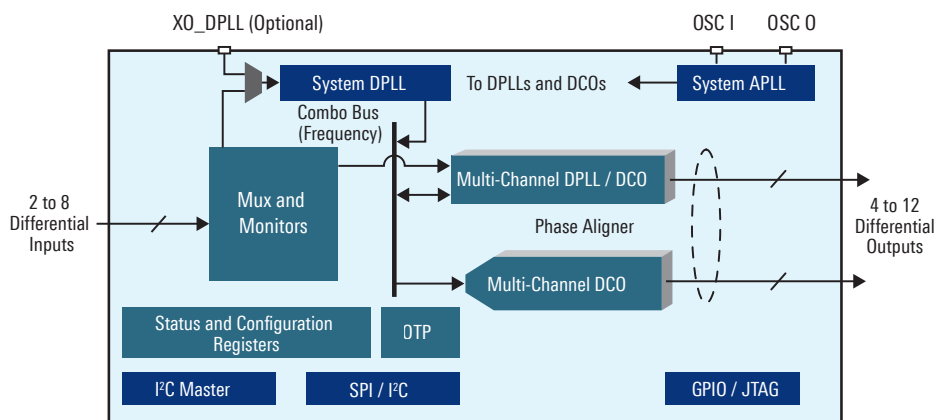# CLOCKMATRIX™ OVERVIEW

The Renesas ClockMatrix™ family of multi-channel timing devices reduces the complexity and cost of clock trees by replacing multiple timing chips with a single timing resource. The devices support a wide range of frequencies and signal types at their inputs and outputs.

ClockMatrix devices include two types of timing channels: Digital PLL / Digitally Controlled Oscillator (DPLL/DCO) channels and DCO only channels. Any DCO can free run based on the local oscillator. They can be controlled by external software or they can be connected to a DPLL channel to supply additional outputs and frequencies for that DPLL.

A wide range of simple to complex timing and synchronization applications are covered by the ClockMatrix family using its flexible architecture, a common register set and a few package types.

ClockMatrix Product Families
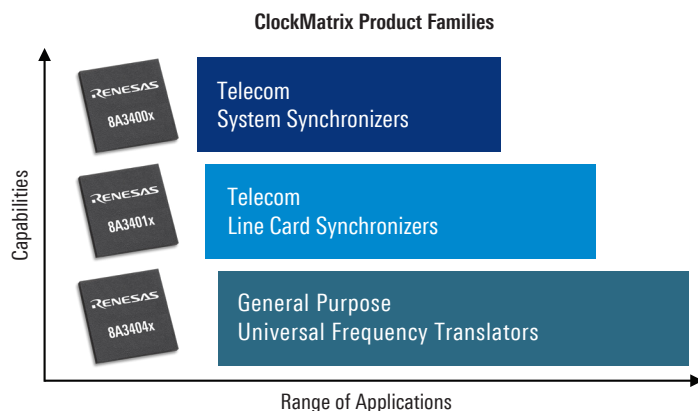
In the ClockMatrix family, the Universal Frequency Translator (UFT™) devices perform jitter attenuation and frequency translation functions for general purpose applications.

Telecom synchronizers generate ITU-T compliant clocks for line cards locked to a system synchronizer while the system synchronizers generate ITU-T compliant clocks for telecom systems.

Highly flexible multi-channel timing devices

- Up to 8 independent channels
- Timings channels configurable as DPLLs or DCOs
- Generates any frequency from 0.5Hz to 1GHz

Ultra-low jitter

- 150fs RMS (typ) 12kHz to 20MHz
- Suitable for 28Gbps and lower rate interfaces

Precision time sync.

- Supports cTE < 5ns for G.8273.2 Classes A, B, C, D
- Input to output phase skew< 100ps
- Output to output phase skew < 50ps

Applications

- IEEE 1588
- Synchronous Ethernet
- eCPRI and CPRI
- 28Gbps and lower rates
- 5G fronthaul and backhaul
- Routers / Switches
- OTN and PTN equipment
- Baseband and Radio Units

Standard compliance

- ITU-T G.8262
- ITU-T G.8262.1
- ITU-T G.8273.2

CLOCKMATRIX FAMILY OVERVIEW

ClockMatrix Family Comparisons

	Universal Frequency Translators	Line Card Synchronizers	System Synchronizers
Jitter Attenuation	Yes	Yes	Yes
Frequency Translation	Yes	Yes	Yes
Hitless Reference Switching	Yes	Yes	Yes
DPLL Loop Filters	17Hz to 12kHz	17Hz to 12kHz	0.09mHz to 12kHz
Reference Frequencies	1kHz to 1GHz	1kHz to 1GHz	0.5Hz to 1GHz
Output Frequencies	0.5Hz to 1GHz	0.5Hz to 1GHz	0.5Hz to 1GHz
Align Clocks with Input Sync Pulse	Yes	Yes	Yes
Sync Pulse over PWM	No	Yes	Yes
Data over PWM	No	Yes	Yes
EEC1 and EEC2 per G.8262	No	No	Yes
eEEC per G.8262.1	No	No	Yes
Telecom Boundary Clock per G.8273.2	No	No	Yes

Universal Frequency Translator Family

	8A34041	8A34042	8A34043	8A34044	8A34045
Inputs (Diff / SE)	8 / 16	7 / 14	2 / 4	4 / 8	2 / 4
Outputs (Diff / SE)	12 / 24	8 / 16	4 / 8	12 / 24	12 / 24
DPLL / DCO Channels	8	4	4	4	2
DCO Channels	0	0	0	4	6
Package	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN	10 x 10 mm 72-QFN	10 x 10 mm 72-QFN

Line Card Synchronizer Family / System Synchronizer Family

	Line Card Synchronizer Family			System Synchronizer Family				
	8A34011	8A34012	8A34013	8A34001	8A34002	8A34003	8A34004	8A34046
Inputs (Diff / SE)	8 / 16	7 /14	2 / 4	8 /16	7 /14	2 / 4	2 / 4	4 / 8
Outputs (Diff / SE)	12 / 24	8 / 16	4 / 8	12 / 24	8 / 16	4 / 8	4 / 8	12 / 24
DPLL / DCO Channels	8	4	4	8	4	4	2	4
DCO Channels	0	0	0	0	0	0	0	4
Package	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN	7 x 7 mm 48-QFN	10 x 10 mm 72-QFN

To learn how PTP Clock Manager software can help you easily implement synchronization in IEEE 1588 systems visit **renesas.com/clockmanager**

To request samples, download documentation or learn more visit **renesas.com/clockmatrix**

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